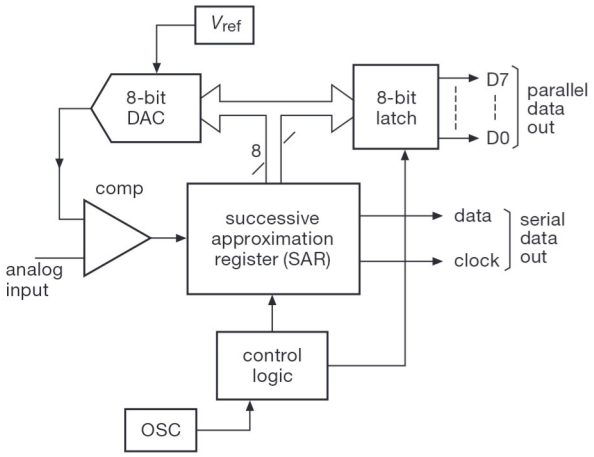


**Figure 13.31.** Successive-approximation ADC.

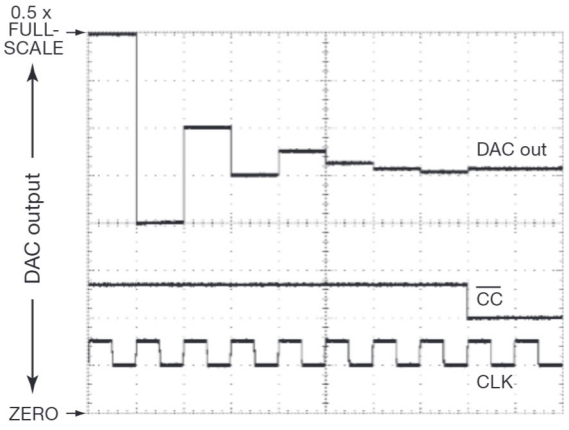


**Figure 13.32.** 'Scope trace of an 8-bit successive-approximation DAC's analog output converging to the final value. It's a binary search, with first guess equal to half of full scale. Note clock waveform and conversion-complete flag.

of 100 Ω resistors terminates the signal input with the usual 50 Ω expected by RF signals.

## *13.7 ADCs II: Successive approximation*

In the classic successive-approximation technique (sometimes called "SAR") you try various output codes by feeding them into a DAC and comparing the result with the analog input present at an input comparator (Figure 13.31). The way it's usually done is to set all bits initially to 0. Then, beginning with the most significant bit, each bit in turn is set provisionally to 1. If the D/A output does not exceed the input signal voltage, the bit is left as a 1; otherwise it is set back to 0. For an $n$-bit ADC, $n$ such steps are required. What you're doing is called a *binary search*, in the language of computer science.[39] A successive-approximation ADC has a BEGIN CONVERSION input and a CONVERSION DONE output. The digital output may be provided in parallel format (all bits at once, on $n$ separate output lines), in serial format ($n$ successive output bits, MSB first, on a single output line), or both.

In our electronics course the students construct a successive-approximation ADC, complete with DAC, comparator, and control logic. Figure 13.32 shows the successive outputs from the DAC, along with the eight clock pulses, as the trial analog output converges to the input voltage. And Figure 13.33 shows the full 8-bit "tree," a pretty picture you can generate by watching the DAC output while driving the input with a slow ramp that runs over the full analog input range.

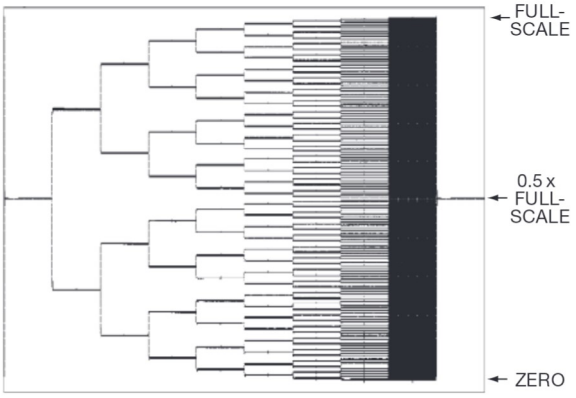


**Figure 13.33.** Accumulated 'scope trace of the 8-bit SAR's full "tree."

Successive-approximation ADCs are intermediate in speed and accuracy (compared with the faster flash converters, or the more accurate but slower techniques used in "delta–sigma" converters, and multislope integrating converters); see Tables 13.5 and 13.6. They require $n$ settling times of the DAC for $n$-bit precision. Typical conversion times are in the vicinity of 1 μs, with accuracies of 8 to 18 bits commonly available. This type of converter operates on a brief sample of the input voltage, and if the input is changing during the conversion, the error is no greater than the change during that time; however, spikes on the input are disastrous. Although generally quite accurate,

[39] Historically this goes *way* back: in 1556 a mathematician by the name of Tartaglia proposed using a set of weights (1 lb, 2 lb, 4 lb. . . 32 lb) in just such a manner to determine the weight of an object in the minimum number of trials on a balance.

these converters require accurately trimmed resistor networks, and they can have strange nonlinearities and "missing codes." One way to prevent missing codes is to use a chain of $2^n$ resistors and analog switches to generate the trial analog voltages, in the manner of the resistor-string DACs of §13.2.1; this technique was used in NSC's ADC0800-series 8-bit ADCs.

In contemporary successive-approximation ADCs, the conventional resistive DAC (*R*–2*R* or resistor string, used internally to generate the analog voltages for the trial codes) is usually replaced with a *charge-redistribution* DAC architecture (Figure 13.34).[40] This scheme requires a set of binary-weighted *capacitors*, which nowadays is easy enough to fabricate and trim on-chip. (So an 18-bit converter like the AD7641 contains, remarkably enough, a set[41] of 18 binary-scaled capacitors going from some $C_0$, $2C_0$, ..., to a final $131{,}072C_0$; these capacitors are really small, with the capacitance of $C_0$ measured in the *femto*farads – f F, or 0.001 pF.)

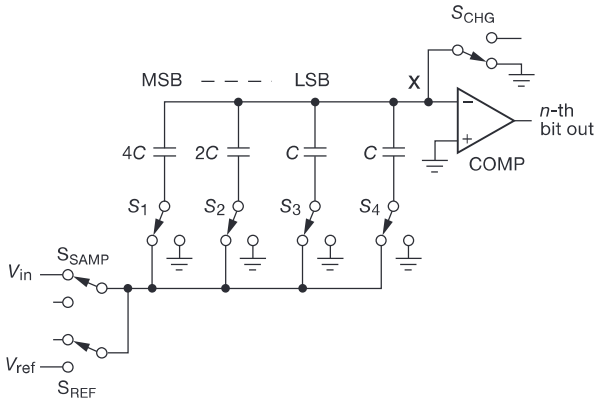


**Figure 13.34.** A capacitor-based "charge-redistribution" scheme replaces the *R*–2*R* resistor ladder in many successive-approximation ADCs. The capacitor beyond the LSB is not used in the bit testing, but is needed to preserve the exact fractional ratios.

To understand how it works, look at the operation of the simplified 3-bit converter in the figure.

1. The switches are shown in the *sample* part of the cycle, during which the voltage across each of the capacitors follows (or *tracks*) the input signal.
2. Switch $S_{SAMP}$ is opened, leaving the capacitors all holding the sampled input voltage.
3. Switch $S_{CHG}$ is then opened, so the input to the comparator can move around as trial codes are applied to the bit switches $S_1$–$S_3$; for example, if the bit switches are all set to ground, the comparator input $X$ would be at a voltage $-V_{in}$.
4. Now, to measure the held value of $V_{in}$, the bit switches are operated in turn: first the MSB switch $S_1$ is switched to $+V_{ref}$ (the full-scale range of the ADC), while $S_2$, $S_3$, and $S_4$ are switched to ground; this adds an offset of $V_{ref}/2$ to that $-V_{in}$ (it's a capacitive voltage divider: call it "charge redistribution" if you prefer).
5. The comparator's output now indicates the MSB: HIGH if $V_{in} > V_{ref}/2$, LOW otherwise.
6. As with the classic successive-approximation procedure, that switch is either returned to ground or left at $V_{ref}$, accordingly; the next-lower bit value is then tested similarly, with the process continuing in $n$ steps (here $n$=3) to determine the full $n$-bit converted value.

### 13.7.1 A simple SAR example

Successive-approximation ADCs can be extremely easy to use, as illustrated by the circuit in Figure 13.35. The SPI serial interface is simplicity itself: assertion of CS′ starts conversion, with successive bits clocked out by SCK (as each clock pulse triggers the SAR conversion of a new bit). The timing allows you to keep both serial lines quiet before assertion of CS′, as shown, to minimize coupled digital noise. This family of relatively low-speed converters integrates on-chip track-and-hold, and includes three speed grades, three resolutions (8, 10, and 12 bits), and four packaging options (single, dual, quad, and octal): 36 choices! (The figure shows how to construct the part numbers.) The single units, like the 12-bit 1 Msps specimen in the figure, come in tiny SOT23-6 packages, with prices (in single quantities) ranging from about $2 (8 bit, 200 ksps) to $4.50 (12 bit, 1 Msps).

The input of an ADC is often less benign than something like an op-amp, where we've come to expect a high impedance (very low input current), and low capacitance. Figure 13.36 shows the equivalent input circuit of this converter, with its 26 pF sampling capacitor that the input signal must drive. This is not much of a burden at the relatively low frequencies here; but it's something to keep in mind, for example in the circuit of Figure 13.37 with its much higher resolution (18 bits) and somewhat higher speeds.

### 13.7.2 Variations on successive approximation

A variation known as a "tracking ADC" uses an up–down counter to generate successive trial codes; it is slow in responding to jumps in the input signal, but it follows

[40] There are also hybrid designs, in which a charge redistribution DAC is used to subdivide the steps of a coarse resistor-string DAC.

[41] Actually, *two* such sets, because its input is differential.

**Table 13.5 Selected Successive-approximation A-to-D Converters[a]**

| Part # | ADCs per pkg | Bits | Conv Rate max (Msps) | Analog BW −3dB (MHz) | Channels/ADC | Single-ended | Differential | Internal Ref | Interface[k] | Power typ (mW) | Power at sps, $V_S$ | Analog Input $V_{in}$ min (V) | Analog Input $V_{in}$ max (V) | Analog Input $I_{bias}$ max (µA) | Supply $V_S$ min (V) | Supply $V_S$ max (V) | $I_{PD}$[h] (µA) | Pkgs, Pins SOIC | Pkgs, Pins TTSOP | Pkgs, Pins SOT-23 | Pkgs, Pins Smaller | Cost qty 25 ($US) | Comments |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| AD7927 | 1 | 12 | 0.2 | 8.2 | 8 | • | - | - | S | 3.6[m] | 200k, 3 | 0 | $V_{ref}$[e] | 1 | 2.7 | 5.25 | 0.5[m] | - | 20 | - | - | 5.33 | A |
| ADS7866 | 1 | 12 | 0.2 | 8 | 1 | • | - | - | S | 0.4 | 200k, 1.6 | 0 | $V_S$ | 1 | 1.2 | 3.6 | 0.3[m] | - | - | 6 | - | 3.69 | B |
| ADC121S | 1 | 12 | 1 | 11 | 1 | • | - | - | S | 2 | 1M, 3 | 0 | $V_S$ | 1 | 2.7 | 5.25 | 1[t] | - | - | 6 | 6 | 3.17 | C |
| ADS7881 | 1 | 12 | 4 | 50 | 1 | • | p | • | P | 95 | 4M, 5 | 0 | $V_{ref}$ | 0.5[t] | 4.75 | 5.25 | 2.5[m] | - | 48 | - | 48 | 14.52 | D |
| MAX11131 | 1 | 12 | 3 | 50 | 16 | • | • | - | S | 15 | 3M | 0 | $V_{ref}$ | 1.5 | 2.4 | 3.6 | 6[m] | - | 28 | - | 28 | 12.24 | E,Q |
| ADS7945[b] | 1 | 14 | 2 | 15 | 2 | - | • | - | S | 20 | 2M, 5 | 0 | $V_{ref}$ | 0.002 | 2.7 | 5.25 | 2.5[m] | - | - | - | 16 | 7.50 | F |
| MAX1300[d] | 1 | 16 | 0.11 | 0.7 | 8 | • | • | • | S | 17[m] | 100k, 5 | −16 | 16 | 1250 | 4.75 | 5.25 | 0.5[t] | - | 24 | - | - | 11.00 | M |
| LTC1609 | 1 | 16 | 0.2 | 1 | 1 | • | - | • | S | 65[c] | 200k, 5 | −10 | 10 | - | 4.75 | 5.25 | 10[t] | 20 | 28 | - | - | 20.42 | N |
| AD7685 | 1 | 16 | 0.25 | 2 | 1 | - | • | - | S | 2.7[c] | 200k, 2.5 | 0 | $V_{ref}$ | 0.001[t] | 2.3 | 5.5 | 0.05[m] | - | 10 | - | - | 11.31 | N |
| MAX11046 | 8 | 16 | 0.25 | 4 | 1 | • | - | • | P | 240 | 250k, 5 | −5 | 5 | 1 | 4.75 | 5.25 | 10[m] | - | 64 | - | 56 | 19.48 | O |
| MAX11166 | 1 | 16 | 0.5 | 6 | 1 | • | - | • | S | 26 | 500k, 5 | −5 | 5 | 10 | 4.75 | 5.25 | 10[m] | - | - | - | 12 | 35.20 | G,P |
| ADS8326 | 1 | 16 | 0.2 | 0.5 | 1 | - | • | - | S | 3.8[c] | 200k, 2.7 | 0 | $V_{ref}$ | 0.05[t] | 2.7 | 3.6[g] | 0.1[t] | - | 8 | - | - | 9.88 | N |
| AD7699 | 1 | 16 | 0.5 | 14 | 8 | • | - | • | S | 5.2 | 100k, 5 | 0 | $V_{ref}$ | 0.001[t] | 4.5 | 5.5 | 0.05[t] | - | - | - | 20 | 12.00 | H,N |
| ADS8319 | 1 | 16 | 0.5 | 15 | 1 | - | • | - | S | 18[c] | 500k, 5 | 0 | $V_{ref}$ | 0.001[t] | 4.5 | 5.5 | 0.3[m] | - | - | - | 10 | 11.86 | N,L |
| AD7985 | 1 | 16 | 2.5 | 19 | 1 | • | - | • | S | 28 | 2.5M, 5 | 0 | $V_{ref}$ | 0.25[t] | 4.75 | 5.25 | 1[t] | - | - | - | 20 | 28.18 | J,R |
| AD7690 | 1 | 18 | 0.4 | 9 | 1 | - | • | - | S | 4.3[c] | 100k, 5 | 0 | $V_{ref}$ | 0.001[t] | 4.75 | 5.25 | 0.05[m] | - | 10 | - | 9 | 30.19 | N,U |
| AD7982 | 1 | 18 | 1 | 9.0 | 1 | - | • | - | S | 7[c] | 1M, 2.7 | 0 | $V_{ref}$ | 0.2[t] | 2.38 | 2.63 | 0.35[t] | - | 10 | - | - | 33.52 | N |
| ADS8881 | 1 | 18 | 1 | 30 | 1 | - | • | - | S | 5.5[c] | 1M, 3 | 0 | $V_{ref}$ | 0.005[t] | 2.7 | 3.6 | 100[m] | - | 10 | - | 10 | 36.54 | N,V |
| LTC2379-18 | 1 | 18 | 1.6 | 34 | 1 | - | • | - | S | 18[c] | 1.6M | 0 | $V_{ref}$ | 1 | 2.38 | 2.63 | 100[m] | - | 16 | - | 16 | 42.79 | K,N |
| AD7641 | 1 | 18 | 2 | 50 | 1 | - | • | • | P,S | 75[c] | 2M, 2.5 | 0 | $V_{ref}$ | 18[t] | 2.37 | 2.62 | 0.6[t] | - | 48 | - | 48 | 43.56 | N |
| AD7767-2 | 1 | 24 | 0.032 | - | 1 | - | • | - | S | 8.5 | 1M | 0 | $V_{ref}$ | - | 2.38 | 2.63 | 1[t] | - | 16 | - | - | 14.32 | S |
| AD7767 | 1 | 24 | 0.128 | - | 1 | - | • | - | S | 15 | 1M | 0 | $V_{ref}$ | - | 2.38 | 2.63 | 1[t] | - | 16 | - | - | 14.32 | T |

**Notes:** (a) listed by accuracy and speed; all feature "no missing codes"; all permit external Vref input. (b) the ADS7946 is the same, without diff'l input. (c) power scales linearly with sample rate. (d) MAX1301 has half the number of inputs, in 20-pin TSSOP. (e) or to 2Vref, see datasheet. (f) with ext ref. (g) or 4.5-5.5V. (h) supply current during shutdown, power-down, or quiescent. (k) S=serial, P=parallel. (p) pseudo-differential.

**Comments: A:** sequencer; AD7928=1Msps. **B:** 10-bits='67, 8-bits='68, $1.80; 280ksps at $V_S$>1.6V; 8nA typ off, power-off after each conversion, 0.4µW at 100 per second, 44µW at 20ksps and $V_S$=1.2V. **C:** ADC121S051=500ksps, ADC121S021=200ksps. **D:** digital I/O supply 2.7V-5.25V. **E:** digital I/O supply 1.5V-3.6V. **F:** digital I/O supply 1.65V to $V_S$. **G:** digital I/O supply 2.3V-5.25V. **H:** digital I/O supply 1.8V to $V_S$. **J:** digital supply 2.4V-2.6V; digital I/O supply 1.8V-2.7V. **K:** digital I/O supply 1.7V-5.3V. **L:** digital I/O supply 2.4V-5.5V. **M:** PGA, 7 gain choices; 8 singled-ended or 4 diff'l inputs; $V_{in}$ up to ±3$V_{ref}$ or 6$V_{ref}$, or up to ±16V with $V_S$=5V. **N:** charge-redistribution (capacitive) SAR; power scales linearly with sample rate. **O:** 8 independent ADCs, simultaneous sampling; 6-ch=MAX11045, 4-ch=MAX11044. **P:** true "Beyond-the-Rails" without input dividers, ±5V with single $V_S$=+5; int $V_{ref}$ 17ppm/°C max. **Q:** FIFO; averaging; 1, 2, 4, .. 32 channel sequencer. **R:** int ref 10ppm/°C,typ; digital supply 2.4-2.6V. **S:** 32x oversampling, on-chip FIR filter. **T:** 8x oversampling, on-chip FIR filter. **U:** 100dB min SNR, 125dB typ THD. **V:** digital I/O supply 1.65-3.6V; ADS886x are 16-bit diff'l and single-ended versions; family includes slower versions, to 100ksps.

smooth changes somewhat more rapidly than a successive-approximation converter. For large changes its slew rate is proportional to its internal clocking rate. The succession of up–down bits is itself serial, a simple form of *delta modulation*.

Another variation is *CVSD* (continuously variable-slope delta modulation), a simple scheme that is sometimes used for 1-bit serial encoding of speech, for example in wireless phones. With CVSD modulation the 1s and 0s represent steps (up or down) of the input waveform, but with the step size adaptively changing according to the past history of the wave. For example, the step size corresponding to a 1 increases if the last few bits have all been 1s, according to a preset rule. The decoder knows the rule, so it can recreate an approximate replica of the (quantized) original analog input. In the past you could get CVSD chips, but in contemporary practice this is implemented in software in a microcontroller or DSP chip.

### 13.7.3 An A/D conversion example

Before continuing on to the important "integrating" conversion techniques (V-to-F, multislope, and *delta–sigma*), let's look at a demanding application example using a successive-approximation ADC: a low-noise, high-stability 18-bit converter with 2 Msps conversion rate.

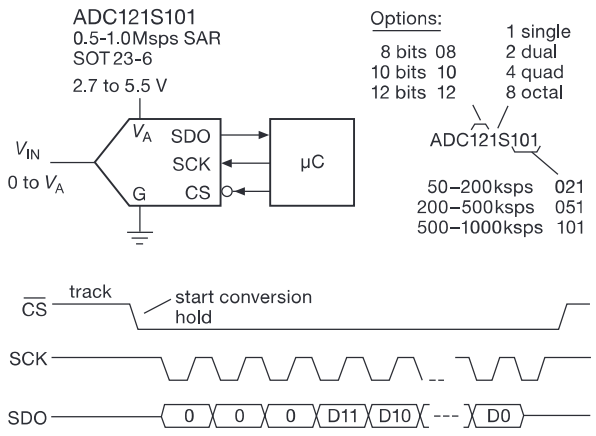


**Figure 13.35.** National Semiconductor's ADC08/10/12S family of simple-to-use successive-approximation ADC with SPI serial output.

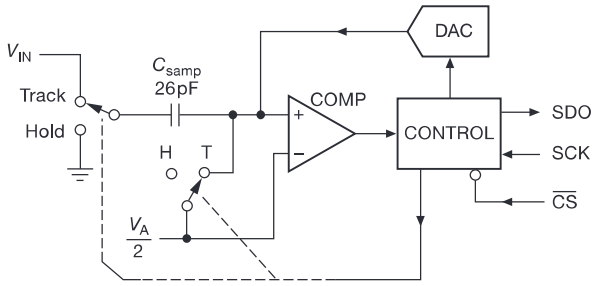


**Figure 13.36.** Block diagram of the ADC in Figure 13.35. The input signal drives the track-and-hold capacitor $C_{samp}$ during acquisition.

Figure 13.37 shows a typical high-performance ADC, in this case Analog Devices' 18-bit 2 Msps PulSAR-series AD7641 converter. The AD7641 uses three positive power supplies,[42] with the nice characteristic that they may be turned on and off in any sequence.

The AD7641 has a full scale range of $\pm V_{ref}$, as is common with low-voltage ADCs. To maintain quiet conversions it's desirable to use a large voltage reference and signal voltage ranges. The $AV_{DD}$ supply is 2.5 V, so the (differential) analog inputs are limited to 0 V to +2.5 V. If we use the maximum allowed +2.5 V reference, we get up to ±2.5 V (differential) full scale: as +IN goes from 0 V to +2.5 V, −IN will have to go from +2.5 V to 0 V (otherwise we'd have only a 17-bit converter). For an 18-bit converter this corresponds to a differential LSB step of just 19 µV. You have to take great care with such small signals, especially when the converter's sample rate is 2 MHz, and the −3dB bandwidth corresponding to its aperture time is 50 MHz – there's plenty of analog noise in these bandwidths,[43] aided and abetted by coupled digital noise from the happenings at the output end.

Both the signal and voltage reference inputs experience charge-injection pulses from the charge-redistribution conversion process, so we use sizable capacitors (the datasheet's recommended 2.7 nF) on these pins to maintain a quiet voltage.[44] Op-amps don't like direct capacitive loads, because they cause ringing in combination with the inductive closed-loop output impedance (see §4.6.2 and the section on capacitive loads in Chapter *4x*), hence the 15 Ω series resistors. This *RC* also acts as a 4 MHz low-pass filter to reduce out-of-band noise; in this bandwidth an LSB corresponds to a more relaxed noise density of 9.6 nV/$\sqrt{\text{Hz}}$. Note that the series resistor in the $V_{ref}$ path is larger (120 Ω) because we need to limit the peak current during power-supply startup, and the dc reference does not need the bandwidth of the signal paths.

The circuit shows an amplifier setup optimized for wideband operation with a single-ended input in the range 0 V to +1.25 V. The AD8021 is a wideband low-noise op-amp that is suggested in the ADC's datasheet. This may not be the best part to use,[45] but we'll continue our narrative with the manufacturer's suggested op-amp. The amplifier pair generates an accurate unipolarity differential output from the unipolarity single-ended input: the top stage has a noninverting voltage gain of +2, and the bottom inverting stage a gain of −2. Note the low resistor values, to maintain bandwidth and also reduce Johnson noise. To help ensure equal time delays, separate signal paths are used, instead of the alternative of cascaded amplifiers. Note how the inverting op-amp is biased at $V_{ref}/3$ to create the desired +2.5 V to 0 V signal. The two op-amp pathways have different noise gains, but the AD8021 lets us add a 10 pF capacitor to its compensation node to rolloff the response to achieve approximately equal bandwidths. To deal with the op-amp's high 7.5 µA input bias current, we've rigged

[42] Separate +2.5 V pins for the analog and digital sections, and a digital I/O pin that accepts +2.3 V to +3.6 V. Low-voltage ICs often need several supply voltages, requiring separate regulators.

[43] In a 50 MHz bandwidth, 19 µV rms noise corresponds to a noise density $e_n$ of just 2.7 nV/$\sqrt{\text{Hz}}$.

[44] Consider what's going on inside this successive-approximation ADC when operating at its full "warp-mode" speed of 2 Msps: its comparator has to make a new 19 µV decision every ∼20 ns. Hectic!

[45] The choice is a bit curious, because this op-amp is not "precision" – its maximum offset voltage is an unimpressive 1 mV, and its input bias current is a rather high 7.5 µA – evidently design tradeoffs needed to achieve far more speed than is needed here (100 MHz bandwidth, 20 ns settling time).

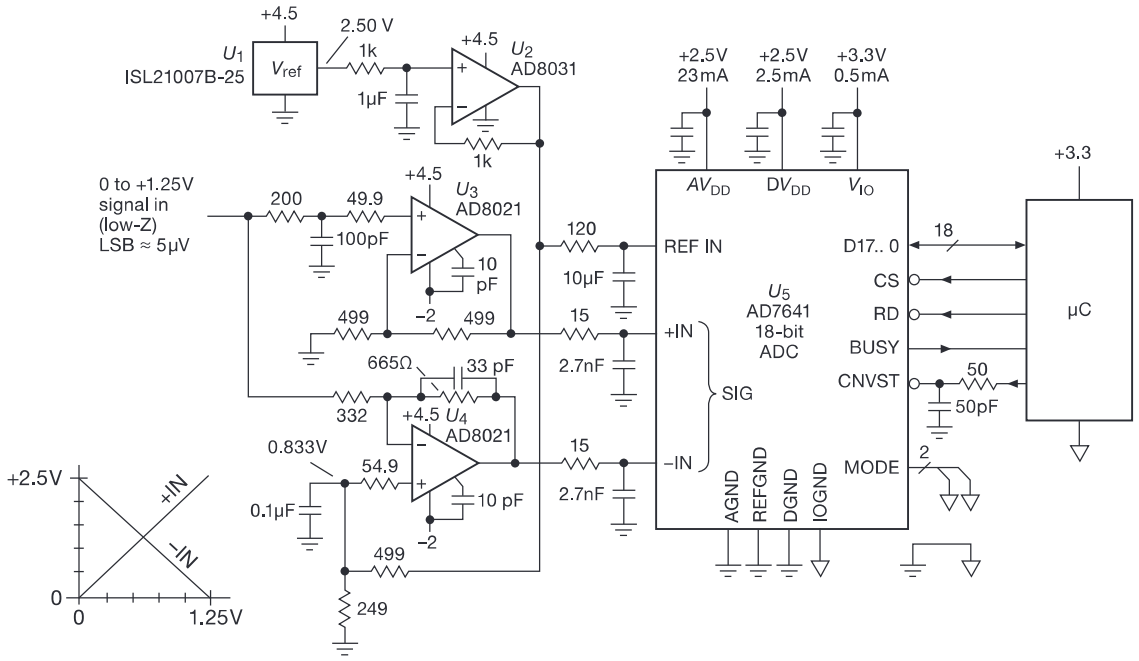


**Figure 13.37.** The AD7641 18-bit successive-approximation ADC, configured with fast op-amps for 2 Msps conversions.

up equal dc resistances seen at the inverting and noninverting inputs: this is effective here, because the typical offset current (0.1 $\mu$A) is 75 times smaller than the bias current itself.

The Intersil ISL21007/9BFB825 voltage reference (Table 9.8 on page 678) exploits floating-gate technology (i.e., a buried charged capacitor, §9.10.4) to achieve remarkably low drift over time ($<$10 ppm/$\sqrt{\text{kHr}}$). It has excellent initial accuracy (0.02%), and low tempco (3 ppm/°C). We've added a noise-quieting filter, and an op-amp is used to buffer the 3.3 mA load current to minimize power dissipation in the reference IC. The op-amps are powered from +4.5 V and −2.0 V, derived from the same ±5 V power that provides the regulated dc for the ADC (Figure 13.38), so that the op-amps are powered up at the same time as the ADC, thus minimizing clamp currents in the converter's input diodes at startup. Another way to prevent ADC input overdrive is to use a clamping op-amp like the AD8036, but this part has even larger dc errors than the AD8021. But there's a nice solution here, namely to clamp the $C_{\text{COMP}}$ pin of the AD8021 op-amp with a pair of low-capacitance (2 pF) SD101 Schottky diodes, one to ground and the other to the ADC's +2.5 V supply, as shown in Figure 13.39.[46]

The AD7641 converter is shown in its 18-bit parallel data mode, selecting by grounding both MODE pins.[47] The CNVST′ start-conversion signal is *RC* filtered (2.5 ns) to slow its fall-time and help prevent undershoot, etc., as suggested by Analog Devices. The CNVST′ signal should not return to the HIGH state until conversion is finished, about 400 ns in its high-speed "warp" mode.

## 13.8 ADCs III: integrating

### 13.8.1 Voltage-to-frequency conversion

We continue our tour of A/D conversion techniques with the V-to-F (or V/F) converter. In this method an analog input voltage is converted to an output pulse train whose frequency is proportional to the input level. This can be done simply by charging a capacitor with a current proportional to the input level and discharging it when the ramp reaches a preset threshold. For greater accuracy, a feedback method is generally used. In one technique you compare

[46] The AD8021 datasheet does not tell you about this trick. But it does show a simplified schematic, from which you can see that the signal at the $C_{\text{COMP}}$ pin is the (high-impedance) output of the gain stages, on its way to the zero-offset complementary emitter followers that form the output stage (Figure 13.39); i.e., it is a clampable high-*Z* replica of the output signal.

[47] The other choices are 16-bit parallel (two READ cycles), 8-bit parallel (three READ cycles), or SPI (clocked out over 18 clock cycles).