Computer Architecture & Design

Coen 316

Lab Experiment #1

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4017 5600

Section DN-X

Professor Dr. Fadi Alzouri

Performed on September 21, 2023

Due on October 5, 2023

“I certify that this submission is my original work and meets the Faculty’s Expectations of Originality.”

1) Introduction/Objectives

The objective of the first Coen 316 lab is to design a 32-bit Arithmetic and Logic Unit (ALU) in VHDL, which will used in the development of a CPU across the five labs. The ALU is responsible for performing various arithmetic and logic operations on two 32-bit input operands, as determined by control signals. These control signals allow the ALU to execute operations such as addition, subtraction, logical AND, OR, XOR, and NOR. Additionally, it should be able to detect overflow conditions as well as zero conditions. Overall, the objective of this lab aims to design, simulate, and implement the ALU using VHDL which will be used to verify its correct functionality through simulation, and demonstrate its operation on a Nexys A7 FPGA board.

2) Theory

ALU: "Arithmetic and Logic Unit", it is a key component of a computer's central processing unit (CPU) responsible for performing arithmetic and logical operations.

VHDL: "VHSIC Hardware Description Language", it is a programming language used for describing the behavior and structure of electronic systems.

FPGA: "Field-Programmable Gate Array,", it is a programmable hardware device that allows users to configure digital circuits to perform specific tasks.

CPU: "Central Processing Unit", it is the primary component of a computer that executes instructions and performs calculations.

MSB: "Most Significant Bit", it refers to the leftmost (or highest-weighted) bit in a binary number.

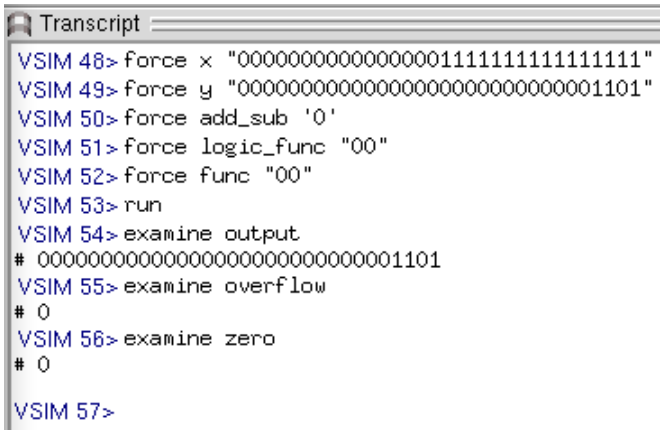
LSB: "Least Significant Bit", it refers to the rightmost (or lowest-weighted) bit in a binary number.

Overflow: In the context of arithmetic operations, overflow occurs when the result of an operation exceeds the range that can be represented with the available number of bits.

3) Tasks, Results and Discussion

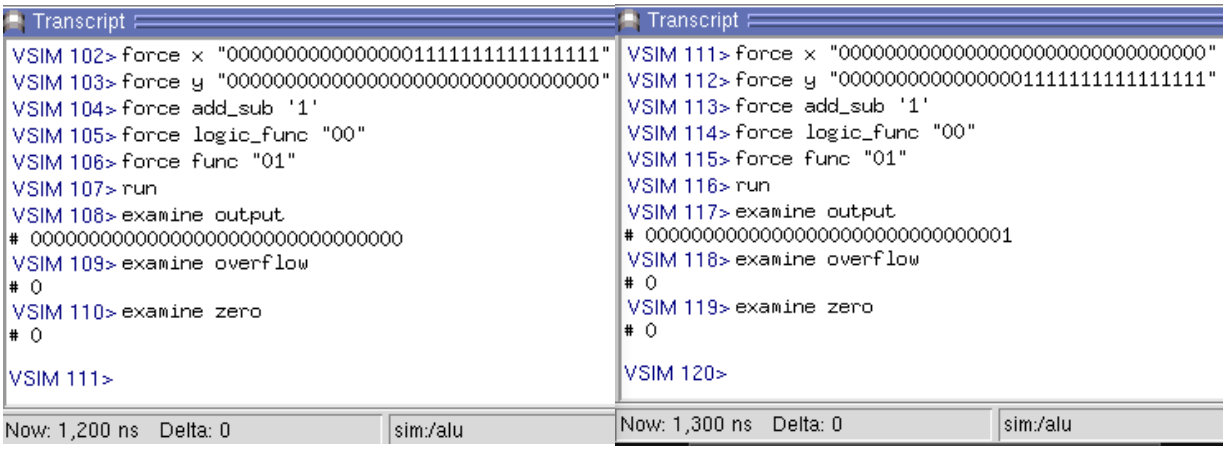
The following tasks are run by inputting DO codes found in the appendix. This section will show the results of each relevant input as well as discuss its behavior.

3.1) Output y, func = “00” (See appendix 5.2.1)



To test func = “00”, we first set “y” to be equal to 00000000000000000000000000001101 and we expect the output to always be equal to that regardless of the inputs of “add_sub” and “logic_func”. The first DO code of 5.2.1 tests the general output “y”, the second DO tests when changing “add_sub” while the third DO code tests when changing “logic_func”. In all three cases, the output is 00000000000000000000000000001101, thus func = “00” functions accordingly.

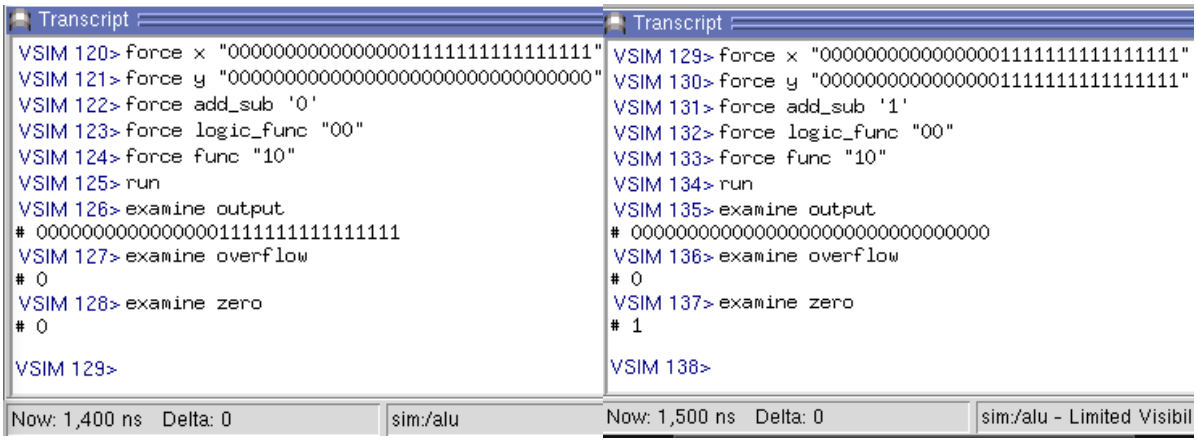
3.2) Output “000...MSB” of adder_subttract, func = “01” (See appendix 5.2.2)



Func = ”01” sets a specified register to 1 if input “x” is smaller than input “y” and 0 otherwise. The left example has “x” greater than “y”, thus we expect an output of 0 in which we do. On the other hand, for the right example, the input “x” is smaller than the input “y”, thus we expect an output of 1 in which we do.

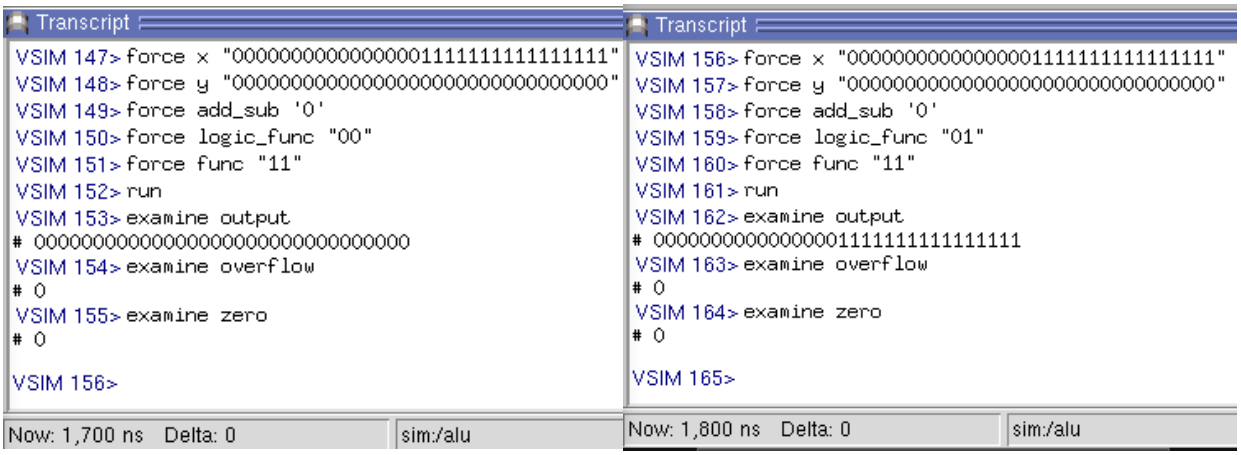
This behavior is obtained by performing “x – y” and checking the MSB of this result assuming it is a signed bit. If “x < y”, then this operation will yield a negative answer thus the MSB will be 1. If “x > y”, then this operation will yield a positive answer thus the MSB will be 0. This MSB will then be used in the func = “01” to determine the output of the system.

3.3) Output of adder_subtract, func = “10” (See appendix 5.2.3)

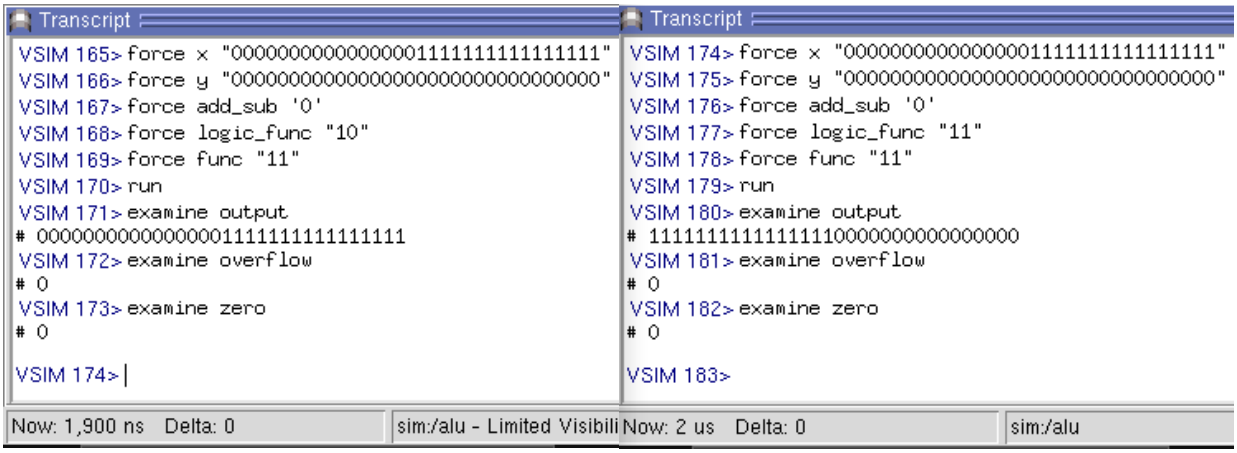


Given a set of “x” and “y” inputs, func = “10” will calculate the addition or the subtraction of the two inputs based on “add_sub”. In the left example, “add_sub” is ‘0’ which represents the addition operation. In the right example, “add_sub” is ‘1’ which represents the subtraction operation. In both cases, the results behave as expected.

3.4) Output of logic unit, func = “11” (See appendix 5.2.4)

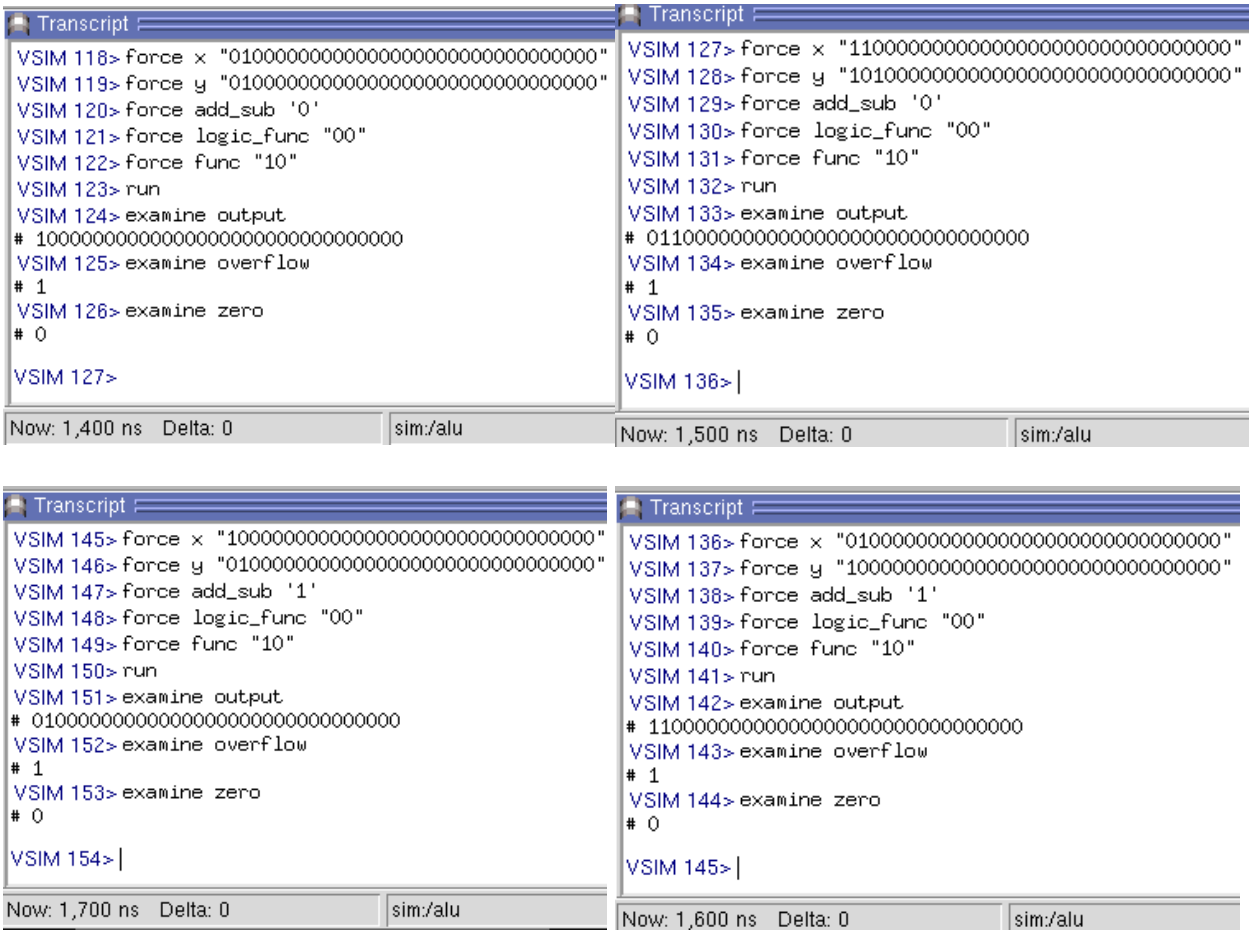


For the left example, given logic_func = “00”, the logic unit is an AND gate. Since input y is all zeros, the output also yields zeros. For the right example, logic_func = “01” which is an OR gate. The output being equal to input x as input y is all zeros.



For the left example, given logic_func = “10”, the logic unit is an XOR gate which outputs 1 only when both inputs are the opposite and 0 when both inputs are the same. Here, x and y are the same in the first half and they are different in the second half, thus we expect full of zeros in the first half and full of ones in the second half which we do get based on the left image above. For the right example, logic_func = “11” which is an NOR gate. This gate will output 1 if and only if both inputs are zeros. For our inputs, both x and y have zeros in the first half which means we expect the output to yields ones in the first half and zeros in the second half in which we do.

3.5) Overflow (See appendix 5.2.5)



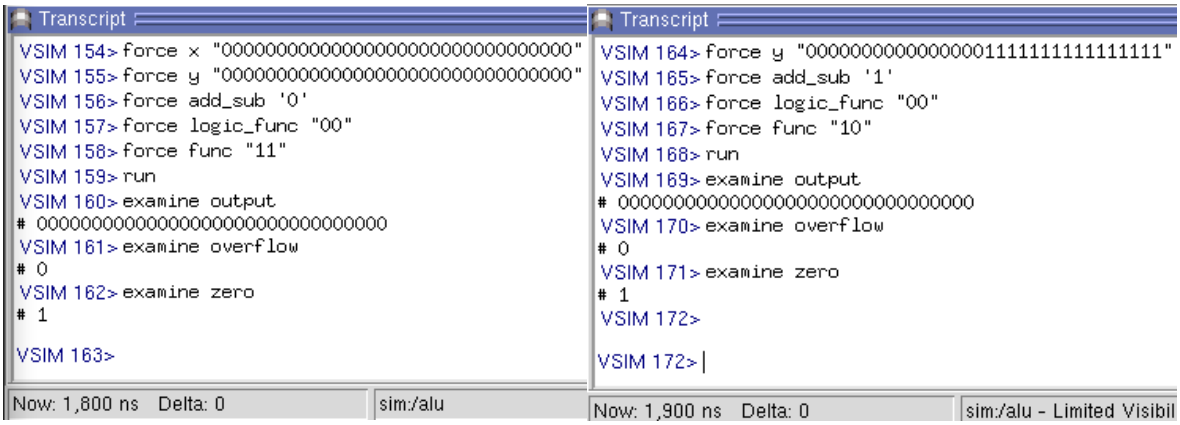
Top Left: Adding two positive num (x + y) and a negative result is obtained

Top Right: Adding two negative numbers (-x + -y) and a positive result is obtained

Bottom Left: Subtracting two operands of opposite sign (-x - y)

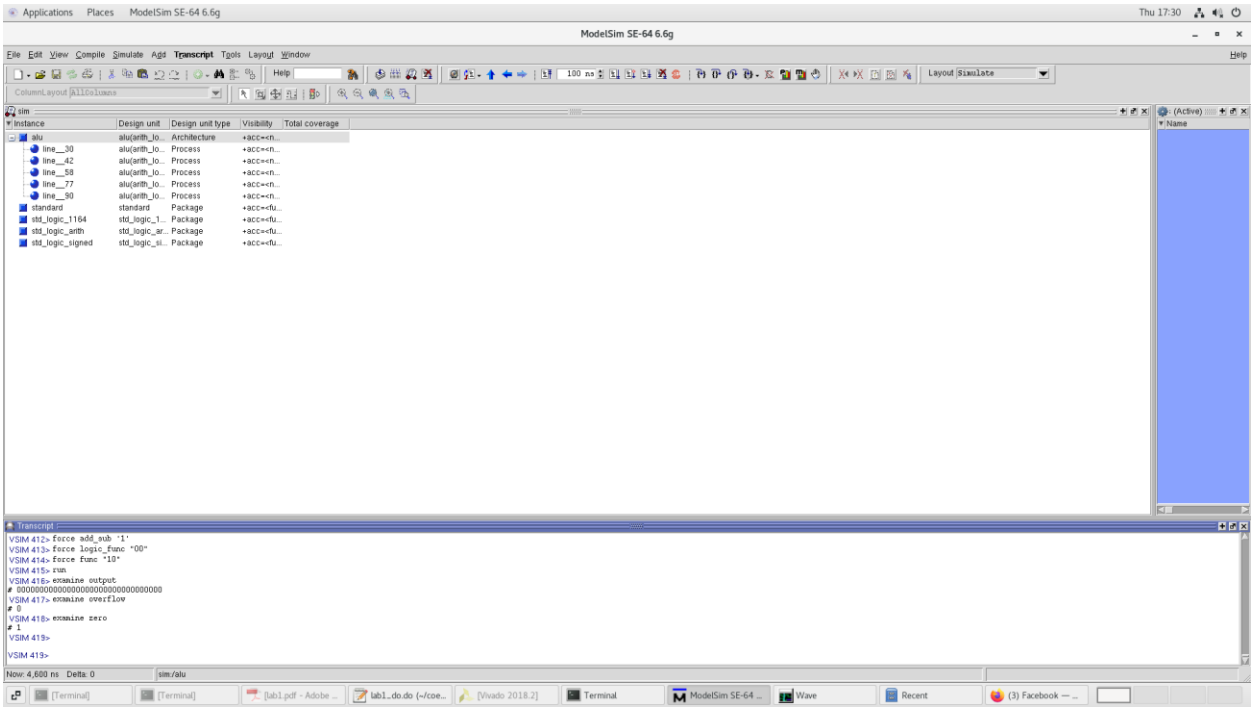
Bottom Right: Subtracting two operands of opposite sign (x - - y)

3.6) Zeros (See appendix 5.2.6)

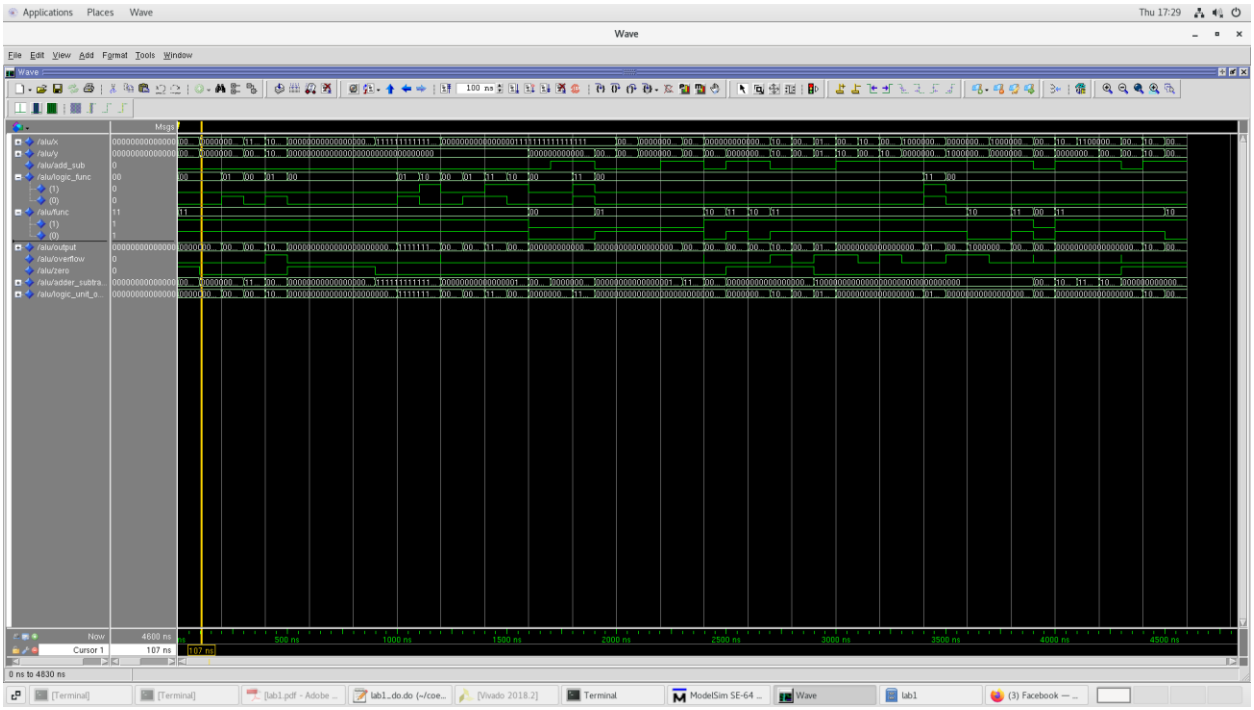


With func = “11”, the output of logic unit of x AND y yields all zeros due to x and y input being all zeros. As such, the zero is set to one (left image). With func = “10” and add_sub = ‘1’, we perform a subtraction between x and y, yielding zero. As such, zero is set to 1.

3.7) ModelSim Transcript



3.8) ModelSim Wave View



4) Conclusions

In conclusion, lab 1 of the course Coen 316 provided a comprehensive hands-on experience in designing, implementing and simulating a 32-bit Arithmetic and Logic Unit (ALU) using VHDL. This lab allows students to practice implementing various arithmetic and logic operations, to understand the difference between signed and unsigned bit as well as to detect overflows and zeros. Then, by simulating the design in ModelSim, it allowed the students to verify its output under various inputs, while the implementation on the Nexys A7 FPGA board demonstrated its practical functionality. In the end, this lab has provided valuable insights into digital design, FPGA-based hardware implementation, and the foundational components of a CPU, setting the foundation for the upcoming labs.

5) Appendix

5.1) Code

5.1.1) VHDL Code

```
-- coen 316 lab1
-- Andre Hei Wang Law
-- 4017 5600

library IEEE;
use IEEE.std_logic_1164.all;
use ieee.std_logic_signed.all;

entity alu is
	port (
	x, y: in std_logic_vector(31 downto 0);		-- two input
operands
	add_sub:	in std_logic;			-- 0=add, 1=sub
	logic_func:	in std_logic_vector(1 downto 0); -- 00=AND,
01=OR, 10=XOR, 11=NOR
	func:		in std_logic_vector(1 downto 0); -- 00=lui,
01=setless, 10=arith, 11=logic
	output:		out std_logic_vector(31 downto 0);
	overflow:	out std_logic;
	zero:		out std_logic);
end alu;

architecture arith_logic_unit of alu is

-- signal
signal adder_subtract_output, logic_unit_output: std_logic_vector(31
downto 0);

begin
	-- adder_subtract (add_sub)
	process(x, y, add_sub)
	begin
		-- check for addition or substraction
		if add_sub = '0' then
			adder_subtract_output <= x + y;		-- addition
		elsif add_sub = '1' then
			adder_subtract_output <= x - y;		-- substraction
		end if;
	end process;

	-- LINE 40
```

```
	-- logic unit (logic_func)
	process(x, y, logic_func)
	begin
		-- check for logic (AND, OR, XOR, NOR)
		if logic_func = "00" then
			logic_unit_output <= x AND y;	-- AND
		elsif logic_func = "01" then
			logic_unit_output <= x OR y;	-- OR
		elsif logic_func = "10" then
			logic_unit_output <= x XOR y;	-- XOR
		elsif logic_func = "11" then
			logic_unit_output <= x NOR y;	-- NOR
		end if;
	end process;

	-- mux (func)
	process(y, adder_subtract_output, logic_unit_output, func)
	begin
		-- determines output
		if func = "00" then
			output <= y;				-- y
		elsif func = "01" then
			-- output = 1 if x < y
			-- output = 0 otherwise
			-- "000...MSB" of adder_subttract
			output <= "00000000000000000000000000000000" &
adder_subtract_output(31);
		elsif func = "10" then
			output <= adder_subtract_output; -- output of
adder_subtract
		elsif func = "11" then
			output <= logic_unit_output;		-- output of
logic unit
		end if;
	end process;

	-- zero
	process(adder_subtract_output)
	begin
		-- zero = 1 when output of the adder_subtract unit is all
0s
		-- zero = 0 otherwise
		if adder_subtract_output =
"00000000000000000000000000000000" then
			zero <= '1';
		else
			zero <= '0';
		end if;
```

```
	end process;

	-- overflow
	process(adder_subtract_output, add_sub, x, y)
	begin
		-- overflow = 1 when:
			-- 1. Adding two positive num (x + y) and a negative
result is obtained
			-- 2. Adding two negative numbers (-x + -y) and a
possitive result is obtained
			-- 3. Substracting two operands of opposite sign (-x -
y)
			-- 4. Substracting two operands of opposite sign (x -
-y)

		-- 1. and 2. Addition
		if add_sub = '0' then
			if (x(31) = '0' and y(31) = '0' and
adder_subtract_output(31) = '1') or
			   (x(31) = '1' and y(31) = '1' and
adder_subtract_output(31) = '0') then
				overflow <= '1'; -- Overflow detected
			else
				overflow <= '0'; -- No overflow
			end if;
			--overflow <= (not(x(31)) AND not(y(31)) AND
adder_subtract_output(31)) OR (x(31) AND y(31) AND
not(adder_subtract_output(31)));

		-- 3. and 4. Substraction
		elsif add_sub = '1' then
			if (x(31) = '0' and y(31) = '1' and
adder_subtract_output(31) = '1') or
			   (x(31) = '1' and y(31) = '0' and
adder_subtract_output(31) = '0') then
				overflow <= '1'; -- Overflow detected
			else
				overflow <= '0'; -- No overflow
			end if;
			--overflow <= (x(31) AND not(y(31)) AND
not(adder_subtract_output(31))) OR (not(x(31)) AND y(31) AND
adder_subtract_output(31));
		end if;
	end process;

end arith_logic_unit;
```

5.1.2) Board Wrapper Version of the Original VHDL Code

```
-- coen 316 lab1
-- Andre Hei Wang Law
-- 4017 5600

-- board wrapper version

library IEEE;
use IEEE.std_logic_1164.all;
use ieee.std_logic_signed.all;

entity alu_board  is
     port (
    x_in, y_in: in std_logic_vector(3 downto 0);  -- Input ports for
low-order 4 bits of x and y
     add_sub:   in std_logic;                      -- 0=add, 1=sub
     logic_func:      in std_logic_vector(1 downto 0); -- 00=AND,
01=OR, 10=XOR, 11=NOR
     func:      in std_logic_vector(1 downto 0); -- 00=lui,
01=setless, 10=arith, 11=logic
    output_out: out std_logic_vector(3 downto 0); -- Output port for
low-order 4 bits of output
     overflow:  out std_logic;
     zero:      out std_logic);
end alu_board ;

architecture board_wrapper of alu_board  is

-- signal
signal adder_subtract_output, logic_unit_output: std_logic_vector(31
downto 0);
signal x, y, output : std_logic_vector(31 downto 0);

begin
     -- board wrapper
     -- assign port inputs to internal signals x and y
     x(3 downto 0) <= x_in(3) & x_in(2) & x_in(1) & x_in(0) ;
     y(3 downto 0) <= y_in(3) & y_in(2) & y_in(1) & y_in(0) ;
     x(31 downto 4) <= (others => '0');
     y(31 downto 4) <= (others => '0');
     output_out(3 downto 0) <= output(3 downto 0);

     -- adder_subtract (add_sub)
     process(x, y, add_sub)
     begin
          -- check for addition or substraction
          if add_sub = '0' then
```

```
                adder_subtract_output <= x + y;        -- addition
            elsif add_sub = '1' then
                adder_subtract_output <= x - y;        -- substraction
            end if;
      end process;

      -- LINE 40
      -- logic unit (logic_func)
      process(x, y, logic_func)
      begin
            -- check for logic (AND, OR, XOR, NOR)
            if logic_func = "00" then
                logic_unit_output <= x AND y;    -- AND
            elsif logic_func = "01" then
                logic_unit_output <= x OR y;     -- OR
            elsif logic_func = "10" then
                logic_unit_output <= x XOR y;    -- XOR
            elsif logic_func = "11" then
                logic_unit_output <= x NOR y;    -- NOR
            end if;
      end process;

      -- mux (func)
      process(y, adder_subtract_output, logic_unit_output, func)
      begin
            -- determines output
            if func = "00" then
                output <= y;                     -- y
            elsif func = "01" then
                -- output = 1 if x < y
                -- output = 0 otherwise
                -- "000...MSB" of adder_subttract
                output <= "00000000000000000000000000000000" &
adder_subtract_output(31);
            elsif func = "10" then
                output <= adder_subtract_output; -- output of
adder_subtract
            elsif func = "11" then
                output <= logic_unit_output;          -- output of
logic unit
            end if;
      end process;

      -- zero
      process(adder_subtract_output)
      begin
            -- zero = 1 when output of the adder_subtract unit is all
0s
```

```
            -- zero = 0 otherwise
            if adder_subtract_output =
"00000000000000000000000000000000" then
                  zero <= '1';
            else
                  zero <= '0';
            end if;
      end process;

      -- overflow
      process(adder_subtract_output, add_sub, x, y)
      begin
            -- overflow = 1 when:
                  -- 1. Adding two positive num (x + y) and a negative
result is obtained
                  -- 2. Adding two negative numbers (-x + -y) and a
possitive result is obtained
                  -- 3. Substracting two operands of opposite sign (-x -
y)
                  -- 4. Substracting two operands of opposite sign (x -
-y)

            -- 1. and 2. Addition
            if add_sub = '0' then
                  if (x(31) = '0' and y(31) = '0' and
adder_subtract_output(31) = '1') or
                     (x(31) = '1' and y(31) = '1' and
adder_subtract_output(31) = '0') then
                        overflow <= '1'; -- Overflow detected
                  else
                        overflow <= '0'; -- No overflow
                  end if;
                  --overflow <= (not(x(31)) AND not(y(31)) AND
adder_subtract_output(31)) OR (x(31) AND y(31) AND
not(adder_subtract_output(31)));

            -- 3. and 4. Substraction
            elsif add_sub = '1' then
                  if (x(31) = '0' and y(31) = '1' and
adder_subtract_output(31) = '1') or
                     (x(31) = '1' and y(31) = '0' and
adder_subtract_output(31) = '0') then
                        overflow <= '1'; -- Overflow detected
                  else
                        overflow <= '0'; -- No overflow
                  end if;
                  --overflow <= (x(31) AND not(y(31)) AND
not(adder_subtract_output(31))) OR (not(x(31)) AND y(31) AND
```

```
adder_subtract_output(31));
            end if;
      end process;

end board_wrapper;
```

5.2.1) DO File to Test Various Output – y (func = “00”)

```
force x "00000000000000001111111111111111"
force y "00000000000000000000000000001101"
force add_sub '0'
force logic_func "00"
force func "00"
run
examine output
examine overflow
examine zero

force x "00000000000000001111111111111111"
force y "00000000000000000000000000001101"
force add_sub '1'
force logic_func "00"
force func "00"
run
examine output
examine overflow
examine zero

force x "00000000000000001111111111111111"
force y "00000000000000000000000000001101"
force add_sub '1'
force logic_func "11"
force func "00"
run
examine output
examine overflow
examine zero
```

5.2.2) DO File to Test Various Output – “000...MSB” of adder_subttract (func = “01”)

```
force x "00000000000000001111111111111111"
force y "00000000000000000000000000000000"
force add_sub '1'
force logic_func "00"
```

```
force func "01"
run
examine output
examine overflow
examine zero

force x "00000000000000000000000000000000"
force y "00000000000000001111111111111111"
force add_sub '1'
force logic_func "00"
force func "01"
run
examine output
examine overflow
examine zero
```

5.2.3) DO File to Test Various Output – output of adder_subtract (func = “10”)

```
force x "00000000000000001111111111111111"
force y "00000000000000000000000000000000"
force add_sub '0'
force logic_func "00"
force func "10"
run
examine output
examine overflow
examine zero

force x "00000000000000001111111111111111"
force y "00000000000000001111111111111111"
force add_sub '1'
force logic_func "00"
force func "10"
run
examine output
examine overflow
examine zero
```

5.2.4) DO File to Test Various Output – Logic unit, AND, OR, XOR, NOR (func = “11”)

```
force x "00000000000000001111111111111111"
force y "00000000000000000000000000000000"
force add_sub '0'
force logic_func "00"
force func "11"
```

```
run
examine output
examine overflow
examine zero

force x "00000000000000001111111111111111"
force y "00000000000000000000000000000000"
force add_sub '0'
force logic_func "01"
force func "11"
run
examine output
examine overflow
examine zero

force x "00000000000000001111111111111111"
force y "00000000000000000000000000000000"
force add_sub '0'
force logic_func "10"
force func "11"
run
examine output
examine overflow
examine zero

force x "00000000000000001111111111111111"
force y "00000000000000000000000000000000"
force add_sub '0'
force logic_func "11"
force func "11"
run
examine output
examine overflow
examine zero
```

5.2.5) DO File to Test Various Output – Overflow (MSB = ‘1’)

```
force x "00000000000000000000000000000000"
force y "01000000000000000000000000000000"
force add_sub '0'
force logic_func "00"
force func "10"
run
examine output
examine overflow
examine zero
```

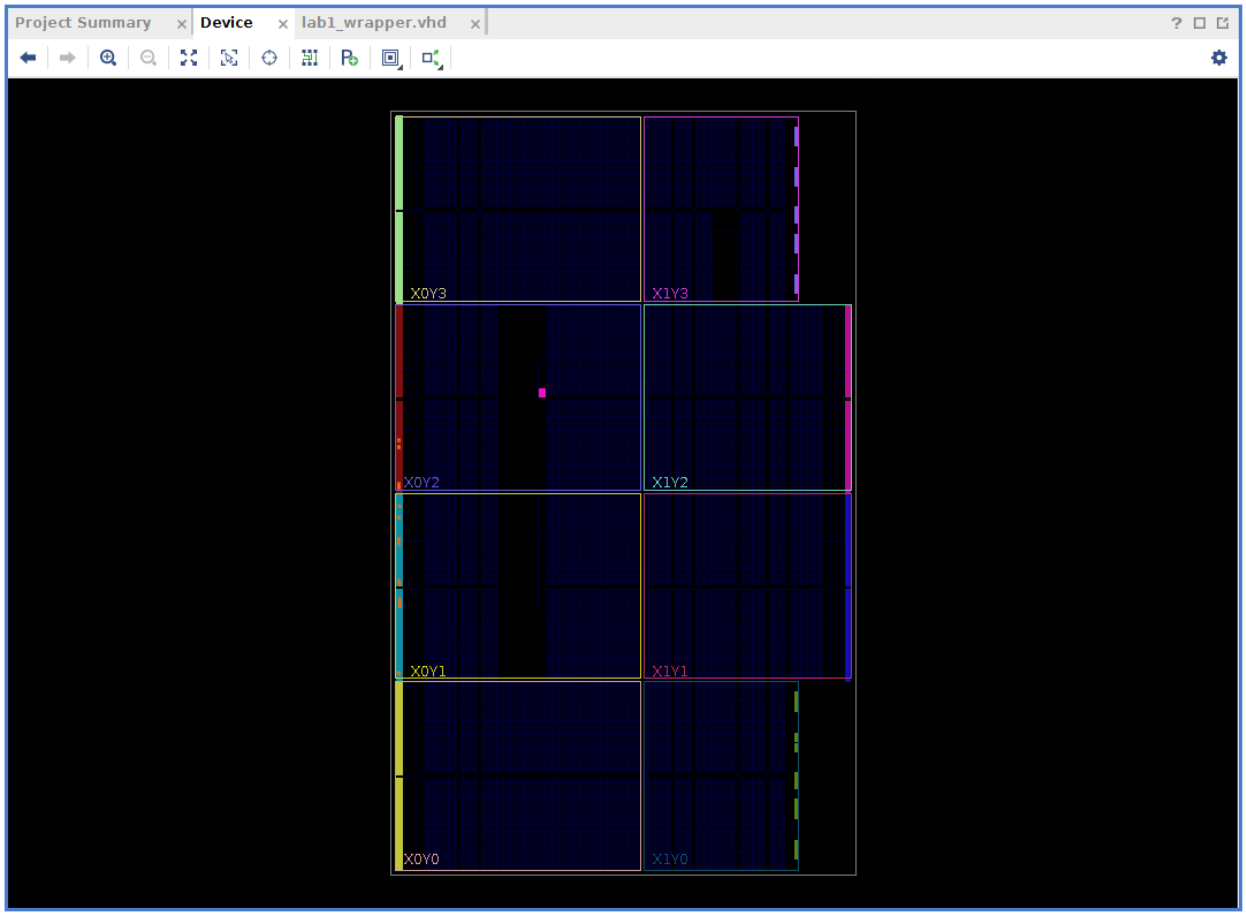
```
force x "01000000000000000000000000000000"
force y "01000000000000000000000000000000"
force add_sub '0'
force logic_func "00"
force func "10"
run
examine output
examine overflow
examine zero

force x "11000000000000000000000000000000"
force y "10100000000000000000000000000000"
force add_sub '0'
force logic_func "00"
force func "10"
run
examine output
examine overflow
examine zero

force x "01000000000000000000000000000000"
force y "10000000000000000000000000000000"
force add_sub '1'
force logic_func "00"
force func "10"
run
examine output
examine overflow
examine zero

force x "10000000000000000000000000000000"
force y "01000000000000000000000000000000"
force add_sub '1'
force logic_func "00"
force func "10"
run
examine output
examine overflow
examine zero
```

5.2.6) DO File to Test Various Output – Zero (add_sub = '1' and add_sub = '0')

```
force x "00000000000000000000000000000000"
force y "00000000000000000000000000000000"
force add_sub '0'
```

```
force logic_func "00"
force func "11"
run
examine output
examine overflow
examine zero

force x "00000000000000001111111111111111"
force y "00000000000000001111111111111111"
force add_sub '1'
force logic_func "00"
force func "10"
run
examine output
examine overflow
examine zero
```

5.3) Synthesis Log



Warning Discussion: While there is no critical error, we have 13 warnings, in which most is about the unused inputs such as “output_reg”, “logic_unit_output_reg”. This doesn’t cause any problem to the functionality of this sytem.

```
*** Running vivado
    with args -log alu_board.vds -m64 -product Vivado -mode batch -messageDb vivado.pb
-notrace -source alu_board.tcl


****** Vivado v2018.2 (64-bit)
  **** SW Build 2258646 on Thu Jun 14 20:02:38 MDT 2018
  **** IP Build 2256618 on Thu Jun 14 22:10:49 MDT 2018
    ** Copyright 1986-2018 Xilinx, Inc. All Rights Reserved.

source alu_board.tcl -notrace
Command: synth_design -top alu_board -part xc7a100tcsg324-1
Starting synth_design
Attempting to get a license for feature 'Synthesis' and/or device 'xc7a100t'
INFO: [Common 17-349] Got license for feature 'Synthesis' and/or device 'xc7a100t'
INFO: Launching helper process for spawning children vivado processes
INFO: Helper process launched with PID 28374
---------------------------------------------------------------------------------
Starting RTL Elaboration : Time (s): cpu = 00:00:02 ; elapsed = 00:00:04 . Memory
(MB): peak = 1468.590 ; gain = 86.727 ; free physical = 81343 ; free virtual = 154593
---------------------------------------------------------------------------------
INFO: [Synth 8-638] synthesizing module 'alu_board'
[/nfs/home/l/l_heiwan/coen316/lab1/lab1_wrapper.vhd:22]
INFO: [Synth 8-256] done synthesizing module 'alu_board' (1#1)
[/nfs/home/l/l_heiwan/coen316/lab1/lab1_wrapper.vhd:22]
---------------------------------------------------------------------------------
Finished RTL Elaboration : Time (s): cpu = 00:00:03 ; elapsed = 00:00:06 . Memory
(MB): peak = 1513.230 ; gain = 131.367 ; free physical = 81356 ; free virtual = 154606
---------------------------------------------------------------------------------
```

```
Report Check Netlist:
+------+------------------+-------+---------+-------+------------------+
|      |Item              |Errors |Warnings |Status |Description       |
+------+------------------+-------+---------+-------+------------------+
|1     |multi_driven_nets |      0|        0|Passed |Multi driven nets |
+------+------------------+-------+---------+-------+------------------+
-------------------------------------------------------------------------------
Start Handling Custom Attributes
-------------------------------------------------------------------------------
-------------------------------------------------------------------------------
Finished Handling Custom Attributes : Time (s): cpu = 00:00:03 ; elapsed = 00:00:06 .
Memory (MB): peak = 1513.230 ; gain = 131.367 ; free physical = 81355 ; free virtual =
154605
-------------------------------------------------------------------------------
-------------------------------------------------------------------------------
Finished RTL Optimization Phase 1 : Time (s): cpu = 00:00:03 ; elapsed = 00:00:06 .
Memory (MB): peak = 1513.230 ; gain = 131.367 ; free physical = 81355 ; free virtual =
154605
-------------------------------------------------------------------------------
INFO: [Device 21-403] Loading part xc7a100tcsg324-1
INFO: [Project 1-570] Preparing netlist for logic optimization

Processing XDC Constraints
Initializing timing engine
Parsing XDC File [/nfs/home/l/l_heiwan/coen316/lab1/lab1_constraints.xdc]
Finished Parsing XDC File [/nfs/home/l/l_heiwan/coen316/lab1/lab1_constraints.xdc]
INFO: [Project 1-236] Implementation specific constraints were found while reading
constraint file [/nfs/home/l/l_heiwan/coen316/lab1/lab1_constraints.xdc]. These
constraints will be ignored for synthesis but will be used in implementation. Impacted
constraints are listed in the file [.Xil/alu_board_propImpl.xdc].
Resolution: To avoid this warning, move constraints listed in
[.Xil/alu_board_propImpl.xdc] to another XDC file and exclude this new file from
synthesis with the used_in_synthesis property (File Properties dialog in GUI) and re-
run elaboration/synthesis.
Completed Processing XDC Constraints

INFO: [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.

Constraint Validation Runtime : Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory
(MB): peak = 1878.156 ; gain = 0.000 ; free physical = 81012 ; free virtual = 154263
-------------------------------------------------------------------------------
Finished Constraint Validation : Time (s): cpu = 00:00:16 ; elapsed = 00:01:08 .
Memory (MB): peak = 1878.156 ; gain = 496.293 ; free physical = 81164 ; free virtual =
154414
-------------------------------------------------------------------------------
-------------------------------------------------------------------------------
Start Loading Part and Timing Information
-------------------------------------------------------------------------------
Loading part: xc7a100tcsg324-1
-------------------------------------------------------------------------------
Finished Loading Part and Timing Information : Time (s): cpu = 00:00:16 ; elapsed =
00:01:08 . Memory (MB): peak = 1878.156 ; gain = 496.293 ; free physical = 81164 ;
free virtual = 154414
-------------------------------------------------------------------------------
-------------------------------------------------------------------------------
Start Applying 'set_property' XDC Constraints
```

```
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished applying 'set_property' XDC Constraints : Time (s): cpu = 00:00:16 ; elapsed
= 00:01:08 . Memory (MB): peak = 1878.156 ; gain = 496.293 ; free physical = 81166 ;
free virtual = 154416
---------------------------------------------------------------------------------
INFO: [Synth 8-5818] HDL ADVISOR - The operator resource <adder> is shared. To prevent
sharing consider applying a KEEP on the output of the operator
[/nfs/home/l/l_heiwan/coen316/lab1/lab1_wrapper.vhd:41]
WARNING: [Synth 8-3936] Found unconnected internal register 'output_reg' and it is
trimmed from '32' to '4' bits. [/nfs/home/l/l_heiwan/coen316/lab1/lab1_wrapper.vhd:35]
WARNING: [Synth 8-3936] Found unconnected internal register 'logic_unit_output_reg'
and it is trimmed from '32' to '4' bits.
[/nfs/home/l/l_heiwan/coen316/lab1/lab1_wrapper.vhd:54]
WARNING: [Synth 8-327] inferring latch for variable 'output_reg'
[/nfs/home/l/l_heiwan/coen316/lab1/lab1_wrapper.vhd:35]
WARNING: [Synth 8-327] inferring latch for variable 'logic_unit_output_reg'
[/nfs/home/l/l_heiwan/coen316/lab1/lab1_wrapper.vhd:54]
---------------------------------------------------------------------------------
Finished RTL Optimization Phase 2 : Time (s): cpu = 00:00:16 ; elapsed = 00:01:08 .
Memory (MB): peak = 1878.156 ; gain = 496.293 ; free physical = 81157 ; free virtual =
154408
---------------------------------------------------------------------------------

Report RTL Partitions:
+-+--------------+------------+----------+
| |RTL Partition |Replication |Instances |
+-+--------------+------------+----------+
+-+--------------+------------+----------+
---------------------------------------------------------------------------------
Start RTL Component Statistics
---------------------------------------------------------------------------------
Detailed RTL Component Info :
+---Adders :
          3 Input     32 Bit       Adders := 1
+---XORs :
          2 Input      4 Bit         XORs := 1
+---Muxes :
          2 Input     32 Bit        Muxes := 1
          4 Input      4 Bit        Muxes := 2
          2 Input      1 Bit        Muxes := 1
          4 Input      1 Bit        Muxes := 2
---------------------------------------------------------------------------------
Finished RTL Component Statistics
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start RTL Hierarchical Component Statistics
---------------------------------------------------------------------------------
Hierarchical RTL Component report
Module alu_board
Detailed RTL Component Info :
+---Adders :
          3 Input     32 Bit       Adders := 1
+---XORs :
          2 Input      4 Bit         XORs := 1
+---Muxes :
          2 Input     32 Bit        Muxes := 1
          4 Input      4 Bit        Muxes := 2
```

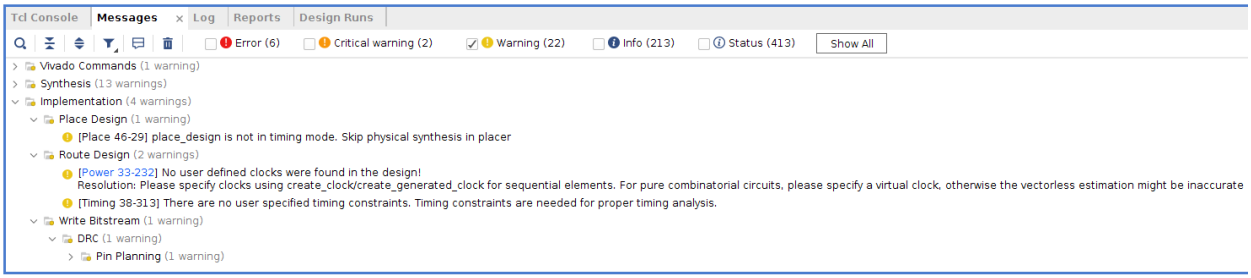
```
          2 Input      1 Bit        Muxes := 1
          4 Input      1 Bit        Muxes := 2
---------------------------------------------------------------------------------
Finished RTL Hierarchical Component Statistics
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start Part Resource Summary
---------------------------------------------------------------------------------
Part Resources:
DSPs: 240 (col length:80)
BRAMs: 270 (col length: RAMB18 80 RAMB36 40)
---------------------------------------------------------------------------------
Finished Part Resource Summary
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start Cross Boundary and Area Optimization
---------------------------------------------------------------------------------
Warning: Parallel synthesis criteria is not met
WARNING: [Synth 8-3332] Sequential element (output_reg[3]) is unused and will be
removed from module alu_board.
WARNING: [Synth 8-3332] Sequential element (output_reg[2]) is unused and will be
removed from module alu_board.
WARNING: [Synth 8-3332] Sequential element (output_reg[1]) is unused and will be
removed from module alu_board.
WARNING: [Synth 8-3332] Sequential element (output_reg[0]) is unused and will be
removed from module alu_board.
WARNING: [Synth 8-3332] Sequential element (logic_unit_output_reg[3]) is unused and
will be removed from module alu_board.
WARNING: [Synth 8-3332] Sequential element (logic_unit_output_reg[2]) is unused and
will be removed from module alu_board.
WARNING: [Synth 8-3332] Sequential element (logic_unit_output_reg[1]) is unused and
will be removed from module alu_board.
WARNING: [Synth 8-3332] Sequential element (logic_unit_output_reg[0]) is unused and
will be removed from module alu_board.
---------------------------------------------------------------------------------
Finished Cross Boundary and Area Optimization : Time (s): cpu = 00:00:16 ; elapsed =
00:01:09 . Memory (MB): peak = 1878.156 ; gain = 496.293 ; free physical = 81136 ;
free virtual = 154388
---------------------------------------------------------------------------------

Report RTL Partitions:
+-+--------------+------------+----------+
| |RTL Partition |Replication |Instances |
+-+--------------+------------+----------+
+-+--------------+------------+----------+
---------------------------------------------------------------------------------
Start Applying XDC Timing Constraints
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished Applying XDC Timing Constraints : Time (s): cpu = 00:00:23 ; elapsed =
00:01:27 . Memory (MB): peak = 1878.156 ; gain = 496.293 ; free physical = 81019 ;
free virtual = 154271
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start Timing Optimization
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished Timing Optimization : Time (s): cpu = 00:00:23 ; elapsed = 00:01:27 . Memory
```

```
(MB): peak = 1878.156 ; gain = 496.293 ; free physical = 81019 ; free virtual = 154271
---------------------------------------------------------------------------------

Report RTL Partitions:
+-+--------------+------------+----------+
| |RTL Partition |Replication |Instances |
+-+--------------+------------+----------+
+-+--------------+------------+----------+
---------------------------------------------------------------------------------
Start Technology Mapping
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished Technology Mapping : Time (s): cpu = 00:00:23 ; elapsed = 00:01:27 . Memory
(MB): peak = 1878.156 ; gain = 496.293 ; free physical = 81019 ; free virtual = 154271
---------------------------------------------------------------------------------

Report RTL Partitions:
+-+--------------+------------+----------+
| |RTL Partition |Replication |Instances |
+-+--------------+------------+----------+
+-+--------------+------------+----------+
---------------------------------------------------------------------------------
Start IO Insertion
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start Flattening Before IO Insertion
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished Flattening Before IO Insertion
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start Final Netlist Cleanup
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished Final Netlist Cleanup
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished IO Insertion : Time (s): cpu = 00:00:24 ; elapsed = 00:01:28 . Memory (MB):
peak = 1878.156 ; gain = 496.293 ; free physical = 81019 ; free virtual = 154271
---------------------------------------------------------------------------------

Report Check Netlist:
+------+------------------+-------+---------+-------+------------------+
|      |Item              |Errors |Warnings |Status |Description       |
+------+------------------+-------+---------+-------+------------------+
|1     |multi_driven_nets |      0|        0|Passed |Multi driven nets |
+------+------------------+-------+---------+-------+------------------+
---------------------------------------------------------------------------------
Start Renaming Generated Instances
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished Renaming Generated Instances : Time (s): cpu = 00:00:24 ; elapsed =
00:01:28 . Memory (MB): peak = 1878.156 ; gain = 496.293 ; free physical = 81019 ;
free virtual = 154271
---------------------------------------------------------------------------------

Report RTL Partitions:
+-+--------------+------------+----------+
```

```
| |RTL Partition |Replication |Instances |
+-+--------------+------------+----------+
+-+--------------+------------+----------+
---------------------------------------------------------------------------------
Start Rebuilding User Hierarchy
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished Rebuilding User Hierarchy : Time (s): cpu = 00:00:24 ; elapsed = 00:01:28 .
Memory (MB): peak = 1878.156 ; gain = 496.293 ; free physical = 81019 ; free virtual =
154271
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start Renaming Generated Ports
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished Renaming Generated Ports : Time (s): cpu = 00:00:24 ; elapsed = 00:01:28 .
Memory (MB): peak = 1878.156 ; gain = 496.293 ; free physical = 81019 ; free virtual =
154271
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start Handling Custom Attributes
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished Handling Custom Attributes : Time (s): cpu = 00:00:24 ; elapsed = 00:01:28 .
Memory (MB): peak = 1878.156 ; gain = 496.293 ; free physical = 81019 ; free virtual =
154271
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start Renaming Generated Nets
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished Renaming Generated Nets : Time (s): cpu = 00:00:24 ; elapsed = 00:01:28 .
Memory (MB): peak = 1878.156 ; gain = 496.293 ; free physical = 81019 ; free virtual =
154271
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start Writing Synthesis Report
---------------------------------------------------------------------------------

Report BlackBoxes:
+-+--------------+----------+
| |BlackBox name |Instances |
+-+--------------+----------+
+-+--------------+----------+

Report Cell Usage:
+------+-----+------+
|      |Cell |Count |
+------+-----+------+
|1     |LUT4 |     3|
|2     |LUT5 |     6|
|3     |LUT6 |     7|
|4     |IBUF |    13|
|5     |OBUF |     6|
+------+-----+------+

Report Instance Areas:
+------+---------+-------+------+
```

```
|      |Instance |Module |Cells |
+------+---------+-------+------+
|1     |top      |       |    35|
+------+---------+-------+------+
-------------------------------------------------------------------------------
Finished Writing Synthesis Report : Time (s): cpu = 00:00:24 ; elapsed = 00:01:28 .
Memory (MB): peak = 1878.156 ; gain = 496.293 ; free physical = 81019 ; free virtual =
154271
-------------------------------------------------------------------------------
Synthesis finished with 0 errors, 0 critical warnings and 12 warnings.
Synthesis Optimization Runtime : Time (s): cpu = 00:00:13 ; elapsed = 00:00:30 .
Memory (MB): peak = 1878.156 ; gain = 131.367 ; free physical = 81073 ; free virtual =
154325
Synthesis Optimization Complete : Time (s): cpu = 00:00:24 ; elapsed = 00:01:28 .
Memory (MB): peak = 1878.156 ; gain = 496.293 ; free physical = 81083 ; free virtual =
154335
INFO: [Project 1-571] Translating synthesized netlist
INFO: [Netlist 29-17] Analyzing 13 Unisim elements for replacement
INFO: [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
INFO: [Project 1-570] Preparing netlist for logic optimization
INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
INFO: [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.

INFO: [Common 17-83] Releasing license: Synthesis
15 Infos, 12 Warnings, 0 Critical Warnings and 0 Errors encountered.
synth_design completed successfully
synth_design: Time (s): cpu = 00:00:26 ; elapsed = 00:01:30 . Memory (MB): peak =
1908.801 ; gain = 539.664 ; free physical = 81063 ; free virtual = 154315
WARNING: [Constraints 18-5210] No constraint will be written out.
INFO: [Common 17-1381] The checkpoint
'/nfs/home/l/l_heiwan/coen316/lab1/vivado_test_v2/vivado_leb1_v2/vivado_leb1_v2.runs/s
ynth_1/alu_board.dcp' has been generated.
INFO: [runtcl-4] Executing : report_utilization -file alu_board_utilization_synth.rpt
-pb alu_board_utilization_synth.pb
report_utilization: Time (s): cpu = 00:00:00.05 ; elapsed = 00:00:00.12 . Memory (MB):
peak = 1932.820 ; gain = 0.000 ; free physical = 81066 ; free virtual = 154318
INFO: [Common 17-206] Exiting Vivado at Wed Oct  4 17:58:37 2023...
```

5.4) Implementation Log



Warning Discussion: For the implementation log, we have 22 warnings. The warnings are about the lack of timing mode, user defined clock as well as timing constraints. Due to that, our system

may not behave as expected in terms of timing and performance which may result in many issues when we generate the Bitstream.

```
*** Running vivado
    with args -log alu_board.vdi -applog -m64 -product Vivado -messageDb vivado.pb -
mode batch -source alu_board.tcl -notrace


****** Vivado v2018.2 (64-bit)
  **** SW Build 2258646 on Thu Jun 14 20:02:38 MDT 2018
  **** IP Build 2256618 on Thu Jun 14 22:10:49 MDT 2018
    ** Copyright 1986-2018 Xilinx, Inc. All Rights Reserved.

source alu_board.tcl -notrace
Command: link_design -top alu_board -part xc7a100tcsg324-1
Design is defaulting to srcset: sources_1
Design is defaulting to constrset: constrs_1
INFO: [Netlist 29-17] Analyzing 13 Unisim elements for replacement
INFO: [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
INFO: [Project 1-479] Netlist was created with Vivado 2018.2
INFO: [Device 21-403] Loading part xc7a100tcsg324-1
INFO: [Project 1-570] Preparing netlist for logic optimization
Parsing XDC File [/nfs/home/l/l_heiwan/coen316/lab1/lab1_constraints.xdc]
CRITICAL WARNING: [Common 17-69] Command failed: 'H18' is not a valid site or package
pin name. [/nfs/home/l/l_heiwan/coen316/lab1/lab1_constraints.xdc:21]
Finished Parsing XDC File [/nfs/home/l/l_heiwan/coen316/lab1/lab1_constraints.xdc]
INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
INFO: [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.

7 Infos, 0 Warnings, 1 Critical Warnings and 0 Errors encountered.
link_design completed successfully
link_design: Time (s): cpu = 00:00:11 ; elapsed = 00:00:58 . Memory (MB): peak =
1702.559 ; gain = 328.414 ; free physical = 81127 ; free virtual = 154417
Command: opt_design
Attempting to get a license for feature 'Implementation' and/or device 'xc7a100t'
INFO: [Common 17-349] Got license for feature 'Implementation' and/or device
'xc7a100t'
Running DRC as a precondition to command opt_design

Starting DRC Task
INFO: [DRC 23-27] Running DRC with 8 threads
INFO: [Project 1-461] DRC finished with 0 Errors
INFO: [Project 1-462] Please refer to the DRC report (report_drc) for more
information.

Time (s): cpu = 00:00:01 ; elapsed = 00:00:04 . Memory (MB): peak = 1777.586 ; gain =
75.027 ; free physical = 81124 ; free virtual = 154414

Starting Cache Timing Information Task
INFO: [Timing 38-35] Done setting XDC timing constraints.
Ending Cache Timing Information Task | Checksum: 1ba47c1aa

Time (s): cpu = 00:00:15 ; elapsed = 00:01:10 . Memory (MB): peak = 2219.082 ; gain =
```

```
441.496 ; free physical = 80705 ; free virtual = 153995

Starting Logic Optimization Task

Phase 1 Retarget
INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
INFO: [Opt 31-49] Retargeted 0 cell(s).
Phase 1 Retarget | Checksum: 1ba47c1aa

Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00.02 . Memory (MB): peak = 2219.082 ;
gain = 0.000 ; free physical = 80730 ; free virtual = 154020
INFO: [Opt 31-389] Phase Retarget created 0 cells and removed 0 cells

Phase 2 Constant propagation
INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
Phase 2 Constant propagation | Checksum: 1ba47c1aa

Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00.02 . Memory (MB): peak = 2219.082 ;
gain = 0.000 ; free physical = 80730 ; free virtual = 154020
INFO: [Opt 31-389] Phase Constant propagation created 0 cells and removed 0 cells

Phase 3 Sweep
Phase 3 Sweep | Checksum: 1ba47c1aa

Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00.03 . Memory (MB): peak = 2219.082 ;
gain = 0.000 ; free physical = 80730 ; free virtual = 154020
INFO: [Opt 31-389] Phase Sweep created 0 cells and removed 0 cells

Phase 4 BUFG optimization
Phase 4 BUFG optimization | Checksum: 1ba47c1aa

Time (s): cpu = 00:00:00.02 ; elapsed = 00:00:00.03 . Memory (MB): peak = 2219.082 ;
gain = 0.000 ; free physical = 80730 ; free virtual = 154020
INFO: [Opt 31-662] Phase BUFG optimization created 0 cells of which 0 are BUFGs and
removed 0 cells.

Phase 5 Shift Register Optimization
Phase 5 Shift Register Optimization | Checksum: 1ba47c1aa

Time (s): cpu = 00:00:00.02 ; elapsed = 00:00:00.03 . Memory (MB): peak = 2219.082 ;
gain = 0.000 ; free physical = 80730 ; free virtual = 154020
INFO: [Opt 31-389] Phase Shift Register Optimization created 0 cells and removed 0
cells

Phase 6 Post Processing Netlist
Phase 6 Post Processing Netlist | Checksum: 1ba47c1aa

Time (s): cpu = 00:00:00.02 ; elapsed = 00:00:00.03 . Memory (MB): peak = 2219.082 ;
gain = 0.000 ; free physical = 80730 ; free virtual = 154020
INFO: [Opt 31-389] Phase Post Processing Netlist created 0 cells and removed 0 cells

Starting Connectivity Check Task

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2219.082 ; gain =
0.000 ; free physical = 80730 ; free virtual = 154020
Ending Logic Optimization Task | Checksum: 1ba47c1aa

Time (s): cpu = 00:00:00.02 ; elapsed = 00:00:00.03 . Memory (MB): peak = 2219.082 ;
```

```
gain = 0.000 ; free physical = 80730 ; free virtual = 154020

Starting Power Optimization Task
INFO: [Pwropt 34-132] Skipping clock gating for clocks with a period < 2.00 ns.
Ending Power Optimization Task | Checksum: 1ba47c1aa

Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00.05 . Memory (MB): peak = 2219.086 ;
gain = 0.004 ; free physical = 80730 ; free virtual = 154020

Starting Final Cleanup Task
Ending Final Cleanup Task | Checksum: 1ba47c1aa

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2219.086 ; gain =
0.000 ; free physical = 80730 ; free virtual = 154020
INFO: [Common 17-83] Releasing license: Implementation
23 Infos, 0 Warnings, 1 Critical Warnings and 0 Errors encountered.
opt_design completed successfully
opt_design: Time (s): cpu = 00:00:17 ; elapsed = 00:01:14 . Memory (MB): peak =
2219.086 ; gain = 516.527 ; free physical = 80730 ; free virtual = 154020
INFO: [Timing 38-480] Writing timing data to binary archive.
Writing placer database...
Writing XDEF routing.
Writing XDEF routing logical nets.
Writing XDEF routing special nets.
Write XDEF Complete: Time (s): cpu = 00:00:00.03 ; elapsed = 00:00:00.02 . Memory
(MB): peak = 2251.102 ; gain = 0.004 ; free physical = 80727 ; free virtual = 154018
INFO: [Common 17-1381] The checkpoint
'/nfs/home/l/l_heiwan/coen316/lab1/vivado_test_v2/vivado_leb1_v2/vivado_leb1_v2.runs/i
mpl_1/alu_board_opt.dcp' has been generated.
INFO: [runtcl-4] Executing : report_drc -file alu_board_drc_opted.rpt -pb
alu_board_drc_opted.pb -rpx alu_board_drc_opted.rpx
Command: report_drc -file alu_board_drc_opted.rpt -pb alu_board_drc_opted.pb -rpx
alu_board_drc_opted.rpx
INFO: [IP_Flow 19-234] Refreshing IP repositories
INFO: [IP_Flow 19-1704] No user IP repositories specified
INFO: [IP_Flow 19-2313] Loaded Vivado IP repository
'/CMC/tools/xilinx/Vivado_2018.2/Vivado/2018.2/data/ip'.
INFO: [DRC 23-27] Running DRC with 8 threads
INFO: [Coretcl 2-168] The results of DRC are in file
/nfs/home/l/l_heiwan/coen316/lab1/vivado_test_v2/vivado_leb1_v2/vivado_leb1_v2.runs/im
pl_1/alu_board_drc_opted.rpt.
report_drc completed successfully
report_drc: Time (s): cpu = 00:00:04 ; elapsed = 00:00:07 . Memory (MB): peak =
2323.137 ; gain = 72.027 ; free physical = 80699 ; free virtual = 153990
Command: place_design
Attempting to get a license for feature 'Implementation' and/or device 'xc7a100t'
INFO: [Common 17-349] Got license for feature 'Implementation' and/or device
'xc7a100t'
INFO: [DRC 23-27] Running DRC with 8 threads
INFO: [Vivado_Tcl 4-198] DRC finished with 0 Errors
INFO: [Vivado_Tcl 4-199] Please refer to the DRC report (report_drc) for more
information.
Running DRC as a precondition to command place_design
INFO: [DRC 23-27] Running DRC with 8 threads
INFO: [Vivado_Tcl 4-198] DRC finished with 0 Errors
INFO: [Vivado_Tcl 4-199] Please refer to the DRC report (report_drc) for more
information.
```

```
Starting Placer Task
INFO: [Place 30-611] Multithreading enabled for place_design using a maximum of 8 CPUs

Phase 1 Placer Initialization

Phase 1.1 Placer Initialization Netlist Sorting
Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB):
peak = 2323.137 ; gain = 0.000 ; free physical = 80694 ; free virtual = 153984
Phase 1.1 Placer Initialization Netlist Sorting | Checksum: 11f970856

Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00.03 . Memory (MB): peak = 2323.137 ;
gain = 0.000 ; free physical = 80694 ; free virtual = 153984
Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB):
peak = 2323.137 ; gain = 0.000 ; free physical = 80694 ; free virtual = 153984

Phase 1.2 IO Placement/ Clock Placement/ Build Placer Device
INFO: [Timing 38-35] Done setting XDC timing constraints.
Phase 1.2 IO Placement/ Clock Placement/ Build Placer Device | Checksum: ef51f4b0

Time (s): cpu = 00:00:00.62 ; elapsed = 00:00:00.55 . Memory (MB): peak = 2323.137 ;
gain = 0.000 ; free physical = 80688 ; free virtual = 153980

Phase 1.3 Build Placer Netlist Model
Phase 1.3 Build Placer Netlist Model | Checksum: 139371e35

Time (s): cpu = 00:00:00.66 ; elapsed = 00:00:00.58 . Memory (MB): peak = 2323.137 ;
gain = 0.000 ; free physical = 80688 ; free virtual = 153980

Phase 1.4 Constrain Clocks/Macros
Phase 1.4 Constrain Clocks/Macros | Checksum: 139371e35

Time (s): cpu = 00:00:00.67 ; elapsed = 00:00:00.58 . Memory (MB): peak = 2323.137 ;
gain = 0.000 ; free physical = 80688 ; free virtual = 153980
Phase 1 Placer Initialization | Checksum: 139371e35

Time (s): cpu = 00:00:00.67 ; elapsed = 00:00:00.58 . Memory (MB): peak = 2323.137 ;
gain = 0.000 ; free physical = 80688 ; free virtual = 153980

Phase 2 Global Placement

Phase 2.1 Floorplanning
Phase 2.1 Floorplanning | Checksum: 139371e35

Time (s): cpu = 00:00:00.70 ; elapsed = 00:00:00.61 . Memory (MB): peak = 2323.137 ;
gain = 0.000 ; free physical = 80686 ; free virtual = 153978
WARNING: [Place 46-29] place_design is not in timing mode. Skip physical synthesis in
placer
Phase 2 Global Placement | Checksum: 13ef44abb

Time (s): cpu = 00:00:03 ; elapsed = 00:00:01 . Memory (MB): peak = 2402.160 ; gain =
79.023 ; free physical = 80655 ; free virtual = 153946

Phase 3 Detail Placement

Phase 3.1 Commit Multi Column Macros
Phase 3.1 Commit Multi Column Macros | Checksum: 13ef44abb

Time (s): cpu = 00:00:03 ; elapsed = 00:00:01 . Memory (MB): peak = 2402.160 ; gain =
```

```
79.023 ; free physical = 80655 ; free virtual = 153946

Phase 3.2 Commit Most Macros & LUTRAMs
Phase 3.2 Commit Most Macros & LUTRAMs | Checksum: 1782f7d91

Time (s): cpu = 00:00:03 ; elapsed = 00:00:01 . Memory (MB): peak = 2402.160 ; gain =
79.023 ; free physical = 80654 ; free virtual = 153946

Phase 3.3 Area Swap Optimization
Phase 3.3 Area Swap Optimization | Checksum: 15db6ed33

Time (s): cpu = 00:00:03 ; elapsed = 00:00:01 . Memory (MB): peak = 2402.160 ; gain =
79.023 ; free physical = 80654 ; free virtual = 153945

Phase 3.4 Pipeline Register Optimization
Phase 3.4 Pipeline Register Optimization | Checksum: 15db6ed33

Time (s): cpu = 00:00:03 ; elapsed = 00:00:01 . Memory (MB): peak = 2402.160 ; gain =
79.023 ; free physical = 80654 ; free virtual = 153945

Phase 3.5 Small Shape Detail Placement
Phase 3.5 Small Shape Detail Placement | Checksum: 26336c14f

Time (s): cpu = 00:00:03 ; elapsed = 00:00:01 . Memory (MB): peak = 2402.160 ; gain =
79.023 ; free physical = 80650 ; free virtual = 153942

Phase 3.6 Re-assign LUT pins
Phase 3.6 Re-assign LUT pins | Checksum: 26336c14f

Time (s): cpu = 00:00:03 ; elapsed = 00:00:01 . Memory (MB): peak = 2402.160 ; gain =
79.023 ; free physical = 80650 ; free virtual = 153942

Phase 3.7 Pipeline Register Optimization
Phase 3.7 Pipeline Register Optimization | Checksum: 26336c14f

Time (s): cpu = 00:00:03 ; elapsed = 00:00:01 . Memory (MB): peak = 2402.160 ; gain =
79.023 ; free physical = 80650 ; free virtual = 153942
Phase 3 Detail Placement | Checksum: 26336c14f

Time (s): cpu = 00:00:03 ; elapsed = 00:00:01 . Memory (MB): peak = 2402.160 ; gain =
79.023 ; free physical = 80650 ; free virtual = 153942

Phase 4 Post Placement Optimization and Clean-Up

Phase 4.1 Post Commit Optimization
Phase 4.1 Post Commit Optimization | Checksum: 26336c14f

Time (s): cpu = 00:00:03 ; elapsed = 00:00:01 . Memory (MB): peak = 2402.160 ; gain =
79.023 ; free physical = 80650 ; free virtual = 153942

Phase 4.2 Post Placement Cleanup
Phase 4.2 Post Placement Cleanup | Checksum: 26336c14f

Time (s): cpu = 00:00:03 ; elapsed = 00:00:01 . Memory (MB): peak = 2402.160 ; gain =
79.023 ; free physical = 80652 ; free virtual = 153944

Phase 4.3 Placer Reporting
Phase 4.3 Placer Reporting | Checksum: 26336c14f
```

```
Time (s): cpu = 00:00:03 ; elapsed = 00:00:01 . Memory (MB): peak = 2402.160 ; gain =
79.023 ; free physical = 80652 ; free virtual = 153944

Phase 4.4 Final Placement Cleanup
Phase 4.4 Final Placement Cleanup | Checksum: 26336c14f

Time (s): cpu = 00:00:03 ; elapsed = 00:00:01 . Memory (MB): peak = 2402.160 ; gain =
79.023 ; free physical = 80652 ; free virtual = 153944
Phase 4 Post Placement Optimization and Clean-Up | Checksum: 26336c14f

Time (s): cpu = 00:00:03 ; elapsed = 00:00:01 . Memory (MB): peak = 2402.160 ; gain =
79.023 ; free physical = 80652 ; free virtual = 153944
Ending Placer Task | Checksum: 164242381

Time (s): cpu = 00:00:03 ; elapsed = 00:00:01 . Memory (MB): peak = 2402.160 ; gain =
79.023 ; free physical = 80670 ; free virtual = 153962
INFO: [Common 17-83] Releasing license: Implementation
41 Infos, 1 Warnings, 1 Critical Warnings and 0 Errors encountered.
place_design completed successfully
place_design: Time (s): cpu = 00:00:05 ; elapsed = 00:00:05 . Memory (MB): peak =
2402.160 ; gain = 79.023 ; free physical = 80670 ; free virtual = 153962
INFO: [Timing 38-480] Writing timing data to binary archive.
Writing placer database...
Writing XDEF routing.
Writing XDEF routing logical nets.
Writing XDEF routing special nets.
Write XDEF Complete: Time (s): cpu = 00:00:00.03 ; elapsed = 00:00:00.02 . Memory
(MB): peak = 2402.160 ; gain = 0.000 ; free physical = 80670 ; free virtual = 153963
INFO: [Common 17-1381] The checkpoint
'/nfs/home/l/l_heiwan/coen316/lab1/vivado_test_v2/vivado_leb1_v2/vivado_leb1_v2.runs/i
mpl_1/alu_board_placed.dcp' has been generated.
INFO: [runtcl-4] Executing : report_io -file alu_board_io_placed.rpt
report_io: Time (s): cpu = 00:00:00.08 ; elapsed = 00:00:00.17 . Memory (MB): peak =
2402.160 ; gain = 0.000 ; free physical = 80671 ; free virtual = 153963
INFO: [runtcl-4] Executing : report_utilization -file alu_board_utilization_placed.rpt
-pb alu_board_utilization_placed.pb
report_utilization: Time (s): cpu = 00:00:00.05 ; elapsed = 00:00:00.13 . Memory (MB):
peak = 2402.160 ; gain = 0.000 ; free physical = 80675 ; free virtual = 153966
INFO: [runtcl-4] Executing : report_control_sets -verbose -file
alu_board_control_sets_placed.rpt
report_control_sets: Time (s): cpu = 00:00:00.03 ; elapsed = 00:00:00.10 . Memory
(MB): peak = 2402.160 ; gain = 0.000 ; free physical = 80677 ; free virtual = 153969
Command: route_design
Attempting to get a license for feature 'Implementation' and/or device 'xc7a100t'
INFO: [Common 17-349] Got license for feature 'Implementation' and/or device
'xc7a100t'
Running DRC as a precondition to command route_design
INFO: [DRC 23-27] Running DRC with 8 threads
INFO: [Vivado_Tcl 4-198] DRC finished with 0 Errors
INFO: [Vivado_Tcl 4-199] Please refer to the DRC report (report_drc) for more
information.


Starting Routing Task
INFO: [Route 35-254] Multithreading enabled for route_design using a maximum of 8 CPUs
Checksum: PlaceDB: a1bd30de ConstDB: 0 ShapeSum: c266f2a3 RouteDB: 0
```

```
Phase 1 Build RT Design
Phase 1 Build RT Design | Checksum: 9cb15b26

Time (s): cpu = 00:00:24 ; elapsed = 00:00:20 . Memory (MB): peak = 2442.766 ; gain =
40.605 ; free physical = 80536 ; free virtual = 153829
Post Restoration Checksum: NetGraph: 72390a4d NumContArr: 2a7850d9 Constraints: 0
Timing: 0

Phase 2 Router Initialization
INFO: [Route 35-64] No timing constraints were detected. The router will operate in
resource-optimization mode.

Phase 2.1 Fix Topology Constraints
Phase 2.1 Fix Topology Constraints | Checksum: 9cb15b26

Time (s): cpu = 00:00:25 ; elapsed = 00:00:20 . Memory (MB): peak = 2448.754 ; gain =
46.594 ; free physical = 80504 ; free virtual = 153797

Phase 2.2 Pre Route Cleanup
Phase 2.2 Pre Route Cleanup | Checksum: 9cb15b26

Time (s): cpu = 00:00:25 ; elapsed = 00:00:20 . Memory (MB): peak = 2448.754 ; gain =
46.594 ; free physical = 80504 ; free virtual = 153797
 Number of Nodes with overlaps = 0
Phase 2 Router Initialization | Checksum: e9bf0ed7

Time (s): cpu = 00:00:25 ; elapsed = 00:00:20 . Memory (MB): peak = 2456.020 ; gain =
53.859 ; free physical = 80502 ; free virtual = 153794

Phase 3 Initial Routing
Phase 3 Initial Routing | Checksum: 1ae1173b4

Time (s): cpu = 00:00:25 ; elapsed = 00:00:21 . Memory (MB): peak = 2456.020 ; gain =
53.859 ; free physical = 80500 ; free virtual = 153792

Phase 4 Rip-up And Reroute

Phase 4.1 Global Iteration 0
 Number of Nodes with overlaps = 1
 Number of Nodes with overlaps = 0
Phase 4.1 Global Iteration 0 | Checksum: e1852293

Time (s): cpu = 00:00:25 ; elapsed = 00:00:21 . Memory (MB): peak = 2456.020 ; gain =
53.859 ; free physical = 80500 ; free virtual = 153792
Phase 4 Rip-up And Reroute | Checksum: e1852293

Time (s): cpu = 00:00:25 ; elapsed = 00:00:21 . Memory (MB): peak = 2456.020 ; gain =
53.859 ; free physical = 80500 ; free virtual = 153792

Phase 5 Delay and Skew Optimization
Phase 5 Delay and Skew Optimization | Checksum: e1852293

Time (s): cpu = 00:00:25 ; elapsed = 00:00:21 . Memory (MB): peak = 2456.020 ; gain =
53.859 ; free physical = 80500 ; free virtual = 153792

Phase 6 Post Hold Fix

Phase 6.1 Hold Fix Iter
```

```
Phase 6.1 Hold Fix Iter | Checksum: e1852293

Time (s): cpu = 00:00:25 ; elapsed = 00:00:21 . Memory (MB): peak = 2456.020 ; gain =
53.859 ; free physical = 80500 ; free virtual = 153792
Phase 6 Post Hold Fix | Checksum: e1852293

Time (s): cpu = 00:00:25 ; elapsed = 00:00:21 . Memory (MB): peak = 2456.020 ; gain =
53.859 ; free physical = 80500 ; free virtual = 153792

Phase 7 Route finalize

Router Utilization Summary
  Global Vertical Routing Utilization    = 0.0322932 %
  Global Horizontal Routing Utilization  = 0.004973 %
  Routable Net Status*
  *Does not include unroutable nets such as driverless and loadless.
  Run report_route_status for detailed report.
  Number of Failed Nets                = 0
  Number of Unrouted Nets              = 0
  Number of Partially Routed Nets      = 0
  Number of Node Overlaps              = 0

Congestion Report
North Dir 1x1 Area, Max Cong = 21.6216%, No Congested Regions.
South Dir 1x1 Area, Max Cong = 16.2162%, No Congested Regions.
East Dir 1x1 Area, Max Cong = 5.88235%, No Congested Regions.
West Dir 1x1 Area, Max Cong = 5.88235%, No Congested Regions.

------------------------------
Reporting congestion hotspots
------------------------------
Direction: North
----------------
Congested clusters found at Level 0
Effective congestion level: 0 Aspect Ratio: 1 Sparse Ratio: 0
Direction: South
----------------
Congested clusters found at Level 0
Effective congestion level: 0 Aspect Ratio: 1 Sparse Ratio: 0
Direction: East
----------------
Congested clusters found at Level 0
Effective congestion level: 0 Aspect Ratio: 1 Sparse Ratio: 0
Direction: West
----------------
Congested clusters found at Level 0
Effective congestion level: 0 Aspect Ratio: 1 Sparse Ratio: 0

Phase 7 Route finalize | Checksum: e1852293

Time (s): cpu = 00:00:25 ; elapsed = 00:00:21 . Memory (MB): peak = 2456.020 ; gain =
53.859 ; free physical = 80499 ; free virtual = 153791

Phase 8 Verifying routed nets

 Verification completed successfully
Phase 8 Verifying routed nets | Checksum: e1852293
```

```
Time (s): cpu = 00:00:25 ; elapsed = 00:00:21 . Memory (MB): peak = 2458.020 ; gain =
55.859 ; free physical = 80498 ; free virtual = 153790

Phase 9 Depositing Routes
Phase 9 Depositing Routes | Checksum: 110efca31

Time (s): cpu = 00:00:25 ; elapsed = 00:00:21 . Memory (MB): peak = 2458.020 ; gain =
55.859 ; free physical = 80499 ; free virtual = 153791
INFO: [Route 35-16] Router Completed Successfully

Time (s): cpu = 00:00:25 ; elapsed = 00:00:21 . Memory (MB): peak = 2458.020 ; gain =
55.859 ; free physical = 80532 ; free virtual = 153824

Routing Is Done.
INFO: [Common 17-83] Releasing license: Implementation
54 Infos, 1 Warnings, 1 Critical Warnings and 0 Errors encountered.
route_design completed successfully
route_design: Time (s): cpu = 00:00:27 ; elapsed = 00:00:25 . Memory (MB): peak =
2458.020 ; gain = 55.859 ; free physical = 80532 ; free virtual = 153824
INFO: [Timing 38-480] Writing timing data to binary archive.
Writing placer database...
Writing XDEF routing.
Writing XDEF routing logical nets.
Writing XDEF routing special nets.
Write XDEF Complete: Time (s): cpu = 00:00:00.04 ; elapsed = 00:00:00.03 . Memory
(MB): peak = 2458.020 ; gain = 0.000 ; free physical = 80531 ; free virtual = 153824
INFO: [Common 17-1381] The checkpoint
'/nfs/home/l/l_heiwan/coen316/lab1/vivado_test_v2/vivado_leb1_v2/vivado_leb1_v2.runs/i
mpl_1/alu_board_routed.dcp' has been generated.
INFO: [runtcl-4] Executing : report_drc -file alu_board_drc_routed.rpt -pb
alu_board_drc_routed.pb -rpx alu_board_drc_routed.rpx
Command: report_drc -file alu_board_drc_routed.rpt -pb alu_board_drc_routed.pb -rpx
alu_board_drc_routed.rpx
INFO: [DRC 23-27] Running DRC with 8 threads
INFO: [Coretcl 2-168] The results of DRC are in file
/nfs/home/l/l_heiwan/coen316/lab1/vivado_test_v2/vivado_leb1_v2/vivado_leb1_v2.runs/im
pl_1/alu_board_drc_routed.rpt.
report_drc completed successfully
INFO: [runtcl-4] Executing : report_methodology -file
alu_board_methodology_drc_routed.rpt -pb alu_board_methodology_drc_routed.pb -rpx
alu_board_methodology_drc_routed.rpx
Command: report_methodology -file alu_board_methodology_drc_routed.rpt -pb
alu_board_methodology_drc_routed.pb -rpx alu_board_methodology_drc_routed.rpx
INFO: [Timing 38-35] Done setting XDC timing constraints.
INFO: [Timing 38-35] Done setting XDC timing constraints.
INFO: [DRC 23-133] Running Methodology with 8 threads
INFO: [Coretcl 2-1520] The results of Report Methodology are in file
/nfs/home/l/l_heiwan/coen316/lab1/vivado_test_v2/vivado_leb1_v2/vivado_leb1_v2.runs/im
pl_1/alu_board_methodology_drc_routed.rpt.
report_methodology completed successfully
INFO: [runtcl-4] Executing : report_power -file alu_board_power_routed.rpt -pb
alu_board_power_summary_routed.pb -rpx alu_board_power_routed.rpx
Command: report_power -file alu_board_power_routed.rpt -pb
alu_board_power_summary_routed.pb -rpx alu_board_power_routed.rpx
WARNING: [Power 33-232] No user defined clocks were found in the design!
Resolution: Please specify clocks using create_clock/create_generated_clock for
sequential elements. For pure combinatorial circuits, please specify a virtual clock,
otherwise the vectorless estimation might be inaccurate
```

```
INFO: [Timing 38-35] Done setting XDC timing constraints.
Running Vector-less Activity Propagation...

Finished Running Vector-less Activity Propagation
66 Infos, 2 Warnings, 1 Critical Warnings and 0 Errors encountered.
report_power failed
INFO: [runtcl-4] Executing : report_route_status -file alu_board_route_status.rpt -pb
alu_board_route_status.pb
INFO: [runtcl-4] Executing : report_timing_summary -max_paths 10 -file
alu_board_timing_summary_routed.rpt -pb alu_board_timing_summary_routed.pb -rpx
alu_board_timing_summary_routed.rpx -warn_on_violation
INFO: [Timing 38-91] UpdateTimingParams: Speed grade: -1, Delay Type: min_max, Timing
Stage: Requireds.
INFO: [Timing 38-191] Multithreading enabled for timing update using a maximum of 8
CPUs
WARNING: [Timing 38-313] There are no user specified timing constraints. Timing
constraints are needed for proper timing analysis.
INFO: [runtcl-4] Executing : report_incremental_reuse -file
alu_board_incremental_reuse_routed.rpt
INFO: [Vivado_Tcl 4-545] No incremental reuse to report, no incremental placement and
routing data was found.
INFO: [runtcl-4] Executing : report_clock_utilization -file
alu_board_clock_utilization_routed.rpt
INFO: [runtcl-4] Executing : report_bus_skew -warn_on_violation -file
alu_board_bus_skew_routed.rpt -pb alu_board_bus_skew_routed.pb -rpx
alu_board_bus_skew_routed.rpx
INFO: [Timing 38-91] UpdateTimingParams: Speed grade: -1, Delay Type: min_max, Timing
Stage: Requireds.
INFO: [Timing 38-191] Multithreading enabled for timing update using a maximum of 8
CPUs
INFO: [Common 17-206] Exiting Vivado at Wed Oct  4 18:02:15 2023...

*** Running vivado
    with args -log alu_board.vdi -applog -m64 -product Vivado -messageDb vivado.pb -
mode batch -source alu_board.tcl -notrace


****** Vivado v2018.2 (64-bit)
  **** SW Build 2258646 on Thu Jun 14 20:02:38 MDT 2018
  **** IP Build 2256618 on Thu Jun 14 22:10:49 MDT 2018
    ** Copyright 1986-2018 Xilinx, Inc. All Rights Reserved.

source alu_board.tcl -notrace
Command: open_checkpoint alu_board_routed.dcp

Starting open_checkpoint Task

Time (s): cpu = 00:00:00.07 ; elapsed = 00:00:00.23 . Memory (MB): peak = 1343.129 ;
gain = 0.000 ; free physical = 81447 ; free virtual = 154741
INFO: [Netlist 29-17] Analyzing 13 Unisim elements for replacement
INFO: [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
INFO: [Project 1-479] Netlist was created with Vivado 2018.2
INFO: [Device 21-403] Loading part xc7a100tcsg324-1
INFO: [Project 1-570] Preparing netlist for logic optimization
INFO: [Timing 38-478] Restoring timing data from binary archive.
INFO: [Timing 38-479] Binary timing data restore complete.
INFO: [Project 1-856] Restoring constraints from binary archive.
INFO: [Project 1-853] Binary constraint restore complete.
```

```
Reading XDEF placement.
Reading placer database...
Reading XDEF routing.
Read XDEF File: Time (s): cpu = 00:00:00.13 ; elapsed = 00:00:00.39 . Memory (MB):
peak = 2128.250 ; gain = 0.004 ; free physical = 80718 ; free virtual = 154012
Restored from archive | CPU: 0.390000 secs | Memory: 0.965797 MB |
Finished XDEF File Restore: Time (s): cpu = 00:00:00.13 ; elapsed = 00:00:00.40 .
Memory (MB): peak = 2128.250 ; gain = 0.004 ; free physical = 80718 ; free virtual =
154012
INFO: [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.

INFO: [Project 1-604] Checkpoint was created with Vivado v2018.2 (64-bit) build
2258646
open_checkpoint: Time (s): cpu = 00:00:26 ; elapsed = 00:02:07 . Memory (MB): peak =
2128.250 ; gain = 785.125 ; free physical = 80718 ; free virtual = 154012
Command: write_bitstream -force alu_board.bit
Attempting to get a license for feature 'Implementation' and/or device 'xc7a100t'
INFO: [Common 17-349] Got license for feature 'Implementation' and/or device
'xc7a100t'
Running DRC as a precondition to command write_bitstream
INFO: [IP_Flow 19-234] Refreshing IP repositories
INFO: [IP_Flow 19-1704] No user IP repositories specified
INFO: [IP_Flow 19-2313] Loaded Vivado IP repository
'/CMC/tools/xilinx/Vivado_2018.2/Vivado/2018.2/data/ip'.
INFO: [DRC 23-27] Running DRC with 8 threads
ERROR: [DRC NSTD-1] Unspecified I/O Standard: 5 out of 19 logical ports use I/O
standard (IOSTANDARD) value 'DEFAULT', instead of a user assigned specific value. This
may cause I/O contention or incompatibility with the board power or connectivity
affecting performance, signal integrity or in extreme cases cause damage to the device
or the components to which it is connected. To correct this violation, specify all I/O
standards. This design will fail to generate a bitstream unless all logical ports have
a user specified I/O standard value defined. To allow bitstream creation with
unspecified I/O standard values (not recommended), use this command: set_property
SEVERITY {Warning} [get_drc_checks NSTD-1].  NOTE: When using the Vivado Runs
infrastructure (e.g. launch_runs Tcl command), add this command to a .tcl file and add
that file as a pre-hook for write_bitstream step for the implementation run. Problem
ports: y_in[3:0], and zero.
ERROR: [DRC UCIO-1] Unconstrained Logical Port: 5 out of 19 logical ports have no user
assigned specific location constraint (LOC). This may cause I/O contention or
incompatibility with the board power or connectivity affecting performance, signal
integrity or in extreme cases cause damage to the device or the components to which it
is connected. To correct this violation, specify all pin locations. This design will
fail to generate a bitstream unless all logical ports have a user specified site LOC
constraint defined.  To allow bitstream creation with unspecified pin locations (not
recommended), use this command: set_property SEVERITY {Warning} [get_drc_checks UCIO-
1].  NOTE: When using the Vivado Runs infrastructure (e.g. launch_runs Tcl command),
add this command to a .tcl file and add that file as a pre-hook for write_bitstream
step for the implementation run.  Problem ports: y_in[3:0], and zero.
WARNING: [DRC CFGBVS-1] Missing CFGBVS and CONFIG_VOLTAGE Design Properties: Neither
the CFGBVS nor CONFIG_VOLTAGE voltage property is set in the current_design.
Configuration bank voltage select (CFGBVS) must be set to VCCO or GND, and
CONFIG_VOLTAGE must be set to the correct configuration voltage, in order to determine
the I/O voltage support for the pins in bank 0.  It is suggested to specify these
either using the 'Edit Device Properties' function in the GUI or directly in the XDC
file using the following syntax:

 set_property CFGBVS value1 [current_design]
```

```
 #where value1 is either VCCO or GND

 set_property CONFIG_VOLTAGE value2 [current_design]
 #where value2 is the voltage provided to configuration bank 0

Refer to the device configuration user guide for more information.
INFO: [Vivado 12-3199] DRC finished with 2 Errors, 1 Warnings
INFO: [Vivado 12-3200] Please refer to the DRC report (report_drc) for more
information.
ERROR: [Vivado 12-1345] Error(s) found during DRC. Bitgen not run.
INFO: [Common 17-83] Releasing license: Implementation
19 Infos, 1 Warnings, 0 Critical Warnings and 3 Errors encountered.
write_bitstream failed
write_bitstream: Time (s): cpu = 00:00:04 ; elapsed = 00:00:08 . Memory (MB): peak =
2328.301 ; gain = 200.051 ; free physical = 80674 ; free virtual = 153968
ERROR: [Common 17-39] 'write_bitstream' failed due to earlier errors.

INFO: [Common 17-206] Exiting Vivado at Wed Oct  4 18:04:58 2023...
```

5.5) Constrain .xdc File

```
# Vivado does not support old UCF syntax
# must use XDC syntax
set_property -dict { PACKAGE_PIN J15 IOSTANDARD LVCMOS33 } [ get_ports { add_sub }];
set_property -dict { PACKAGE_PIN L16 IOSTANDARD LVCMOS33 } [ get_ports { x_in[0] } ] ;
set_property -dict { PACKAGE_PIN M13 IOSTANDARD LVCMOS33 } [ get_ports { x_in[1] } ] ;
set_property -dict { PACKAGE_PIN K15 IOSTANDARD LVCMOS33 } [ get_ports { x_in[2] } ] ;
set_property -dict { PACKAGE_PIN H17 IOSTANDARD LVCMOS33 } [ get_ports { x_in[3] } ] ;

set_property -dict { PACKAGE_PIN J14 IOSTANDARD LVCMOS33 } [ get_ports
{ logic_func[0] }];
set_property -dict { PACKAGE_PIN T9 IOSTANDARD LVCMOS33 } [ get_ports
{ logic_func[1] } ] ;

set_property -dict { PACKAGE_PIN R18 IOSTANDARD LVCMOS33 } [ get_ports { func[0] } ];
set_property -dict { PACKAGE_PIN P17 IOSTANDARD LVCMOS33 } [ get_ports { func[1] } ] ;

set_property -dict { PACKAGE_PIN R17 IOSTANDARD LVCMOS33 } [ get_ports
{ output_out[0] } ];
set_property -dict { PACKAGE_PIN R16 IOSTANDARD LVCMOS33 } [ get_ports
{ output_out[1] } ] ;
set_property -dict { PACKAGE_PIN T14 IOSTANDARD LVCMOS33 } [ get_ports
{ output_out[2] } ] ;
set_property -dict { PACKAGE_PIN T15 IOSTANDARD LVCMOS33 } [ get_ports
{ output_out[3] } ] ;

set_property -dict { PACKAGE_PIN L14 IOSTANDARD LVCMOS33 } [ get_ports
{ overflow } ] ;
set_property -dict { PACKAGE_PIN H18 IOSTANDARD LVCMOS33 } [ get_ports { zero } ] ;
```