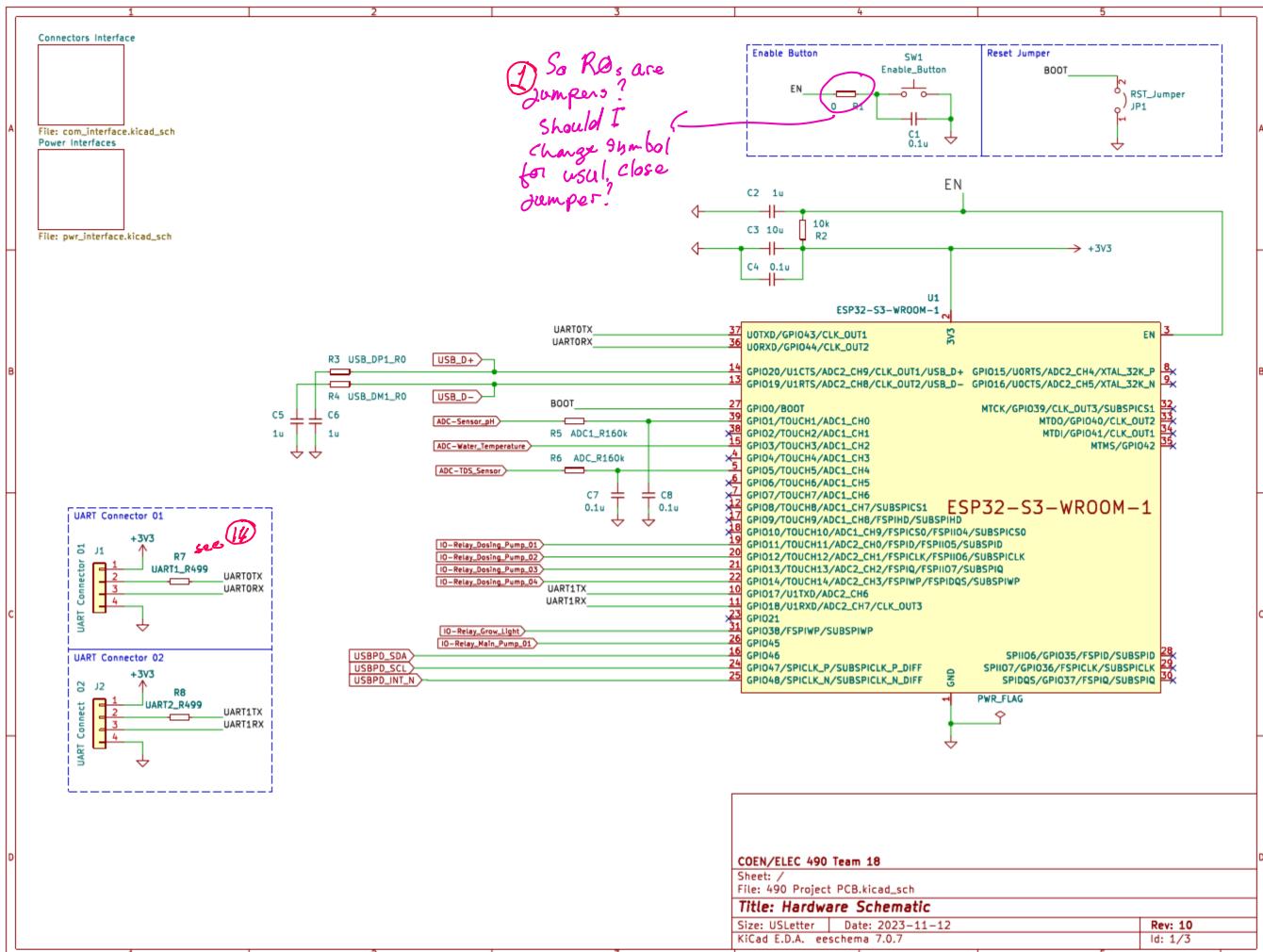


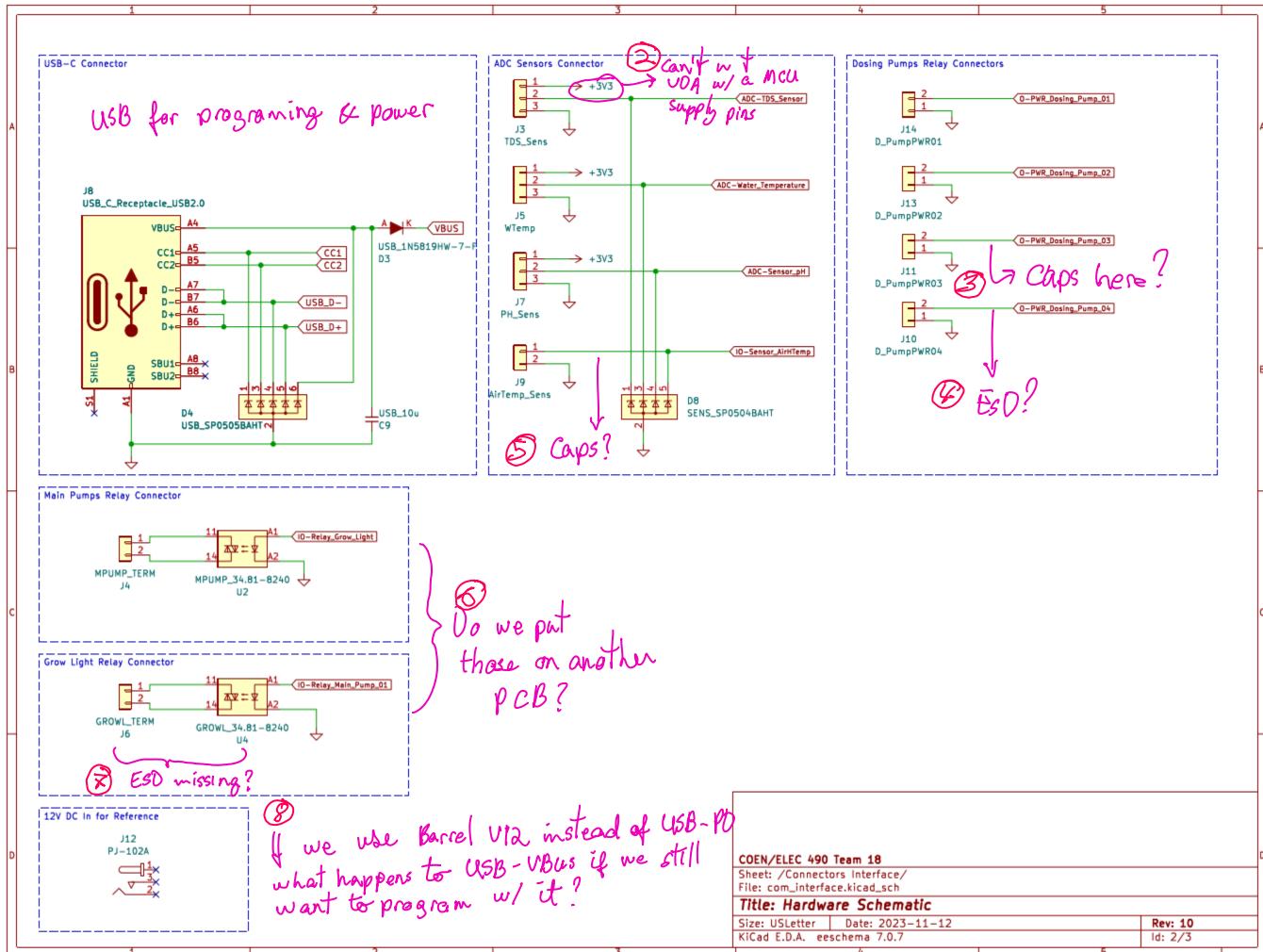
# 490 Project PCB

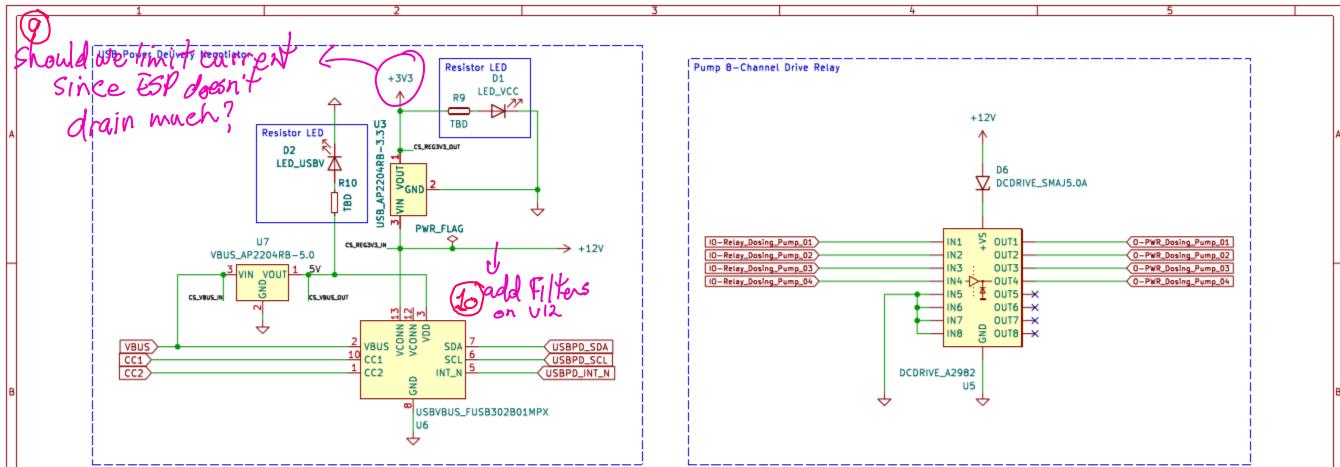
Page 1 sur 3



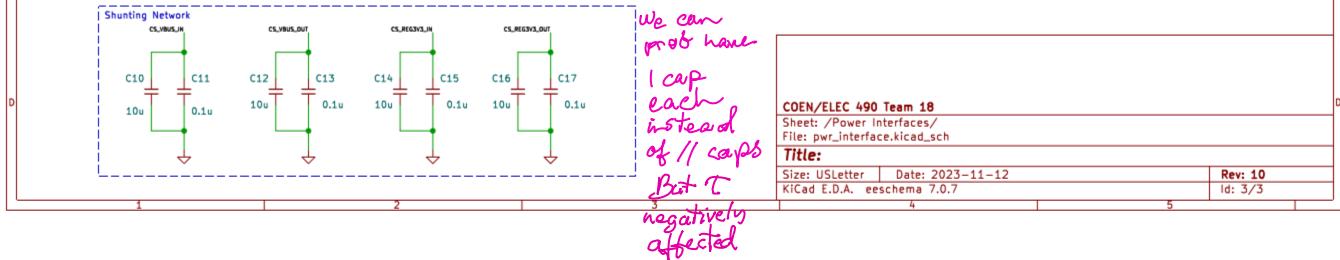
# 490 Project PCB

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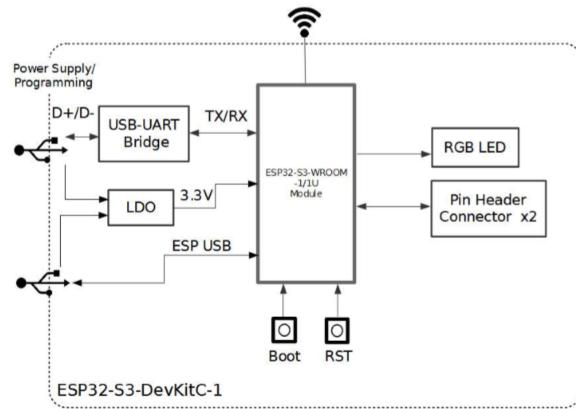


- We could use USB-PD to set higher voltage for the pumps
- I think this one only needs to be set once, others can anyway

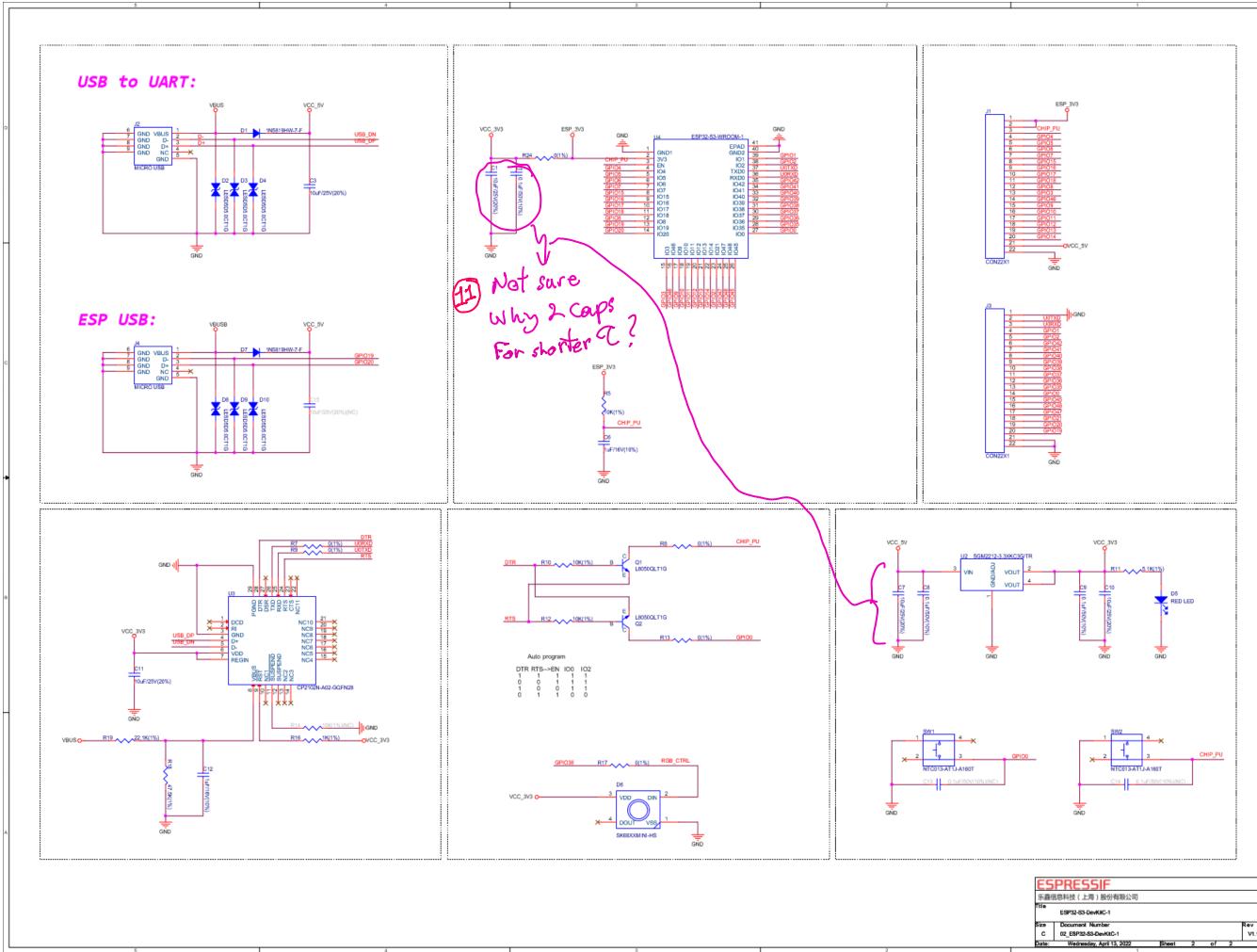


# Reference Schematic for ESP32

## System Block:



ESPRESSIF	
乐鑫信息科技（上海）股份有限公司	
File	ESP32-S3-DevKitC-1
Edt	Document Number
C	001
Date	Wednesday April 13, 2022
Sheet	1 of 2
Ver	v1.1



## 6 Peripheral Schematics

This is the typical application circuit of the module connected with peripheral components (for example, power supply, antenna, reset button, JTAG interface, and UART interface).

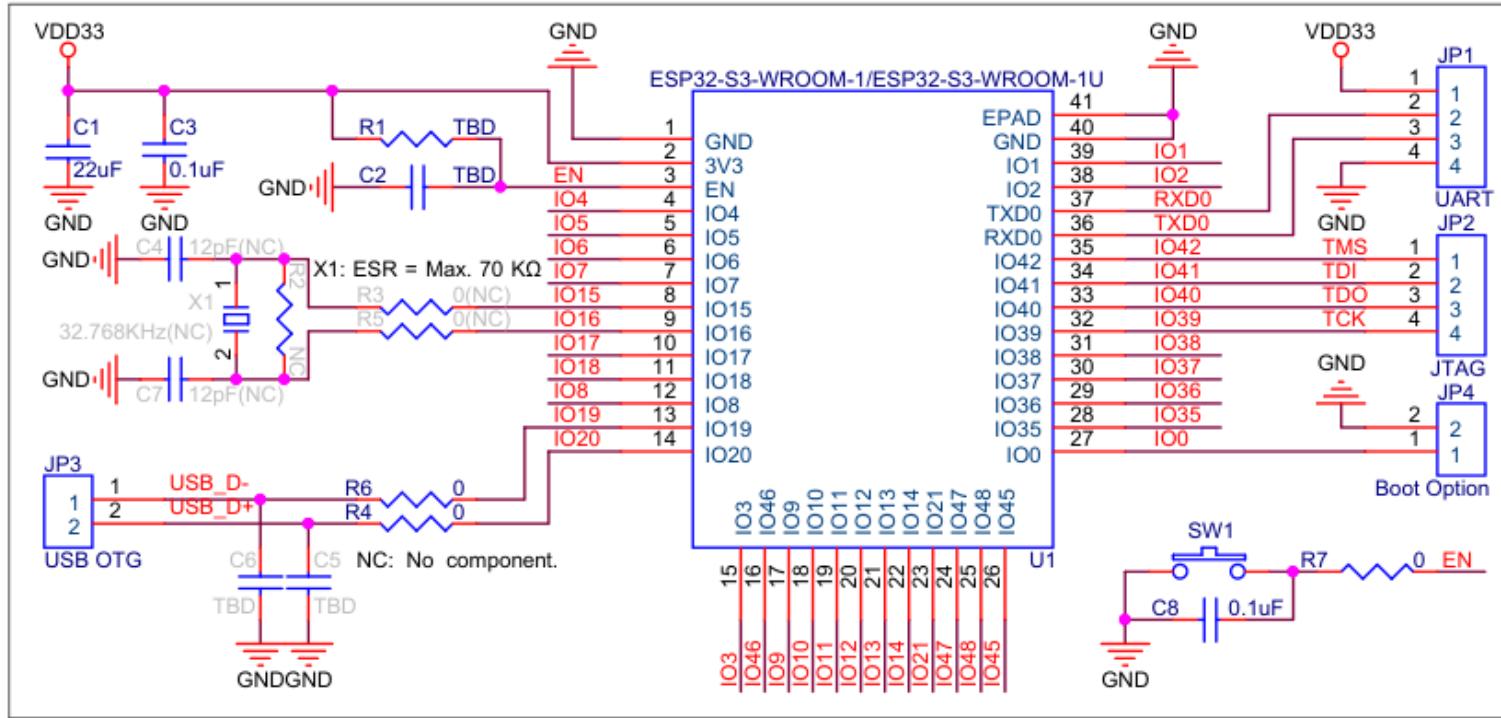


Figure 7: Peripheral Schematics

- Soldering the EPAD to the ground of the base board is not a must, however, it can optimize thermal performance. If you choose to solder it, please apply the correct amount of soldering paste. Too much soldering paste may increase the gap between the module and the baseboard. As result, the adhesion between other pins and the baseboard may be poor.
- To ensure that the power supply to the ESP32-S3 chip is stable during power-up, it is advised to add an RC delay circuit at the EN pin. The recommended setting for the RC delay circuit is usually  $R = 10 \text{ k}\Omega$  and  $C = 1 \mu\text{F}$ . However, specific parameters should be adjusted based on the power-up timing of the module and the power-up and reset sequence timing of the chip. For ESP32-S3's power-up and reset sequence timing diagram, please refer to [ESP32-S3 Series Datasheet > Section Power Supply](#).

## 2.1.2 Analog Power Supply

Pin2 VDD3P3, pin3 VDD3P3, pin55 VDDA, and pin56 VDDA are the analog power supply pins working at 3.0 V ~ 3.6 V.

*How?* (12) *cannot find*

Please be noted that the sudden increase in current draw, when ESP32-S3 is transmitting signals, may cause a power rail collapse. Therefore, it is highly recommended to add a  $10 \mu\text{F}$  capacitor to the power pin2 and power pin3 VDD3P3, which can work in conjunction with the  $1 \mu\text{F}$  capacitor. In addition, a CLC filter circuit needs to be added near VDD3P3 pins so as to suppress high-frequency harmonics. The recommended rated current of the inductor is 500 mA or above. Refer to Figure 4 to place the appropriate decoupling capacitors near each analog power pin.

## 2.1.1 Digital Power Supply

em Reset VDD3P3\_CPU of ESP32-S3 supplies power to CPU IO with a voltage range of 3.0 V ~ 3.6 V. It is recommended to add an extra  $0.1 \mu\text{F}$  decoupling capacitor close to VDD3P3\_CPU.

Pin29 VDD\_SPI can serve as the power supply output at either 1.8 V or 3.3 V (default). It is recommended to add extra  $0.1 \mu\text{F}$  and  $1 \mu\text{F}$  decoupling capacitors close to VDD\_SPI.

- When VDD\_SPI operates at 1.8 V, it is powered by the internal flash voltage regulator on the chip. The typical current the flash voltage regulator can offer is 40 mA.
- When VDD\_SPI operates at 3.3 V, it is driven directly by VDD3P3\_RTC through the internal  $R_{SPI}$  resistor with a typical value of  $14 \Omega$ . Therefore, there will be some voltage drop from VDD3P3\_RTC.

Depending on the value of EFUSE\_VDD\_SPI\_FORCE, the VDD\_SPI voltage of ESP32-S3 can be controlled in two ways.

Table 1: VDD\_SPI Voltage Control

EFUSE_VDD_SPI_FORCE	GPIO45	eFuse <sup>1</sup>	Voltage	VDD_SPI power source <sup>2</sup>
0	0	Ignored	3.3 V	VDD3P3_RTC via $R_{SPI}$
	1		1.8 V	Flash Voltage Regulator
1	Ignored	0	1.8 V	Flash Voltage Regulator
		1	3.3 V	VDD3P3_RTC via $R_{SPI}$

<sup>1</sup> eFuse: EFUSE\_VDD\_SPI\_TIEH

<sup>2</sup> See [ESP32-S3 Series Datasheet](#) > Section Power Scheme

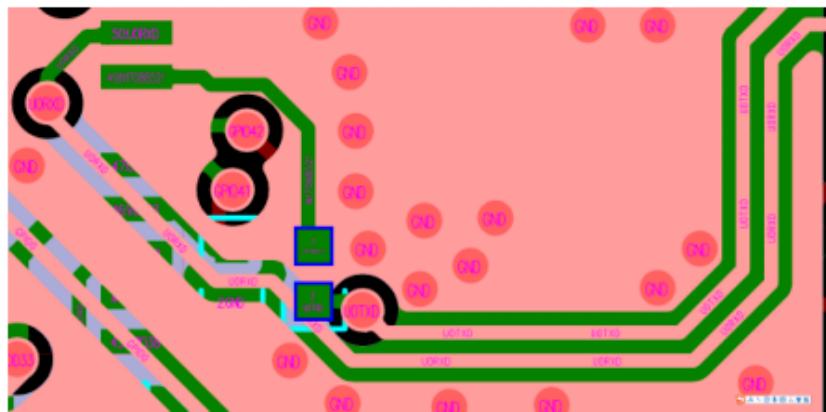
VDD\_SPI can also be the power supply input driven by an external power supply.

### Notice:

- For ESP32-S3 chips with in-package flash/PSRAM, VDD\_SPI is fixed to 1.8 V or 3.3 V, so it is not required to configure GPIO45.
- When using VDD\_SPI as the power supply output for in-package or off-package 3.3 V flash/PSRAM, considering a voltage drop due to the  $R_{SPI}$  resistor, VDD3P3\_RTC is suggested to be 3.0 V or above to meet the flash/PSRAM's minimum working voltage requirement.

### 3.7 UART

- The series resistor on the U0TXD trace needs to be placed close to the ESP32-S3 chip side and away from the crystal.
  - The U0TXD and U0RXD traces on the top layer should be as short as possible.
  - The UART trace should be surrounded by ground copper and ground vias stitching.



**Figure 26:** ESP32-S3 UART0 Layout