Computer Architecture & Design

Coen 316

Lab Experiment #2

Andre Hei Wang Law

4017 5600

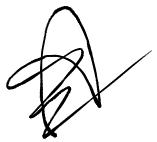
Section DN-X

Professor Dr. Fadi Alzouri

Performed on October 5, 2023

Due on October 26, 2023

“I certify that this submission is my original work and meets the Faculty’s Expectations of

Originality.”

**1) Introduction/Objectives**

The objective of the second lab of COEN 316 is to design and implement a multi-port register file using VHDL. The register file is a 32x32, meaning it has 32 registers with 32 bits each. Students will also learn how to manage synchronous and asynchronous operations from reset, writing and reading inputs. By coding, synthesizing, implementing and simulating this register file, students will gain hands-on experience in computer architecture design and FPGA implementation, allowing them to understand the principles of a register file.

**2) Theory**

**read\_a** and **read\_b**: They specify which registers are read from

**din**: It provides data to be written

**write\_address**: It determines the target register for writing

**write**: It enables/disables writing, reset clears all registers

**clk**: It controls the timing of write operations

**out\_a** and **out\_b**: They provide the data read from the specified registers

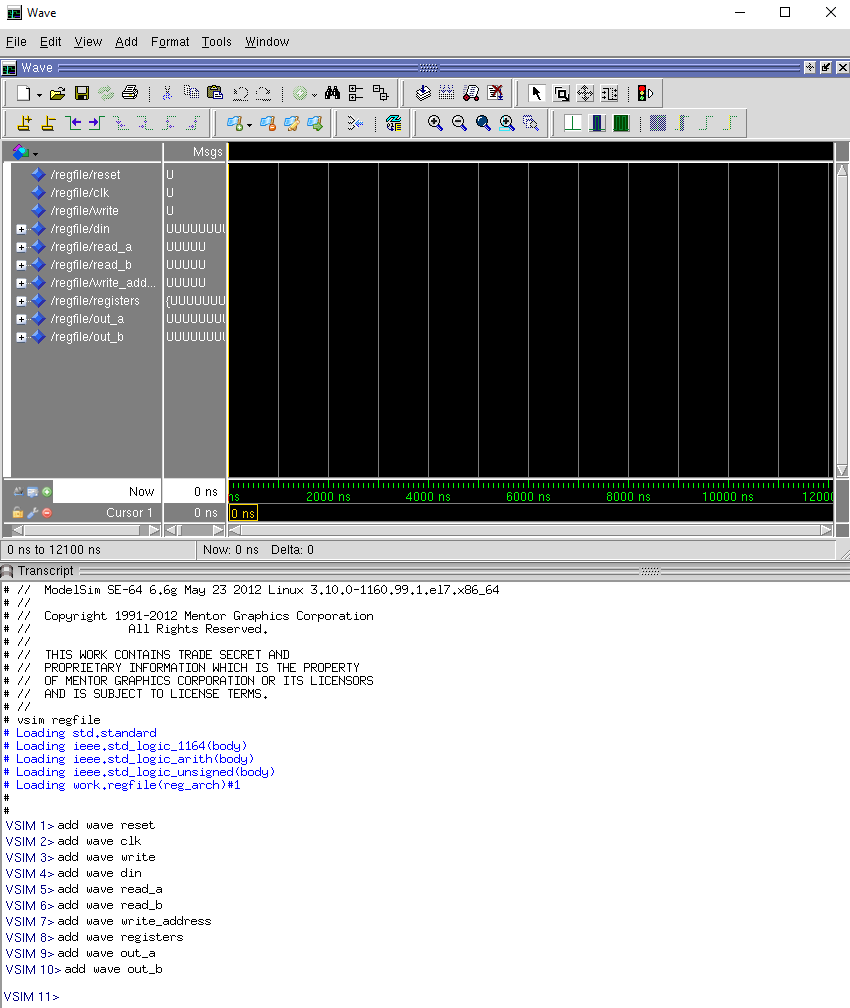
**Synchronous Operations**: Timing dependent on clock signal

**Asynchronous** **Operations**: Timing independent on clock signal

**3) Tasks, Results and Discussion**

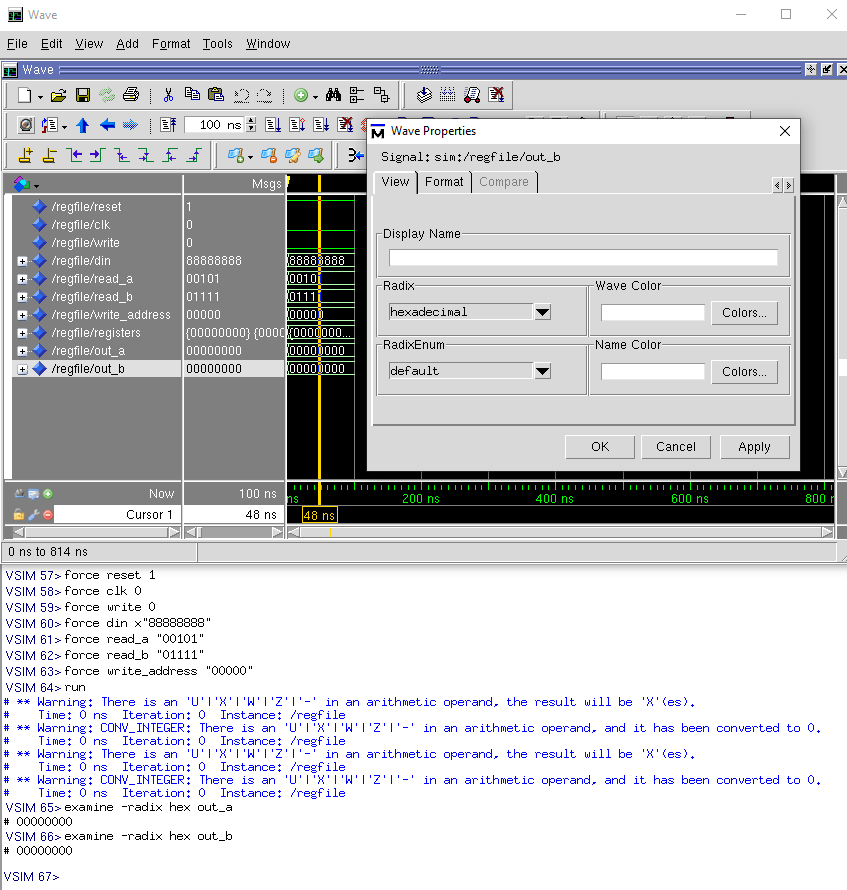
*For the results below, all VHDL code and DO code will be at the appendix.*

**3.1) Setup**



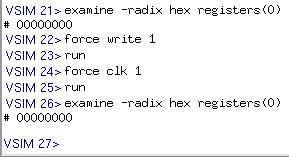
The first step done was to get the wave window and add the waves for the inputs and outputs.

**3.2) Initialize Values**



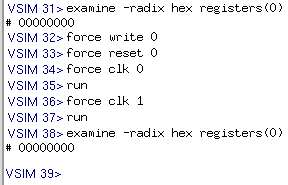
This step changed the radix format readings of din, registers, out\_a and out\_b into hexadecimal so it becomes easier to read the data. We also populated the inputs in this step.

**3.3) Test Writing Into “registers” (reset = 1, write = 1, rising edge clk)**



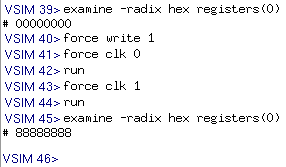
Since write\_address is at 00000, if registers were changed, it should be displayed during examine -radix hex registers(0). However, nothing changed which is the expected results as reset is still set at 1 despite write being 1 and having a rising edge clk.

**3.4) Test Writing Into “registers” (reset = 0, write = 0, rising edge clk)**



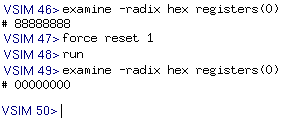
Here, the registers(0) remains unchanged despite having reset set to 0 and having a rising edge clk. This is due to the fact that write is set to zero.

**3.5) Test Writing Into “registers” (reset = 0, write = 1, rising edge clk)**



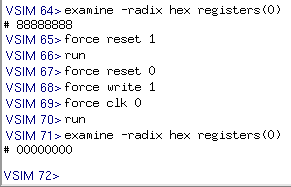
With write set to 1, we can finally write into registers(0) the value of din 88888888 Hex.

**3.6) Test Reset (reset =1, no rising edge clk)**



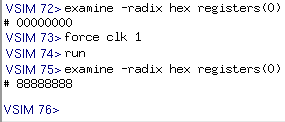
Reset is an asynchronous active-high input, thus it doesn’t require a rising edge clk for it to activate. This can be seen here where force reset 1 does indeed resets the data inside registers(0).

**3.7) Test Writing Into “registers” (reset = 0, write = 1, independent of rising edge clk)**



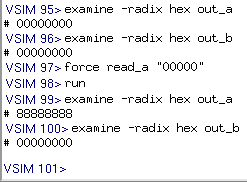
Similarly to 3.5), reset is set to 0, write is at 1 and clk start at 0. However without the rising edge clk 1, registers(0) won’t change. The examine output shows that it remains 00000000 from reset.

**3.8) Test Writing Into “registers” (clk = 1)**



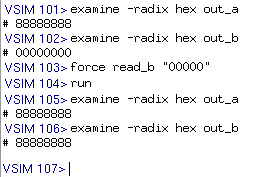
Following the last step, by having a rising edge, force clk 1, we can examine that the register(0) has indeed changed from 00000000 to 88888888.

**3.9) Display Output (read\_a "00000" and read\_b "01111")**



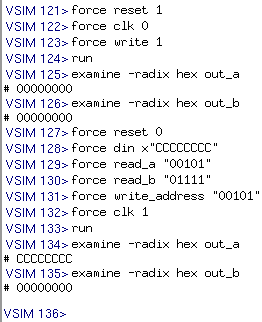
Knowing that in 3.2) Initialize Values, we have set read\_a "00101" and read\_b "01111". When examining both out\_a and out\_b, we notice that their values are all zeros. This is normal as the only data written in the registers is on registers(0). As such, by changing read\_a to 00000 and running it, we notice that out\_a has now changed.

**3.10) Display Output (read\_a "00000" and read\_b "00000")**



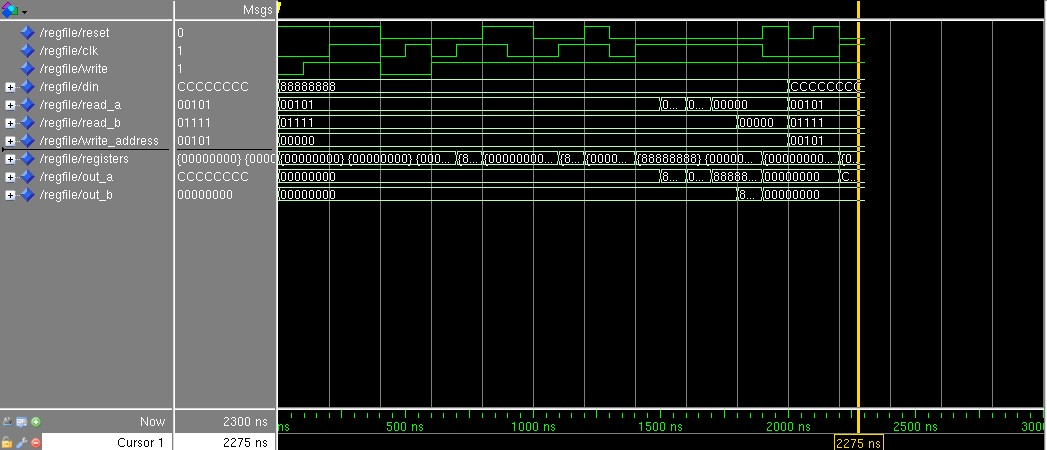
Here, since both are reading off registers(0), the output of both examine out\_a and out\_b is 88888888. Notice that the reading is done asynchronously where it is independent of the clock input. This behavior is the correct one.

**3.11) Test Write on Different Address (write\_address "00101", read\_a "00101")**



In this test, we changed the location of write\_address to 00101. Then, we wrote din CCCCCCCC into it with proper inputs (reset = 0, write = 1, rising edge). The “examine -radix hex out\_a” shows that we have successfully written into registers(5) and the reading’s behavior is correct.

**3.12) ModelSim Exported Wave View**



**4) Conclusions**

In conclusion, lab 2 – register file has provided a comprehensive hands-on experience of digital design principles of a multi-port register file. Through the use of VHDL, students learned to create a 32 x 32 register file with both synchronous and asynchronous operations. Then, students also integrated the design to ModelSim for simulation and used Xilinx Vivado tools for FPGA implementation. By testing difference cases of inputs with the DO file, students gained valuable insights into the behavior of a 32 x 32 register file. In the end this Coen 316 lab improved the student’s understanding of digital system which will be important for future labs.

**5) Appendix**

**5.1) VHDL Code**

-- coen 316 lab  
-- Andre Hei Wang Law  
-- 4017 5600  
  
**library** IEEE;  
**use** IEEE.std\_logic\_1164.**all**;  
**use** IEEE.std\_logic\_unsigned.**all**;  
  
**entity** regfile **is**  
 **port** (  
 din: **in** std\_logic\_vector(31 **downto** 0); -- data written to specific register  
 reset: **in** std\_logic; -- asynchronous active-high reset input  
 clk: **in** std\_logic; -- clock input  
 write: **in** std\_logic; -- write control signal  
 read\_a: **in** std\_logic\_vector(4 **downto** 0); -- address for read port A  
 read\_b: **in** std\_logic\_vector(4 **downto** 0); -- address for read port B  
 write\_address: **in** std\_logic\_vector(4 **downto** 0); -- address for write port  
 out\_a: **out** std\_logic\_vector(31 **downto** 0); -- data output for read port A  
 out\_b: **out** std\_logic\_vector(31 **downto** 0)); -- data output for read port B  
**end** regfile;  
  
**architecture** reg\_arch **of** regfile **is**  
 **type** reg\_array **is** **array** (0 **to** 31) **of** std\_logic\_vector(31 **downto** 0); -- 32 reg, each 32 bits  
 **signal** registers : reg\_array; -- register file, all zeros  
   
**begin**  
 **process**(reset, clk)  
 **begin**  
 **if** (reset = '1') **then** -- reset (asynchronous)   
 registers <= (**others** => (**others** => '0')); -- clear all reg. zeros  
 **elsif** (clk'event **and** clk='1') **then** -- click (synchronous), rising edge  
 **if** (write = '1') **then** -- check for active write signal  
 registers(conv\_integer(write\_address)) <= din; -- write   
 **end** **if**;  
 **end** **if**;  
 **end** **process**;  
  
 -- reading (asynchronous)  
 out\_a <= registers(conv\_integer(read\_a)); -- read data from read\_a  
 out\_b <= registers(conv\_integer(read\_b)); -- read data from read\_b  
  
**end** **architecture** reg\_arch;

**5.2) Board Wrapper Version of the Original VHDL Code**

-- coen 316 lab  
-- Andre Hei Wang Law  
-- 4017 5600  
  
-- board wrapper version  
  
**library** IEEE;  
**use** IEEE.std\_logic\_1164.**all**;  
**use** IEEE.std\_logic\_unsigned.**all**;  
  
**entity** regfile **is**  
 **port** (  
 -- (original)  
 din: **in** std\_logic\_vector(3 **downto** 0); -- data written to specific register  
 reset: **in** std\_logic; -- asynchronous active-high reset input  
 clk: **in** std\_logic; -- clock input  
 write: **in** std\_logic; -- write control signal  
 read\_a: **in** std\_logic\_vector(1 **downto** 0); -- address for read port A  
 read\_b: **in** std\_logic\_vector(1 **downto** 0); -- address for read port B  
 write\_address: **in** std\_logic\_vector(1 **downto** 0); -- address for write port  
 out\_a: **out** std\_logic\_vector(3 **downto** 0); -- data output for read port A  
 out\_b: **out** std\_logic\_vector(3 **downto** 0)); -- data output for read port B  
**end** regfile;  
  
**architecture** reg\_arch **of** regfile **is**  
 **type** reg\_array **is** **array** (0 **to** 31) **of** std\_logic\_vector(31 **downto** 0); -- 32 reg, each 32 bits  
 **signal** registers : reg\_array; -- register file, all zeros  
   
 -- board wrapper (new)  
 **signal** din\_wrap, out\_a\_wrap, out\_b\_wrap : std\_logic\_vector(31 **downto** 0);  
 **signal** read\_a\_wrap, read\_b\_wrap, write\_address\_wrap : std\_logic\_vector(4 **downto** 0);  
  
**begin**  
 -- board wrapper (left side new, right side original)  
 din\_wrap(31 **downto** 4) <= (**others** => '0');  
 din\_wrap(3 **downto** 0) <= din(3) & din(2) & din(1) & din(0);  
 read\_a\_wrap(4 **downto** 2) <= (**others** => '0');  
 read\_a\_wrap(1 **downto** 0) <= read\_a(1) & read\_a(0);  
 read\_b\_wrap(4 **downto** 2) <= (**others** => '0');  
 read\_b\_wrap(1 **downto** 0) <= read\_b(1) & read\_b(0);  
 write\_address\_wrap(4 **downto** 2) <= (**others** => '0');  
 write\_address\_wrap(1 **downto** 0) <= write\_address(1) & write\_address(0);  
   
 -- board wrapper (left side original, right side new)  
 -- output (notice it's 3 downto 0 and not 31 downto 0)  
 out\_a(3 **downto** 0) <= out\_a\_wrap(3 **downto** 0);  
 out\_b(3 **downto** 0) <= out\_b\_wrap(3 **downto** 0);   
  
 **process**(reset, clk)  
 **begin**  
 **if** (reset = '1') **then** -- reset (asynchronous)   
 registers <= (**others** => (**others** => '0')); -- clear all reg. zeros  
 **elsif** (clk'event **and** clk='1') **then** -- click (synchronous), rising edge  
 **if** (write = '1') **then** -- check for active write signal  
 registers(conv\_integer(write\_address\_wrap)) <= din\_wrap; -- write   
 **end** **if**;  
 **end** **if**;  
 **end** **process**;  
  
 -- reading (asynchronous)  
 out\_a\_wrap <= registers(conv\_integer(read\_a\_wrap)); -- read data from read\_a  
 out\_b\_wrap <= registers(conv\_integer(read\_b\_wrap)); -- read data from read\_b  
  
**end** **architecture** reg\_arch;

**5.3) DO File to Test Various Output**

# coen 316   
# Andre Hei Wang Law  
# 4017 5600  
  
# 3.1 Setup  
add wave **reset**  
**add** wave clk  
**add** wave write  
**add** wave din  
**add** wave read\_a  
**add** wave read\_b  
**add** wave write\_address  
**add** wave registers  
**add** wave out\_a  
**add** wave out\_b  
  
# 3.2 Initialize Values  
# 88888888 Hex is 1000 x 8 times in Binary  
**force** **reset** 1  
**force** clk 0  
**force** write 0  
**force** din x"88888888"  
**force** read\_a "00101"  
**force** read\_b "01111"  
**force** write\_address "00000"  
run  
examine -radix **hex** out\_a   
examine -radix **hex** out\_b  
  
# 3.3) Test Writing Into “registers” (reset = 1, write = 1, rising edge clk)  
examine -radix **hex** registers(0)  
**force** write 1  
run  
**force** clk 1  
run  
examine -radix **hex** registers(0)  
  
# 3.4) Test Writing Into “registers” (reset = 0, write = 0, rising edge clk)  
examine -radix **hex** registers(0)  
**force** write 0  
**force** **reset** 0  
**force** clk 0  
run  
**force** clk 1  
run  
examine -radix **hex** registers(0)  
  
# 3.5) Test Writing Into “registers” (reset = 0, write = 1, rising edge clk)  
examine -radix **hex** registers(0)  
**force** write 1  
**force** clk 0  
run  
**force** clk 1  
run  
examine -radix **hex** registers(0)  
  
# 3.6) Test Reset (reset = 1, no rising edge clk)  
examine -radix **hex** registers(0)  
**force** **reset** 1  
run  
examine -radix **hex** registers(0)  
  
# 3.7) Test Writing Into “registers” (reset = 0, write = 1, independent of rising edge clk)  
examine -radix **hex** registers(0)  
**force** **reset** 1  
run  
**force** **reset** 0  
**force** write 1  
**force** clk 0  
run  
examine -radix **hex** registers(0)  
  
# 3.8) Rising Edge (clk = 1)  
examine -radix **hex** registers(0)  
**force** clk 1  
run  
examine -radix **hex** registers(0)  
  
# 3.9) Display Output (read\_a "00000" and read\_b "01111")  
examine -radix **hex** out\_a  
examine -radix **hex** out\_b  
**force** read\_a "00000"  
run  
examine -radix **hex** out\_a  
examine -radix **hex** out\_b  
  
# 3.10) Display Output (read\_a "00000" and read\_b "00000")  
examine -radix **hex** out\_a  
examine -radix **hex** out\_b  
**force** read\_b "00000"  
run  
examine -radix **hex** out\_a  
examine -radix **hex** out\_b  
  
# 3.11) Test Write on Different Address (write\_address "00101", read\_a "00101")  
**force** **reset** 1  
**force** clk 0  
**force** write 1  
run  
examine -radix **hex** out\_a   
examine -radix **hex** out\_b  
**force** **reset** 0  
**force** din x"CCCCCCCC"  
**force** read\_a "00101"  
**force** read\_b "01111"  
**force** write\_address "00101"  
**force** clk 1  
run  
examine -radix **hex** out\_a   
examine -radix **hex** out\_b

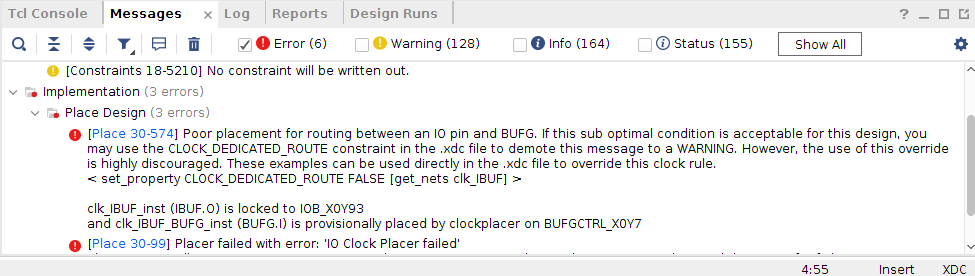
**5.3) Synthesis Log**

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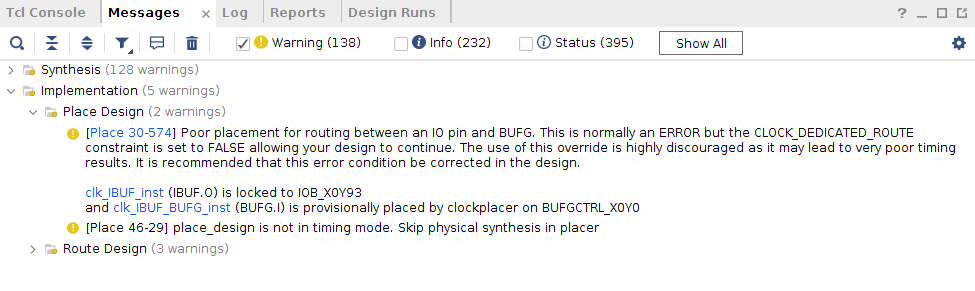
**Warning Discussions:** When running the synthesis, there were no critical warning nor error message. However, we received 128 yellow warnings about unused sequential elements which is simply due to the fact that our board wrapper version of the code has many unused registers.

*\*\*\** Running vivado  
 with args -log regfile.vds -m64 -product Vivado -mode batch -messageDb vivado.pb -notrace -source regfile.tcl  
  
  
**\*\*\*\*\***\* Vivado v2018.2 (64-bit)  
 *\*\*\**\* SW Build 2258646 on Thu Jun 14 20:02:38 MDT 2018  
 *\*\*\**\* IP Build 2256618 on Thu Jun 14 22:10:49 MDT 2018  
 \*\* Copyright 1986-2018 Xilinx, Inc. All Rights Reserved.  
  
source regfile.tcl -notrace  
Command: synth\_design -top regfile -part xc7a100tcsg324-1  
Starting synth\_design  
Attempting to get a license for feature 'Synthesis' and/or device 'xc7a100t'  
INFO: [Common 17-349] Got license for feature 'Synthesis' and/or device 'xc7a100t'  
INFO: Launching helper process for spawning children vivado processes  
INFO: Helper process launched with PID 18758   
---------------------------------------------------------------------------------  
Starting RTL Elaboration : Time (s): cpu = 00:00:02 ; elapsed = 00:00:04 . Memory (MB): peak = 1467.594 ; gain = 85.727 ; free physical = 121965 ; free virtual = 157033  
---------------------------------------------------------------------------------  
INFO: [Synth 8-638] synthesizing module 'regfile' [/nfs/home/l/l*\_heiwan/coen316/lab2/lab2\_*wrapper*\_register\_*file.vhd:25]  
INFO: [Synth 8-256] done synthesizing module 'regfile' (1#1) [/nfs/home/l/l*\_heiwan/coen316/lab2/lab2\_*wrapper*\_register\_*file.vhd:25]  
---------------------------------------------------------------------------------  
Finished RTL Elaboration : Time (s): cpu = 00:00:03 ; elapsed = 00:00:06 . Memory (MB): peak = 1513.234 ; gain = 131.367 ; free physical = 121975 ; free virtual = 157044  
---------------------------------------------------------------------------------  
  
Report Check Netlist:   
+------+------------------+-------+---------+-------+------------------+  
| |Item |Errors |Warnings |Status |Description |  
+------+------------------+-------+---------+-------+------------------+  
|1 |multi*\_driven\_*nets | 0| 0|Passed |Multi driven nets |  
+------+------------------+-------+---------+-------+------------------+  
---------------------------------------------------------------------------------  
Start Handling Custom Attributes  
---------------------------------------------------------------------------------  
---------------------------------------------------------------------------------  
Finished Handling Custom Attributes : Time (s): cpu = 00:00:03 ; elapsed = 00:00:06 . Memory (MB): peak = 1513.234 ; gain = 131.367 ; free physical = 121976 ; free virtual = 157044  
---------------------------------------------------------------------------------  
---------------------------------------------------------------------------------  
Finished RTL Optimization Phase 1 : Time (s): cpu = 00:00:03 ; elapsed = 00:00:06 . Memory (MB): peak = 1513.234 ; gain = 131.367 ; free physical = 121976 ; free virtual = 157044  
---------------------------------------------------------------------------------  
INFO: [Device 21-403] Loading part xc7a100tcsg324-1  
INFO: [Project 1-570] Preparing netlist for logic optimization  
  
Processing XDC Constraints  
Initializing timing engine  
Parsing XDC File [/nfs/home/l/l*\_heiwan/coen316/lab2/lab2\_*constraints.xdc]  
Finished Parsing XDC File [/nfs/home/l/l*\_heiwan/coen316/lab2/lab2\_*constraints.xdc]  
INFO: [Project 1-236] Implementation specific constraints were found while reading constraint file [/nfs/home/l/l*\_heiwan/coen316/lab2/lab2\_*constraints.xdc]. These constraints will be ignored for synthesis but will be used in implementation. Impacted constraints are listed in the file [.Xil/regfile\_propImpl.xdc].  
Resolution: To avoid this warning, move constraints listed in [.Xil/regfile*\_propImpl.xdc] to another XDC file and exclude this new file from synthesis with the used\_*in\_synthesis property (File Properties dialog in GUI) and re-run elaboration/synthesis.  
Completed Processing XDC Constraints  
  
INFO: [Project 1-111] Unisim Transformation Summary:  
No Unisim elements were transformed.  
  
Constraint Validation Runtime : Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.03 . Memory (MB): peak = 1885.160 ; gain = 0.000 ; free physical = 121707 ; free virtual = 156775  
---------------------------------------------------------------------------------  
Finished Constraint Validation : Time (s): cpu = 00:00:15 ; elapsed = 00:01:07 . Memory (MB): peak = 1885.160 ; gain = 503.293 ; free physical = 121790 ; free virtual = 156858  
---------------------------------------------------------------------------------  
---------------------------------------------------------------------------------  
Start Loading Part and Timing Information  
---------------------------------------------------------------------------------  
Loading part: xc7a100tcsg324-1  
---------------------------------------------------------------------------------  
Finished Loading Part and Timing Information : Time (s): cpu = 00:00:15 ; elapsed = 00:01:07 . Memory (MB): peak = 1885.160 ; gain = 503.293 ; free physical = 121790 ; free virtual = 156858  
---------------------------------------------------------------------------------  
---------------------------------------------------------------------------------  
Start Applying 'set\_property' XDC Constraints  
---------------------------------------------------------------------------------  
---------------------------------------------------------------------------------  
Finished applying 'set\_property' XDC Constraints : Time (s): cpu = 00:00:15 ; elapsed = 00:01:08 . Memory (MB): peak = 1885.160 ; gain = 503.293 ; free physical = 121792 ; free virtual = 156860  
---------------------------------------------------------------------------------  
INFO: [Synth 8-5546] ROM "registers\_reg[0]" won't be mapped to RAM because it is too sparse  
INFO: [Synth 8-5546] ROM "registers\_reg[1]" won't be mapped to RAM because it is too sparse  
INFO: [Synth 8-5546] ROM "registers\_reg[2]" won't be mapped to RAM because it is too sparse  
INFO: [Synth 8-5546] ROM "registers\_reg[3]" won't be mapped to RAM because it is too sparse  
INFO: [Synth 8-5546] ROM "registers\_reg[4]" won't be mapped to RAM because it is too sparse  
INFO: [Synth 8-5546] ROM "registers\_reg[5]" won't be mapped to RAM because it is too sparse  
INFO: [Synth 8-5546] ROM "registers\_reg[6]" won't be mapped to RAM because it is too sparse  
INFO: [Synth 8-5546] ROM "registers\_reg[7]" won't be mapped to RAM because it is too sparse  
INFO: [Synth 8-5546] ROM "registers\_reg[8]" won't be mapped to RAM because it is too sparse  
INFO: [Synth 8-5546] ROM "registers\_reg[9]" won't be mapped to RAM because it is too sparse  
INFO: [Synth 8-5546] ROM "registers\_reg[10]" won't be mapped to RAM because it is too sparse  
INFO: [Synth 8-5546] ROM "registers\_reg[11]" won't be mapped to RAM because it is too sparse  
INFO: [Synth 8-5546] ROM "registers\_reg[12]" won't be mapped to RAM because it is too sparse  
INFO: [Synth 8-5546] ROM "registers\_reg[13]" won't be mapped to RAM because it is too sparse  
INFO: [Synth 8-5546] ROM "registers\_reg[14]" won't be mapped to RAM because it is too sparse  
INFO: [Synth 8-5546] ROM "registers\_reg[15]" won't be mapped to RAM because it is too sparse  
INFO: [Synth 8-5546] ROM "registers\_reg[16]" won't be mapped to RAM because it is too sparse  
INFO: [Synth 8-5546] ROM "registers\_reg[17]" won't be mapped to RAM because it is too sparse  
INFO: [Synth 8-5546] ROM "registers\_reg[18]" won't be mapped to RAM because it is too sparse  
INFO: [Synth 8-5546] ROM "registers\_reg[19]" won't be mapped to RAM because it is too sparse  
INFO: [Synth 8-5546] ROM "registers\_reg[20]" won't be mapped to RAM because it is too sparse  
INFO: [Synth 8-5546] ROM "registers\_reg[21]" won't be mapped to RAM because it is too sparse  
INFO: [Synth 8-5546] ROM "registers\_reg[22]" won't be mapped to RAM because it is too sparse  
INFO: [Synth 8-5546] ROM "registers\_reg[23]" won't be mapped to RAM because it is too sparse  
INFO: [Synth 8-5546] ROM "registers\_reg[24]" won't be mapped to RAM because it is too sparse  
INFO: [Synth 8-5546] ROM "registers\_reg[25]" won't be mapped to RAM because it is too sparse  
INFO: [Synth 8-5546] ROM "registers\_reg[26]" won't be mapped to RAM because it is too sparse  
INFO: [Synth 8-5546] ROM "registers\_reg[27]" won't be mapped to RAM because it is too sparse  
INFO: [Synth 8-5546] ROM "registers\_reg[28]" won't be mapped to RAM because it is too sparse  
INFO: [Synth 8-5546] ROM "registers\_reg[29]" won't be mapped to RAM because it is too sparse  
INFO: [Synth 8-5546] ROM "registers\_reg[30]" won't be mapped to RAM because it is too sparse  
INFO: [Synth 8-5546] ROM "registers\_reg[31]" won't be mapped to RAM because it is too sparse  
---------------------------------------------------------------------------------  
Finished RTL Optimization Phase 2 : Time (s): cpu = 00:00:16 ; elapsed = 00:01:09 . Memory (MB): peak = 1885.160 ; gain = 503.293 ; free physical = 121784 ; free virtual = 156852  
---------------------------------------------------------------------------------  
  
Report RTL Partitions:   
+-+--------------+------------+----------+  
| |RTL Partition |Replication |Instances |  
+-+--------------+------------+----------+  
+-+--------------+------------+----------+  
---------------------------------------------------------------------------------  
Start RTL Component Statistics   
---------------------------------------------------------------------------------  
Detailed RTL Component Info :   
+---Registers :   
 32 Bit Registers := 32   
+---Muxes :   
 2 Input 1 Bit Muxes := 4   
---------------------------------------------------------------------------------  
Finished RTL Component Statistics   
---------------------------------------------------------------------------------  
---------------------------------------------------------------------------------  
Start RTL Hierarchical Component Statistics   
---------------------------------------------------------------------------------  
Hierarchical RTL Component report   
Module regfile   
Detailed RTL Component Info :   
+---Registers :   
 32 Bit Registers := 32   
+---Muxes :   
 2 Input 1 Bit Muxes := 4   
---------------------------------------------------------------------------------  
Finished RTL Hierarchical Component Statistics  
---------------------------------------------------------------------------------  
---------------------------------------------------------------------------------  
Start Part Resource Summary  
---------------------------------------------------------------------------------  
Part Resources:  
DSPs: 240 (col length:80)  
BRAMs: 270 (col length: RAMB18 80 RAMB36 40)  
---------------------------------------------------------------------------------  
Finished Part Resource Summary  
---------------------------------------------------------------------------------  
---------------------------------------------------------------------------------  
Start Cross Boundary and Area Optimization  
---------------------------------------------------------------------------------  
Warning: Parallel synthesis criteria is not met   
INFO: [Synth 8-4471] merging register 'registers*\_reg[5][31:0]' into 'registers\_*reg[4][31:0]' [/nfs/home/l/l*\_heiwan/coen316/lab2/lab2\_*wrapper*\_register\_*file.vhd:51]  
INFO: [Synth 8-4471] merging register 'registers*\_reg[6][31:0]' into 'registers\_*reg[4][31:0]' [/nfs/home/l/l*\_heiwan/coen316/lab2/lab2\_*wrapper*\_register\_*file.vhd:51]  
INFO: [Synth 8-4471] merging register 'registers*\_reg[7][31:0]' into 'registers\_*reg[4][31:0]' [/nfs/home/l/l*\_heiwan/coen316/lab2/lab2\_*wrapper*\_register\_*file.vhd:51]  
INFO: [Synth 8-4471] merging register 'registers*\_reg[8][31:0]' into 'registers\_*reg[4][31:0]' [/nfs/home/l/l*\_heiwan/coen316/lab2/lab2\_*wrapper*\_register\_*file.vhd:51]  
INFO: [Synth 8-4471] merging register 'registers*\_reg[9][31:0]' into 'registers\_*reg[4][31:0]' [/nfs/home/l/l*\_heiwan/coen316/lab2/lab2\_*wrapper*\_register\_*file.vhd:51]  
INFO: [Synth 8-4471] merging register 'registers*\_reg[10][31:0]' into 'registers\_*reg[4][31:0]' [/nfs/home/l/l*\_heiwan/coen316/lab2/lab2\_*wrapper*\_register\_*file.vhd:51]  
INFO: [Synth 8-4471] merging register 'registers*\_reg[11][31:0]' into 'registers\_*reg[4][31:0]' [/nfs/home/l/l*\_heiwan/coen316/lab2/lab2\_*wrapper*\_register\_*file.vhd:51]  
INFO: [Synth 8-4471] merging register 'registers*\_reg[12][31:0]' into 'registers\_*reg[4][31:0]' [/nfs/home/l/l*\_heiwan/coen316/lab2/lab2\_*wrapper*\_register\_*file.vhd:51]  
INFO: [Synth 8-4471] merging register 'registers*\_reg[13][31:0]' into 'registers\_*reg[4][31:0]' [/nfs/home/l/l*\_heiwan/coen316/lab2/lab2\_*wrapper*\_register\_*file.vhd:51]  
INFO: [Synth 8-4471] merging register 'registers*\_reg[14][31:0]' into 'registers\_*reg[4][31:0]' [/nfs/home/l/l*\_heiwan/coen316/lab2/lab2\_*wrapper*\_register\_*file.vhd:51]  
INFO: [Synth 8-4471] merging register 'registers*\_reg[15][31:0]' into 'registers\_*reg[4][31:0]' [/nfs/home/l/l*\_heiwan/coen316/lab2/lab2\_*wrapper*\_register\_*file.vhd:51]  
INFO: [Synth 8-4471] merging register 'registers*\_reg[16][31:0]' into 'registers\_*reg[4][31:0]' [/nfs/home/l/l*\_heiwan/coen316/lab2/lab2\_*wrapper*\_register\_*file.vhd:51]  
INFO: [Synth 8-4471] merging register 'registers*\_reg[17][31:0]' into 'registers\_*reg[4][31:0]' [/nfs/home/l/l*\_heiwan/coen316/lab2/lab2\_*wrapper*\_register\_*file.vhd:51]  
INFO: [Synth 8-4471] merging register 'registers*\_reg[18][31:0]' into 'registers\_*reg[4][31:0]' [/nfs/home/l/l*\_heiwan/coen316/lab2/lab2\_*wrapper*\_register\_*file.vhd:51]  
INFO: [Synth 8-4471] merging register 'registers*\_reg[19][31:0]' into 'registers\_*reg[4][31:0]' [/nfs/home/l/l*\_heiwan/coen316/lab2/lab2\_*wrapper*\_register\_*file.vhd:51]  
INFO: [Synth 8-4471] merging register 'registers*\_reg[20][31:0]' into 'registers\_*reg[4][31:0]' [/nfs/home/l/l*\_heiwan/coen316/lab2/lab2\_*wrapper*\_register\_*file.vhd:51]  
INFO: [Synth 8-4471] merging register 'registers*\_reg[21][31:0]' into 'registers\_*reg[4][31:0]' [/nfs/home/l/l*\_heiwan/coen316/lab2/lab2\_*wrapper*\_register\_*file.vhd:51]  
INFO: [Synth 8-4471] merging register 'registers*\_reg[22][31:0]' into 'registers\_*reg[4][31:0]' [/nfs/home/l/l*\_heiwan/coen316/lab2/lab2\_*wrapper*\_register\_*file.vhd:51]  
INFO: [Synth 8-4471] merging register 'registers*\_reg[23][31:0]' into 'registers\_*reg[4][31:0]' [/nfs/home/l/l*\_heiwan/coen316/lab2/lab2\_*wrapper*\_register\_*file.vhd:51]  
INFO: [Synth 8-4471] merging register 'registers*\_reg[24][31:0]' into 'registers\_*reg[4][31:0]' [/nfs/home/l/l*\_heiwan/coen316/lab2/lab2\_*wrapper*\_register\_*file.vhd:51]  
INFO: [Synth 8-4471] merging register 'registers*\_reg[25][31:0]' into 'registers\_*reg[4][31:0]' [/nfs/home/l/l*\_heiwan/coen316/lab2/lab2\_*wrapper*\_register\_*file.vhd:51]  
INFO: [Synth 8-4471] merging register 'registers*\_reg[26][31:0]' into 'registers\_*reg[4][31:0]' [/nfs/home/l/l*\_heiwan/coen316/lab2/lab2\_*wrapper*\_register\_*file.vhd:51]  
INFO: [Synth 8-4471] merging register 'registers*\_reg[27][31:0]' into 'registers\_*reg[4][31:0]' [/nfs/home/l/l*\_heiwan/coen316/lab2/lab2\_*wrapper*\_register\_*file.vhd:51]  
INFO: [Synth 8-4471] merging register 'registers*\_reg[28][31:0]' into 'registers\_*reg[4][31:0]' [/nfs/home/l/l*\_heiwan/coen316/lab2/lab2\_*wrapper*\_register\_*file.vhd:51]  
INFO: [Synth 8-4471] merging register 'registers*\_reg[29][31:0]' into 'registers\_*reg[4][31:0]' [/nfs/home/l/l*\_heiwan/coen316/lab2/lab2\_*wrapper*\_register\_*file.vhd:51]  
INFO: [Synth 8-4471] merging register 'registers*\_reg[30][31:0]' into 'registers\_*reg[4][31:0]' [/nfs/home/l/l*\_heiwan/coen316/lab2/lab2\_*wrapper*\_register\_*file.vhd:51]  
INFO: [Synth 8-4471] merging register 'registers*\_reg[31][31:0]' into 'registers\_*reg[4][31:0]' [/nfs/home/l/l*\_heiwan/coen316/lab2/lab2\_*wrapper*\_register\_*file.vhd:51]  
WARNING: [Synth 8-6014] Unused sequential element registers*\_reg[5] was removed. [/nfs/home/l/l\_*heiwan/coen316/lab2/lab2*\_wrapper\_*register\_file.vhd:51]  
WARNING: [Synth 8-6014] Unused sequential element registers*\_reg[6] was removed. [/nfs/home/l/l\_*heiwan/coen316/lab2/lab2*\_wrapper\_*register\_file.vhd:51]  
WARNING: [Synth 8-6014] Unused sequential element registers*\_reg[7] was removed. [/nfs/home/l/l\_*heiwan/coen316/lab2/lab2*\_wrapper\_*register\_file.vhd:51]  
WARNING: [Synth 8-6014] Unused sequential element registers*\_reg[8] was removed. [/nfs/home/l/l\_*heiwan/coen316/lab2/lab2*\_wrapper\_*register\_file.vhd:51]  
WARNING: [Synth 8-6014] Unused sequential element registers*\_reg[9] was removed. [/nfs/home/l/l\_*heiwan/coen316/lab2/lab2*\_wrapper\_*register\_file.vhd:51]  
WARNING: [Synth 8-6014] Unused sequential element registers*\_reg[10] was removed. [/nfs/home/l/l\_*heiwan/coen316/lab2/lab2*\_wrapper\_*register\_file.vhd:51]  
WARNING: [Synth 8-6014] Unused sequential element registers*\_reg[11] was removed. [/nfs/home/l/l\_*heiwan/coen316/lab2/lab2*\_wrapper\_*register\_file.vhd:51]  
WARNING: [Synth 8-6014] Unused sequential element registers*\_reg[12] was removed. [/nfs/home/l/l\_*heiwan/coen316/lab2/lab2*\_wrapper\_*register\_file.vhd:51]  
WARNING: [Synth 8-6014] Unused sequential element registers*\_reg[13] was removed. [/nfs/home/l/l\_*heiwan/coen316/lab2/lab2*\_wrapper\_*register\_file.vhd:51]  
WARNING: [Synth 8-6014] Unused sequential element registers*\_reg[14] was removed. [/nfs/home/l/l\_*heiwan/coen316/lab2/lab2*\_wrapper\_*register\_file.vhd:51]  
WARNING: [Synth 8-6014] Unused sequential element registers*\_reg[15] was removed. [/nfs/home/l/l\_*heiwan/coen316/lab2/lab2*\_wrapper\_*register\_file.vhd:51]  
WARNING: [Synth 8-6014] Unused sequential element registers*\_reg[16] was removed. [/nfs/home/l/l\_*heiwan/coen316/lab2/lab2*\_wrapper\_*register\_file.vhd:51]  
WARNING: [Synth 8-6014] Unused sequential element registers*\_reg[17] was removed. [/nfs/home/l/l\_*heiwan/coen316/lab2/lab2*\_wrapper\_*register\_file.vhd:51]  
WARNING: [Synth 8-6014] Unused sequential element registers*\_reg[18] was removed. [/nfs/home/l/l\_*heiwan/coen316/lab2/lab2*\_wrapper\_*register\_file.vhd:51]  
WARNING: [Synth 8-6014] Unused sequential element registers*\_reg[19] was removed. [/nfs/home/l/l\_*heiwan/coen316/lab2/lab2*\_wrapper\_*register\_file.vhd:51]  
WARNING: [Synth 8-6014] Unused sequential element registers*\_reg[20] was removed. [/nfs/home/l/l\_*heiwan/coen316/lab2/lab2*\_wrapper\_*register\_file.vhd:51]  
WARNING: [Synth 8-6014] Unused sequential element registers*\_reg[21] was removed. [/nfs/home/l/l\_*heiwan/coen316/lab2/lab2*\_wrapper\_*register\_file.vhd:51]  
WARNING: [Synth 8-6014] Unused sequential element registers*\_reg[22] was removed. [/nfs/home/l/l\_*heiwan/coen316/lab2/lab2*\_wrapper\_*register\_file.vhd:51]  
WARNING: [Synth 8-6014] Unused sequential element registers*\_reg[23] was removed. [/nfs/home/l/l\_*heiwan/coen316/lab2/lab2*\_wrapper\_*register\_file.vhd:51]  
WARNING: [Synth 8-6014] Unused sequential element registers*\_reg[24] was removed. [/nfs/home/l/l\_*heiwan/coen316/lab2/lab2*\_wrapper\_*register\_file.vhd:51]  
WARNING: [Synth 8-6014] Unused sequential element registers*\_reg[25] was removed. [/nfs/home/l/l\_*heiwan/coen316/lab2/lab2*\_wrapper\_*register\_file.vhd:51]  
WARNING: [Synth 8-6014] Unused sequential element registers*\_reg[26] was removed. [/nfs/home/l/l\_*heiwan/coen316/lab2/lab2*\_wrapper\_*register\_file.vhd:51]  
WARNING: [Synth 8-6014] Unused sequential element registers*\_reg[27] was removed. [/nfs/home/l/l\_*heiwan/coen316/lab2/lab2*\_wrapper\_*register\_file.vhd:51]  
WARNING: [Synth 8-6014] Unused sequential element registers*\_reg[28] was removed. [/nfs/home/l/l\_*heiwan/coen316/lab2/lab2*\_wrapper\_*register\_file.vhd:51]  
WARNING: [Synth 8-6014] Unused sequential element registers*\_reg[29] was removed. [/nfs/home/l/l\_*heiwan/coen316/lab2/lab2*\_wrapper\_*register\_file.vhd:51]  
WARNING: [Synth 8-6014] Unused sequential element registers*\_reg[30] was removed. [/nfs/home/l/l\_*heiwan/coen316/lab2/lab2*\_wrapper\_*register\_file.vhd:51]  
WARNING: [Synth 8-6014] Unused sequential element registers*\_reg[31] was removed. [/nfs/home/l/l\_*heiwan/coen316/lab2/lab2*\_wrapper\_*register\_file.vhd:51]  
WARNING: [Synth 8-3332] Sequential element (registers\_reg[0][31]) is unused and will be removed from module regfile.  
WARNING: [Synth 8-3332] Sequential element (registers\_reg[0][30]) is unused and will be removed from module regfile.  
WARNING: [Synth 8-3332] Sequential element (registers\_reg[0][29]) is unused and will be removed from module regfile.  
WARNING: [Synth 8-3332] Sequential element (registers\_reg[0][28]) is unused and will be removed from module regfile.  
WARNING: [Synth 8-3332] Sequential element (registers\_reg[0][27]) is unused and will be removed from module regfile.  
WARNING: [Synth 8-3332] Sequential element (registers\_reg[0][26]) is unused and will be removed from module regfile.  
WARNING: [Synth 8-3332] Sequential element (registers\_reg[0][25]) is unused and will be removed from module regfile.  
WARNING: [Synth 8-3332] Sequential element (registers\_reg[0][24]) is unused and will be removed from module regfile.  
WARNING: [Synth 8-3332] Sequential element (registers\_reg[0][23]) is unused and will be removed from module regfile.  
WARNING: [Synth 8-3332] Sequential element (registers\_reg[0][22]) is unused and will be removed from module regfile.  
WARNING: [Synth 8-3332] Sequential element (registers\_reg[0][21]) is unused and will be removed from module regfile.  
WARNING: [Synth 8-3332] Sequential element (registers\_reg[0][20]) is unused and will be removed from module regfile.  
WARNING: [Synth 8-3332] Sequential element (registers\_reg[0][19]) is unused and will be removed from module regfile.  
WARNING: [Synth 8-3332] Sequential element (registers\_reg[0][18]) is unused and will be removed from module regfile.  
WARNING: [Synth 8-3332] Sequential element (registers\_reg[0][17]) is unused and will be removed from module regfile.  
WARNING: [Synth 8-3332] Sequential element (registers\_reg[0][16]) is unused and will be removed from module regfile.  
WARNING: [Synth 8-3332] Sequential element (registers\_reg[0][15]) is unused and will be removed from module regfile.  
WARNING: [Synth 8-3332] Sequential element (registers\_reg[0][14]) is unused and will be removed from module regfile.  
WARNING: [Synth 8-3332] Sequential element (registers\_reg[0][13]) is unused and will be removed from module regfile.  
WARNING: [Synth 8-3332] Sequential element (registers\_reg[0][12]) is unused and will be removed from module regfile.  
WARNING: [Synth 8-3332] Sequential element (registers\_reg[0][11]) is unused and will be removed from module regfile.  
WARNING: [Synth 8-3332] Sequential element (registers\_reg[0][10]) is unused and will be removed from module regfile.  
WARNING: [Synth 8-3332] Sequential element (registers\_reg[0][9]) is unused and will be removed from module regfile.  
WARNING: [Synth 8-3332] Sequential element (registers\_reg[0][8]) is unused and will be removed from module regfile.  
WARNING: [Synth 8-3332] Sequential element (registers\_reg[0][7]) is unused and will be removed from module regfile.  
WARNING: [Synth 8-3332] Sequential element (registers\_reg[0][6]) is unused and will be removed from module regfile.  
WARNING: [Synth 8-3332] Sequential element (registers\_reg[0][5]) is unused and will be removed from module regfile.  
WARNING: [Synth 8-3332] Sequential element (registers\_reg[0][4]) is unused and will be removed from module regfile.  
WARNING: [Synth 8-3332] Sequential element (registers\_reg[1][31]) is unused and will be removed from module regfile.  
WARNING: [Synth 8-3332] Sequential element (registers\_reg[1][30]) is unused and will be removed from module regfile.  
WARNING: [Synth 8-3332] Sequential element (registers\_reg[1][29]) is unused and will be removed from module regfile.  
WARNING: [Synth 8-3332] Sequential element (registers\_reg[1][28]) is unused and will be removed from module regfile.  
WARNING: [Synth 8-3332] Sequential element (registers\_reg[1][27]) is unused and will be removed from module regfile.  
WARNING: [Synth 8-3332] Sequential element (registers\_reg[1][26]) is unused and will be removed from module regfile.  
WARNING: [Synth 8-3332] Sequential element (registers\_reg[1][25]) is unused and will be removed from module regfile.  
WARNING: [Synth 8-3332] Sequential element (registers\_reg[1][24]) is unused and will be removed from module regfile.  
WARNING: [Synth 8-3332] Sequential element (registers\_reg[1][23]) is unused and will be removed from module regfile.  
WARNING: [Synth 8-3332] Sequential element (registers\_reg[1][22]) is unused and will be removed from module regfile.  
WARNING: [Synth 8-3332] Sequential element (registers\_reg[1][21]) is unused and will be removed from module regfile.  
WARNING: [Synth 8-3332] Sequential element (registers\_reg[1][20]) is unused and will be removed from module regfile.  
WARNING: [Synth 8-3332] Sequential element (registers\_reg[1][19]) is unused and will be removed from module regfile.  
WARNING: [Synth 8-3332] Sequential element (registers\_reg[1][18]) is unused and will be removed from module regfile.  
WARNING: [Synth 8-3332] Sequential element (registers\_reg[1][17]) is unused and will be removed from module regfile.  
WARNING: [Synth 8-3332] Sequential element (registers\_reg[1][16]) is unused and will be removed from module regfile.  
WARNING: [Synth 8-3332] Sequential element (registers\_reg[1][15]) is unused and will be removed from module regfile.  
WARNING: [Synth 8-3332] Sequential element (registers\_reg[1][14]) is unused and will be removed from module regfile.  
WARNING: [Synth 8-3332] Sequential element (registers\_reg[1][13]) is unused and will be removed from module regfile.  
WARNING: [Synth 8-3332] Sequential element (registers\_reg[1][12]) is unused and will be removed from module regfile.  
WARNING: [Synth 8-3332] Sequential element (registers\_reg[1][11]) is unused and will be removed from module regfile.  
WARNING: [Synth 8-3332] Sequential element (registers\_reg[1][10]) is unused and will be removed from module regfile.  
WARNING: [Synth 8-3332] Sequential element (registers\_reg[1][9]) is unused and will be removed from module regfile.  
WARNING: [Synth 8-3332] Sequential element (registers\_reg[1][8]) is unused and will be removed from module regfile.  
WARNING: [Synth 8-3332] Sequential element (registers\_reg[1][7]) is unused and will be removed from module regfile.  
WARNING: [Synth 8-3332] Sequential element (registers\_reg[1][6]) is unused and will be removed from module regfile.  
WARNING: [Synth 8-3332] Sequential element (registers\_reg[1][5]) is unused and will be removed from module regfile.  
WARNING: [Synth 8-3332] Sequential element (registers\_reg[1][4]) is unused and will be removed from module regfile.  
WARNING: [Synth 8-3332] Sequential element (registers\_reg[2][31]) is unused and will be removed from module regfile.  
WARNING: [Synth 8-3332] Sequential element (registers\_reg[2][30]) is unused and will be removed from module regfile.  
WARNING: [Synth 8-3332] Sequential element (registers\_reg[2][29]) is unused and will be removed from module regfile.  
WARNING: [Synth 8-3332] Sequential element (registers\_reg[2][28]) is unused and will be removed from module regfile.  
WARNING: [Synth 8-3332] Sequential element (registers\_reg[2][27]) is unused and will be removed from module regfile.  
WARNING: [Synth 8-3332] Sequential element (registers\_reg[2][26]) is unused and will be removed from module regfile.  
WARNING: [Synth 8-3332] Sequential element (registers\_reg[2][25]) is unused and will be removed from module regfile.  
WARNING: [Synth 8-3332] Sequential element (registers\_reg[2][24]) is unused and will be removed from module regfile.  
WARNING: [Synth 8-3332] Sequential element (registers\_reg[2][23]) is unused and will be removed from module regfile.  
WARNING: [Synth 8-3332] Sequential element (registers\_reg[2][22]) is unused and will be removed from module regfile.  
WARNING: [Synth 8-3332] Sequential element (registers\_reg[2][21]) is unused and will be removed from module regfile.  
WARNING: [Synth 8-3332] Sequential element (registers\_reg[2][20]) is unused and will be removed from module regfile.  
WARNING: [Synth 8-3332] Sequential element (registers\_reg[2][19]) is unused and will be removed from module regfile.  
WARNING: [Synth 8-3332] Sequential element (registers\_reg[2][18]) is unused and will be removed from module regfile.  
WARNING: [Synth 8-3332] Sequential element (registers\_reg[2][17]) is unused and will be removed from module regfile.  
WARNING: [Synth 8-3332] Sequential element (registers\_reg[2][16]) is unused and will be removed from module regfile.  
WARNING: [Synth 8-3332] Sequential element (registers\_reg[2][15]) is unused and will be removed from module regfile.  
WARNING: [Synth 8-3332] Sequential element (registers\_reg[2][14]) is unused and will be removed from module regfile.  
WARNING: [Synth 8-3332] Sequential element (registers\_reg[2][13]) is unused and will be removed from module regfile.  
WARNING: [Synth 8-3332] Sequential element (registers\_reg[2][12]) is unused and will be removed from module regfile.  
WARNING: [Synth 8-3332] Sequential element (registers\_reg[2][11]) is unused and will be removed from module regfile.  
WARNING: [Synth 8-3332] Sequential element (registers\_reg[2][10]) is unused and will be removed from module regfile.  
WARNING: [Synth 8-3332] Sequential element (registers\_reg[2][9]) is unused and will be removed from module regfile.  
WARNING: [Synth 8-3332] Sequential element (registers\_reg[2][8]) is unused and will be removed from module regfile.  
WARNING: [Synth 8-3332] Sequential element (registers\_reg[2][7]) is unused and will be removed from module regfile.  
WARNING: [Synth 8-3332] Sequential element (registers\_reg[2][6]) is unused and will be removed from module regfile.  
WARNING: [Synth 8-3332] Sequential element (registers\_reg[2][5]) is unused and will be removed from module regfile.  
WARNING: [Synth 8-3332] Sequential element (registers\_reg[2][4]) is unused and will be removed from module regfile.  
WARNING: [Synth 8-3332] Sequential element (registers\_reg[3][31]) is unused and will be removed from module regfile.  
WARNING: [Synth 8-3332] Sequential element (registers\_reg[3][30]) is unused and will be removed from module regfile.  
WARNING: [Synth 8-3332] Sequential element (registers\_reg[3][29]) is unused and will be removed from module regfile.  
WARNING: [Synth 8-3332] Sequential element (registers\_reg[3][28]) is unused and will be removed from module regfile.  
WARNING: [Synth 8-3332] Sequential element (registers\_reg[3][27]) is unused and will be removed from module regfile.  
WARNING: [Synth 8-3332] Sequential element (registers\_reg[3][26]) is unused and will be removed from module regfile.  
WARNING: [Synth 8-3332] Sequential element (registers\_reg[3][25]) is unused and will be removed from module regfile.  
WARNING: [Synth 8-3332] Sequential element (registers\_reg[3][24]) is unused and will be removed from module regfile.  
WARNING: [Synth 8-3332] Sequential element (registers\_reg[3][23]) is unused and will be removed from module regfile.  
WARNING: [Synth 8-3332] Sequential element (registers\_reg[3][22]) is unused and will be removed from module regfile.  
WARNING: [Synth 8-3332] Sequential element (registers\_reg[3][21]) is unused and will be removed from module regfile.  
WARNING: [Synth 8-3332] Sequential element (registers\_reg[3][20]) is unused and will be removed from module regfile.  
WARNING: [Synth 8-3332] Sequential element (registers\_reg[3][19]) is unused and will be removed from module regfile.  
WARNING: [Synth 8-3332] Sequential element (registers\_reg[3][18]) is unused and will be removed from module regfile.  
WARNING: [Synth 8-3332] Sequential element (registers\_reg[3][17]) is unused and will be removed from module regfile.  
WARNING: [Synth 8-3332] Sequential element (registers\_reg[3][16]) is unused and will be removed from module regfile.  
INFO: [Common 17-14] Message 'Synth 8-3332' appears 100 times and further instances of the messages will be disabled. Use the Tcl command set*\_msg\_*config to change the current settings.  
---------------------------------------------------------------------------------  
Finished Cross Boundary and Area Optimization : Time (s): cpu = 00:00:16 ; elapsed = 00:01:09 . Memory (MB): peak = 1885.160 ; gain = 503.293 ; free physical = 121766 ; free virtual = 156836  
---------------------------------------------------------------------------------  
  
Report RTL Partitions:   
+-+--------------+------------+----------+  
| |RTL Partition |Replication |Instances |  
+-+--------------+------------+----------+  
+-+--------------+------------+----------+  
---------------------------------------------------------------------------------  
Start Applying XDC Timing Constraints  
---------------------------------------------------------------------------------  
---------------------------------------------------------------------------------  
Finished Applying XDC Timing Constraints : Time (s): cpu = 00:00:23 ; elapsed = 00:01:27 . Memory (MB): peak = 1885.160 ; gain = 503.293 ; free physical = 121639 ; free virtual = 156709  
---------------------------------------------------------------------------------  
---------------------------------------------------------------------------------  
Start Timing Optimization  
---------------------------------------------------------------------------------  
---------------------------------------------------------------------------------  
Finished Timing Optimization : Time (s): cpu = 00:00:23 ; elapsed = 00:01:27 . Memory (MB): peak = 1885.160 ; gain = 503.293 ; free physical = 121639 ; free virtual = 156709  
---------------------------------------------------------------------------------  
  
Report RTL Partitions:   
+-+--------------+------------+----------+  
| |RTL Partition |Replication |Instances |  
+-+--------------+------------+----------+  
+-+--------------+------------+----------+  
---------------------------------------------------------------------------------  
Start Technology Mapping  
---------------------------------------------------------------------------------  
---------------------------------------------------------------------------------  
Finished Technology Mapping : Time (s): cpu = 00:00:23 ; elapsed = 00:01:27 . Memory (MB): peak = 1885.160 ; gain = 503.293 ; free physical = 121639 ; free virtual = 156709  
---------------------------------------------------------------------------------  
  
Report RTL Partitions:   
+-+--------------+------------+----------+  
| |RTL Partition |Replication |Instances |  
+-+--------------+------------+----------+  
+-+--------------+------------+----------+  
---------------------------------------------------------------------------------  
Start IO Insertion  
---------------------------------------------------------------------------------  
---------------------------------------------------------------------------------  
Start Flattening Before IO Insertion  
---------------------------------------------------------------------------------  
---------------------------------------------------------------------------------  
Finished Flattening Before IO Insertion  
---------------------------------------------------------------------------------  
---------------------------------------------------------------------------------  
Start Final Netlist Cleanup  
---------------------------------------------------------------------------------  
---------------------------------------------------------------------------------  
Finished Final Netlist Cleanup  
---------------------------------------------------------------------------------  
---------------------------------------------------------------------------------  
Finished IO Insertion : Time (s): cpu = 00:00:23 ; elapsed = 00:01:28 . Memory (MB): peak = 1885.160 ; gain = 503.293 ; free physical = 121639 ; free virtual = 156709  
---------------------------------------------------------------------------------  
  
Report Check Netlist:   
+------+------------------+-------+---------+-------+------------------+  
| |Item |Errors |Warnings |Status |Description |  
+------+------------------+-------+---------+-------+------------------+  
|1 |multi*\_driven\_*nets | 0| 0|Passed |Multi driven nets |  
+------+------------------+-------+---------+-------+------------------+  
---------------------------------------------------------------------------------  
Start Renaming Generated Instances  
---------------------------------------------------------------------------------  
---------------------------------------------------------------------------------  
Finished Renaming Generated Instances : Time (s): cpu = 00:00:23 ; elapsed = 00:01:28 . Memory (MB): peak = 1885.160 ; gain = 503.293 ; free physical = 121639 ; free virtual = 156709  
---------------------------------------------------------------------------------  
  
Report RTL Partitions:   
+-+--------------+------------+----------+  
| |RTL Partition |Replication |Instances |  
+-+--------------+------------+----------+  
+-+--------------+------------+----------+  
---------------------------------------------------------------------------------  
Start Rebuilding User Hierarchy  
---------------------------------------------------------------------------------  
---------------------------------------------------------------------------------  
Finished Rebuilding User Hierarchy : Time (s): cpu = 00:00:23 ; elapsed = 00:01:28 . Memory (MB): peak = 1885.160 ; gain = 503.293 ; free physical = 121639 ; free virtual = 156709  
---------------------------------------------------------------------------------  
---------------------------------------------------------------------------------  
Start Renaming Generated Ports  
---------------------------------------------------------------------------------  
---------------------------------------------------------------------------------  
Finished Renaming Generated Ports : Time (s): cpu = 00:00:23 ; elapsed = 00:01:28 . Memory (MB): peak = 1885.160 ; gain = 503.293 ; free physical = 121639 ; free virtual = 156709  
---------------------------------------------------------------------------------  
---------------------------------------------------------------------------------  
Start Handling Custom Attributes  
---------------------------------------------------------------------------------  
---------------------------------------------------------------------------------  
Finished Handling Custom Attributes : Time (s): cpu = 00:00:23 ; elapsed = 00:01:28 . Memory (MB): peak = 1885.160 ; gain = 503.293 ; free physical = 121639 ; free virtual = 156709  
---------------------------------------------------------------------------------  
---------------------------------------------------------------------------------  
Start Renaming Generated Nets  
---------------------------------------------------------------------------------  
---------------------------------------------------------------------------------  
Finished Renaming Generated Nets : Time (s): cpu = 00:00:23 ; elapsed = 00:01:28 . Memory (MB): peak = 1885.160 ; gain = 503.293 ; free physical = 121639 ; free virtual = 156709  
---------------------------------------------------------------------------------  
---------------------------------------------------------------------------------  
Start Writing Synthesis Report  
---------------------------------------------------------------------------------  
  
Report BlackBoxes:   
+-+--------------+----------+  
| |BlackBox name |Instances |  
+-+--------------+----------+  
+-+--------------+----------+  
  
Report Cell Usage:   
+------+-----+------+  
| |Cell |Count |  
+------+-----+------+  
|1 |BUFG | 1|  
|2 |LUT3 | 4|  
|3 |LUT6 | 8|  
|4 |FDCE | 16|  
|5 |IBUF | 13|  
|6 |OBUF | 8|  
+------+-----+------+  
  
Report Instance Areas:   
+------+---------+-------+------+  
| |Instance |Module |Cells |  
+------+---------+-------+------+  
|1 |top | | 50|  
+------+---------+-------+------+  
---------------------------------------------------------------------------------  
Finished Writing Synthesis Report : Time (s): cpu = 00:00:23 ; elapsed = 00:01:28 . Memory (MB): peak = 1885.160 ; gain = 503.293 ; free physical = 121639 ; free virtual = 156709  
---------------------------------------------------------------------------------  
Synthesis finished with 0 errors, 0 critical warnings and 171 warnings.  
Synthesis Optimization Runtime : Time (s): cpu = 00:00:13 ; elapsed = 00:00:31 . Memory (MB): peak = 1885.160 ; gain = 131.367 ; free physical = 121697 ; free virtual = 156767  
Synthesis Optimization Complete : Time (s): cpu = 00:00:23 ; elapsed = 00:01:28 . Memory (MB): peak = 1885.160 ; gain = 503.293 ; free physical = 121706 ; free virtual = 156776  
INFO: [Project 1-571] Translating synthesized netlist  
INFO: [Netlist 29-17] Analyzing 13 Unisim elements for replacement  
INFO: [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds  
INFO: [Project 1-570] Preparing netlist for logic optimization  
INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).  
INFO: [Project 1-111] Unisim Transformation Summary:  
No Unisim elements were transformed.  
  
INFO: [Common 17-83] Releasing license: Synthesis  
74 Infos, 127 Warnings, 0 Critical Warnings and 0 Errors encountered.  
synth\_design completed successfully  
synth\_design: Time (s): cpu = 00:00:25 ; elapsed = 00:01:29 . Memory (MB): peak = 1885.160 ; gain = 516.020 ; free physical = 121693 ; free virtual = 156763  
WARNING: [Constraints 18-5210] No constraint will be written out.  
INFO: [Common 17-1381] The checkpoint '/nfs/home/l/l*\_heiwan/coen316/lab2/vivado\_*test/lab2*\_v1/lab2\_*v1.runs/synth\_1/regfile.dcp' has been generated.  
INFO: [runtcl-4] Executing : report*\_utilization -file regfile\_*utilization*\_synth.rpt -pb regfile\_*utilization\_synth.pb  
report\_utilization: Time (s): cpu = 00:00:00.05 ; elapsed = 00:00:00.14 . Memory (MB): peak = 1885.160 ; gain = 0.000 ; free physical = 121693 ; free virtual = 156763  
INFO: [Common 17-206] Exiting Vivado at Wed Oct 25 13:29:35 2023...

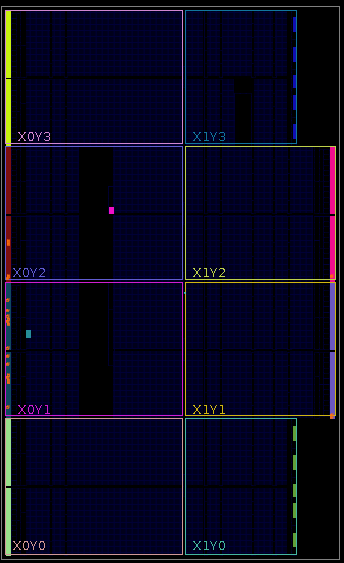
**5.4) Implementation Log**

****

**Warning Discussions:** When first running the implementation, we receive a red error concerning the clock rule. As such, after adding “set\_property CLOCK\_DEDICATED\_ROUTE FALSE [get\_nets clk]”, this error was then solved.



**Warning Discussions:** The red error message is gone. We only have a total of 5 warnings for the implementations. Two of which is related to “Place Design” and three of which is related to “Route Design”. While all these warning have something to do with timing and clock checks route, it won’t be detrimental to the functionality of this project.



The above image is the implemented design.

\*\*\* Running vivado  
 **with** args -log regfile.vdi -applog -m64 -product Vivado -messageDb vivado.pb -mode batch -source regfile.tcl -notrace  
  
  
\*\*\*\*\*\* Vivado v2018.2 (64-bit)  
 \*\*\*\* SW Build 2258646 on Thu Jun 14 20:02:38 MDT 2018  
 \*\*\*\* IP Build 2256618 on Thu Jun 14 22:10:49 MDT 2018  
 \*\* Copyright 1986-2018 Xilinx, Inc. All Rights Reserved.  
  
source regfile.tcl -notrace  
Command: link\_design -top regfile -part xc7a100tcsg324-1  
Design is defaulting to srcset: sources\_1  
Design is defaulting to constrset: constrs\_1  
INFO: [Netlist 29-17] Analyzing 13 Unisim elements for replacement  
INFO: [Netlist 29-28] Unisim Transformation completed **in** 0 CPU seconds  
INFO: [Project 1-479] Netlist was created **with** Vivado 2018.2  
INFO: [Device 21-403] Loading part xc7a100tcsg324-1  
INFO: [Project 1-570] Preparing netlist for logic optimization  
Parsing XDC File [/nfs/home/l/l\_heiwan/coen316/lab2/lab2\_constraints.xdc]  
Finished Parsing XDC File [/nfs/home/l/l\_heiwan/coen316/lab2/lab2\_constraints.xdc]  
INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).  
INFO: [Project 1-111] Unisim Transformation Summary:  
No Unisim elements were transformed.  
  
7 Infos, 0 Warnings, 0 Critical Warnings and 0 Errors encountered.  
link\_design completed successfully  
link\_design: Time (s): cpu = 00:00:10 ; elapsed = 00:00:59 . Memory (MB): peak = 1645.535 ; gain = 271.387 ; free physical = 121806 ; free virtual = 156874  
Command: opt\_design  
Attempting to get a license for feature 'Implementation' and/or device 'xc7a100t'  
INFO: [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a100t'  
Running DRC as a precondition to command opt\_design  
  
Starting DRC Task  
INFO: [DRC 23-27] Running DRC **with** 8 threads  
INFO: [Project 1-461] DRC finished **with** 0 Errors  
INFO: [Project 1-462] Please refer to the DRC report (report\_drc) for more information.  
  
Time (s): cpu = 00:00:02 ; elapsed = 00:00:04 . Memory (MB): peak = 1725.562 ; gain = 80.027 ; free physical = 121800 ; free virtual = 156868  
  
Starting Cache Timing Information Task  
INFO: [Timing 38-35] Done setting XDC timing constraints.  
Ending Cache Timing Information Task | Checksum: 15828eaf8  
  
Time (s): cpu = 00:00:15 ; elapsed = 00:01:08 . Memory (MB): peak = 2186.059 ; gain = 460.496 ; free physical = 121391 ; free virtual = 156460  
  
Starting Logic Optimization Task  
  
Phase 1 Retarget  
INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).  
INFO: [Opt 31-49] Retargeted 0 cell(s).  
Phase 1 Retarget | Checksum: 15828eaf8  
  
Time (s): cpu = 00:00:00.02 ; elapsed = 00:00:00.02 . Memory (MB): peak = 2186.059 ; gain = 0.000 ; free physical = 121419 ; free virtual = 156488  
INFO: [Opt 31-389] Phase Retarget created 0 cells and removed 0 cells  
  
Phase 2 Constant propagation  
INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).  
Phase 2 Constant propagation | Checksum: 15828eaf8  
  
Time (s): cpu = 00:00:00.02 ; elapsed = 00:00:00.02 . Memory (MB): peak = 2186.059 ; gain = 0.000 ; free physical = 121419 ; free virtual = 156488  
INFO: [Opt 31-389] Phase Constant propagation created 0 cells and removed 0 cells  
  
Phase 3 Sweep  
Phase 3 Sweep | Checksum: 15828eaf8  
  
Time (s): cpu = 00:00:00.02 ; elapsed = 00:00:00.02 . Memory (MB): peak = 2186.059 ; gain = 0.000 ; free physical = 121419 ; free virtual = 156488  
INFO: [Opt 31-389] Phase Sweep created 0 cells and removed 0 cells  
  
Phase 4 BUFG optimization  
Phase 4 BUFG optimization | Checksum: 15828eaf8  
  
Time (s): cpu = 00:00:00.02 ; elapsed = 00:00:00.03 . Memory (MB): peak = 2186.059 ; gain = 0.000 ; free physical = 121419 ; free virtual = 156488  
INFO: [Opt 31-662] Phase BUFG optimization created 0 cells of which 0 are BUFGs and removed 0 cells.  
  
Phase 5 Shift Register Optimization  
Phase 5 Shift Register Optimization | Checksum: 15828eaf8  
  
Time (s): cpu = 00:00:00.02 ; elapsed = 00:00:00.03 . Memory (MB): peak = 2186.059 ; gain = 0.000 ; free physical = 121419 ; free virtual = 156488  
INFO: [Opt 31-389] Phase Shift Register Optimization created 0 cells and removed 0 cells  
  
Phase 6 Post Processing Netlist  
Phase 6 Post Processing Netlist | Checksum: 15828eaf8  
  
Time (s): cpu = 00:00:00.02 ; elapsed = 00:00:00.03 . Memory (MB): peak = 2186.059 ; gain = 0.000 ; free physical = 121419 ; free virtual = 156488  
INFO: [Opt 31-389] Phase Post Processing Netlist created 0 cells and removed 0 cells  
  
Starting Connectivity Check Task  
  
Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2186.059 ; gain = 0.000 ; free physical = 121419 ; free virtual = 156488  
Ending Logic Optimization Task | Checksum: 15828eaf8  
  
Time (s): cpu = 00:00:00.03 ; elapsed = 00:00:00.03 . Memory (MB): peak = 2186.059 ; gain = 0.000 ; free physical = 121419 ; free virtual = 156488  
  
Starting Power Optimization Task  
INFO: [Pwropt 34-132] Skipping clock gating for clocks **with** a period < 2.00 ns.  
Ending Power Optimization Task | Checksum: 15828eaf8  
  
Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00.06 . Memory (MB): peak = 2186.062 ; gain = 0.004 ; free physical = 121419 ; free virtual = 156488  
  
Starting Final Cleanup Task  
Ending Final Cleanup Task | Checksum: 15828eaf8  
  
Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2186.062 ; gain = 0.000 ; free physical = 121419 ; free virtual = 156488  
INFO: [Common 17-83] Releasing license: Implementation  
23 Infos, 0 Warnings, 0 Critical Warnings and 0 Errors encountered.  
opt\_design completed successfully  
opt\_design: Time (s): cpu = 00:00:17 ; elapsed = 00:01:12 . Memory (MB): peak = 2186.062 ; gain = 540.527 ; free physical = 121419 ; free virtual = 156488  
INFO: [Timing 38-480] Writing timing data to binary archive.  
Writing placer database...  
Writing XDEF routing.  
Writing XDEF routing logical nets.  
Writing XDEF routing special nets.  
Write XDEF Complete: Time (s): cpu = 00:00:00.04 ; elapsed = 00:00:00.03 . Memory (MB): peak = 2218.078 ; gain = 0.004 ; free physical = 121416 ; free virtual = 156486  
INFO: [Common 17-1381] The checkpoint '/nfs/home/l/l\_heiwan/coen316/lab2/vivado\_test/lab2\_v1/lab2\_v1.runs/impl\_1/regfile\_opt.dcp' has been generated.  
INFO: [runtcl-4] Executing : report\_drc -file regfile\_drc\_opted.rpt -pb regfile\_drc\_opted.pb -rpx regfile\_drc\_opted.rpx  
Command: report\_drc -file regfile\_drc\_opted.rpt -pb regfile\_drc\_opted.pb -rpx regfile\_drc\_opted.rpx  
INFO: [IP\_Flow 19-234] Refreshing IP repositories  
INFO: [IP\_Flow 19-1704] No user IP repositories specified  
INFO: [IP\_Flow 19-2313] Loaded Vivado IP repository '/CMC/tools/xilinx/Vivado\_2018.2/Vivado/2018.2/data/ip'.  
INFO: [DRC 23-27] Running DRC **with** 8 threads  
INFO: [Coretcl 2-168] The results of DRC are **in** file /nfs/home/l/l\_heiwan/coen316/lab2/vivado\_test/lab2\_v1/lab2\_v1.runs/impl\_1/regfile\_drc\_opted.rpt.  
report\_drc completed successfully  
report\_drc: Time (s): cpu = 00:00:04 ; elapsed = 00:00:07 . Memory (MB): peak = 2298.117 ; gain = 80.031 ; free physical = 121376 ; free virtual = 156444  
Command: place\_design  
Attempting to get a license for feature 'Implementation' and/or device 'xc7a100t'  
INFO: [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a100t'  
INFO: [DRC 23-27] Running DRC **with** 8 threads  
INFO: [Vivado\_Tcl 4-198] DRC finished **with** 0 Errors  
INFO: [Vivado\_Tcl 4-199] Please refer to the DRC report (report\_drc) for more information.  
Running DRC as a precondition to command place\_design  
INFO: [DRC 23-27] Running DRC **with** 8 threads  
INFO: [Vivado\_Tcl 4-198] DRC finished **with** 0 Errors  
INFO: [Vivado\_Tcl 4-199] Please refer to the DRC report (report\_drc) for more information.  
  
Starting Placer Task  
INFO: [Place 30-611] Multithreading enabled for place\_design using a maximum of 8 CPUs  
  
Phase 1 Placer Initialization  
  
Phase 1.1 Placer Initialization Netlist Sorting  
Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2298.117 ; gain = 0.000 ; free physical = 121373 ; free virtual = 156441  
Phase 1.1 Placer Initialization Netlist Sorting | Checksum: 887f4e82  
  
Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.03 . Memory (MB): peak = 2298.117 ; gain = 0.000 ; free physical = 121373 ; free virtual = 156441  
Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2298.117 ; gain = 0.000 ; free physical = 121373 ; free virtual = 156441  
  
Phase 1.2 IO Placement/ Clock Placement/ Build Placer Device  
INFO: [Timing 38-35] Done setting XDC timing constraints.  
WARNING: [Place 30-574] Poor placement for routing between an IO pin and BUFG. This is normally an ERROR but the CLOCK\_DEDICATED\_ROUTE constraint is set to FALSE allowing your design to continue. The use of this override is highly discouraged as it may lead to very poor timing results. It is recommended that this error condition be corrected **in** the design.  
  
 clk\_IBUF\_inst (IBUF.O) is locked to IOB\_X0Y93  
 clk\_IBUF\_BUFG\_inst (BUFG.I) is provisionally placed by clockplacer on BUFGCTRL\_X0Y0  
Resolution: Poor placement of an IO pin and a BUFG has resulted **in** the router using a non-dedicated path between the two. There are several things that could trigger this DRC, each of which can cause unpredictable clock insertion delays that result **in** poor timing. This DRC could be caused by any of the following: (a) a clock port was placed on a pin that is not a CCIO-pin (b)the BUFG has not been placed **in** the same half of the device or SLR as the CCIO-pin (c) a single ended clock has been placed on the N-Side of a differential pair CCIO-pin.  
Phase 1.2 IO Placement/ Clock Placement/ Build Placer Device | Checksum: bc3db83b  
  
Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.63 . Memory (MB): peak = 2298.117 ; gain = 0.000 ; free physical = 121374 ; free virtual = 156443  
  
Phase 1.3 Build Placer Netlist Model  
Phase 1.3 Build Placer Netlist Model | Checksum: 1a56b6418  
  
Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.66 . Memory (MB): peak = 2298.117 ; gain = 0.000 ; free physical = 121374 ; free virtual = 156443  
  
Phase 1.4 Constrain Clocks/Macros  
Phase 1.4 Constrain Clocks/Macros | Checksum: 1a56b6418  
  
Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.67 . Memory (MB): peak = 2298.117 ; gain = 0.000 ; free physical = 121374 ; free virtual = 156443  
Phase 1 Placer Initialization | Checksum: 1a56b6418  
  
Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.67 . Memory (MB): peak = 2298.117 ; gain = 0.000 ; free physical = 121374 ; free virtual = 156443  
  
Phase 2 Global Placement  
  
Phase 2.1 Floorplanning  
Phase 2.1 Floorplanning | Checksum: 1a56b6418  
  
Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.69 . Memory (MB): peak = 2298.117 ; gain = 0.000 ; free physical = 121372 ; free virtual = 156441  
WARNING: [Place 46-29] place\_design is not **in** timing mode. Skip physical synthesis **in** placer  
Phase 2 Global Placement | Checksum: 12bf51b96  
  
Time (s): cpu = 00:00:03 ; elapsed = 00:00:01 . Memory (MB): peak = 2410.164 ; gain = 112.047 ; free physical = 121335 ; free virtual = 156403  
  
Phase 3 Detail Placement  
  
Phase 3.1 Commit Multi Column Macros  
Phase 3.1 Commit Multi Column Macros | Checksum: 12bf51b96  
  
Time (s): cpu = 00:00:03 ; elapsed = 00:00:01 . Memory (MB): peak = 2410.164 ; gain = 112.047 ; free physical = 121335 ; free virtual = 156403  
  
Phase 3.2 Commit Most Macros & LUTRAMs  
Phase 3.2 Commit Most Macros & LUTRAMs | Checksum: 1828258a9  
  
Time (s): cpu = 00:00:03 ; elapsed = 00:00:01 . Memory (MB): peak = 2410.164 ; gain = 112.047 ; free physical = 121335 ; free virtual = 156403  
  
Phase 3.3 Area Swap Optimization  
Phase 3.3 Area Swap Optimization | Checksum: be36d709  
  
Time (s): cpu = 00:00:03 ; elapsed = 00:00:01 . Memory (MB): peak = 2410.164 ; gain = 112.047 ; free physical = 121334 ; free virtual = 156403  
  
Phase 3.4 Pipeline Register Optimization  
Phase 3.4 Pipeline Register Optimization | Checksum: be36d709  
  
Time (s): cpu = 00:00:03 ; elapsed = 00:00:01 . Memory (MB): peak = 2410.164 ; gain = 112.047 ; free physical = 121334 ; free virtual = 156403  
  
Phase 3.5 Small Shape Detail Placement  
Phase 3.5 Small Shape Detail Placement | Checksum: b78b51c7  
  
Time (s): cpu = 00:00:03 ; elapsed = 00:00:01 . Memory (MB): peak = 2410.164 ; gain = 112.047 ; free physical = 121330 ; free virtual = 156399  
  
Phase 3.6 Re-assign LUT pins  
Phase 3.6 Re-assign LUT pins | Checksum: b78b51c7  
  
Time (s): cpu = 00:00:03 ; elapsed = 00:00:01 . Memory (MB): peak = 2410.164 ; gain = 112.047 ; free physical = 121330 ; free virtual = 156399  
  
Phase 3.7 Pipeline Register Optimization  
Phase 3.7 Pipeline Register Optimization | Checksum: b78b51c7  
  
Time (s): cpu = 00:00:03 ; elapsed = 00:00:01 . Memory (MB): peak = 2410.164 ; gain = 112.047 ; free physical = 121330 ; free virtual = 156399  
Phase 3 Detail Placement | Checksum: b78b51c7  
  
Time (s): cpu = 00:00:03 ; elapsed = 00:00:01 . Memory (MB): peak = 2410.164 ; gain = 112.047 ; free physical = 121330 ; free virtual = 156399  
  
Phase 4 Post Placement Optimization and Clean-Up  
  
Phase 4.1 Post Commit Optimization  
Phase 4.1 Post Commit Optimization | Checksum: b78b51c7  
  
Time (s): cpu = 00:00:04 ; elapsed = 00:00:01 . Memory (MB): peak = 2410.164 ; gain = 112.047 ; free physical = 121330 ; free virtual = 156399  
  
Phase 4.2 Post Placement Cleanup  
Phase 4.2 Post Placement Cleanup | Checksum: b78b51c7  
  
Time (s): cpu = 00:00:04 ; elapsed = 00:00:01 . Memory (MB): peak = 2410.164 ; gain = 112.047 ; free physical = 121332 ; free virtual = 156401  
  
Phase 4.3 Placer Reporting  
Phase 4.3 Placer Reporting | Checksum: b78b51c7  
  
Time (s): cpu = 00:00:04 ; elapsed = 00:00:01 . Memory (MB): peak = 2410.164 ; gain = 112.047 ; free physical = 121332 ; free virtual = 156401  
  
Phase 4.4 Final Placement Cleanup  
Phase 4.4 Final Placement Cleanup | Checksum: b78b51c7  
  
Time (s): cpu = 00:00:04 ; elapsed = 00:00:01 . Memory (MB): peak = 2410.164 ; gain = 112.047 ; free physical = 121332 ; free virtual = 156401  
Phase 4 Post Placement Optimization and Clean-Up | Checksum: b78b51c7  
  
Time (s): cpu = 00:00:04 ; elapsed = 00:00:01 . Memory (MB): peak = 2410.164 ; gain = 112.047 ; free physical = 121332 ; free virtual = 156401  
Ending Placer Task | Checksum: 2bc47609  
  
Time (s): cpu = 00:00:04 ; elapsed = 00:00:01 . Memory (MB): peak = 2410.164 ; gain = 112.047 ; free physical = 121349 ; free virtual = 156418  
INFO: [Common 17-83] Releasing license: Implementation  
41 Infos, 2 Warnings, 0 Critical Warnings and 0 Errors encountered.  
place\_design completed successfully  
place\_design: Time (s): cpu = 00:00:05 ; elapsed = 00:00:05 . Memory (MB): peak = 2410.164 ; gain = 112.047 ; free physical = 121349 ; free virtual = 156418  
INFO: [Timing 38-480] Writing timing data to binary archive.  
Writing placer database...  
Writing XDEF routing.  
Writing XDEF routing logical nets.  
Writing XDEF routing special nets.  
Write XDEF Complete: Time (s): cpu = 00:00:00.04 ; elapsed = 00:00:00.02 . Memory (MB): peak = 2410.164 ; gain = 0.000 ; free physical = 121350 ; free virtual = 156419  
INFO: [Common 17-1381] The checkpoint '/nfs/home/l/l\_heiwan/coen316/lab2/vivado\_test/lab2\_v1/lab2\_v1.runs/impl\_1/regfile\_placed.dcp' has been generated.  
INFO: [runtcl-4] Executing : report\_io -file regfile\_io\_placed.rpt  
report\_io: Time (s): cpu = 00:00:00.08 ; elapsed = 00:00:00.15 . Memory (MB): peak = 2410.164 ; gain = 0.000 ; free physical = 121349 ; free virtual = 156418  
INFO: [runtcl-4] Executing : report\_utilization -file regfile\_utilization\_placed.rpt -pb regfile\_utilization\_placed.pb  
report\_utilization: Time (s): cpu = 00:00:00.06 ; elapsed = 00:00:00.13 . Memory (MB): peak = 2410.164 ; gain = 0.000 ; free physical = 121355 ; free virtual = 156424  
INFO: [runtcl-4] Executing : report\_control\_sets -verbose -file regfile\_control\_sets\_placed.rpt  
report\_control\_sets: Time (s): cpu = 00:00:00.02 ; elapsed = 00:00:00.09 . Memory (MB): peak = 2410.164 ; gain = 0.000 ; free physical = 121355 ; free virtual = 156424  
Command: route\_design  
Attempting to get a license for feature 'Implementation' and/or device 'xc7a100t'  
INFO: [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a100t'  
Running DRC as a precondition to command route\_design  
INFO: [DRC 23-27] Running DRC **with** 8 threads  
WARNING: [DRC PLCK-12] Clock Placer Checks: Poor placement for routing between an IO pin and BUFG.   
Resolution: Poor placement of an IO pin and a BUFG has resulted **in** the router using a non-dedicated path between the two. There are several things that could trigger this DRC, each of which can cause unpredictable clock insertion delays that result **in** poor timing. This DRC could be caused by any of the following: (a) a clock port was placed on a pin that is not a CCIO-pin (b)the BUFG has not been placed **in** the same half of the device or SLR as the CCIO-pin (c) a single ended clock has been placed on the N-Side of a differential pair CCIO-pin.  
 This is normally an ERROR but the CLOCK\_DEDICATED\_ROUTE constraint is set to FALSE allowing your design to continue. The use of this override is highly discouraged as it may lead to very poor timing results. It is recommended that this error condition be corrected **in** the design.  
  
 clk\_IBUF\_inst (IBUF.O) is locked to IOB\_X0Y93  
 clk\_IBUF\_BUFG\_inst (BUFG.I) is provisionally placed by clockplacer on BUFGCTRL\_X0Y0  
INFO: [Vivado\_Tcl 4-198] DRC finished **with** 0 Errors, 1 Warnings  
INFO: [Vivado\_Tcl 4-199] Please refer to the DRC report (report\_drc) for more information.  
  
  
Starting Routing Task  
INFO: [Route 35-254] Multithreading enabled for route\_design using a maximum of 8 CPUs  
Checksum: PlaceDB: 424ce60 ConstDB: 0 ShapeSum: 279fa7a9 RouteDB: 0  
  
Phase 1 Build RT Design  
Phase 1 Build RT Design | Checksum: 1307bb19a  
  
Time (s): cpu = 00:00:24 ; elapsed = 00:00:20 . Memory (MB): peak = 2450.168 ; gain = 40.004 ; free physical = 121207 ; free virtual = 156276  
Post Restoration Checksum: NetGraph: acc37377 NumContArr: 83b83e23 Constraints: 0 Timing: 0  
  
Phase 2 Router Initialization  
INFO: [Route 35-64] No timing constraints were detected. The router will operate **in** resource-optimization mode.  
  
Phase 2.1 Fix Topology Constraints  
Phase 2.1 Fix Topology Constraints | Checksum: 1307bb19a  
  
Time (s): cpu = 00:00:24 ; elapsed = 00:00:20 . Memory (MB): peak = 2457.156 ; gain = 46.992 ; free physical = 121175 ; free virtual = 156244  
  
Phase 2.2 Pre Route Cleanup  
Phase 2.2 Pre Route Cleanup | Checksum: 1307bb19a  
  
Time (s): cpu = 00:00:24 ; elapsed = 00:00:20 . Memory (MB): peak = 2457.156 ; gain = 46.992 ; free physical = 121175 ; free virtual = 156244  
 Number of Nodes **with** overlaps = 0  
Phase 2 Router Initialization | Checksum: 91430244  
  
Time (s): cpu = 00:00:24 ; elapsed = 00:00:20 . Memory (MB): peak = 2466.422 ; gain = 56.258 ; free physical = 121167 ; free virtual = 156236  
  
Phase 3 Initial Routing  
Phase 3 Initial Routing | Checksum: 4c26a122  
  
Time (s): cpu = 00:00:25 ; elapsed = 00:00:20 . Memory (MB): peak = 2466.422 ; gain = 56.258 ; free physical = 121168 ; free virtual = 156237  
  
Phase 4 Rip-up And Reroute  
  
Phase 4.1 Global Iteration 0  
 Number of Nodes **with** overlaps = 4  
 Number of Nodes **with** overlaps = 0  
Phase 4.1 Global Iteration 0 | Checksum: bf7350a9  
  
Time (s): cpu = 00:00:25 ; elapsed = 00:00:20 . Memory (MB): peak = 2466.422 ; gain = 56.258 ; free physical = 121168 ; free virtual = 156237  
Phase 4 Rip-up And Reroute | Checksum: bf7350a9  
  
Time (s): cpu = 00:00:25 ; elapsed = 00:00:20 . Memory (MB): peak = 2466.422 ; gain = 56.258 ; free physical = 121168 ; free virtual = 156237  
  
Phase 5 Delay and Skew Optimization  
Phase 5 Delay and Skew Optimization | Checksum: bf7350a9  
  
Time (s): cpu = 00:00:25 ; elapsed = 00:00:20 . Memory (MB): peak = 2466.422 ; gain = 56.258 ; free physical = 121168 ; free virtual = 156237  
  
Phase 6 Post Hold Fix  
  
Phase 6.1 Hold Fix Iter  
Phase 6.1 Hold Fix Iter | Checksum: bf7350a9  
  
Time (s): cpu = 00:00:25 ; elapsed = 00:00:20 . Memory (MB): peak = 2466.422 ; gain = 56.258 ; free physical = 121168 ; free virtual = 156237  
Phase 6 Post Hold Fix | Checksum: bf7350a9  
  
Time (s): cpu = 00:00:25 ; elapsed = 00:00:20 . Memory (MB): peak = 2466.422 ; gain = 56.258 ; free physical = 121168 ; free virtual = 156237  
  
Phase 7 Route finalize  
  
Router Utilization Summary  
 Global Vertical Routing Utilization = 0.0163207 %  
 Global Horizontal Routing Utilization = 0.016624 %  
 Routable Net Status\*  
 \*Does not include unroutable nets such as driverless and loadless.  
 Run report\_route\_status for detailed report.  
 Number of Failed Nets = 0  
 Number of Unrouted Nets = 0  
 Number of Partially Routed Nets = 0  
 Number of Node Overlaps = 0  
  
Congestion Report  
North Dir 1x1 Area, Max Cong = 15.3153%, No Congested Regions.  
South Dir 1x1 Area, Max Cong = 25.2252%, No Congested Regions.  
East Dir 1x1 Area, Max Cong = 7.35294%, No Congested Regions.  
West Dir 1x1 Area, Max Cong = 14.7059%, No Congested Regions.  
  
------------------------------  
Reporting congestion hotspots  
------------------------------  
Direction: North  
----------------  
Congested clusters found at Level 0  
Effective congestion level: 0 Aspect Ratio: 1 Sparse Ratio: 0  
Direction: South  
----------------  
Congested clusters found at Level 0  
Effective congestion level: 0 Aspect Ratio: 1 Sparse Ratio: 0  
Direction: East  
----------------  
Congested clusters found at Level 0  
Effective congestion level: 0 Aspect Ratio: 1 Sparse Ratio: 0  
Direction: West  
----------------  
Congested clusters found at Level 0  
Effective congestion level: 0 Aspect Ratio: 1 Sparse Ratio: 0  
  
Phase 7 Route finalize | Checksum: bf7350a9  
  
Time (s): cpu = 00:00:25 ; elapsed = 00:00:20 . Memory (MB): peak = 2466.422 ; gain = 56.258 ; free physical = 121168 ; free virtual = 156237  
  
Phase 8 Verifying routed nets  
  
 Verification completed successfully  
Phase 8 Verifying routed nets | Checksum: bf7350a9  
  
Time (s): cpu = 00:00:25 ; elapsed = 00:00:20 . Memory (MB): peak = 2468.422 ; gain = 58.258 ; free physical = 121167 ; free virtual = 156236  
  
Phase 9 Depositing Routes  
Phase 9 Depositing Routes | Checksum: 8f74ad82  
  
Time (s): cpu = 00:00:25 ; elapsed = 00:00:20 . Memory (MB): peak = 2468.422 ; gain = 58.258 ; free physical = 121167 ; free virtual = 156236  
INFO: [Route 35-16] Router Completed Successfully  
  
Time (s): cpu = 00:00:25 ; elapsed = 00:00:20 . Memory (MB): peak = 2468.422 ; gain = 58.258 ; free physical = 121202 ; free virtual = 156271  
  
Routing Is Done.  
INFO: [Common 17-83] Releasing license: Implementation  
54 Infos, 3 Warnings, 0 Critical Warnings and 0 Errors encountered.  
route\_design completed successfully  
route\_design: Time (s): cpu = 00:00:27 ; elapsed = 00:00:25 . Memory (MB): peak = 2468.422 ; gain = 58.258 ; free physical = 121203 ; free virtual = 156272  
INFO: [Timing 38-480] Writing timing data to binary archive.  
Writing placer database...  
Writing XDEF routing.  
Writing XDEF routing logical nets.  
Writing XDEF routing special nets.  
Write XDEF Complete: Time (s): cpu = 00:00:00.04 ; elapsed = 00:00:00.05 . Memory (MB): peak = 2468.422 ; gain = 0.000 ; free physical = 121201 ; free virtual = 156271  
INFO: [Common 17-1381] The checkpoint '/nfs/home/l/l\_heiwan/coen316/lab2/vivado\_test/lab2\_v1/lab2\_v1.runs/impl\_1/regfile\_routed.dcp' has been generated.  
INFO: [runtcl-4] Executing : report\_drc -file regfile\_drc\_routed.rpt -pb regfile\_drc\_routed.pb -rpx regfile\_drc\_routed.rpx  
Command: report\_drc -file regfile\_drc\_routed.rpt -pb regfile\_drc\_routed.pb -rpx regfile\_drc\_routed.rpx  
INFO: [DRC 23-27] Running DRC **with** 8 threads  
INFO: [Coretcl 2-168] The results of DRC are **in** file /nfs/home/l/l\_heiwan/coen316/lab2/vivado\_test/lab2\_v1/lab2\_v1.runs/impl\_1/regfile\_drc\_routed.rpt.  
report\_drc completed successfully  
INFO: [runtcl-4] Executing : report\_methodology -file regfile\_methodology\_drc\_routed.rpt -pb regfile\_methodology\_drc\_routed.pb -rpx regfile\_methodology\_drc\_routed.rpx  
Command: report\_methodology -file regfile\_methodology\_drc\_routed.rpt -pb regfile\_methodology\_drc\_routed.pb -rpx regfile\_methodology\_drc\_routed.rpx  
INFO: [Timing 38-35] Done setting XDC timing constraints.  
INFO: [Timing 38-35] Done setting XDC timing constraints.  
INFO: [DRC 23-133] Running Methodology **with** 8 threads  
INFO: [Coretcl 2-1520] The results of Report Methodology are **in** file /nfs/home/l/l\_heiwan/coen316/lab2/vivado\_test/lab2\_v1/lab2\_v1.runs/impl\_1/regfile\_methodology\_drc\_routed.rpt.  
report\_methodology completed successfully  
INFO: [runtcl-4] Executing : report\_power -file regfile\_power\_routed.rpt -pb regfile\_power\_summary\_routed.pb -rpx regfile\_power\_routed.rpx  
Command: report\_power -file regfile\_power\_routed.rpt -pb regfile\_power\_summary\_routed.pb -rpx regfile\_power\_routed.rpx  
WARNING: [Power 33-232] No user defined clocks were found **in** the design!  
Resolution: Please specify clocks using create\_clock/create\_generated\_clock for sequential elements. For pure combinatorial circuits, please specify a virtual clock, otherwise the vectorless estimation might be inaccurate  
INFO: [Timing 38-35] Done setting XDC timing constraints.  
Running Vector-less Activity Propagation...  
  
Finished Running Vector-less Activity Propagation  
66 Infos, 4 Warnings, 0 Critical Warnings and 0 Errors encountered.  
report\_power failed  
INFO: [runtcl-4] Executing : report\_route\_status -file regfile\_route\_status.rpt -pb regfile\_route\_status.pb  
INFO: [runtcl-4] Executing : report\_timing\_summary -max\_paths 10 -file regfile\_timing\_summary\_routed.rpt -pb regfile\_timing\_summary\_routed.pb -rpx regfile\_timing\_summary\_routed.rpx -warn\_on\_violation   
INFO: [Timing 38-91] UpdateTimingParams: Speed grade: -1, Delay Type: min\_max, Timing Stage: Requireds.  
INFO: [Timing 38-191] Multithreading enabled for timing update using a maximum of 8 CPUs  
WARNING: [Timing 38-313] There are no user specified timing constraints. Timing constraints are needed for proper timing analysis.  
INFO: [runtcl-4] Executing : report\_incremental\_reuse -file regfile\_incremental\_reuse\_routed.rpt  
INFO: [Vivado\_Tcl 4-545] No incremental reuse to report, no incremental placement and routing data was found.  
INFO: [runtcl-4] Executing : report\_clock\_utilization -file regfile\_clock\_utilization\_routed.rpt  
INFO: [runtcl-4] Executing : report\_bus\_skew -warn\_on\_violation -file regfile\_bus\_skew\_routed.rpt -pb regfile\_bus\_skew\_routed.pb -rpx regfile\_bus\_skew\_routed.rpx  
INFO: [Timing 38-91] UpdateTimingParams: Speed grade: -1, Delay Type: min\_max, Timing Stage: Requireds.  
INFO: [Timing 38-191] Multithreading enabled for timing update using a maximum of 8 CPUs  
INFO: [Common 17-206] Exiting Vivado at Wed Oct 25 13:33:04 2023...  
  
\*\*\* Running vivado  
 **with** args -log regfile.vdi -applog -m64 -product Vivado -messageDb vivado.pb -mode batch -source regfile.tcl -notrace  
  
  
\*\*\*\*\*\* Vivado v2018.2 (64-bit)  
 \*\*\*\* SW Build 2258646 on Thu Jun 14 20:02:38 MDT 2018  
 \*\*\*\* IP Build 2256618 on Thu Jun 14 22:10:49 MDT 2018  
 \*\* Copyright 1986-2018 Xilinx, Inc. All Rights Reserved.  
  
source regfile.tcl -notrace  
Command: open\_checkpoint regfile\_routed.dcp  
  
Starting open\_checkpoint Task  
  
Time (s): cpu = 00:00:00.06 ; elapsed = 00:00:00.23 . Memory (MB): peak = 1343.133 ; gain = 0.000 ; free physical = 122101 ; free virtual = 157171  
INFO: [Netlist 29-17] Analyzing 13 Unisim elements for replacement  
INFO: [Netlist 29-28] Unisim Transformation completed **in** 0 CPU seconds  
INFO: [Project 1-479] Netlist was created **with** Vivado 2018.2  
INFO: [Device 21-403] Loading part xc7a100tcsg324-1  
INFO: [Project 1-570] Preparing netlist for logic optimization  
INFO: [Timing 38-478] Restoring timing data from binary archive.  
INFO: [Timing 38-479] Binary timing data restore complete.  
INFO: [Project 1-856] Restoring constraints from binary archive.  
INFO: [Project 1-853] Binary constraint restore complete.  
Reading XDEF placement.  
Reading placer database...  
Reading XDEF routing.  
Read XDEF File: Time (s): cpu = 00:00:00.14 ; elapsed = 00:00:00.40 . Memory (MB): peak = 2136.254 ; gain = 0.004 ; free physical = 121375 ; free virtual = 156446  
Restored from archive | CPU: 0.390000 secs | Memory: 0.973389 MB |  
Finished XDEF File Restore: Time (s): cpu = 00:00:00.14 ; elapsed = 00:00:00.40 . Memory (MB): peak = 2136.254 ; gain = 0.004 ; free physical = 121375 ; free virtual = 156446  
INFO: [Project 1-111] Unisim Transformation Summary:  
No Unisim elements were transformed.  
  
INFO: [Project 1-604] Checkpoint was created **with** Vivado v2018.2 (64-bit) build 2258646  
open\_checkpoint: Time (s): cpu = 00:00:27 ; elapsed = 00:02:06 . Memory (MB): peak = 2136.254 ; gain = 793.125 ; free physical = 121374 ; free virtual = 156445  
Command: write\_bitstream -force regfile.bit  
Attempting to get a license for feature 'Implementation' and/or device 'xc7a100t'  
INFO: [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a100t'  
Running DRC as a precondition to command write\_bitstream  
INFO: [IP\_Flow 19-234] Refreshing IP repositories  
INFO: [IP\_Flow 19-1704] No user IP repositories specified  
INFO: [IP\_Flow 19-2313] Loaded Vivado IP repository '/CMC/tools/xilinx/Vivado\_2018.2/Vivado/2018.2/data/ip'.  
INFO: [DRC 23-27] Running DRC **with** 8 threads  
WARNING: [DRC CFGBVS-1] Missing CFGBVS and CONFIG\_VOLTAGE Design Properties: Neither the CFGBVS nor CONFIG\_VOLTAGE voltage property is set **in** the current\_design. Configuration bank voltage select (CFGBVS) must be set to VCCO or GND, and CONFIG\_VOLTAGE must be set to the correct configuration voltage, **in** order to determine the I/O voltage support for the pins **in** bank 0. It is suggested to specify these either using the 'Edit Device Properties' function **in** the GUI or directly **in** the XDC file using the following syntax:  
  
 set\_property CFGBVS value1 [current\_design]  
 #where value1 is either VCCO or GND  
  
 set\_property CONFIG\_VOLTAGE value2 [current\_design]  
 #where value2 is the voltage provided to configuration bank 0  
  
Refer to the device configuration user guide for more information.  
INFO: [Vivado 12-3199] DRC finished **with** 0 Errors, 1 Warnings  
INFO: [Vivado 12-3200] Please refer to the DRC report (report\_drc) for more information.  
INFO: [Designutils 20-2272] Running write\_bitstream **with** 8 threads.  
Loading data files...  
Loading site data...  
Loading route data...  
Processing options...  
Creating bitmap...  
Creating bitstream...  
Writing bitstream ./regfile.bit...  
INFO: [Vivado 12-1842] Bitgen Completed Successfully.  
INFO: [Common 17-83] Releasing license: Implementation  
21 Infos, 1 Warnings, 0 Critical Warnings and 0 Errors encountered.  
write\_bitstream completed successfully  
write\_bitstream: Time (s): cpu = 00:00:12 ; elapsed = 00:00:17 . Memory (MB): peak = 2609.094 ; gain = 472.840 ; free physical = 121305 ; free virtual = 156384  
INFO: [Common 17-206] Exiting Vivado at Wed Oct 25 13:36:02 2023...

**5.5) Constrain .xdc File**

# Vivado does not support old UCF syntax  
# must use XDC syntax  
  
set\_property **CLOCK\_DEDICATED\_ROUTE** FALSE [get\_nets clk]  
  
##Switches  
set\_property -**dict** { PACKAGE\_PIN **J15** IOSTANDARD LVCMOS33 } [ get\_ports { reset } ];  
set\_property -**dict** { PACKAGE\_PIN L16 IOSTANDARD LVCMOS33 } [ get\_ports { clk } ];  
set\_property -**dict** { PACKAGE\_PIN M13 IOSTANDARD LVCMOS33 } [ get\_ports { write } ];  
  
set\_property -**dict** { PACKAGE\_PIN R15 IOSTANDARD LVCMOS33 } [ get\_ports { **din[0]** } ];  
set\_property -**dict** { PACKAGE\_PIN R17 IOSTANDARD LVCMOS33 } [ get\_ports { **din[1]** } ];  
set\_property -**dict** { PACKAGE\_PIN T18 IOSTANDARD LVCMOS33 } [ get\_ports { **din[2]** } ];  
set\_property -**dict** { PACKAGE\_PIN U18 IOSTANDARD LVCMOS33 } [ get\_ports { **din[3]** } ];  
  
set\_property -**dict** { PACKAGE\_PIN R13 IOSTANDARD LVCMOS33 } [ get\_ports { read\_a[0] } ];  
set\_property -**dict** { PACKAGE\_PIN T8 IOSTANDARD LVCMOS33 } [ get\_ports { read\_a[1] } ];  
  
set\_property -**dict** { PACKAGE\_PIN U8 IOSTANDARD LVCMOS33 } [ get\_ports { read\_b[0] } ];  
set\_property -**dict** { PACKAGE\_PIN R16 IOSTANDARD LVCMOS33 } [ get\_ports { read\_b[1] }];  
  
set\_property -**dict** { PACKAGE\_PIN T13 IOSTANDARD LVCMOS33 } [ get\_ports { write\_address[0] } ];  
set\_property -**dict** { PACKAGE\_PIN H6 IOSTANDARD LVCMOS33 } [ get\_ports { write\_address[1] } ];  
  
## LEDs  
set\_property -**dict** { PACKAGE\_PIN H17 IOSTANDARD LVCMOS33 } [ get\_ports { out\_a[0] } ];  
set\_property -**dict** { PACKAGE\_PIN K15 IOSTANDARD LVCMOS33 } [ get\_ports { out\_a[1] } ];  
set\_property -**dict** { PACKAGE\_PIN **J13** IOSTANDARD LVCMOS33 } [ get\_ports { out\_a[2] } ];  
set\_property -**dict** { PACKAGE\_PIN N14 IOSTANDARD LVCMOS33 } [ get\_ports { out\_a[3] } ];  
  
set\_property -**dict** { PACKAGE\_PIN R18 IOSTANDARD LVCMOS33 } [ get\_ports { out\_b[0] } ];  
set\_property -**dict** { PACKAGE\_PIN V17 IOSTANDARD LVCMOS33 } [ get\_ports { out\_b[1] } ];  
set\_property -**dict** { PACKAGE\_PIN U17 IOSTANDARD LVCMOS33 } [ get\_ports { out\_b[2] } ];  
set\_property -**dict** { PACKAGE\_PIN U16 IOSTANDARD LVCMOS33 } [ get\_ports { out\_b[3] } ];