Computer Architecture & Design

Coen 316

Lab Experiment #3

Andre Hei Wang Law

4017 5600

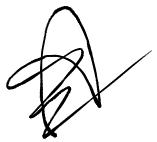
Section DN-X

Professor Dr. Fadi Alzouri

Performed on October 26, 2023

Due on November 9, 2023

“I certify that this submission is my original work and meets the Faculty’s Expectations of

Originality.”

**1) Introduction/Objectives**

For the third lab of COEN 316, students will learn about the design and implementation of a Next-Address Unit while focusing on the generation of the next address to be stored in the Program Counter (PC) register. Students will also delve into the encoding format of the jump and branch instructions. Then, by coding and simulating the program onto a FPGA board, it ensures that the students have hands on experience of their own designed Next-Address Unit.

**2) Theory**

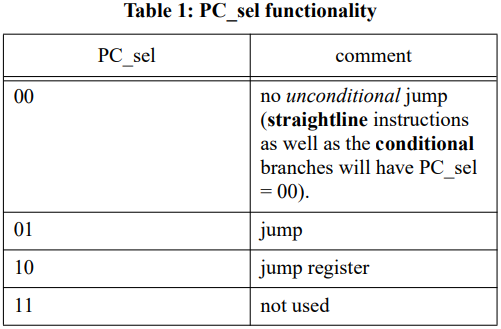
jump there ; jump to memory location “there”

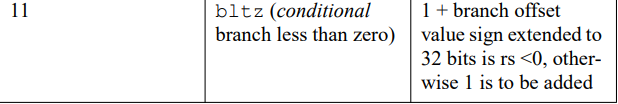
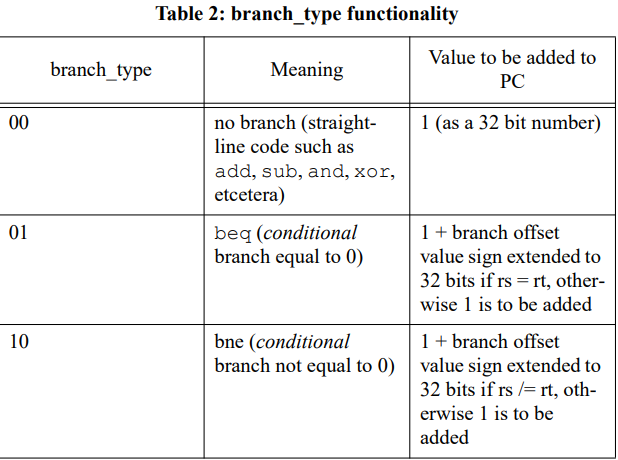
jr rs ; jump to memory location whose address is in rs

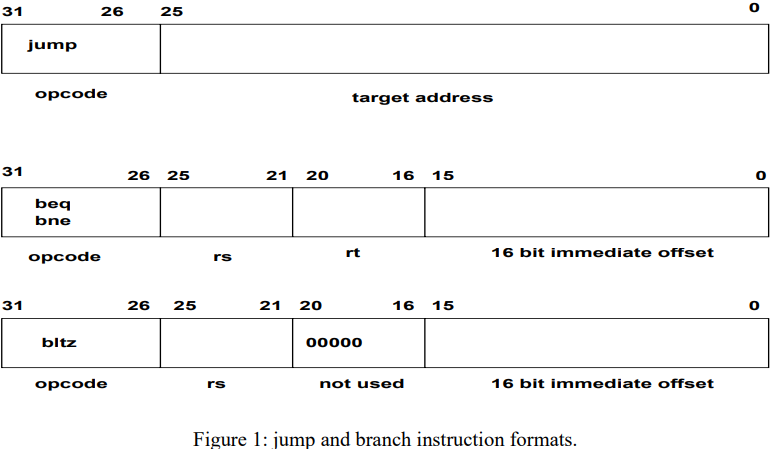
beq rs,rt, loop ; jump to memory location “loop” if rs=rt

bne rs,rt, loop ; jump to memory location ”loop” if rs /= rt

bltz rs, loop ; jump to memory location “loop” if rs < 0





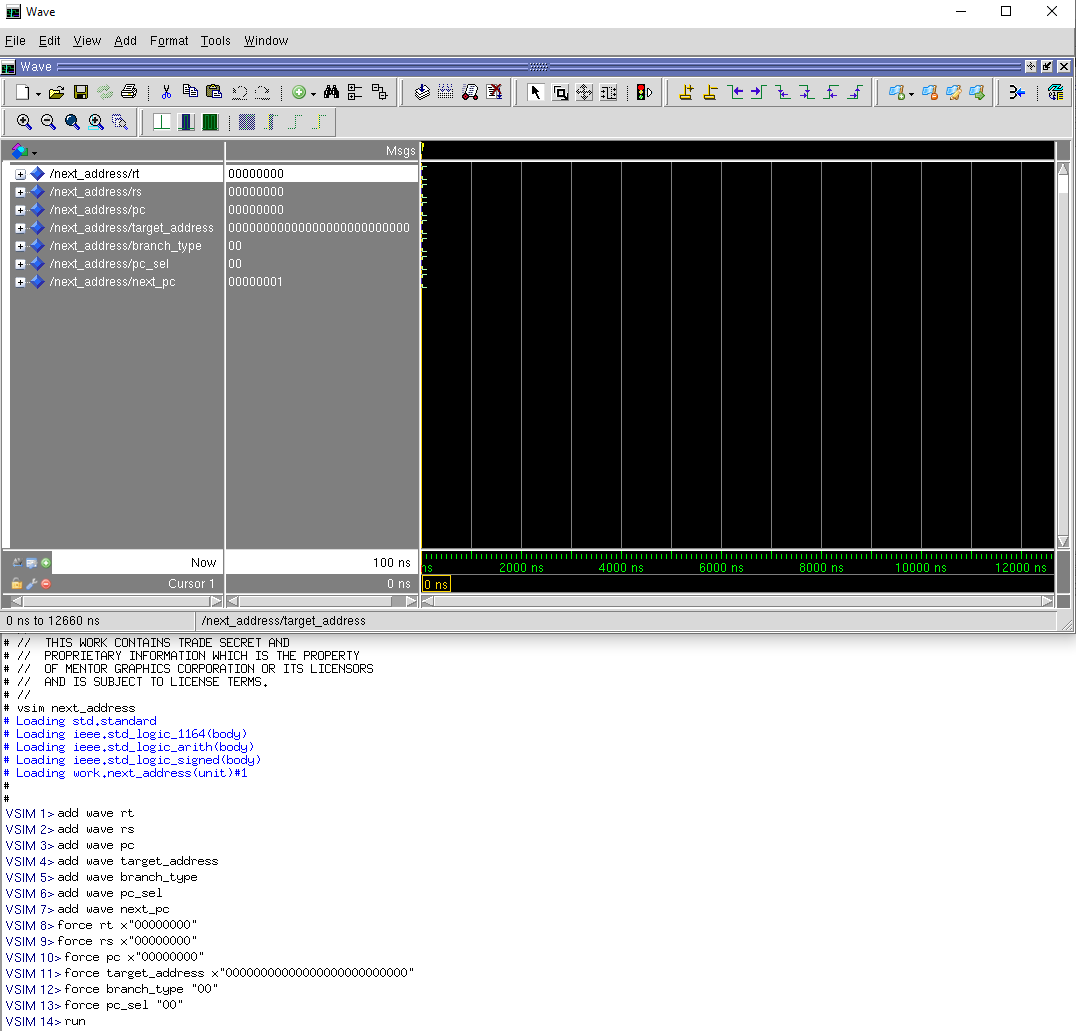


**3) Tasks, Results and Discussion**

The following tasks are run by inputting DO codes found in the appendix. This section will

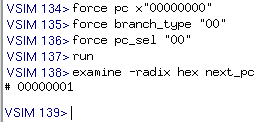
show the results of each relevant input as well as discuss its behavior.

**3.1) Setup**



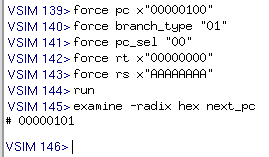
The first step done was to get the wave window and add the waves for the inputs and outputs. Then, we populated the inputs. We also changed the format of some into radix hexadecimal.

**3.2) pc\_sel "00" and branch\_type "00"**



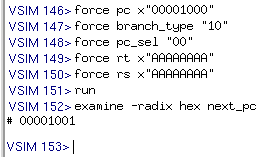
With both pc\_sel and branch\_type being “00”, the pc counter will simply increment by 1. This can be seen when initially, the next\_pc is set to 00000000, but when we run it with pc\_sel “00” and branch\_type “00”, it increased by 1, thus next\_pc is 00000001.

**3.3) pc\_sel "00" and branch\_type "01", false**



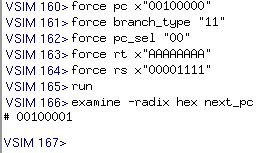
For branch\_type “01”, the condition is true if rt is equal to rs and false otherwise. Here, we test the **false** functionality. If false, add 1 to pc value. In this case, the pc started at 00000100, but after running this false beq branch, it incremented by one and became 00000101.

**3.4) pc\_sel "00" and branch\_type "10", false**



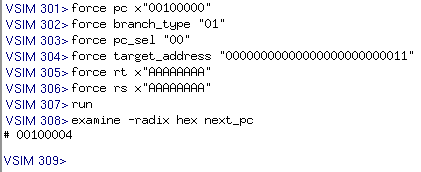
For branch\_type “10”, the condition is true of rs is not equal to rt and false otherwise. Here, we test the **false** functionality. If false, add 1 to pc value. In this case, the pc started at 00001000, but after running this false bne branch, it incremented by one and became 00001001.

**3.5) pc\_sel "00" and branch\_type "11", false**



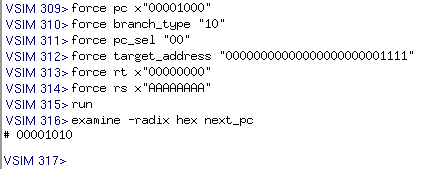
For branch\_type “11”, the condition is true of rs is less than zero and false otherwise. Here, we test the **false** functionality. If false, add 1 to pc value. In this case, the pc started at 00100000, but after running this false bltz branch, it incremented by one and became 00100001.

**3.6) pc\_sel "00" and branch\_type "01", true**



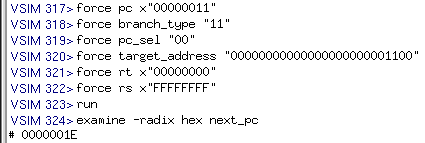
For branch\_type “01”, the condition is true if rt is equal to rs and false otherwise. Here, we test the **true** functionality. If true, add 1 and branch offset value sign extended to 32 bits to pc value. In this case, the pc started at 00100000, but after running this true beq branch, the pc value became (original pc value + 1 + target\_address) or (00100000 + 1 + 3 = 00100004).

**3.7) pc\_sel "00" and branch\_type "10", true**



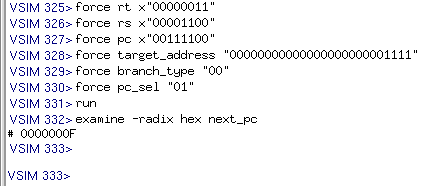
For branch\_type “10”, the condition is true if rt is not equal to rs and false otherwise. Here, we test the **true** functionality. If true, add 1 and branch offset value sign extended to 32 bits to pc value. In this case, the pc started at 00001000, but after running this true bne branch, the pc value became (original pc value + 1 + target\_address) or (00001000 + 1 + F = 00001010).

**3.8) pc\_sel "00" and branch\_type "11", true**



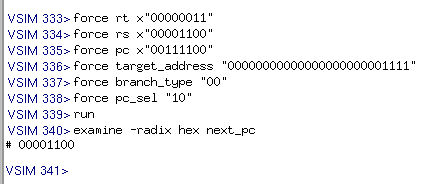
For branch\_type “11”, the condition is true of rs is less than zero and false otherwise. Here, we test the **true** functionality. If true, add 1 and branch offset value sign extended to 32 bits to pc value. In this case, the pc started at 00000011, but after running this true bltz branch, the pc value became (original pc value + 1 + target\_address) or (00000011 + 1 + C = 0000001E).

**3.9) pc\_sel "01"**



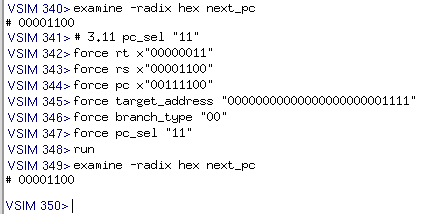
Given pc\_sel “01”, the functionality is jump towards the target\_address. Here, branch\_type, rt and rs don’t affect the next\_pc at all. The only important values are the pc\_sel “01” and the target\_address. As such, even if pc has an initial value of 00111100, the next\_pc target corresponds to 00000000000000000000001111 or 0000000F.

**3.10) pc\_sel "10"**



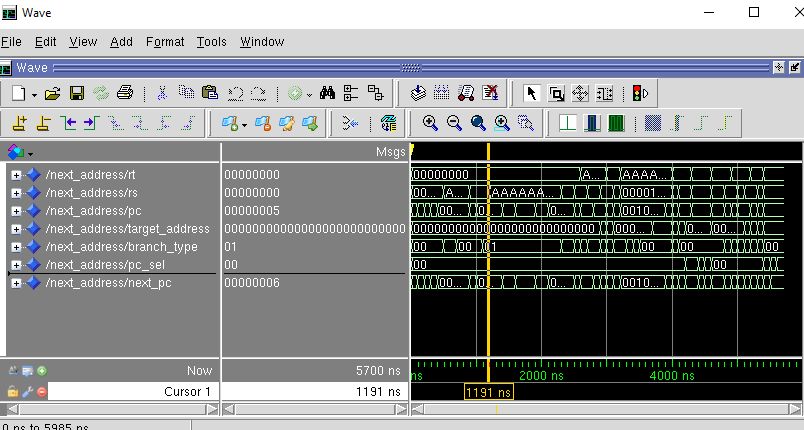
Given pc\_sel “10”, the functionality is jump towards the memory location of address rs. Here, branch\_type, rt and target\_address don’t affect the next\_pc at all. The only important values are the pc\_sel “01” and the rs address. As such, even if pc has an initial value of 00111100, the next\_pc target corresponds to rs or 00001100.

**3.11) pc\_sel "11"**



Knowing that pc\_sel “11” is not used, the output next\_pc shouldn’t change. This can be seen when next\_pc’s initial and final value are both 00001100, unchanged.

**3.12) ModelSim Wave View**



**4) Conclusions**

In conclusion, this lab allowed the students to work on the fundamentals of a Next-Address Unit which is responsible for managing the program flow through jump and branch instructions. In addition, students have successfully created a VHDL-based design for this Unit through the incorporations of multiplexers, adders, and other necessary components to handle various scenarios of control signals. Then, the students also simulated their design using Modelsim and Xilinx Vivado to verify their correctness, while implementing on a FPGA board confirmed the functionalities on a real hardware. In the end, these hands-on experiences allowed the students to comprehend the fundamentals of a Next-Address Unit.

**5) Appendix**

**5.1) VHDL Code**

**library** IEEE;  
**use** IEEE.std\_logic\_1164.**all**;  
**use** IEEE.std\_logic\_signed.**all**;  
  
**entity** next\_address **is**  
**port**(  
 -- inputs  
 rt, rs: **in** std\_logic\_vector(31 **downto** 0);  
 pc: **in** std\_logic\_vector(31 **downto** 0);  
 target\_address: **in** std\_logic\_vector(25 **downto** 0);  
 branch\_type: **in** std\_logic\_vector(1 **downto** 0);  
 pc\_sel: **in** std\_logic\_vector(1 **downto** 0);  
   
 -- output  
 next\_pc: **out** std\_logic\_vector(31 **downto** 0));  
**end** next\_address;  
  
**architecture** unit **of** next\_address **is**  
  
-- signal  
**signal** tar\_addr\_signed\_32: std\_logic\_vector(31 **downto** 0);  
**signal** branch\_offset\_signed\_32: std\_logic\_vector(31 **downto** 0);  
**signal** branch\_offset: std\_logic\_vector(31 **downto** 0);  
  
**begin**  
 -- calculate "pseudo-direct" addressing to fill entire 32 bit  
 -- target address for "jump" instructions  
 tar\_addr\_signed\_32(31 **downto** 26) <= (**others** => target\_address(25)); -- fill with ones or zeros  
 tar\_addr\_signed\_32(25 **downto** 0) <= target\_address; -- fill the rest   
   
 -- branch offset for no unconditional jump instructions  
 branch\_offset\_signed\_32(31 **downto** 16) <= (**others** => target\_address(15)); -- fill with ones or zeros  
 branch\_offset\_signed\_32(15 **downto** 0) <= target\_address(15 **downto** 0); -- fill the rest   
  
 -- PC\_sel functionality  
 **process**(pc\_sel, rs, branch\_offset, pc, tar\_addr\_signed\_32)  
 **begin**  
 **if** (pc\_sel = "00") **then** -- no unconditional jump  
 next\_pc <= branch\_offset + pc + 1;  
 **elsif** (pc\_sel = "01") **then** -- jump  
 next\_pc <= tar\_addr\_signed\_32;  
 **elsif** (pc\_sel = "10") **then** -- jump register  
 next\_pc <= rs;  
 **elsif** (pc\_sel = "11") **then** -- not used  
 -- do nothing  
 **end** **if**;  
 **end** **process**;  
   
 -- branch\_type functionality  
 **process**(branch\_type, rs, rt, branch\_offset, branch\_offset\_signed\_32)  
 **begin**  
 **if** (branch\_type = "00") **then** -- no branch  
 branch\_offset <= (**others** => '0');  
 **elsif** (branch\_type = "01") **then** -- beq (equal to 0)  
 **if** (rs = rt) **then**  
 branch\_offset <= branch\_offset\_signed\_32;  
 **else**  
 branch\_offset <= (**others** => '0');  
 **end** **if**;  
 **elsif** (branch\_type = "10") **then** -- bne (not equal to 0)  
 **if** (rs /= rt) **then**  
 branch\_offset <= branch\_offset\_signed\_32;  
 **else**  
 branch\_offset <= (**others** => '0');  
 **end** **if**;  
 **elsif** (branch\_type = "11") **then** -- bltz (less then 0)  
 **if** (rs(31) = '1') **then** -- means rs is negative, or < 0  
 branch\_offset <= branch\_offset\_signed\_32;  
 **else**  
 branch\_offset <= (**others** => '0');  
 **end** **if**;  
 **end** **if**;  
 **end** **process**;  
**end** unit;

**5.2) Board Wrapper Version**

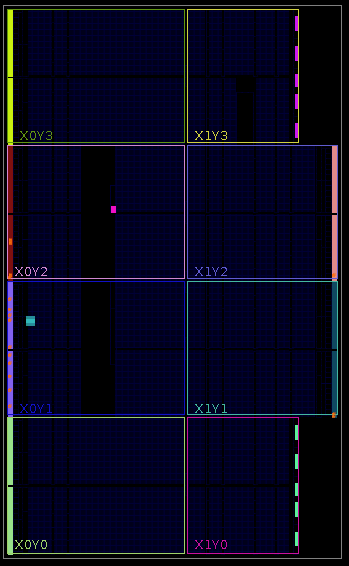
**library** IEEE;  
**use** IEEE.std\_logic\_1164.**all**;  
**use** IEEE.std\_logic\_signed.**all**;  
  
**entity** next\_address **is**  
**port**(  
 -- inputs  
 --rt, rs: in std\_logic\_vector(31 downto 0);  
 --pc: in std\_logic\_vector(31 downto 0);  
 --target\_address: in std\_logic\_vector(25 downto 0);  
 branch\_type: **in** std\_logic\_vector(1 **downto** 0);  
 pc\_sel: **in** std\_logic\_vector(1 **downto** 0);  
 -- output  
 --next\_pc: out std\_logic\_vector(31 downto 0));  
   
 -- new inputs  
 rt\_in, rs\_in: **in** std\_logic\_vector(1 **downto** 0);  
 pc\_in: **in** std\_logic\_vector(2 **downto** 0);  
 target\_address\_in: **in** std\_logic\_vector(2 **downto** 0);  
 -- new output  
 next\_pc\_out: **out** std\_logic\_vector(2 **downto** 0));  
**end** next\_address;  
  
**architecture** unit **of** next\_address **is**  
  
-- signal  
**signal** tar\_addr\_signed\_32: std\_logic\_vector(31 **downto** 0);  
**signal** branch\_offset\_signed\_32: std\_logic\_vector(31 **downto** 0);  
**signal** branch\_offset: std\_logic\_vector(31 **downto** 0);  
  
**signal** rt, rs, pc, next\_pc: std\_logic\_vector(31 **downto** 0);  
**signal** target\_address: std\_logic\_vector(25 **downto** 0);  
  
**begin**  
 rt(1 **downto** 0) <= rt\_in(1) & rt\_in(0);  
 rt(31 **downto** 2)<= (**others** => '0');  
   
 rs(1 **downto** 0) <= rs\_in(1) & rs\_in(0);  
 rs(31 **downto** 2)<= (**others** => '0');  
   
 pc(2 **downto** 0) <= pc\_in(2) & pc\_in(1) & pc\_in(0);  
 pc(31 **downto** 3)<= (**others** => '0');  
  
 target\_address(2 **downto** 0) <= target\_address\_in(2) & target\_address\_in(1) & target\_address\_in(0);  
 target\_address(25 **downto** 3)<= (**others** => '0');  
   
 next\_pc\_out(2 **downto** 0) <= next\_pc(2 **downto** 0);  
  
 -- calculate "pseudo-direct" addressing to fill entire 32 bit  
 -- target address for "jump" instructions  
 tar\_addr\_signed\_32(31 **downto** 3) <= (**others** => target\_address(2)); -- fill with ones or zeros  
 tar\_addr\_signed\_32(2 **downto** 0) <= target\_address(2 **downto** 0); -- fill the rest   
   
 -- branch offset for no unconditional jump instructions  
 branch\_offset\_signed\_32(31 **downto** 3) <= (**others** => target\_address(2)); -- fill with ones or zeros  
 branch\_offset\_signed\_32(2 **downto** 0) <= target\_address(2 **downto** 0); -- fill the rest   
  
 -- PC\_sel functionality  
 **process**(pc\_sel, rs, branch\_offset, pc, tar\_addr\_signed\_32)  
 **begin**  
 **if** (pc\_sel = "00") **then** -- no unconditional jump  
 next\_pc <= branch\_offset + pc + 1;  
 **elsif** (pc\_sel = "01") **then** -- jump  
 next\_pc <= tar\_addr\_signed\_32;  
 **elsif** (pc\_sel = "10") **then** -- jump register  
 next\_pc <= rs;  
 **elsif** (pc\_sel = "11") **then** -- not used  
 -- do nothing  
 **end** **if**;  
 **end** **process**;  
   
 -- branch\_type functionality  
 **process**(branch\_type, rs, rt, branch\_offset, branch\_offset\_signed\_32)  
 **begin**  
 **if** (branch\_type = "00") **then** -- no branch  
 branch\_offset <= (**others** => '0');  
 **elsif** (branch\_type = "01") **then** -- beq (equal to 0)  
 **if** (rs = rt) **then**  
 branch\_offset <= branch\_offset\_signed\_32;  
 **else**  
 branch\_offset <= (**others** => '0');  
 **end** **if**;  
 **elsif** (branch\_type = "10") **then** -- bne (not equal to 0)  
 **if** (rs /= rt) **then**  
 branch\_offset <= branch\_offset\_signed\_32;  
 **else**  
 branch\_offset <= (**others** => '0');  
 **end** **if**;  
 **elsif** (branch\_type = "11") **then** -- bltz (less then 0)  
 **if** (rs(1) = '1') **then** -- means rs is negative, or < 0  
 branch\_offset <= branch\_offset\_signed\_32;  
 **else**  
 branch\_offset <= (**others** => '0');  
 **end** **if**;  
 **end** **if**;  
 **end** **process**;  
**end** unit;

**5.3) DO File**

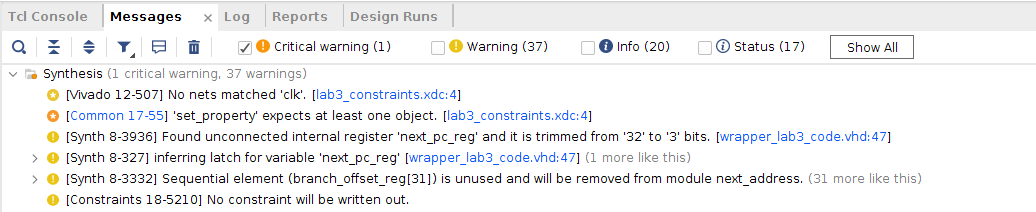
# DO File  
# 3.1 setup  
add wave rt  
add wave rs  
add wave pc  
add wave target\_address  
add wave branch\_type  
add wave pc\_sel  
add wave next\_pc  
force rt x"00000000"  
force rs x"00000000"  
force pc x"00000000"  
force target\_address "00000000000000000000000000"  
force branch\_type "00"  
force pc\_sel "00"  
run  
  
# 3.2 pc\_sel "00" and branch\_type "00"  
force pc x"00000000"  
force branch\_type "00"  
force pc\_sel "00"  
run  
examine -radix hex next\_pc  
  
# 3.3 pc\_sel "00" and branch\_type "01", false  
force pc x"00000100"  
force branch\_type "01"  
force pc\_sel "00"  
force rt x"00000000"  
force rs x"AAAAAAAA"  
run  
examine -radix hex next\_pc  
  
# 3.4 pc\_sel "00" and branch\_type "10", false  
force pc x"00001000"  
force branch\_type "10"  
force pc\_sel "00"  
force rt x"AAAAAAAA"  
force rs x"AAAAAAAA"  
run  
examine -radix hex next\_pc  
  
# 3.5 pc\_sel "00" and branch\_type "11", false  
force pc x"00100000"  
force branch\_type "11"  
force pc\_sel "00"  
force rt x"AAAAAAAA"  
force rs x"00001111"  
run  
examine -radix hex next\_pc  
  
# 3.6 pc\_sel "00" and branch\_type "01", true  
force pc x"00100000"  
force branch\_type "01"  
force pc\_sel "00"  
force target\_address "00000000000000000000000011"  
force rt x"AAAAAAAA"  
force rs x"AAAAAAAA"  
run  
examine -radix hex next\_pc  
  
# 3.7 pc\_sel "00" and branch\_type "10", true  
force pc x"00001000"  
force branch\_type "10"  
force pc\_sel "00"  
force target\_address "00000000000000000000001111"  
force rt x"00000000"  
force rs x"AAAAAAAA"  
run  
examine -radix hex next\_pc  
  
# 3.8 pc\_sel "00" and branch\_type "11", true  
force pc x"00000011"  
force branch\_type "11"  
force pc\_sel "00"  
force target\_address "00000000000000000000001100"  
force rt x"00000000"  
force rs x"FFFFFFFF"  
run  
examine -radix hex next\_pc  
  
# 3.9 pc\_sel "01"   
force rt x"00000011"  
force rs x"00001100"  
force pc x"00111100"  
force target\_address "00000000000000000000001111"  
force branch\_type "00"  
force pc\_sel "01"  
run  
examine -radix hex next\_pc  
  
# 3.10 pc\_sel "10"   
force rt x"00000011"  
force rs x"00001100"  
force pc x"00111100"  
force target\_address "00000000000000000000001111"  
force branch\_type "00"  
force pc\_sel "10"  
run  
examine -radix hex next\_pc  
  
# 3.11 pc\_sel "11"   
force rt x"00000011"  
force rs x"00001100"  
force pc x"00111100"  
force target\_address "00000000000000000000001111"  
force branch\_type "00"  
force pc\_sel "11"  
run  
examine -radix hex next\_pc

**5.4) Constrain .xdc File**

# Vivado does not support old UCF syntax  
# must use XDC syntax  
  
set\_property **CLOCK\_DEDICATED\_ROUTE** FALSE [get\_nets clk]  
  
##Switches  
set\_property -**dict** { PACKAGE\_PIN **J15** IOSTANDARD LVCMOS33 } [ get\_ports { rt\_in[0] } ];  
set\_property -**dict** { PACKAGE\_PIN L16 IOSTANDARD LVCMOS33 } [ get\_ports { rt\_in[1] } ];  
  
set\_property -**dict** { PACKAGE\_PIN M13 IOSTANDARD LVCMOS33 } [ get\_ports { rs\_in[0] } ];  
set\_property -**dict** { PACKAGE\_PIN R15 IOSTANDARD LVCMOS33 } [ get\_ports { rs\_in[1] } ];  
  
set\_property -**dict** { PACKAGE\_PIN R17 IOSTANDARD LVCMOS33 } [ get\_ports { pc\_in[0] } ];  
set\_property -**dict** { PACKAGE\_PIN T18 IOSTANDARD LVCMOS33 } [ get\_ports { pc\_in[1] } ];  
set\_property -**dict** { PACKAGE\_PIN U18 IOSTANDARD LVCMOS33 } [ get\_ports { pc\_in[2] } ];  
  
set\_property -**dict** { PACKAGE\_PIN R13 IOSTANDARD LVCMOS33 } [ get\_ports { target\_address\_in[0] } ];  
set\_property -**dict** { PACKAGE\_PIN T8 IOSTANDARD LVCMOS33 } [ get\_ports { target\_address\_in[1] } ];  
set\_property -**dict** { PACKAGE\_PIN U8 IOSTANDARD LVCMOS33 } [ get\_ports { target\_address\_in[2] } ];  
  
set\_property -**dict** { PACKAGE\_PIN R16 IOSTANDARD LVCMOS33 } [ get\_ports { **branch\_type[0]** }];  
set\_property -**dict** { PACKAGE\_PIN T13 IOSTANDARD LVCMOS33 } [ get\_ports { **branch\_type[1]** } ];  
  
set\_property -**dict** { PACKAGE\_PIN H6 IOSTANDARD LVCMOS33 } [ get\_ports { pc\_sel[0] } ];  
set\_property -**dict** { PACKAGE\_PIN U12 IOSTANDARD LVCMOS33 } [ get\_ports { pc\_sel[1] } ];  
  
## LEDs  
set\_property -**dict** { PACKAGE\_PIN H17 IOSTANDARD LVCMOS33 } [ get\_ports { next\_pc\_out[0] } ];  
set\_property -**dict** { PACKAGE\_PIN K15 IOSTANDARD LVCMOS33 } [ get\_ports { next\_pc\_out[1] } ];  
set\_property -**dict** { PACKAGE\_PIN **J13** IOSTANDARD LVCMOS33 } [ get\_ports { next\_pc\_out[2] } ];



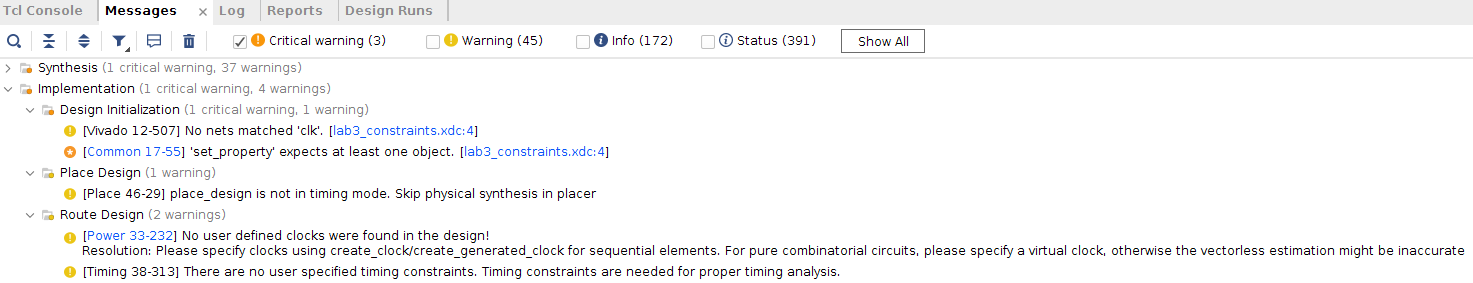
**5.5) Synthesis Log**

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**Warning Discussion:** The critical warning is do to the fact that I have added “set\_property CLOCK\_DEDICATED\_ROUTE FALSE [get\_nets clk]” which is not needed for this lab unlike lab 2. As for the other 39 warnings, they are related to the fact that not all bits are used for this wrapper version of the code, so bits 32 to 3 are trimmed off.

\*\*\* Running vivado  
 with args -log next\_address.vds -m64 -product Vivado -mode batch -messageDb vivado.pb -notrace -source next\_address.tcl  
  
  
\*\*\*\*\*\* Vivado v2018.2 (64-bit)  
 \*\*\*\* SW Build 2258646 on Thu Jun 14 20:02:38 MDT 2018  
 \*\*\*\* IP Build 2256618 on Thu Jun 14 22:10:49 MDT 2018  
 \*\* Copyright 1986-2018 Xilinx, Inc. All Rights Reserved.  
  
source next\_address.tcl -notrace  
Command: synth\_design -top next\_address -part xc7a100tcsg324-1  
Starting synth\_design  
Attempting to **get** a license **for** feature 'Synthesis' **and**/**or** device 'xc7a100t'  
INFO: [Common 17-349] Got license **for** feature 'Synthesis' **and**/**or** device 'xc7a100t'  
INFO: Launching helper process **for** spawning children vivado processes  
INFO: Helper process launched with PID 22726   
---------------------------------------------------------------------------------  
Starting RTL Elaboration : Time (s): cpu = 00:00:02 ; elapsed = 00:00:04 . Memory (MB): peak = 1468.594 ; gain = 86.727 ; free physical = 89873 ; free virtual = 154336  
---------------------------------------------------------------------------------  
INFO: [Synth 8-638] synthesizing module 'next\_address' [/nfs/home/l/l\_heiwan/coen316/lab3/wrapper\_lab3\_code.vhd:24]  
INFO: [Synth 8-256] done synthesizing module 'next\_address' (1#1) [/nfs/home/l/l\_heiwan/coen316/lab3/wrapper\_lab3\_code.vhd:24]  
---------------------------------------------------------------------------------  
Finished RTL Elaboration : Time (s): cpu = 00:00:03 ; elapsed = 00:00:06 . Memory (MB): peak = 1513.234 ; gain = 131.367 ; free physical = 89884 ; free virtual = 154346  
---------------------------------------------------------------------------------  
  
Report Check Netlist:   
+------+------------------+-------+---------+-------+------------------+  
| |Item |Errors |Warnings |Status |Description |  
+------+------------------+-------+---------+-------+------------------+  
|1 |multi\_driven\_nets | 0| 0|Passed |Multi driven nets |  
+------+------------------+-------+---------+-------+------------------+  
---------------------------------------------------------------------------------  
Start Handling Custom Attributes  
---------------------------------------------------------------------------------  
---------------------------------------------------------------------------------  
Finished Handling Custom Attributes : Time (s): cpu = 00:00:03 ; elapsed = 00:00:07 . Memory (MB): peak = 1513.234 ; gain = 131.367 ; free physical = 89885 ; free virtual = 154347  
---------------------------------------------------------------------------------  
---------------------------------------------------------------------------------  
Finished RTL Optimization Phase 1 : Time (s): cpu = 00:00:03 ; elapsed = 00:00:07 . Memory (MB): peak = 1513.234 ; gain = 131.367 ; free physical = 89885 ; free virtual = 154347  
---------------------------------------------------------------------------------  
INFO: [Device 21-403] Loading part xc7a100tcsg324-1  
INFO: [Project 1-570] Preparing netlist **for** logic optimization  
  
Processing XDC Constraints  
Initializing timing engine  
Parsing XDC File [/nfs/home/l/l\_heiwan/coen316/lab3/lab3\_constraints.xdc]  
WARNING: [Vivado 12-507] No nets matched 'clk'. [/nfs/home/l/l\_heiwan/coen316/lab3/lab3\_constraints.xdc:4]  
CRITICAL WARNING: [Common 17-55] 'set\_property' expects at least one object. [/nfs/home/l/l\_heiwan/coen316/lab3/lab3\_constraints.xdc:4]  
Resolution: If [get\_<value>] was used to populate the object, check to make sure **this** command returns at least one valid object.  
Finished Parsing XDC File [/nfs/home/l/l\_heiwan/coen316/lab3/lab3\_constraints.xdc]  
INFO: [Project 1-236] Implementation specific constraints were found **while** reading constraint file [/nfs/home/l/l\_heiwan/coen316/lab3/lab3\_constraints.xdc]. These constraints will be ignored **for** synthesis but will be used **in** implementation. Impacted constraints are listed **in** the file [.Xil/next\_address\_propImpl.xdc].  
Resolution: To avoid **this** warning, move constraints listed **in** [.Xil/next\_address\_propImpl.xdc] to another XDC file **and** exclude **this** new file **from** synthesis with the used\_in\_synthesis property (File Properties dialog **in** GUI) **and** re-run elaboration/synthesis.  
Completed Processing XDC Constraints  
  
INFO: [Project 1-111] Unisim Transformation Summary:  
No Unisim elements were transformed.  
  
Constraint Validation Runtime : Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 1865.684 ; gain = 0.000 ; free physical = 89532 ; free virtual = 153994  
---------------------------------------------------------------------------------  
Finished Constraint Validation : Time (s): cpu = 00:00:16 ; elapsed = 00:01:10 . Memory (MB): peak = 1865.684 ; gain = 483.816 ; free physical = 89665 ; free virtual = 154128  
---------------------------------------------------------------------------------  
---------------------------------------------------------------------------------  
Start Loading Part **and** Timing Information  
---------------------------------------------------------------------------------  
Loading part: xc7a100tcsg324-1  
---------------------------------------------------------------------------------  
Finished Loading Part **and** Timing Information : Time (s): cpu = 00:00:16 ; elapsed = 00:01:10 . Memory (MB): peak = 1865.684 ; gain = 483.816 ; free physical = 89665 ; free virtual = 154128  
---------------------------------------------------------------------------------  
---------------------------------------------------------------------------------  
Start Applying 'set\_property' XDC Constraints  
---------------------------------------------------------------------------------  
---------------------------------------------------------------------------------  
Finished applying 'set\_property' XDC Constraints : Time (s): cpu = 00:00:16 ; elapsed = 00:01:10 . Memory (MB): peak = 1865.684 ; gain = 483.816 ; free physical = 89667 ; free virtual = 154130  
---------------------------------------------------------------------------------  
WARNING: [Synth 8-3936] Found unconnected internal register 'next\_pc\_reg' **and** it **is** trimmed **from** '32' to '3' bits. [/nfs/home/l/l\_heiwan/coen316/lab3/wrapper\_lab3\_code.vhd:47]  
WARNING: [Synth 8-327] inferring latch **for** variable 'next\_pc\_reg' [/nfs/home/l/l\_heiwan/coen316/lab3/wrapper\_lab3\_code.vhd:47]  
WARNING: [Synth 8-327] inferring latch **for** variable 'branch\_offset\_reg' [/nfs/home/l/l\_heiwan/coen316/lab3/wrapper\_lab3\_code.vhd:76]  
---------------------------------------------------------------------------------  
Finished RTL Optimization Phase 2 : Time (s): cpu = 00:00:16 ; elapsed = 00:01:10 . Memory (MB): peak = 1865.684 ; gain = 483.816 ; free physical = 89657 ; free virtual = 154119  
---------------------------------------------------------------------------------  
  
Report RTL Partitions:   
+-+--------------+------------+----------+  
| |RTL Partition |Replication |Instances |  
+-+--------------+------------+----------+  
+-+--------------+------------+----------+  
---------------------------------------------------------------------------------  
Start RTL Component Statistics   
---------------------------------------------------------------------------------  
Detailed RTL Component Info :   
+---Adders :   
 3 Input 3 Bit Adders := 1   
+---Muxes :   
 2 Input 32 Bit Muxes := 6   
 2 Input 3 Bit Muxes := 2   
 2 Input 1 Bit Muxes := 2   
 4 Input 1 Bit Muxes := 1   
---------------------------------------------------------------------------------  
Finished RTL Component Statistics   
---------------------------------------------------------------------------------  
---------------------------------------------------------------------------------  
Start RTL Hierarchical Component Statistics   
---------------------------------------------------------------------------------  
Hierarchical RTL Component report   
Module next\_address   
Detailed RTL Component Info :   
+---Adders :   
 3 Input 3 Bit Adders := 1   
+---Muxes :   
 2 Input 32 Bit Muxes := 6   
 2 Input 3 Bit Muxes := 2   
 2 Input 1 Bit Muxes := 2   
 4 Input 1 Bit Muxes := 1   
---------------------------------------------------------------------------------  
Finished RTL Hierarchical Component Statistics  
---------------------------------------------------------------------------------  
---------------------------------------------------------------------------------  
Start Part Resource Summary  
---------------------------------------------------------------------------------  
Part Resources:  
DSPs: 240 (col length:80)  
BRAMs: 270 (col length: RAMB18 80 RAMB36 40)  
---------------------------------------------------------------------------------  
Finished Part Resource Summary  
---------------------------------------------------------------------------------  
---------------------------------------------------------------------------------  
Start Cross Boundary **and** Area Optimization  
---------------------------------------------------------------------------------  
Warning: Parallel synthesis criteria **is** **not** met   
WARNING: [Synth 8-3332] Sequential element (branch\_offset\_reg[31]) **is** unused **and** will be removed **from** module next\_address.  
WARNING: [Synth 8-3332] Sequential element (branch\_offset\_reg[30]) **is** unused **and** will be removed **from** module next\_address.  
WARNING: [Synth 8-3332] Sequential element (branch\_offset\_reg[29]) **is** unused **and** will be removed **from** module next\_address.  
WARNING: [Synth 8-3332] Sequential element (branch\_offset\_reg[28]) **is** unused **and** will be removed **from** module next\_address.  
WARNING: [Synth 8-3332] Sequential element (branch\_offset\_reg[27]) **is** unused **and** will be removed **from** module next\_address.  
WARNING: [Synth 8-3332] Sequential element (branch\_offset\_reg[26]) **is** unused **and** will be removed **from** module next\_address.  
WARNING: [Synth 8-3332] Sequential element (branch\_offset\_reg[25]) **is** unused **and** will be removed **from** module next\_address.  
WARNING: [Synth 8-3332] Sequential element (branch\_offset\_reg[24]) **is** unused **and** will be removed **from** module next\_address.  
WARNING: [Synth 8-3332] Sequential element (branch\_offset\_reg[23]) **is** unused **and** will be removed **from** module next\_address.  
WARNING: [Synth 8-3332] Sequential element (branch\_offset\_reg[22]) **is** unused **and** will be removed **from** module next\_address.  
WARNING: [Synth 8-3332] Sequential element (branch\_offset\_reg[21]) **is** unused **and** will be removed **from** module next\_address.  
WARNING: [Synth 8-3332] Sequential element (branch\_offset\_reg[20]) **is** unused **and** will be removed **from** module next\_address.  
WARNING: [Synth 8-3332] Sequential element (branch\_offset\_reg[19]) **is** unused **and** will be removed **from** module next\_address.  
WARNING: [Synth 8-3332] Sequential element (branch\_offset\_reg[18]) **is** unused **and** will be removed **from** module next\_address.  
WARNING: [Synth 8-3332] Sequential element (branch\_offset\_reg[17]) **is** unused **and** will be removed **from** module next\_address.  
WARNING: [Synth 8-3332] Sequential element (branch\_offset\_reg[16]) **is** unused **and** will be removed **from** module next\_address.  
WARNING: [Synth 8-3332] Sequential element (branch\_offset\_reg[15]) **is** unused **and** will be removed **from** module next\_address.  
WARNING: [Synth 8-3332] Sequential element (branch\_offset\_reg[14]) **is** unused **and** will be removed **from** module next\_address.  
WARNING: [Synth 8-3332] Sequential element (branch\_offset\_reg[13]) **is** unused **and** will be removed **from** module next\_address.  
WARNING: [Synth 8-3332] Sequential element (branch\_offset\_reg[12]) **is** unused **and** will be removed **from** module next\_address.  
WARNING: [Synth 8-3332] Sequential element (branch\_offset\_reg[11]) **is** unused **and** will be removed **from** module next\_address.  
WARNING: [Synth 8-3332] Sequential element (branch\_offset\_reg[10]) **is** unused **and** will be removed **from** module next\_address.  
WARNING: [Synth 8-3332] Sequential element (branch\_offset\_reg[9]) **is** unused **and** will be removed **from** module next\_address.  
WARNING: [Synth 8-3332] Sequential element (branch\_offset\_reg[8]) **is** unused **and** will be removed **from** module next\_address.  
WARNING: [Synth 8-3332] Sequential element (branch\_offset\_reg[7]) **is** unused **and** will be removed **from** module next\_address.  
WARNING: [Synth 8-3332] Sequential element (branch\_offset\_reg[6]) **is** unused **and** will be removed **from** module next\_address.  
WARNING: [Synth 8-3332] Sequential element (branch\_offset\_reg[5]) **is** unused **and** will be removed **from** module next\_address.  
WARNING: [Synth 8-3332] Sequential element (branch\_offset\_reg[4]) **is** unused **and** will be removed **from** module next\_address.  
WARNING: [Synth 8-3332] Sequential element (branch\_offset\_reg[3]) **is** unused **and** will be removed **from** module next\_address.  
WARNING: [Synth 8-3332] Sequential element (branch\_offset\_reg[2]) **is** unused **and** will be removed **from** module next\_address.  
WARNING: [Synth 8-3332] Sequential element (branch\_offset\_reg[1]) **is** unused **and** will be removed **from** module next\_address.  
WARNING: [Synth 8-3332] Sequential element (branch\_offset\_reg[0]) **is** unused **and** will be removed **from** module next\_address.  
---------------------------------------------------------------------------------  
Finished Cross Boundary **and** Area Optimization : Time (s): cpu = 00:00:17 ; elapsed = 00:01:11 . Memory (MB): peak = 1865.684 ; gain = 483.816 ; free physical = 89639 ; free virtual = 154104  
---------------------------------------------------------------------------------  
  
Report RTL Partitions:   
+-+--------------+------------+----------+  
| |RTL Partition |Replication |Instances |  
+-+--------------+------------+----------+  
+-+--------------+------------+----------+  
---------------------------------------------------------------------------------  
Start Applying XDC Timing Constraints  
---------------------------------------------------------------------------------  
---------------------------------------------------------------------------------  
Finished Applying XDC Timing Constraints : Time (s): cpu = 00:00:24 ; elapsed = 00:01:29 . Memory (MB): peak = 1865.684 ; gain = 483.816 ; free physical = 89509 ; free virtual = 153973  
---------------------------------------------------------------------------------  
---------------------------------------------------------------------------------  
Start Timing Optimization  
---------------------------------------------------------------------------------  
---------------------------------------------------------------------------------  
Finished Timing Optimization : Time (s): cpu = 00:00:24 ; elapsed = 00:01:29 . Memory (MB): peak = 1865.684 ; gain = 483.816 ; free physical = 89509 ; free virtual = 153973  
---------------------------------------------------------------------------------  
  
Report RTL Partitions:   
+-+--------------+------------+----------+  
| |RTL Partition |Replication |Instances |  
+-+--------------+------------+----------+  
+-+--------------+------------+----------+  
---------------------------------------------------------------------------------  
Start Technology Mapping  
---------------------------------------------------------------------------------  
---------------------------------------------------------------------------------  
Finished Technology Mapping : Time (s): cpu = 00:00:24 ; elapsed = 00:01:29 . Memory (MB): peak = 1865.684 ; gain = 483.816 ; free physical = 89508 ; free virtual = 153972  
---------------------------------------------------------------------------------  
  
Report RTL Partitions:   
+-+--------------+------------+----------+  
| |RTL Partition |Replication |Instances |  
+-+--------------+------------+----------+  
+-+--------------+------------+----------+  
---------------------------------------------------------------------------------  
Start IO Insertion  
---------------------------------------------------------------------------------  
---------------------------------------------------------------------------------  
Start Flattening Before IO Insertion  
---------------------------------------------------------------------------------  
---------------------------------------------------------------------------------  
Finished Flattening Before IO Insertion  
---------------------------------------------------------------------------------  
---------------------------------------------------------------------------------  
Start Final Netlist Cleanup  
---------------------------------------------------------------------------------  
---------------------------------------------------------------------------------  
Finished Final Netlist Cleanup  
---------------------------------------------------------------------------------  
---------------------------------------------------------------------------------  
Finished IO Insertion : Time (s): cpu = 00:00:25 ; elapsed = 00:01:30 . Memory (MB): peak = 1865.684 ; gain = 483.816 ; free physical = 89507 ; free virtual = 153971  
---------------------------------------------------------------------------------  
  
Report Check Netlist:   
+------+------------------+-------+---------+-------+------------------+  
| |Item |Errors |Warnings |Status |Description |  
+------+------------------+-------+---------+-------+------------------+  
|1 |multi\_driven\_nets | 0| 0|Passed |Multi driven nets |  
+------+------------------+-------+---------+-------+------------------+  
---------------------------------------------------------------------------------  
Start Renaming Generated Instances  
---------------------------------------------------------------------------------  
---------------------------------------------------------------------------------  
Finished Renaming Generated Instances : Time (s): cpu = 00:00:25 ; elapsed = 00:01:30 . Memory (MB): peak = 1865.684 ; gain = 483.816 ; free physical = 89507 ; free virtual = 153971  
---------------------------------------------------------------------------------  
  
Report RTL Partitions:   
+-+--------------+------------+----------+  
| |RTL Partition |Replication |Instances |  
+-+--------------+------------+----------+  
+-+--------------+------------+----------+  
---------------------------------------------------------------------------------  
Start Rebuilding User Hierarchy  
---------------------------------------------------------------------------------  
---------------------------------------------------------------------------------  
Finished Rebuilding User Hierarchy : Time (s): cpu = 00:00:25 ; elapsed = 00:01:30 . Memory (MB): peak = 1865.684 ; gain = 483.816 ; free physical = 89507 ; free virtual = 153971  
---------------------------------------------------------------------------------  
---------------------------------------------------------------------------------  
Start Renaming Generated Ports  
---------------------------------------------------------------------------------  
---------------------------------------------------------------------------------  
Finished Renaming Generated Ports : Time (s): cpu = 00:00:25 ; elapsed = 00:01:30 . Memory (MB): peak = 1865.684 ; gain = 483.816 ; free physical = 89507 ; free virtual = 153971  
---------------------------------------------------------------------------------  
---------------------------------------------------------------------------------  
Start Handling Custom Attributes  
---------------------------------------------------------------------------------  
---------------------------------------------------------------------------------  
Finished Handling Custom Attributes : Time (s): cpu = 00:00:25 ; elapsed = 00:01:30 . Memory (MB): peak = 1865.684 ; gain = 483.816 ; free physical = 89507 ; free virtual = 153971  
---------------------------------------------------------------------------------  
---------------------------------------------------------------------------------  
Start Renaming Generated Nets  
---------------------------------------------------------------------------------  
---------------------------------------------------------------------------------  
Finished Renaming Generated Nets : Time (s): cpu = 00:00:25 ; elapsed = 00:01:30 . Memory (MB): peak = 1865.684 ; gain = 483.816 ; free physical = 89507 ; free virtual = 153971  
---------------------------------------------------------------------------------  
---------------------------------------------------------------------------------  
Start Writing Synthesis Report  
---------------------------------------------------------------------------------  
  
Report BlackBoxes:   
+-+--------------+----------+  
| |BlackBox name |Instances |  
+-+--------------+----------+  
+-+--------------+----------+  
  
Report Cell Usage:   
+------+-----+------+  
| |Cell |Count |  
+------+-----+------+  
|1 |LUT2 | 1|  
|2 |LUT5 | 3|  
|3 |LUT6 | 3|  
|4 |LD | 3|  
|5 |IBUF | 14|  
|6 |OBUF | 3|  
+------+-----+------+  
  
Report Instance Areas:   
+------+---------+-------+------+  
| |Instance |Module |Cells |  
+------+---------+-------+------+  
|1 |top | | 27|  
+------+---------+-------+------+  
---------------------------------------------------------------------------------  
Finished Writing Synthesis Report : Time (s): cpu = 00:00:25 ; elapsed = 00:01:30 . Memory (MB): peak = 1865.684 ; gain = 483.816 ; free physical = 89507 ; free virtual = 153971  
---------------------------------------------------------------------------------  
Synthesis finished with 0 errors, 0 critical warnings **and** 35 warnings.  
Synthesis Optimization Runtime : Time (s): cpu = 00:00:14 ; elapsed = 00:00:31 . Memory (MB): peak = 1865.684 ; gain = 131.367 ; free physical = 89563 ; free virtual = 154028  
Synthesis Optimization Complete : Time (s): cpu = 00:00:25 ; elapsed = 00:01:30 . Memory (MB): peak = 1865.684 ; gain = 483.816 ; free physical = 89573 ; free virtual = 154038  
INFO: [Project 1-571] Translating synthesized netlist  
INFO: [Netlist 29-17] Analyzing 17 Unisim elements **for** replacement  
INFO: [Netlist 29-28] Unisim Transformation completed **in** 0 CPU seconds  
INFO: [Project 1-570] Preparing netlist **for** logic optimization  
INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).  
INFO: [Project 1-111] Unisim Transformation Summary:  
 A total of 3 instances were transformed.  
 LD => LDCE: 3 instances  
  
INFO: [Common 17-83] Releasing license: Synthesis  
14 Infos, 36 Warnings, 1 Critical Warnings **and** 0 Errors encountered.  
synth\_design completed successfully  
synth\_design: Time (s): cpu = 00:00:27 ; elapsed = 00:01:32 . Memory (MB): peak = 1909.324 ; gain = 540.184 ; free physical = 89562 ; free virtual = 154027  
WARNING: [Constraints 18-5210] No constraint will be written **out**.  
INFO: [Common 17-1381] The checkpoint '/nfs/home/l/l\_heiwan/coen316/lab3/vivado/lab3\_v1/lab3\_v1.runs/synth\_1/next\_address.dcp' has been generated.  
INFO: [runtcl-4] Executing : report\_utilization -file next\_address\_utilization\_synth.rpt -pb next\_address\_utilization\_synth.pb  
report\_utilization: Time (s): cpu = 00:00:00.05 ; elapsed = 00:00:00.14 . Memory (MB): peak = 1933.348 ; gain = 0.000 ; free physical = 89565 ; free virtual = 154029  
INFO: [Common 17-206] Exiting Vivado at Wed Nov 8 18:11:42 2023...

**5.6) Implementation Log**

****

**Warning Discussion:** There is one critical warning and it is the same reason as the one we obtained from the synthesis log related to set\_property which is unneeded. As for the warnings, there are 4 of them which is related to timing and clock constraints.

\*\*\* Running vivado  
 **with** args -log next\_address.vdi -applog -m64 -product Vivado -messageDb vivado.pb -mode batch -source next\_address.tcl -notrace  
  
  
\*\*\*\*\*\* Vivado v2018.2 (64-bit)  
 \*\*\*\* SW Build 2258646 on Thu Jun 14 20:02:38 MDT 2018  
 \*\*\*\* IP Build 2256618 on Thu Jun 14 22:10:49 MDT 2018  
 \*\* Copyright 1986-2018 Xilinx, Inc. All Rights Reserved.  
  
source next\_address.tcl -notrace  
Command: link\_design -top next\_address -part xc7a100tcsg324-1  
Design is defaulting to srcset: sources\_1  
Design is defaulting to constrset: constrs\_1  
INFO: [Netlist 29-17] Analyzing 14 Unisim elements for replacement  
INFO: [Netlist 29-28] Unisim Transformation completed **in** 0 CPU seconds  
INFO: [Project 1-479] Netlist was created **with** Vivado 2018.2  
INFO: [Device 21-403] Loading part xc7a100tcsg324-1  
INFO: [Project 1-570] Preparing netlist for logic optimization  
Parsing XDC File [/nfs/home/l/l\_heiwan/coen316/lab3/lab3\_constraints.xdc]  
WARNING: [Vivado 12-507] No nets matched 'clk'. [/nfs/home/l/l\_heiwan/coen316/lab3/lab3\_constraints.xdc:4]  
CRITICAL WARNING: [Common 17-55] 'set\_property' expects at least one object. [/nfs/home/l/l\_heiwan/coen316/lab3/lab3\_constraints.xdc:4]  
Resolution: If [get\_<value>] was used to populate the object, check to make sure this command returns at least one valid object.  
Finished Parsing XDC File [/nfs/home/l/l\_heiwan/coen316/lab3/lab3\_constraints.xdc]  
INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).  
INFO: [Project 1-111] Unisim Transformation Summary:  
No Unisim elements were transformed.  
  
7 Infos, 1 Warnings, 1 Critical Warnings and 0 Errors encountered.  
link\_design completed successfully  
link\_design: Time (s): cpu = 00:00:11 ; elapsed = 00:01:00 . Memory (MB): peak = 1701.566 ; gain = 327.414 ; free physical = 89662 ; free virtual = 154124  
Command: opt\_design  
Attempting to get a license for feature 'Implementation' and/or device 'xc7a100t'  
INFO: [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a100t'  
Running DRC as a precondition to command opt\_design  
  
Starting DRC Task  
INFO: [DRC 23-27] Running DRC **with** 8 threads  
INFO: [Project 1-461] DRC finished **with** 0 Errors  
INFO: [Project 1-462] Please refer to the DRC report (report\_drc) for more information.  
  
Time (s): cpu = 00:00:02 ; elapsed = 00:00:04 . Memory (MB): peak = 1780.594 ; gain = 79.027 ; free physical = 89653 ; free virtual = 154116  
  
Starting Cache Timing Information Task  
INFO: [Timing 38-35] Done setting XDC timing constraints.  
Ending Cache Timing Information Task | Checksum: 1ae30121e  
  
Time (s): cpu = 00:00:16 ; elapsed = 00:01:12 . Memory (MB): peak = 2217.094 ; gain = 436.500 ; free physical = 89262 ; free virtual = 153725  
  
Starting Logic Optimization Task  
  
Phase 1 Retarget  
INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).  
INFO: [Opt 31-49] Retargeted 0 cell(s).  
Phase 1 Retarget | Checksum: 1ae30121e  
  
Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00.02 . Memory (MB): peak = 2217.094 ; gain = 0.000 ; free physical = 89280 ; free virtual = 153743  
INFO: [Opt 31-389] Phase Retarget created 0 cells and removed 0 cells  
  
Phase 2 Constant propagation  
INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).  
Phase 2 Constant propagation | Checksum: 1ae30121e  
  
Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00.02 . Memory (MB): peak = 2217.094 ; gain = 0.000 ; free physical = 89280 ; free virtual = 153743  
INFO: [Opt 31-389] Phase Constant propagation created 0 cells and removed 0 cells  
  
Phase 3 Sweep  
Phase 3 Sweep | Checksum: 1ae30121e  
  
Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00.02 . Memory (MB): peak = 2217.094 ; gain = 0.000 ; free physical = 89280 ; free virtual = 153743  
INFO: [Opt 31-389] Phase Sweep created 0 cells and removed 0 cells  
  
Phase 4 BUFG optimization  
Phase 4 BUFG optimization | Checksum: 1ae30121e  
  
Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00.03 . Memory (MB): peak = 2217.094 ; gain = 0.000 ; free physical = 89280 ; free virtual = 153743  
INFO: [Opt 31-662] Phase BUFG optimization created 0 cells of which 0 are BUFGs and removed 0 cells.  
  
Phase 5 Shift Register Optimization  
Phase 5 Shift Register Optimization | Checksum: 1ae30121e  
  
Time (s): cpu = 00:00:00.02 ; elapsed = 00:00:00.03 . Memory (MB): peak = 2217.094 ; gain = 0.000 ; free physical = 89280 ; free virtual = 153743  
INFO: [Opt 31-389] Phase Shift Register Optimization created 0 cells and removed 0 cells  
  
Phase 6 Post Processing Netlist  
Phase 6 Post Processing Netlist | Checksum: 1ae30121e  
  
Time (s): cpu = 00:00:00.02 ; elapsed = 00:00:00.03 . Memory (MB): peak = 2217.094 ; gain = 0.000 ; free physical = 89280 ; free virtual = 153743  
INFO: [Opt 31-389] Phase Post Processing Netlist created 0 cells and removed 0 cells  
  
Starting Connectivity Check Task  
  
Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2217.094 ; gain = 0.000 ; free physical = 89280 ; free virtual = 153743  
Ending Logic Optimization Task | Checksum: 1ae30121e  
  
Time (s): cpu = 00:00:00.02 ; elapsed = 00:00:00.03 . Memory (MB): peak = 2217.094 ; gain = 0.000 ; free physical = 89280 ; free virtual = 153743  
  
Starting Power Optimization Task  
INFO: [Pwropt 34-132] Skipping clock gating for clocks **with** a period < 2.00 ns.  
Ending Power Optimization Task | Checksum: 1ae30121e  
  
Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00.05 . Memory (MB): peak = 2217.094 ; gain = 0.000 ; free physical = 89280 ; free virtual = 153743  
  
Starting Final Cleanup Task  
Ending Final Cleanup Task | Checksum: 1ae30121e  
  
Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2217.094 ; gain = 0.000 ; free physical = 89280 ; free virtual = 153743  
INFO: [Common 17-83] Releasing license: Implementation  
23 Infos, 1 Warnings, 1 Critical Warnings and 0 Errors encountered.  
opt\_design completed successfully  
opt\_design: Time (s): cpu = 00:00:17 ; elapsed = 00:01:16 . Memory (MB): peak = 2217.094 ; gain = 515.527 ; free physical = 89280 ; free virtual = 153743  
INFO: [Timing 38-480] Writing timing data to binary archive.  
Writing placer database...  
Writing XDEF routing.  
Writing XDEF routing logical nets.  
Writing XDEF routing special nets.  
Write XDEF Complete: Time (s): cpu = 00:00:00.04 ; elapsed = 00:00:00.02 . Memory (MB): peak = 2249.109 ; gain = 0.004 ; free physical = 89279 ; free virtual = 153742  
INFO: [Common 17-1381] The checkpoint '/nfs/home/l/l\_heiwan/coen316/lab3/vivado/lab3\_v1/lab3\_v1.runs/impl\_1/next\_address\_opt.dcp' has been generated.  
INFO: [runtcl-4] Executing : report\_drc -file next\_address\_drc\_opted.rpt -pb next\_address\_drc\_opted.pb -rpx next\_address\_drc\_opted.rpx  
Command: report\_drc -file next\_address\_drc\_opted.rpt -pb next\_address\_drc\_opted.pb -rpx next\_address\_drc\_opted.rpx  
INFO: [IP\_Flow 19-234] Refreshing IP repositories  
INFO: [IP\_Flow 19-1704] No user IP repositories specified  
INFO: [IP\_Flow 19-2313] Loaded Vivado IP repository '/CMC/tools/xilinx/Vivado\_2018.2/Vivado/2018.2/data/ip'.  
INFO: [DRC 23-27] Running DRC **with** 8 threads  
INFO: [Coretcl 2-168] The results of DRC are **in** file /nfs/home/l/l\_heiwan/coen316/lab3/vivado/lab3\_v1/lab3\_v1.runs/impl\_1/next\_address\_drc\_opted.rpt.  
report\_drc completed successfully  
report\_drc: Time (s): cpu = 00:00:04 ; elapsed = 00:00:07 . Memory (MB): peak = 2329.148 ; gain = 80.031 ; free physical = 89236 ; free virtual = 153699  
Command: place\_design  
Attempting to get a license for feature 'Implementation' and/or device 'xc7a100t'  
INFO: [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a100t'  
INFO: [DRC 23-27] Running DRC **with** 8 threads  
INFO: [Vivado\_Tcl 4-198] DRC finished **with** 0 Errors  
INFO: [Vivado\_Tcl 4-199] Please refer to the DRC report (report\_drc) for more information.  
Running DRC as a precondition to command place\_design  
INFO: [DRC 23-27] Running DRC **with** 8 threads  
INFO: [Vivado\_Tcl 4-198] DRC finished **with** 0 Errors  
INFO: [Vivado\_Tcl 4-199] Please refer to the DRC report (report\_drc) for more information.  
  
Starting Placer Task  
INFO: [Place 30-611] Multithreading enabled for place\_design using a maximum of 8 CPUs  
  
Phase 1 Placer Initialization  
  
Phase 1.1 Placer Initialization Netlist Sorting  
Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2329.148 ; gain = 0.000 ; free physical = 89231 ; free virtual = 153694  
Phase 1.1 Placer Initialization Netlist Sorting | Checksum: 181ad8179  
  
Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.02 . Memory (MB): peak = 2329.148 ; gain = 0.000 ; free physical = 89231 ; free virtual = 153694  
Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2329.148 ; gain = 0.000 ; free physical = 89231 ; free virtual = 153694  
  
Phase 1.2 IO Placement/ Clock Placement/ Build Placer Device  
INFO: [Timing 38-35] Done setting XDC timing constraints.  
Phase 1.2 IO Placement/ Clock Placement/ Build Placer Device | Checksum: 181ad8179  
  
Time (s): cpu = 00:00:00.67 ; elapsed = 00:00:00.61 . Memory (MB): peak = 2329.148 ; gain = 0.000 ; free physical = 89219 ; free virtual = 153682  
  
Phase 1.3 Build Placer Netlist Model  
Phase 1.3 Build Placer Netlist Model | Checksum: 1e93714e2  
  
Time (s): cpu = 00:00:00.73 ; elapsed = 00:00:00.64 . Memory (MB): peak = 2329.148 ; gain = 0.000 ; free physical = 89219 ; free virtual = 153682  
  
Phase 1.4 Constrain Clocks/Macros  
Phase 1.4 Constrain Clocks/Macros | Checksum: 1e93714e2  
  
Time (s): cpu = 00:00:00.73 ; elapsed = 00:00:00.65 . Memory (MB): peak = 2329.148 ; gain = 0.000 ; free physical = 89219 ; free virtual = 153682  
Phase 1 Placer Initialization | Checksum: 1e93714e2  
  
Time (s): cpu = 00:00:00.73 ; elapsed = 00:00:00.65 . Memory (MB): peak = 2329.148 ; gain = 0.000 ; free physical = 89219 ; free virtual = 153682  
  
Phase 2 Global Placement  
  
Phase 2.1 Floorplanning  
Phase 2.1 Floorplanning | Checksum: 1e93714e2  
  
Time (s): cpu = 00:00:00.77 ; elapsed = 00:00:00.68 . Memory (MB): peak = 2329.148 ; gain = 0.000 ; free physical = 89217 ; free virtual = 153680  
WARNING: [Place 46-29] place\_design is not **in** timing mode. Skip physical synthesis **in** placer  
Phase 2 Global Placement | Checksum: 27a471cdb  
  
Time (s): cpu = 00:00:03 ; elapsed = 00:00:01 . Memory (MB): peak = 2401.168 ; gain = 72.020 ; free physical = 89186 ; free virtual = 153649  
  
Phase 3 Detail Placement  
  
Phase 3.1 Commit Multi Column Macros  
Phase 3.1 Commit Multi Column Macros | Checksum: 27a471cdb  
  
Time (s): cpu = 00:00:03 ; elapsed = 00:00:01 . Memory (MB): peak = 2401.168 ; gain = 72.020 ; free physical = 89186 ; free virtual = 153649  
  
Phase 3.2 Commit Most Macros & LUTRAMs  
Phase 3.2 Commit Most Macros & LUTRAMs | Checksum: 1db91fb63  
  
Time (s): cpu = 00:00:03 ; elapsed = 00:00:01 . Memory (MB): peak = 2401.168 ; gain = 72.020 ; free physical = 89186 ; free virtual = 153649  
  
Phase 3.3 Area Swap Optimization  
Phase 3.3 Area Swap Optimization | Checksum: 1d2d83eea  
  
Time (s): cpu = 00:00:03 ; elapsed = 00:00:01 . Memory (MB): peak = 2401.168 ; gain = 72.020 ; free physical = 89186 ; free virtual = 153649  
  
Phase 3.4 Pipeline Register Optimization  
Phase 3.4 Pipeline Register Optimization | Checksum: 1d2d83eea  
  
Time (s): cpu = 00:00:03 ; elapsed = 00:00:01 . Memory (MB): peak = 2401.168 ; gain = 72.020 ; free physical = 89186 ; free virtual = 153649  
  
Phase 3.5 Small Shape Detail Placement  
Phase 3.5 Small Shape Detail Placement | Checksum: 1d6f2e983  
  
Time (s): cpu = 00:00:03 ; elapsed = 00:00:01 . Memory (MB): peak = 2401.168 ; gain = 72.020 ; free physical = 89181 ; free virtual = 153644  
  
Phase 3.6 Re-assign LUT pins  
Phase 3.6 Re-assign LUT pins | Checksum: 1d6f2e983  
  
Time (s): cpu = 00:00:03 ; elapsed = 00:00:01 . Memory (MB): peak = 2401.168 ; gain = 72.020 ; free physical = 89181 ; free virtual = 153644  
  
Phase 3.7 Pipeline Register Optimization  
Phase 3.7 Pipeline Register Optimization | Checksum: 1d6f2e983  
  
Time (s): cpu = 00:00:03 ; elapsed = 00:00:01 . Memory (MB): peak = 2401.168 ; gain = 72.020 ; free physical = 89181 ; free virtual = 153644  
Phase 3 Detail Placement | Checksum: 1d6f2e983  
  
Time (s): cpu = 00:00:03 ; elapsed = 00:00:01 . Memory (MB): peak = 2401.168 ; gain = 72.020 ; free physical = 89181 ; free virtual = 153644  
  
Phase 4 Post Placement Optimization and Clean-Up  
  
Phase 4.1 Post Commit Optimization  
Phase 4.1 Post Commit Optimization | Checksum: 1d6f2e983  
  
Time (s): cpu = 00:00:03 ; elapsed = 00:00:01 . Memory (MB): peak = 2401.168 ; gain = 72.020 ; free physical = 89181 ; free virtual = 153644  
  
Phase 4.2 Post Placement Cleanup  
Phase 4.2 Post Placement Cleanup | Checksum: 1d6f2e983  
  
Time (s): cpu = 00:00:03 ; elapsed = 00:00:01 . Memory (MB): peak = 2401.168 ; gain = 72.020 ; free physical = 89183 ; free virtual = 153646  
  
Phase 4.3 Placer Reporting  
Phase 4.3 Placer Reporting | Checksum: 1d6f2e983  
  
Time (s): cpu = 00:00:03 ; elapsed = 00:00:01 . Memory (MB): peak = 2401.168 ; gain = 72.020 ; free physical = 89183 ; free virtual = 153646  
  
Phase 4.4 Final Placement Cleanup  
Phase 4.4 Final Placement Cleanup | Checksum: 1d6f2e983  
  
Time (s): cpu = 00:00:03 ; elapsed = 00:00:01 . Memory (MB): peak = 2401.168 ; gain = 72.020 ; free physical = 89183 ; free virtual = 153646  
Phase 4 Post Placement Optimization and Clean-Up | Checksum: 1d6f2e983  
  
Time (s): cpu = 00:00:03 ; elapsed = 00:00:01 . Memory (MB): peak = 2401.168 ; gain = 72.020 ; free physical = 89183 ; free virtual = 153646  
Ending Placer Task | Checksum: 153417f87  
  
Time (s): cpu = 00:00:03 ; elapsed = 00:00:01 . Memory (MB): peak = 2401.168 ; gain = 72.020 ; free physical = 89200 ; free virtual = 153663  
INFO: [Common 17-83] Releasing license: Implementation  
41 Infos, 2 Warnings, 1 Critical Warnings and 0 Errors encountered.  
place\_design completed successfully  
place\_design: Time (s): cpu = 00:00:05 ; elapsed = 00:00:05 . Memory (MB): peak = 2401.168 ; gain = 72.020 ; free physical = 89200 ; free virtual = 153663  
INFO: [Timing 38-480] Writing timing data to binary archive.  
Writing placer database...  
Writing XDEF routing.  
Writing XDEF routing logical nets.  
Writing XDEF routing special nets.  
Write XDEF Complete: Time (s): cpu = 00:00:00.04 ; elapsed = 00:00:00.03 . Memory (MB): peak = 2401.168 ; gain = 0.000 ; free physical = 89200 ; free virtual = 153664  
INFO: [Common 17-1381] The checkpoint '/nfs/home/l/l\_heiwan/coen316/lab3/vivado/lab3\_v1/lab3\_v1.runs/impl\_1/next\_address\_placed.dcp' has been generated.  
INFO: [runtcl-4] Executing : report\_io -file next\_address\_io\_placed.rpt  
report\_io: Time (s): cpu = 00:00:00.07 ; elapsed = 00:00:00.16 . Memory (MB): peak = 2401.168 ; gain = 0.000 ; free physical = 89192 ; free virtual = 153655  
INFO: [runtcl-4] Executing : report\_utilization -file next\_address\_utilization\_placed.rpt -pb next\_address\_utilization\_placed.pb  
report\_utilization: Time (s): cpu = 00:00:00.06 ; elapsed = 00:00:00.14 . Memory (MB): peak = 2401.168 ; gain = 0.000 ; free physical = 89201 ; free virtual = 153664  
INFO: [runtcl-4] Executing : report\_control\_sets -verbose -file next\_address\_control\_sets\_placed.rpt  
report\_control\_sets: Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00.10 . Memory (MB): peak = 2401.168 ; gain = 0.000 ; free physical = 89203 ; free virtual = 153666  
Command: route\_design  
Attempting to get a license for feature 'Implementation' and/or device 'xc7a100t'  
INFO: [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a100t'  
Running DRC as a precondition to command route\_design  
INFO: [DRC 23-27] Running DRC **with** 8 threads  
INFO: [Vivado\_Tcl 4-198] DRC finished **with** 0 Errors  
INFO: [Vivado\_Tcl 4-199] Please refer to the DRC report (report\_drc) for more information.  
  
  
Starting Routing Task  
INFO: [Route 35-254] Multithreading enabled for route\_design using a maximum of 8 CPUs  
Checksum: PlaceDB: 98329793 ConstDB: 0 ShapeSum: bb0ee7f4 RouteDB: 0  
  
Phase 1 Build RT Design  
Phase 1 Build RT Design | Checksum: fdfce166  
  
Time (s): cpu = 00:00:26 ; elapsed = 00:00:21 . Memory (MB): peak = 2443.773 ; gain = 42.605 ; free physical = 89057 ; free virtual = 153520  
Post Restoration Checksum: NetGraph: 5f46572c NumContArr: 9eb68a3a Constraints: 0 Timing: 0  
  
Phase 2 Router Initialization  
INFO: [Route 35-64] No timing constraints were detected. The router will operate **in** resource-optimization mode.  
  
Phase 2.1 Fix Topology Constraints  
Phase 2.1 Fix Topology Constraints | Checksum: fdfce166  
  
Time (s): cpu = 00:00:26 ; elapsed = 00:00:21 . Memory (MB): peak = 2449.762 ; gain = 48.594 ; free physical = 89025 ; free virtual = 153488  
  
Phase 2.2 Pre Route Cleanup  
Phase 2.2 Pre Route Cleanup | Checksum: fdfce166  
  
Time (s): cpu = 00:00:26 ; elapsed = 00:00:21 . Memory (MB): peak = 2449.762 ; gain = 48.594 ; free physical = 89025 ; free virtual = 153488  
 Number of Nodes **with** overlaps = 0  
Phase 2 Router Initialization | Checksum: 10994250a  
  
Time (s): cpu = 00:00:26 ; elapsed = 00:00:21 . Memory (MB): peak = 2457.027 ; gain = 55.859 ; free physical = 89022 ; free virtual = 153485  
  
Phase 3 Initial Routing  
Phase 3 Initial Routing | Checksum: ce76cf96  
  
Time (s): cpu = 00:00:26 ; elapsed = 00:00:21 . Memory (MB): peak = 2457.027 ; gain = 55.859 ; free physical = 89020 ; free virtual = 153484  
  
Phase 4 Rip-up And Reroute  
  
Phase 4.1 Global Iteration 0  
 Number of Nodes **with** overlaps = 0  
Phase 4.1 Global Iteration 0 | Checksum: 824cbf09  
  
Time (s): cpu = 00:00:26 ; elapsed = 00:00:21 . Memory (MB): peak = 2457.027 ; gain = 55.859 ; free physical = 89020 ; free virtual = 153483  
Phase 4 Rip-up And Reroute | Checksum: 824cbf09  
  
Time (s): cpu = 00:00:26 ; elapsed = 00:00:21 . Memory (MB): peak = 2457.027 ; gain = 55.859 ; free physical = 89020 ; free virtual = 153483  
  
Phase 5 Delay and Skew Optimization  
Phase 5 Delay and Skew Optimization | Checksum: 824cbf09  
  
Time (s): cpu = 00:00:26 ; elapsed = 00:00:21 . Memory (MB): peak = 2457.027 ; gain = 55.859 ; free physical = 89020 ; free virtual = 153483  
  
Phase 6 Post Hold Fix  
  
Phase 6.1 Hold Fix Iter  
Phase 6.1 Hold Fix Iter | Checksum: 824cbf09  
  
Time (s): cpu = 00:00:26 ; elapsed = 00:00:21 . Memory (MB): peak = 2457.027 ; gain = 55.859 ; free physical = 89020 ; free virtual = 153483  
Phase 6 Post Hold Fix | Checksum: 824cbf09  
  
Time (s): cpu = 00:00:26 ; elapsed = 00:00:21 . Memory (MB): peak = 2457.027 ; gain = 55.859 ; free physical = 89020 ; free virtual = 153483  
  
Phase 7 Route finalize  
  
Router Utilization Summary  
 Global Vertical Routing Utilization = 0.0151021 %  
 Global Horizontal Routing Utilization = 0.0157005 %  
 Routable Net Status\*  
 \*Does not include unroutable nets such as driverless and loadless.  
 Run report\_route\_status for detailed report.  
 Number of Failed Nets = 0  
 Number of Unrouted Nets = 0  
 Number of Partially Routed Nets = 0  
 Number of Node Overlaps = 0  
  
Congestion Report  
North Dir 1x1 Area, Max Cong = 16.2162%, No Congested Regions.  
South Dir 1x1 Area, Max Cong = 21.6216%, No Congested Regions.  
East Dir 1x1 Area, Max Cong = 17.6471%, No Congested Regions.  
West Dir 1x1 Area, Max Cong = 17.6471%, No Congested Regions.  
  
------------------------------  
Reporting congestion hotspots  
------------------------------  
Direction: North  
----------------  
Congested clusters found at Level 0  
Effective congestion level: 0 Aspect Ratio: 1 Sparse Ratio: 0  
Direction: South  
----------------  
Congested clusters found at Level 0  
Effective congestion level: 0 Aspect Ratio: 1 Sparse Ratio: 0  
Direction: East  
----------------  
Congested clusters found at Level 0  
Effective congestion level: 0 Aspect Ratio: 1 Sparse Ratio: 0  
Direction: West  
----------------  
Congested clusters found at Level 0  
Effective congestion level: 0 Aspect Ratio: 1 Sparse Ratio: 0  
  
Phase 7 Route finalize | Checksum: 824cbf09  
  
Time (s): cpu = 00:00:26 ; elapsed = 00:00:21 . Memory (MB): peak = 2457.027 ; gain = 55.859 ; free physical = 89019 ; free virtual = 153483  
  
Phase 8 Verifying routed nets  
  
 Verification completed successfully  
Phase 8 Verifying routed nets | Checksum: 824cbf09  
  
Time (s): cpu = 00:00:26 ; elapsed = 00:00:21 . Memory (MB): peak = 2460.027 ; gain = 58.859 ; free physical = 89019 ; free virtual = 153482  
  
Phase 9 Depositing Routes  
Phase 9 Depositing Routes | Checksum: 824cbf09  
  
Time (s): cpu = 00:00:26 ; elapsed = 00:00:21 . Memory (MB): peak = 2460.027 ; gain = 58.859 ; free physical = 89019 ; free virtual = 153482  
INFO: [Route 35-16] Router Completed Successfully  
  
Time (s): cpu = 00:00:26 ; elapsed = 00:00:21 . Memory (MB): peak = 2460.027 ; gain = 58.859 ; free physical = 89054 ; free virtual = 153517  
  
Routing Is Done.  
INFO: [Common 17-83] Releasing license: Implementation  
54 Infos, 2 Warnings, 1 Critical Warnings and 0 Errors encountered.  
route\_design completed successfully  
route\_design: Time (s): cpu = 00:00:29 ; elapsed = 00:00:26 . Memory (MB): peak = 2460.027 ; gain = 58.859 ; free physical = 89054 ; free virtual = 153517  
INFO: [Timing 38-480] Writing timing data to binary archive.  
Writing placer database...  
Writing XDEF routing.  
Writing XDEF routing logical nets.  
Writing XDEF routing special nets.  
Write XDEF Complete: Time (s): cpu = 00:00:00.04 ; elapsed = 00:00:00.03 . Memory (MB): peak = 2460.027 ; gain = 0.000 ; free physical = 89051 ; free virtual = 153515  
INFO: [Common 17-1381] The checkpoint '/nfs/home/l/l\_heiwan/coen316/lab3/vivado/lab3\_v1/lab3\_v1.runs/impl\_1/next\_address\_routed.dcp' has been generated.  
INFO: [runtcl-4] Executing : report\_drc -file next\_address\_drc\_routed.rpt -pb next\_address\_drc\_routed.pb -rpx next\_address\_drc\_routed.rpx  
Command: report\_drc -file next\_address\_drc\_routed.rpt -pb next\_address\_drc\_routed.pb -rpx next\_address\_drc\_routed.rpx  
INFO: [DRC 23-27] Running DRC **with** 8 threads  
INFO: [Coretcl 2-168] The results of DRC are **in** file /nfs/home/l/l\_heiwan/coen316/lab3/vivado/lab3\_v1/lab3\_v1.runs/impl\_1/next\_address\_drc\_routed.rpt.  
report\_drc completed successfully  
report\_drc: Time (s): cpu = 00:00:03 ; elapsed = 00:00:05 . Memory (MB): peak = 2548.070 ; gain = 88.035 ; free physical = 89045 ; free virtual = 153508  
INFO: [runtcl-4] Executing : report\_methodology -file next\_address\_methodology\_drc\_routed.rpt -pb next\_address\_methodology\_drc\_routed.pb -rpx next\_address\_methodology\_drc\_routed.rpx  
Command: report\_methodology -file next\_address\_methodology\_drc\_routed.rpt -pb next\_address\_methodology\_drc\_routed.pb -rpx next\_address\_methodology\_drc\_routed.rpx  
INFO: [Timing 38-35] Done setting XDC timing constraints.  
INFO: [Timing 38-35] Done setting XDC timing constraints.  
INFO: [DRC 23-133] Running Methodology **with** 8 threads  
INFO: [Coretcl 2-1520] The results of Report Methodology are **in** file /nfs/home/l/l\_heiwan/coen316/lab3/vivado/lab3\_v1/lab3\_v1.runs/impl\_1/next\_address\_methodology\_drc\_routed.rpt.  
report\_methodology completed successfully  
INFO: [runtcl-4] Executing : report\_power -file next\_address\_power\_routed.rpt -pb next\_address\_power\_summary\_routed.pb -rpx next\_address\_power\_routed.rpx  
Command: report\_power -file next\_address\_power\_routed.rpt -pb next\_address\_power\_summary\_routed.pb -rpx next\_address\_power\_routed.rpx  
WARNING: [Power 33-232] No user defined clocks were found **in** the design!  
Resolution: Please specify clocks using create\_clock/create\_generated\_clock for sequential elements. For pure combinatorial circuits, please specify a virtual clock, otherwise the vectorless estimation might be inaccurate  
INFO: [Timing 38-35] Done setting XDC timing constraints.  
Running Vector-less Activity Propagation...  
  
Finished Running Vector-less Activity Propagation  
66 Infos, 3 Warnings, 1 Critical Warnings and 0 Errors encountered.  
report\_power failed  
INFO: [runtcl-4] Executing : report\_route\_status -file next\_address\_route\_status.rpt -pb next\_address\_route\_status.pb  
INFO: [runtcl-4] Executing : report\_timing\_summary -max\_paths 10 -file next\_address\_timing\_summary\_routed.rpt -pb next\_address\_timing\_summary\_routed.pb -rpx next\_address\_timing\_summary\_routed.rpx -warn\_on\_violation   
INFO: [Timing 38-91] UpdateTimingParams: Speed grade: -1, Delay Type: min\_max, Timing Stage: Requireds.  
INFO: [Timing 38-191] Multithreading enabled for timing update using a maximum of 8 CPUs  
WARNING: [Timing 38-313] There are no user specified timing constraints. Timing constraints are needed for proper timing analysis.  
INFO: [runtcl-4] Executing : report\_incremental\_reuse -file next\_address\_incremental\_reuse\_routed.rpt  
INFO: [Vivado\_Tcl 4-545] No incremental reuse to report, no incremental placement and routing data was found.  
INFO: [runtcl-4] Executing : report\_clock\_utilization -file next\_address\_clock\_utilization\_routed.rpt  
INFO: [runtcl-4] Executing : report\_bus\_skew -warn\_on\_violation -file next\_address\_bus\_skew\_routed.rpt -pb next\_address\_bus\_skew\_routed.pb -rpx next\_address\_bus\_skew\_routed.rpx  
INFO: [Timing 38-91] UpdateTimingParams: Speed grade: -1, Delay Type: min\_max, Timing Stage: Requireds.  
INFO: [Timing 38-191] Multithreading enabled for timing update using a maximum of 8 CPUs  
INFO: [Common 17-206] Exiting Vivado at Wed Nov 8 18:16:15 2023...  
  
\*\*\* Running vivado  
 **with** args -log next\_address.vdi -applog -m64 -product Vivado -messageDb vivado.pb -mode batch -source next\_address.tcl -notrace  
  
  
\*\*\*\*\*\* Vivado v2018.2 (64-bit)  
 \*\*\*\* SW Build 2258646 on Thu Jun 14 20:02:38 MDT 2018  
 \*\*\*\* IP Build 2256618 on Thu Jun 14 22:10:49 MDT 2018  
 \*\* Copyright 1986-2018 Xilinx, Inc. All Rights Reserved.  
  
source next\_address.tcl -notrace  
Command: open\_checkpoint next\_address\_routed.dcp  
  
Starting open\_checkpoint Task  
  
Time (s): cpu = 00:00:00.07 ; elapsed = 00:00:00.25 . Memory (MB): peak = 1343.125 ; gain = 0.000 ; free physical = 89978 ; free virtual = 154441  
INFO: [Netlist 29-17] Analyzing 14 Unisim elements for replacement  
INFO: [Netlist 29-28] Unisim Transformation completed **in** 0 CPU seconds  
INFO: [Project 1-479] Netlist was created **with** Vivado 2018.2  
INFO: [Device 21-403] Loading part xc7a100tcsg324-1  
INFO: [Project 1-570] Preparing netlist for logic optimization  
INFO: [Timing 38-478] Restoring timing data from binary archive.  
INFO: [Timing 38-479] Binary timing data restore complete.  
INFO: [Project 1-856] Restoring constraints from binary archive.  
INFO: [Project 1-853] Binary constraint restore complete.  
Reading XDEF placement.  
Reading placer database...  
Reading XDEF routing.  
Read XDEF File: Time (s): cpu = 00:00:00.14 ; elapsed = 00:00:00.43 . Memory (MB): peak = 2128.246 ; gain = 0.004 ; free physical = 89235 ; free virtual = 153699  
Restored from archive | CPU: 0.420000 secs | Memory: 0.954468 MB |  
Finished XDEF File Restore: Time (s): cpu = 00:00:00.14 ; elapsed = 00:00:00.43 . Memory (MB): peak = 2128.246 ; gain = 0.004 ; free physical = 89235 ; free virtual = 153699  
INFO: [Project 1-111] Unisim Transformation Summary:  
No Unisim elements were transformed.  
  
INFO: [Project 1-604] Checkpoint was created **with** Vivado v2018.2 (64-bit) build 2258646  
open\_checkpoint: Time (s): cpu = 00:00:28 ; elapsed = 00:02:14 . Memory (MB): peak = 2128.246 ; gain = 785.125 ; free physical = 89235 ; free virtual = 153699  
Command: write\_bitstream -force next\_address.bit  
Attempting to get a license for feature 'Implementation' and/or device 'xc7a100t'  
INFO: [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a100t'  
Running DRC as a precondition to command write\_bitstream  
INFO: [IP\_Flow 19-234] Refreshing IP repositories  
INFO: [IP\_Flow 19-1704] No user IP repositories specified  
INFO: [IP\_Flow 19-2313] Loaded Vivado IP repository '/CMC/tools/xilinx/Vivado\_2018.2/Vivado/2018.2/data/ip'.  
INFO: [DRC 23-27] Running DRC **with** 8 threads  
WARNING: [DRC CFGBVS-1] Missing CFGBVS and CONFIG\_VOLTAGE Design Properties: Neither the CFGBVS nor CONFIG\_VOLTAGE voltage property is set **in** the current\_design. Configuration bank voltage select (CFGBVS) must be set to VCCO or GND, and CONFIG\_VOLTAGE must be set to the correct configuration voltage, **in** order to determine the I/O voltage support for the pins **in** bank 0. It is suggested to specify these either using the 'Edit Device Properties' function **in** the GUI or directly **in** the XDC file using the following syntax:  
  
 set\_property CFGBVS value1 [current\_design]  
 #where value1 is either VCCO or GND  
  
 set\_property CONFIG\_VOLTAGE value2 [current\_design]  
 #where value2 is the voltage provided to configuration bank 0  
  
Refer to the device configuration user guide for more information.  
WARNING: [DRC PDRC-153] Gated clock check: Net next\_pc\_reg[2]\_i\_2\_n\_0 is a gated clock net sourced by a combinational pin next\_pc\_reg[2]\_i\_2/O, cell next\_pc\_reg[2]\_i\_2. This is not good design practice and will likely impact performance. For SLICE registers, for example, use the CE pin to control the loading of data.  
INFO: [Vivado 12-3199] DRC finished **with** 0 Errors, 2 Warnings  
INFO: [Vivado 12-3200] Please refer to the DRC report (report\_drc) for more information.  
INFO: [Designutils 20-2272] Running write\_bitstream **with** 8 threads.  
Loading data files...  
Loading site data...  
Loading route data...  
Processing options...  
Creating bitmap...  
Creating bitstream...  
Writing bitstream ./next\_address.bit...  
INFO: [Vivado 12-1842] Bitgen Completed Successfully.  
INFO: [Common 17-83] Releasing license: Implementation  
21 Infos, 2 Warnings, 0 Critical Warnings and 0 Errors encountered.  
write\_bitstream completed successfully  
write\_bitstream: Time (s): cpu = 00:00:12 ; elapsed = 00:00:18 . Memory (MB): peak = 2601.086 ; gain = 472.840 ; free physical = 89162 ; free virtual = 153630  
INFO: [Common 17-206] Exiting Vivado at Wed Nov 8 18:19:16 2023...  
  
\*\*\* Running vivado  
 **with** args -log next\_address.vdi -applog -m64 -product Vivado -messageDb vivado.pb -mode batch -source next\_address.tcl -notrace  
  
  
\*\*\*\*\*\* Vivado v2018.2 (64-bit)  
 \*\*\*\* SW Build 2258646 on Thu Jun 14 20:02:38 MDT 2018  
 \*\*\*\* IP Build 2256618 on Thu Jun 14 22:10:49 MDT 2018  
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source next\_address.tcl -notrace  
Command: open\_checkpoint next\_address\_routed.dcp  
  
Starting open\_checkpoint Task  
  
Time (s): cpu = 00:00:00.06 ; elapsed = 00:00:00.23 . Memory (MB): peak = 1343.129 ; gain = 0.000 ; free physical = 89881 ; free virtual = 154345  
INFO: [Netlist 29-17] Analyzing 14 Unisim elements for replacement  
INFO: [Netlist 29-28] Unisim Transformation completed **in** 0 CPU seconds  
INFO: [Project 1-479] Netlist was created **with** Vivado 2018.2  
INFO: [Device 21-403] Loading part xc7a100tcsg324-1