Computer Architecture & Design

Coen 316

Lab Experiment #4 (part 1 and part 2)

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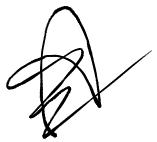
Section DN-X

Professor Dr. Fadi Alzouri

Performed on November 9, 2023

Due on November 23, 2023

“I certify that this submission is my original work and meets the Faculty’s Expectations of

Originality.”

**1) Introduction/Objectives**

In the last Computer Architecture & Design COEN 316 lab, students worked on developing a functional CPU using previous lab’s knowledge as well as other components. For example, some added crucial components are a Control Unit, I-Cache, D-Cache, Sign Extended, etc. With these, the main objective is to design, implemented and test the interactions and functionalities of a CPU.

**2) Theory**

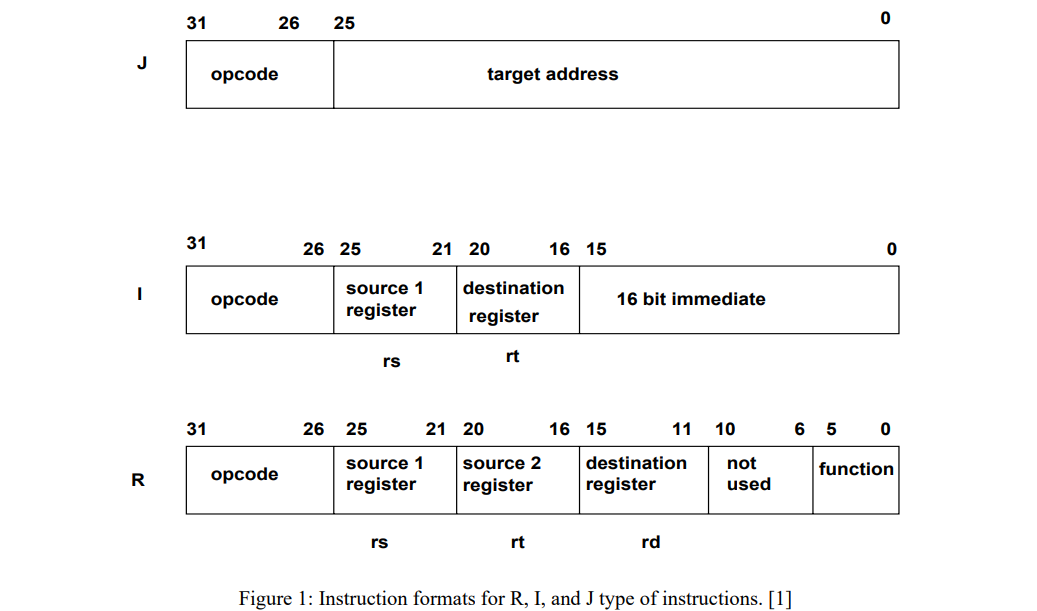


Figure 1 is the MIPS processor instructions where J is the Jump Instruction, I is the Immediate Instruction and R is the Register Instruction.

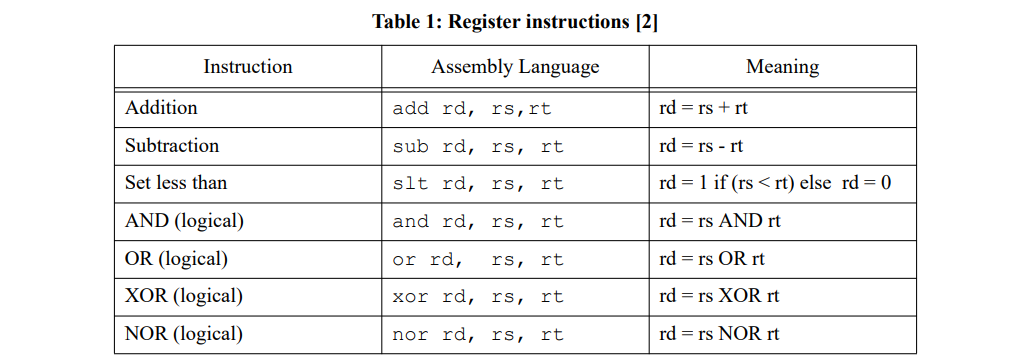


Table 1 is Register Instruction information containing the assembly code as well as its meaning. There is a total of 7 of them.

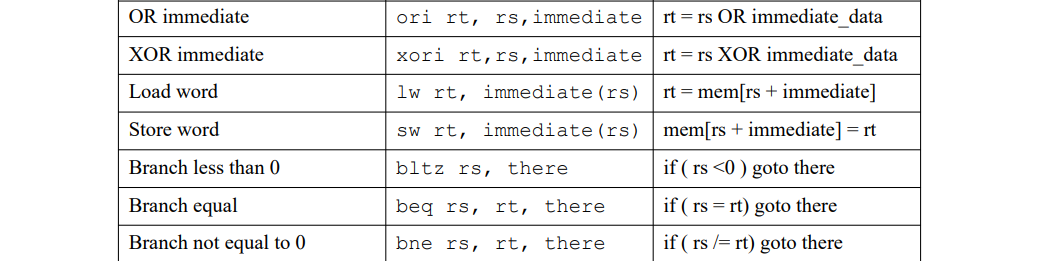
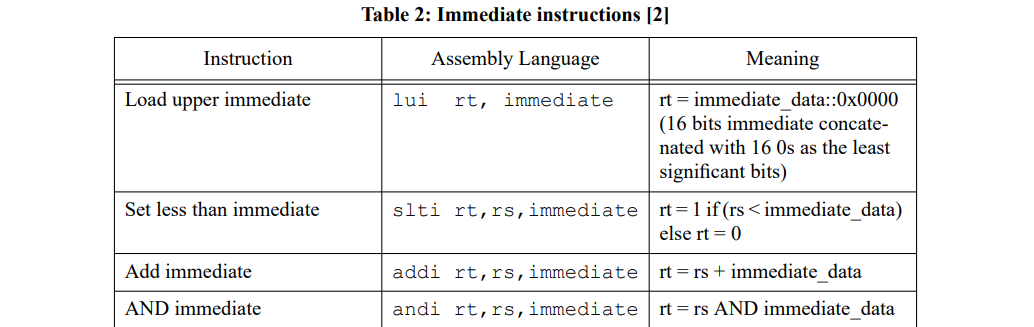


Table 2 is the Immediate Instruction which contains the assembly language code as well as its meaning. There is a total of 11 of them.

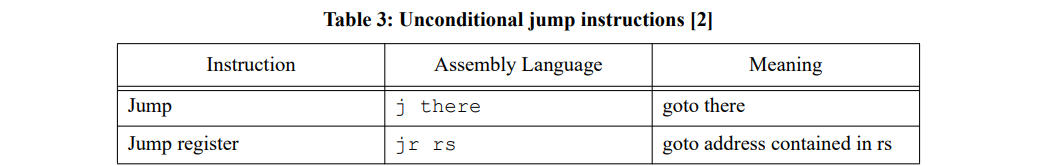
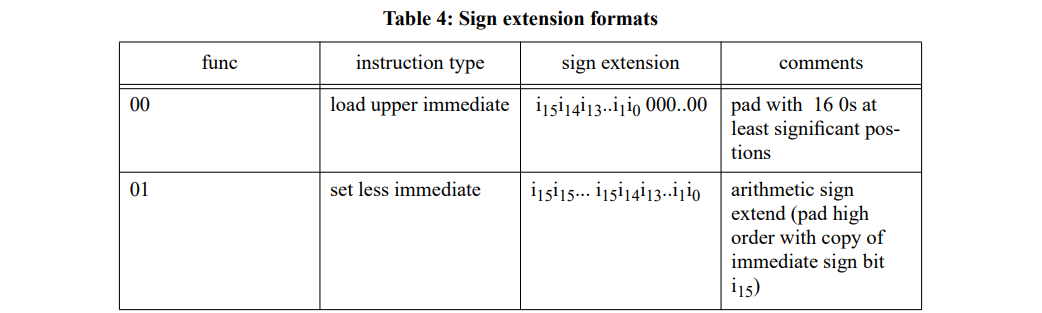
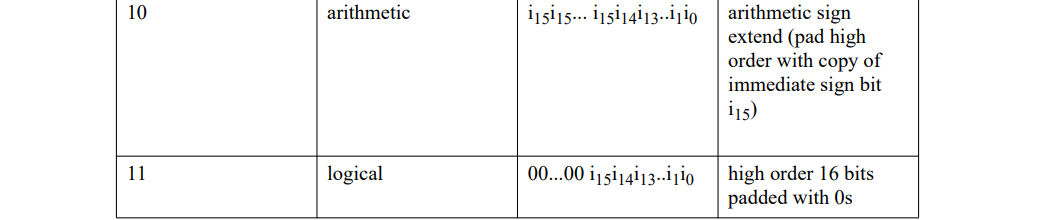
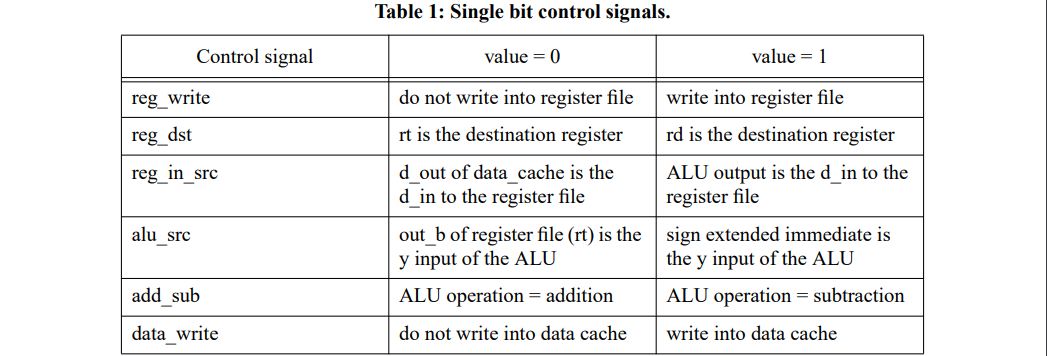


Table 3 is the remaining instruction for the initial 20. These two instructions represent the Jump Instructions and it has an assembly language code and its meaning.





The above table 4 represent the four functions for the sign extension component.



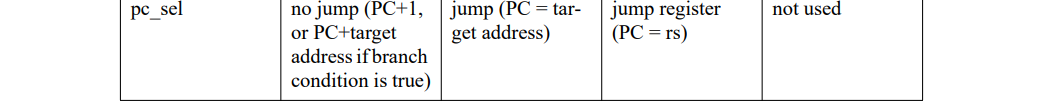
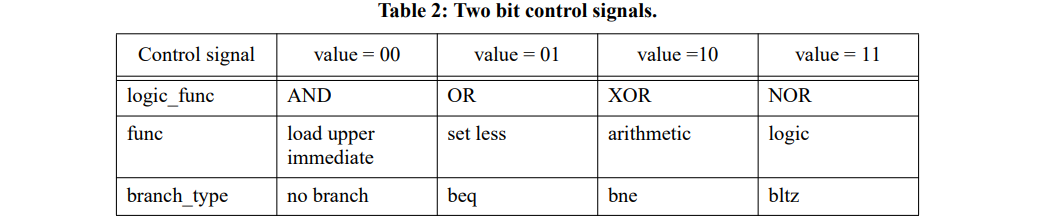
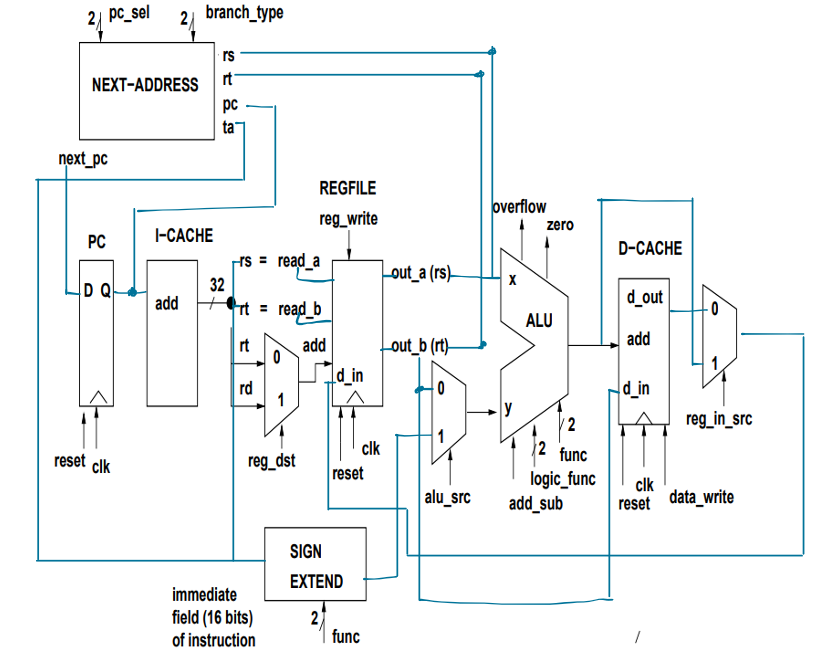


Table 1 and 2 belongs to lab 4 part 2 and they represent 10 control signals used by the function of the control unit. It has a summary of their operations.

**3) Tasks, Results and Discussion**

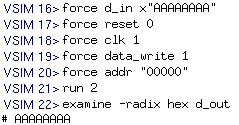
3.1) PART 1: CPU Datapath

CPU Datapath:



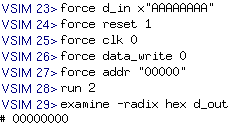
**3.1.1) Data Cache**

**3.1.1.1) Initialize Value**



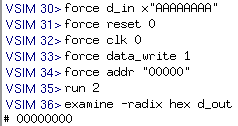
First step is to populate all values with rising edge clk and data\_write 1. Observe d\_out output corresponds to d\_in of AAAAAAAA.

**3.1.1.2) reset 1, clk 0 and data\_write 0**



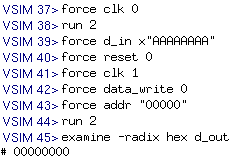
Testing the reset functionality. Result of 00000000 validates this functionality.

**3.1.1.3) data\_write 1, reset 0 and clk 0**



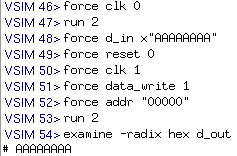
Testing the data\_write functionality without rising edge clk. Result of 00000000 validates this functionality.

**3.1.1.4) data\_write 0, reset 0 and clk 1**



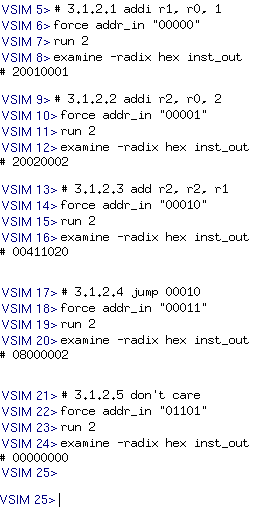
Testing the clk functionality without data\_write. Result of 00000000 validates this functionality.

**3.1.1.5) data\_write 1, reset 0 and clk 1**



Testing the clk functionality with data\_write. Result of AAAAAAAA validates this functionality.

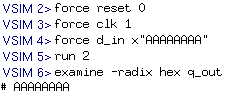
**3.1.2) Instruction Cache**



The i\_cache.vhd works as intended since when prompted for a address input of 5 bits such as 00000, the output inst\_out corresponds to the “hard-wired” program in machine code given in lab 4 part 1 manual.

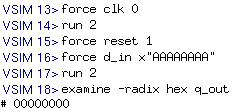
**3.1.3) PC**

**3.1.3.1) Initialize value**



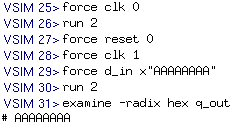
For pc.vhd, we first setup and initialize the values with these inputs. The current output is AAAAAAAA which corresponds to d\_in.

**3.1.3.2) reset 1, clk 0**



Testing the reset functionality. Given reset 1, the output q\_out will become 00000000.

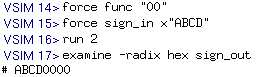
**3.1.3.3) reset 0, clk 1**



Testing the clk functionality. Given reset 0 and clk is a rising edge 1, the output will match d\_in.

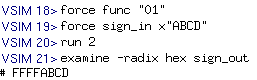
**3.1.4) Sign Extended**

**3.1.4.1) load upper immediate**



Correct behavior, the first 16 bits of sign\_out correspond to sign\_in while the rest are zeros.

**3.1.4.2) arithmetic sign extend (msb = 1)**



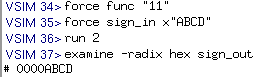
Correct behavior, the first 16 bits of sign\_out correspond to MSB of sign\_in which is 1, so FFFF, while the rest correspond to sign\_in ABCD.

**3.1.4.3) arithmetic sign extend (msb = 0)**



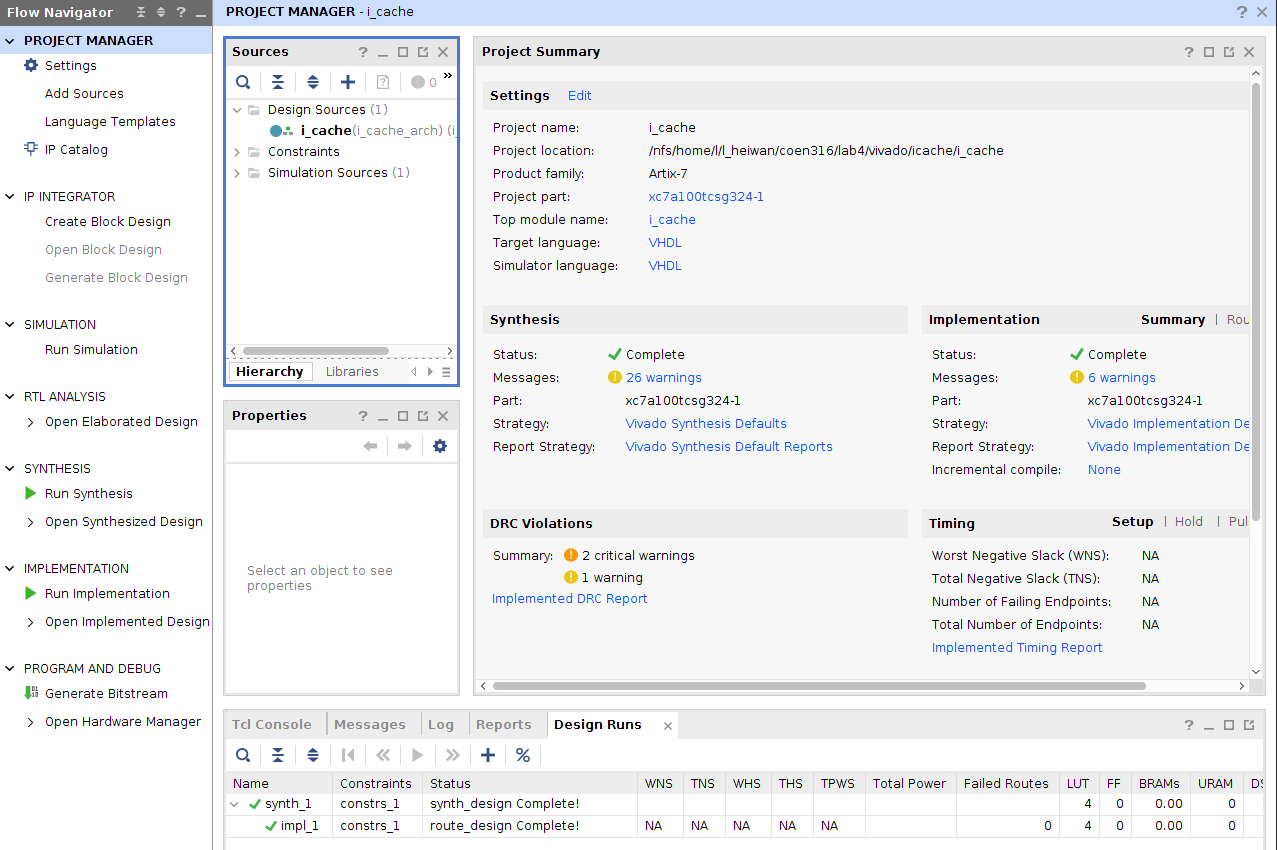
Correct behavior, the first 16 bits of sign\_out correspond to MSB of sign\_in which is 0, so 0000, while the rest correspond to sign\_in ABCD.

**3.1.4.4) logical**

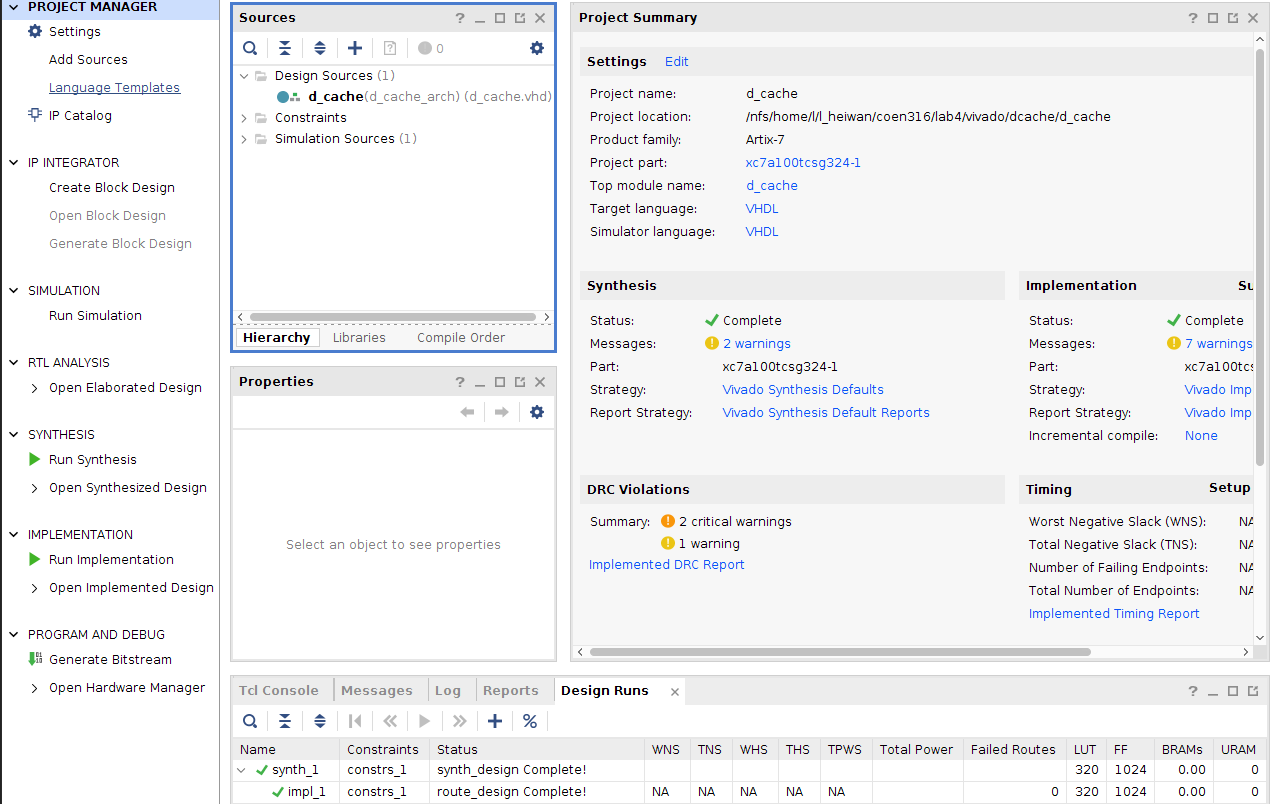


Correct behavior, the first 16 bits of sign\_out are all 0, while the rest correspond to sign\_in ABCD.

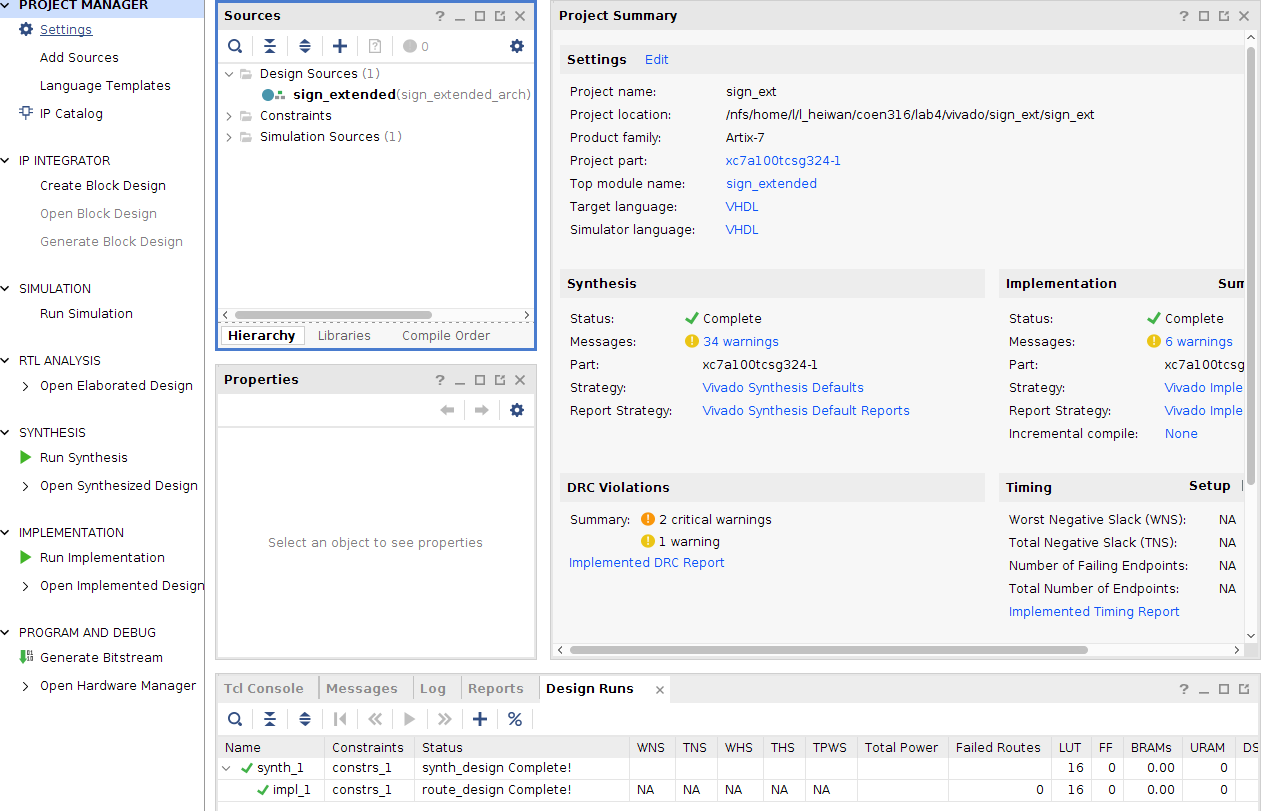
**3.1.5) Vivado Synthesis and Implementation (i\_cache, d\_cache and sign\_extended)**













**3.2) Part 2: Datapath/Control Unit Integration**

**20 Instructions with Opcode and Function Fields and Control Signals:**

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Inst. | Op | Func | Reg\_ write | Reg\_ dst | Reg\_ in\_src | Alu\_ src | Add\_ sub | Data\_ write | Logic\_ func | Func | Branch\_ type | Pc\_ sel |
| Lui | 001111 | 001111 | 1 | 0 | 1 | 1 | 0 (don’t care) | 0 | 00 (don’t care) | 00 | 00 | 00 |
| Add | 000000 | 100000 | 1 | 1 | 1 | 0 | 0 | 0 | 00 | 10 | 00 | 00 |
| Sub | 000000 | 100010 | 1 | 1 | 1 | 0 | 1 | 0 | 00 | 10 | 00 | 00 |
| Slt | 000000 | 101010 | 1 | 1 | 1 | 0 | 1 | 0 | 00 | 01 | 00 | 00 |
| Addi | 001000 | 001000 | 1 | 0 | 1 | 1 | 0 | 0 | 00 | 10 | 00 | 00 |
| Slti | 001010 | 001010 | 1 | 0 | 1 | 1 | 1 | 0 | 00 | 01 | 00 | 00 |
| And | 000000 | 100100 | 1 | 1 | 1 | 0 | 0 | 0 | 00 | 11 | 00 | 00 |
| Or | 000000 | 100101 | 1 | 1 | 1 | 0 | 0 | 0 | 01 | 11 | 00 | 00 |
| Xor | 000000 | 100110 | 1 | 1 | 1 | 0 | 0 | 0 | 10 | 11 | 00 | 00 |
| Nor | 000000 | 100111 | 1 | 1 | 1 | 0 | 0 | 0 | 11 | 11 | 00 | 00 |
| Andi | 001100 | 001100 | 1 | 0 | 1 | 1 | 0 | 0 | 00 | 11 | 00 | 00 |
| Ori | 001101 | 001101 | 1 | 0 | 1 | 1 | 0 | 0 | 01 | 11 | 00 | 00 |
| Xori | 001110 | 001110 | 1 | 0 | 1 | 1 | 0 | 0 | 10 | 11 | 00 | 00 |
| Lw | 100011 | 100011 | 1 | 0 | 0 | 1 | 0 | 0 | 10 (don’t care) | 10 | 00 | 00 |
| Sw | 101011 | 101011 | 0 | 0 | 0 | 1 | 0 | 1 | 00 | 10 | 00 | 00 |
| J | 000010 | 000010 | 0 | 0 | 0 | 0 | 0 | 0 | 00 | 00 | 00 | 01 |
| Jr | 000000 | 001000 | 0 | 0 | 0 | 0 | 0 | 0 | 00 | 00 | 00 | 10 |
| Bltz | 000001 | 000110 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 11 | 00 |
| Beq | 000100 | 000100 | 0 | 0 | 0 | 0 | 0 | 0 | 00 | 00 | 01 | 00 |
| bne | 000101 | 000101 | 0 | 0 | 0 | 0 | 0 | 0 | 00 | 00 | 10 | 00 |

Op: To distinguish among the different instructions.

Func: To distinguish among the different instructions.

Reg\_write: Determines which register is to be written into.

Reg\_dst: Determines rt field or rd field register to be written into.

Reg\_in\_src: Mux for ALU and d\_cache.

Alu\_src: Only signed values care, rest are 0.

Add\_sub: (lab 1) Only adder\_subtract care, rest are 0.

Data\_write: Active write signal.

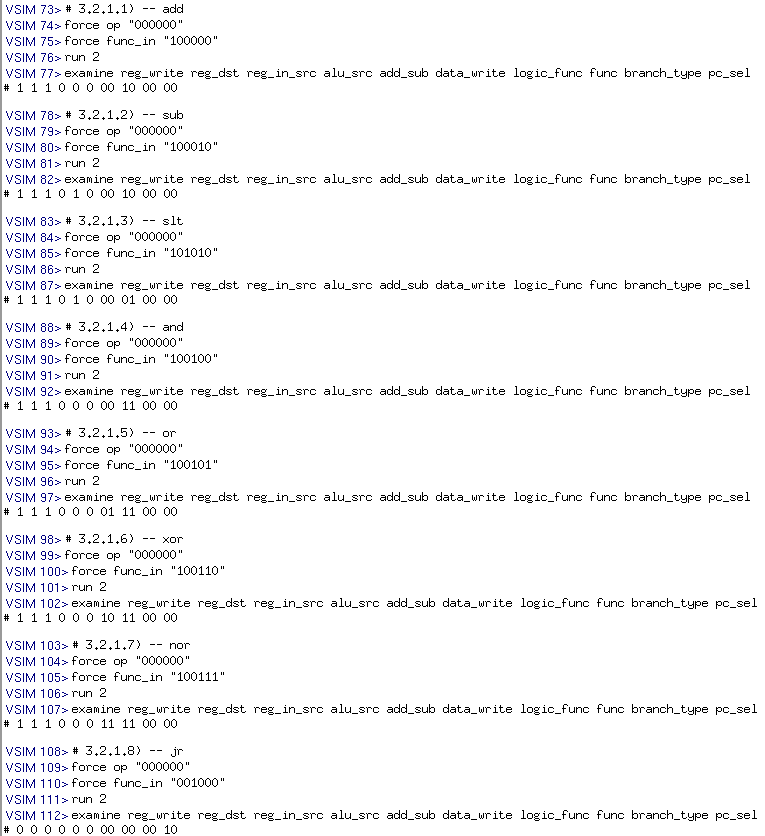
Logic\_func: (lab 1) Only logic unit care, rest are 00.

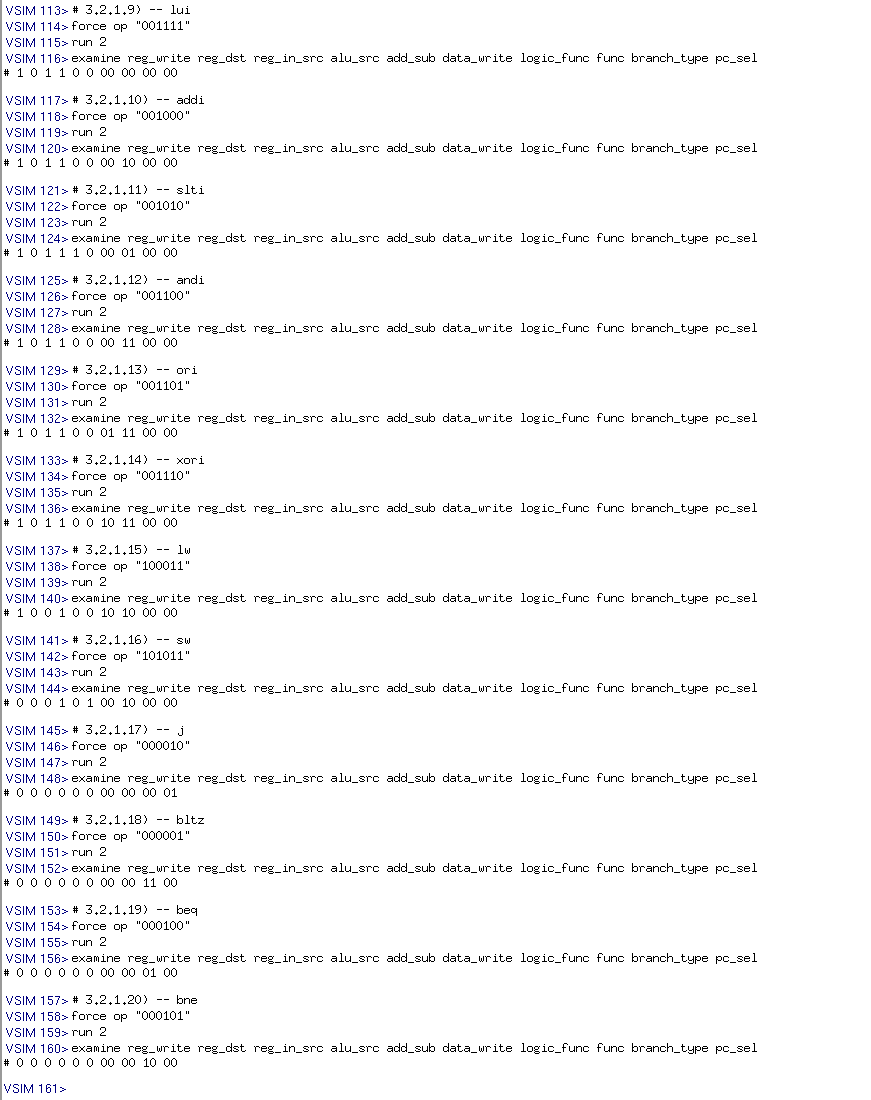
Func: (lab 1) Only lui, slt, adder\_substract and logic unit care, rest are 00.

Branch\_type: (lab 3) Only beq, bne and bltz care, rest are 00.

Pc\_sel: (lab 3) Only jump and jump register care, rest are 00.

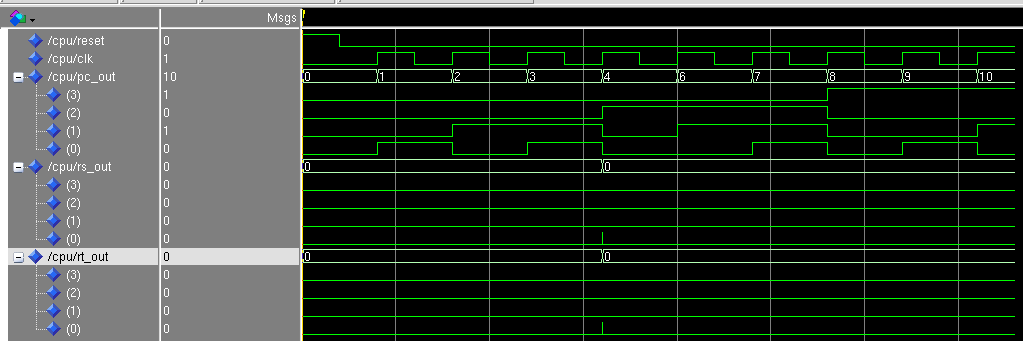
**3.2.1) Control Unit**



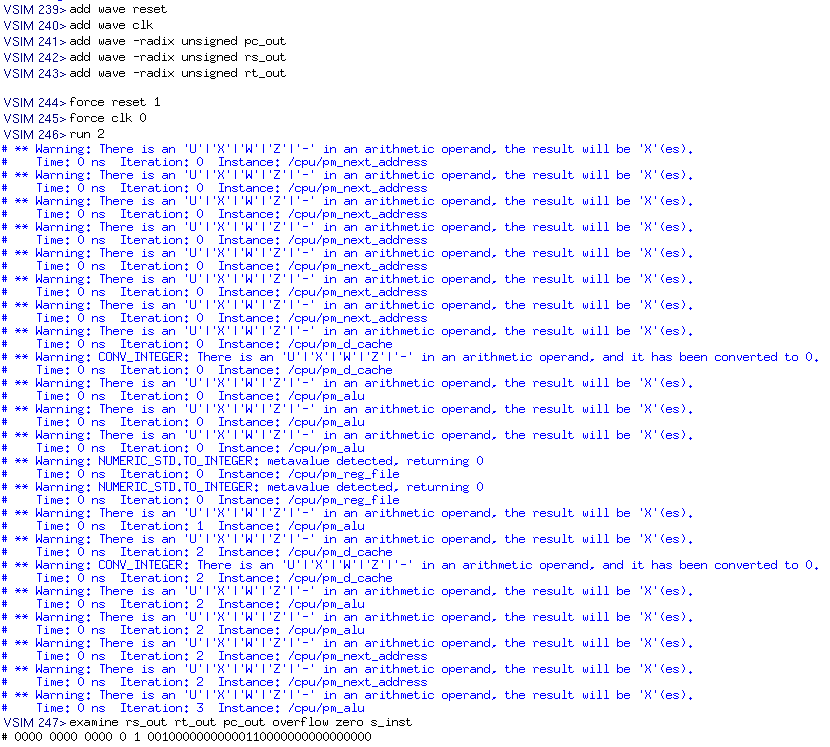


We tested the functionality of control\_unit,vhd by forcing op and func\_in values. By examining the output, we can observe that all 20 instructions match with the table.

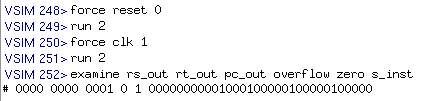
**3.2.2) CPU Datapath**



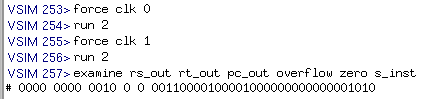
**3.2.2.1) Arithmetic (w/ imm operands)**



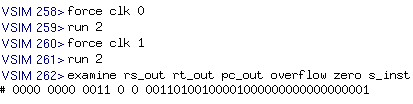
**3.2.2.2) Arithmetic (w/o imm operands)**



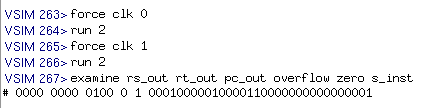
**3.2.2.3) Logic (w/ imm operands)**



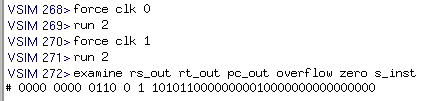
**3.2.2.4) Logic (w/o imm operands)**



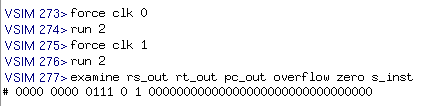
**3.2.2.5) Conditional branch**



**3.2.2.6) Memory access inst**



**3.2.2.7) Don’t care**



Given that rest is 0 and there is a rising edge clk, the cpu will run through each i\_cache machine code line. This can be seen from examine s\_inst which match the i\_cache machine code. For 3.2.2.7, the s\_inst is all zeros as there are no more command in the i\_cache. In this case the cpu will keep going outputting zeros.

**4) Conclusions**

In conclusion, lab 4 allowed for students to experiment on the intricacies of a CPU design through the usage of a CPU Datapath and subsequent components. By working progressively throughout lab 1 until now, students were able to deepen their understanding of CPU architecture. In the end, simulating and verifying the behavior of various instructions provided a comprehensive knowledge on computer architecture which is the main focus of the course COEN 316.

**5) Appendix**

**5.1) VHDL Code**

5.1.1) control\_unit.vhd

**library** IEEE;  
**use** IEEE.std\_logic\_1164.**all**;  
  
**entity** control\_unit **is**  
**port**(  
 op: **in** std\_logic\_vector(5 **downto** 0);  
 func\_in: **in** std\_logic\_vector(5 **downto** 0);  
 reg\_write: **out** std\_logic;  
 reg\_dst: **out** std\_logic;  
 reg\_in\_src: **out** std\_logic;  
 alu\_src: **out** std\_logic;  
 add\_sub: **out** std\_logic;  
 data\_write: **out** std\_logic;  
 logic\_func: **out** std\_logic\_vector(1 **downto** 0);  
 func: **out** std\_logic\_vector(1 **downto** 0);  
 branch\_type: **out** std\_logic\_vector(1 **downto** 0);  
 pc\_sel: **out** std\_logic\_vector(1 **downto** 0));  
**end** control\_unit;  
  
**architecture** control\_unit\_arch **of** control\_unit **is**  
  
**signal** control\_signals: std\_logic\_vector(13 **downto** 0);  
  
**begin**  
 **process**(op, func\_in, control\_signals)  
 **begin**   
 **case**(op) **is**  
 **when** "000000" =>  
 **case**(func\_in) **is**  
 **when** "100000" => control\_signals <= "11100000100000"; -- add  
 **when** "100010" => control\_signals <= "11101000100000"; -- sub  
 **when** "101010" => control\_signals <= "11101000010000"; -- slt  
 **when** "100100" => control\_signals <= "11100000110000"; -- and  
 **when** "100101" => control\_signals <= "11100001110000"; -- or  
 **when** "100110" => control\_signals <= "11100010110000"; -- xor  
 **when** "100111" => control\_signals <= "11100011110000"; -- nor  
 **when** "001000" => control\_signals <= "00000000000010"; -- jr  
 **when** **others** => control\_signals <= "00000000000000";  
 **end** **case**;  
 **when** "001111" => control\_signals <= "10110000000000"; -- lui  
 **when** "001000" => control\_signals <= "10110000100000"; -- addi  
 **when** "001010" => control\_signals <= "10111000010000"; -- slti  
 **when** "001100" => control\_signals <= "10110000110000"; -- andi  
 **when** "001101" => control\_signals <= "10110001110000"; -- ori  
 **when** "001110" => control\_signals <= "10110010110000"; -- xori  
 **when** "100011" => control\_signals <= "10010010100000"; -- lw  
 **when** "101011" => control\_signals <= "00010100100000"; -- sw  
 **when** "000010" => control\_signals <= "00000000000001"; -- j  
 **when** "000001" => control\_signals <= "00000000001100"; -- bltz  
 **when** "000100" => control\_signals <= "00000000000100"; -- beq  
 **when** "000101" => control\_signals <= "00000000001000"; -- bne  
 **when** **others** => control\_signals <= "00000000000000";  
 **end** **case**;  
   
 reg\_write <= control\_signals(13);  
 reg\_dst <= control\_signals(12);  
 reg\_in\_src <= control\_signals(11);  
 alu\_src <= control\_signals(10);  
 add\_sub <= control\_signals(9);  
 data\_write <= control\_signals(8);  
 logic\_func <= control\_signals(7 **downto** 6);  
 func <= control\_signals(5 **downto** 4);  
 branch\_type <= control\_signals(3 **downto** 2);  
 pc\_sel <= control\_signals(1 **downto** 0);  
 **end** **process**;   
**end** control\_unit\_arch;

5.1.2) cpu\_entity.vhd

-- coen 316 lab 4  
-- Andre Hei Wang Law  
-- 4017 5600  
  
**library** IEEE;  
**use** IEEE.std\_logic\_1164.**all**;  
**use** IEEE.std\_logic\_signed.**all**;  
  
**entity** cpu **is**  
**port**(reset: **in** std\_logic;  
 clk: **in** std\_logic;  
 rs\_out, rt\_out: **out** std\_logic\_vector(3 **downto** 0) := (**others** => '0'); -- output ports from reg. file  
 pc\_out: **out** std\_logic\_vector(3 **downto** 0) := (**others** => '0');  
 overflow, zero: **out** std\_logic);   
**end** cpu;  
  
**architecture** datapath\_cpu **of** cpu **is**  
-- initialize components  
 -- next address  
 **component** next\_address  
 **port**(  
 rt, rs: **in** std\_logic\_vector(31 **downto** 0);  
 pc: **in** std\_logic\_vector(31 **downto** 0);  
 target\_address: **in** std\_logic\_vector(25 **downto** 0);  
 branch\_type: **in** std\_logic\_vector(1 **downto** 0);  
 pc\_sel: **in** std\_logic\_vector(1 **downto** 0);  
 next\_pc: **out** std\_logic\_vector(31 **downto** 0));  
 **end** **component**;  
  
 -- pc  
 **component** pc  
 **port**(  
 reset: **in** std\_logic;  
 clk: **in** std\_logic;  
 d\_in: **in** std\_logic\_vector(31 **downto** 0) := (**others** => '0');  
 q\_out: **out** std\_logic\_vector(31 **downto** 0):= (**others** => '0'));  
 **end** **component**;  
  
 -- i\_cache  
 **component** i\_cache  
 **port**(  
 addr\_in: **in** std\_logic\_vector(4 **downto** 0);  
 inst\_out: **out** std\_logic\_vector(31 **downto** 0));  
 **end** **component**;  
  
 -- register file  
 **component** reg\_file  
 **port**(  
 din: **in** std\_logic\_vector(31 **downto** 0); -- data written to specific register  
 reset: **in** std\_logic; -- asynchronous active-high reset input  
 clk: **in** std\_logic; -- clock input  
 write: **in** std\_logic; -- write control signal  
 read\_a: **in** std\_logic\_vector(4 **downto** 0); -- address for read port A  
 read\_b: **in** std\_logic\_vector(4 **downto** 0); -- address for read port B  
 write\_address: **in** std\_logic\_vector(4 **downto** 0); -- address for write port  
 out\_a: **out** std\_logic\_vector(31 **downto** 0); -- data output for read port A  
 out\_b: **out** std\_logic\_vector(31 **downto** 0)); -- data output for read port B  
 **end** **component**;  
  
 -- alu  
 **component** alu  
 **port** (  
 x, y: **in** std\_logic\_vector(31 **downto** 0); -- two input operands  
 add\_sub: **in** std\_logic; -- 0=add, 1=sub  
 logic\_func: **in** std\_logic\_vector(1 **downto** 0); -- 00=AND, 01=OR, 10=XOR, 11=NOR  
 func: **in** std\_logic\_vector(1 **downto** 0); -- 00=lui, 01=setless, 10=arith, 11=logic  
 output: **out** std\_logic\_vector(31 **downto** 0);  
 overflow: **out** std\_logic;  
 zero: **out** std\_logic);  
 **end** **component**;  
  
 -- d\_cache  
 **component** d\_cache  
 **port**(  
 d\_in: **in** std\_logic\_vector(31 **downto** 0);  
 reset: **in** std\_logic;  
 clk: **in** std\_logic;  
 data\_write: **in** std\_logic;  
 addr: **in** std\_logic\_vector(4 **downto** 0);  
 d\_out: **out** std\_logic\_vector(31 **downto** 0));  
 **end** **component**;  
  
 -- sign extend  
 **component** sign\_ext  
 **port**(  
 func: **in** std\_logic\_vector(1 **downto** 0);  
 sign\_in: **in** std\_logic\_vector(15 **downto** 0);  
 sign\_out: **out** std\_logic\_vector(31 **downto** 0));  
 **end** **component**;  
  
 -- control unit  
 **component** control\_unit  
 **port**(  
 op: **in** std\_logic\_vector(5 **downto** 0);  
 func\_in: **in** std\_logic\_vector(5 **downto** 0);  
 reg\_write: **out** std\_logic;  
 reg\_dst: **out** std\_logic;  
 reg\_in\_src: **out** std\_logic;  
 alu\_src: **out** std\_logic;  
 add\_sub: **out** std\_logic;  
 data\_write: **out** std\_logic;  
 logic\_func: **out** std\_logic\_vector(1 **downto** 0);  
 func: **out** std\_logic\_vector(1 **downto** 0);  
 branch\_type: **out** std\_logic\_vector(1 **downto** 0);  
 pc\_sel: **out** std\_logic\_vector(1 **downto** 0));  
 **end** **component**;  
  
-- signals  
 -- control unit  
 --signal s\_op: std\_logic\_vector(5 downto 0);  
 --signal s\_func\_in: std\_logic\_vector(5 downto 0);  
 **signal** s\_reg\_write: std\_logic;  
 **signal** s\_reg\_dst: std\_logic;  
 **signal** s\_reg\_in\_src: std\_logic;  
 **signal** s\_alu\_src: std\_logic;  
 **signal** s\_add\_sub: std\_logic;  
 **signal** s\_data\_write: std\_logic;  
 **signal** s\_logic\_func: std\_logic\_vector(1 **downto** 0);  
 **signal** s\_func: std\_logic\_vector(1 **downto** 0);  
 **signal** s\_branch\_type: std\_logic\_vector(1 **downto** 0);  
 **signal** s\_pc\_sel: std\_logic\_vector(1 **downto** 0);  
   
 **signal** s\_inst: std\_logic\_vector(31 **downto** 0);  
   
 -- next address  
 **signal** s\_out\_a: std\_logic\_vector(31 **downto** 0);  
 **signal** s\_out\_b: std\_logic\_vector(31 **downto** 0);  
 **signal** s\_pc: std\_logic\_vector(31 **downto** 0);  
 **signal** s\_next\_pc: std\_logic\_vector(31 **downto** 0);  
   
 -- pc  
  
 -- i\_cache  
  
 -- register file  
 **signal** s\_reg\_in\_src\_out: std\_logic\_vector(31 **downto** 0);  
 **signal** s\_reg\_dst\_out: std\_logic\_vector(4 **downto** 0);  
  
 -- alu  
 **signal** s\_alu\_src\_out: std\_logic\_vector(31 **downto** 0);  
 **signal** s\_alu: std\_logic\_vector(31 **downto** 0);  
  
 -- d\_cache  
 **signal** s\_d\_out: std\_logic\_vector(31 **downto** 0);  
  
 -- sign extend  
 **signal** s\_sign\_out: std\_logic\_vector(31 **downto** 0);  
  
 -- FOR pm\_pc : "component\_name" USE ENTITY work."entity\_name" ("architecutre\_name");  
 **FOR** pm\_pc : pc **USE** **ENTITY** work.pc (pc\_arch);  
 **FOR** pm\_i\_cache : i\_cache **USE** **ENTITY** work.i\_cache(i\_cache\_arch);  
 **FOR** pm\_reg\_file : reg\_file **USE** **ENTITY** work.regfile (reg\_arch);  
 **FOR** pm\_alu : alu **USE** **ENTITY** work.alu(arith\_logic\_unit);  
 **FOR** pm\_d\_cache : d\_cache **USE** **ENTITY** work.d\_cache(d\_cache\_arch);  
 **FOR** pm\_sign\_ext : sign\_ext **USE** **ENTITY** work.sign\_extended(sign\_extended\_arch);  
 **FOR** pm\_next\_address : next\_address **USE** **ENTITY** work.next\_address(unit);  
 **FOR** pm\_control\_unit : control\_unit **USE** **ENTITY** work.control\_unit(control\_unit\_arch);  
  
**begin**  
 -- port map  
 pm\_pc: pc **port** **map**( -- pc  
 reset => reset,  
 clk => clk,  
 d\_in => s\_next\_pc,  
 q\_out => s\_pc  
 );  
   
 pm\_i\_cache: i\_cache **port** **map**( -- i\_cache  
 addr\_in => s\_pc(4 **downto** 0),  
 inst\_out => s\_inst  
 );  
   
 pm\_reg\_file: reg\_file **port** **map**( -- reg\_file  
 din => s\_reg\_in\_src\_out,  
 reset => reset,  
 clk => clk,  
 write => s\_reg\_write,  
 read\_a => s\_inst(25 **downto** 21),  
 read\_b => s\_inst(20 **downto** 16),  
 write\_address => s\_reg\_dst\_out,  
 out\_a => s\_out\_a,  
 out\_b => s\_out\_b  
 );  
   
 pm\_alu: alu **port** **map**( -- alu  
 x => s\_out\_a,  
 y => s\_alu\_src\_out,  
 add\_sub => s\_add\_sub,  
 logic\_func => s\_logic\_func,  
 func => s\_func,  
 output => s\_alu,  
 overflow => overflow,  
 zero => zero  
 );  
   
 pm\_d\_cache: d\_cache **port** **map**( -- d\_cache  
 d\_in => s\_out\_b,  
 reset => reset,  
 clk => clk,  
 data\_write => s\_data\_write,  
 addr => s\_alu(4 **downto** 0),  
 d\_out => s\_d\_out  
 );  
   
 pm\_sign\_ext: sign\_ext **port** **map**( -- sign\_ext  
 func => s\_func,  
 sign\_in => s\_inst(15 **downto** 0),  
 sign\_out => s\_sign\_out  
 );  
   
 pm\_next\_address: next\_address **port** **map**( -- next address  
 rt => s\_out\_b,  
 rs => s\_out\_a,  
 pc => s\_pc,  
 target\_address => s\_inst(25 **downto** 0),  
 branch\_type => s\_branch\_type,  
 pc\_sel => s\_pc\_sel,  
 next\_pc => s\_next\_pc  
 );  
   
 pm\_control\_unit: control\_unit **port** **map**( -- control\_unit  
 op => s\_inst(31 **downto** 26),  
 func\_in => s\_inst(5 **downto** 0),  
 reg\_write => s\_reg\_write,  
 reg\_dst => s\_reg\_dst,  
 reg\_in\_src => s\_reg\_in\_src,  
 alu\_src => s\_alu\_src,  
 add\_sub => s\_add\_sub,  
 data\_write => s\_data\_write,  
 logic\_func => s\_logic\_func,  
 func => s\_func,  
 branch\_type => s\_branch\_type,  
 pc\_sel => s\_pc\_sel  
 );  
   
 s\_reg\_dst\_out <= s\_inst(20 **downto** 16) **when** (s\_reg\_dst = '0') **else**  
 s\_inst(15 **downto** 11) **when** (s\_reg\_dst = '1');  
   
 s\_alu\_src\_out <= s\_out\_b **when** (s\_alu\_src = '0') **else**  
 s\_sign\_out **when** (s\_alu\_src = '1');  
 s\_reg\_in\_src\_out <= s\_d\_out **when** (s\_reg\_in\_src = '0') **else**  
 s\_alu **when** (s\_reg\_in\_src = '1');  
   
 rs\_out <= s\_out\_a(3) & s\_out\_a(2) & s\_out\_a(1) & s\_out\_a(0);  
 rt\_out <= s\_out\_b(3) & s\_out\_b(2) & s\_out\_b(1) & s\_out\_b(0);  
 pc\_out <= s\_pc(3) & s\_pc(2) & s\_pc(1) & s\_pc(0);  
   
**end** datapath\_cpu;

5.1.3) d\_cache.vhd

**library** IEEE;  
**use** IEEE.std\_logic\_1164.**all**;  
**use** IEEE.std\_logic\_unsigned.**all**;  
  
**entity** d\_cache **is**  
**port**(  
 d\_in: **in** std\_logic\_vector(31 **downto** 0);  
 reset: **in** std\_logic;  
 clk: **in** std\_logic;  
 data\_write: **in** std\_logic;  
 addr: **in** std\_logic\_vector(4 **downto** 0);  
 d\_out: **out** std\_logic\_vector(31 **downto** 0));  
**end** d\_cache;  
  
**architecture** d\_cache\_arch **of** d\_cache **is**  
   
 **type** reg\_array **is** **array** (0 **to** 31) **of** std\_logic\_vector(31 **downto** 0); -- 32 reg, each 32 bits  
 **signal** registers : reg\_array;   
   
**begin**  
 **process**(reset, clk)  
 **begin**  
 **if** (reset = '1') **then** -- reset (asynchronous)   
 registers <= (**others** => (**others** => '0')); -- clear all reg. zeros  
 **elsif** (rising\_edge(clk) **and** data\_write ='1') **then** -- click (synchronous), rising edge  
 registers(conv\_integer(addr)) <= d\_in; -- write   
 **end** **if**;  
 **end** **process**;  
  
 **process**(addr, registers)  
 **begin**  
 d\_out <= registers(conv\_integer(addr)); -- read data from addr  
 **end** **process**;  
   
**end** d\_cache\_arch;

5.1.4) i\_cache.vhd

library IEEE;  
use IEEE.std\_logic\_1164.all;  
  
entity i\_cache is  
port(  
 addr\_in: **in** std\_logic\_vector(4 **downto** 0);  
 inst\_out: out std\_logic\_vector(31 **downto** 0));  
**end** i\_cache;  
  
architecture i\_cache\_arch **of** i\_cache is  
**begin**  
 process(addr\_in)  
 **begin**  
 case(addr\_in) is  
 --**when** "00000" => inst\_out <= "00100000000000110000000000000000"; -- addi r3, r0, 0  
 --**when** "00001" => inst\_out <= "00100000000000010000000000000000"; -- addi r1, r0, 0  
 --**when** "00010" => inst\_out <= "00100000000000100000000000000101"; -- addi r2,r0,5  
 --**when** "00011" => inst\_out <= "00000000001000100000100000100000"; -- add r1,r1,r2  
 --**when** "00100" => inst\_out <= "00100000010000101111111111111111"; -- addi r2, r2, -1  
 --**when** "00101" => inst\_out <= "00010000010000110000000000000001"; -- beq r2,r3 (+1) THERE  
 --**when** "00110" => inst\_out <= "00001000000000000000000000000011"; -- jump 3 (LOOP)  
 --**when** "00111" => inst\_out <= "10101100000000010000000000000000"; -- sw r1, 0(r0)   
 --**when** "01000" => inst\_out <= "10001100000001000000000000000000"; -- lw r4, 0(r0)  
 --**when** "01001" => inst\_out <= "00110000100001000000000000001010"; -- andi r4,r4, 0x000A  
 --**when** "01010" => inst\_out <= "00110100100001000000000000000001"; -- ori r4,r4, 0x0001  
 --**when** "01011" => inst\_out <= "00111000100001000000000000001011"; -- xori r4,r4, 0xB  
 --**when** "01100" => inst\_out <= "00111000100001000000000000000000"; -- xori r4,r4, 0x0000  
   
 -- values based on "machine\_code.txt" found from TED's directory  
 **when** "00000" => inst\_out <= "00100000000000110000000000000000"; -- arithmetic (w/ imm operands), addi r3, r0, 0  
 **when** "00001" => inst\_out <= "00000000001000100000100000100000"; -- arithmetic (w/o imm operands), add r1,r1,r2  
 **when** "00010" => inst\_out <= "00110000100001000000000000001010"; -- logic (w/ imm operands), andi r4,r4, 0x000A  
 **when** "00011" => inst\_out <= "00110100100001000000000000000001"; -- logic (w/o imm operands), ori r4,r4, 0x0001  
 **when** "00100" => inst\_out <= "00010000010000110000000000000001"; -- conditional branch, beq r2,r3 (+1) THERE  
 **when** "00101" => inst\_out <= "00001000000000000000000000000100"; -- unconditional jump, jump 3 (LOOP)  
 **when** "00110" => inst\_out <= "10101100000000010000000000000000"; -- memory access inst, sw r1, 0(r0)   
 **when** others => inst\_out <= "00000000000000000000000000000000"; -- dont care  
 **end** case;  
 **end** process;  
**end** i\_cache\_arch;

5.1.5) lab1\_alu.vhd

-- coen 316 lab1  
-- Andre Hei Wang Law  
-- 4017 5600  
  
**library** IEEE;  
**use** IEEE.std\_logic\_1164.**all**;  
**use** ieee.std\_logic\_signed.**all**;  
  
**entity** alu **is**  
 **port** (  
 x, y: **in** std\_logic\_vector(31 **downto** 0); -- two input operands  
 add\_sub: **in** std\_logic; -- 0=add, 1=sub  
 logic\_func: **in** std\_logic\_vector(1 **downto** 0); -- 00=AND, 01=OR, 10=XOR, 11=NOR  
 func: **in** std\_logic\_vector(1 **downto** 0); -- 00=lui, 01=setless, 10=arith, 11=logic  
 output: **out** std\_logic\_vector(31 **downto** 0);  
 overflow: **out** std\_logic;  
 zero: **out** std\_logic);  
**end** alu;  
  
**architecture** arith\_logic\_unit **of** alu **is**  
-- signal   
**signal** adder\_subtract\_output, logic\_unit\_output: std\_logic\_vector(31 **downto** 0);  
**begin**  
 -- adder\_subtract (add\_sub)  
 **process**(x, y, add\_sub)  
 **begin**  
 -- check for addition or substraction  
 **if** (add\_sub = '0') **then**  
 adder\_subtract\_output <= x + y; -- addition  
 **else**  
 adder\_subtract\_output <= x - y; -- substraction  
 **end** **if**;  
 **end** **process**;  
  
 -- LINE 40  
 -- logic unit (logic\_func)  
 **process**(x, y, logic\_func)  
 **begin**  
 **case** logic\_func **is**  
 **when** "00" =>  
 logic\_unit\_output <= x **AND** y; -- AND  
 **when** "01" =>  
 logic\_unit\_output <= x **OR** y; -- OR  
 **when** "10" =>  
 logic\_unit\_output <= x **XOR** y; -- XOR  
 **when** **others** =>  
 logic\_unit\_output <= **not** (x **OR** y); -- NOR  
 **end** **case**;  
 **end** **process**;  
  
 -- mux (func)  
 **process**(y, adder\_subtract\_output, logic\_unit\_output, func)  
 **begin**  
 -- determines output  
 **case** func **is**  
 **when** "00" =>  
 output <= y; -- y  
 **when** "01" =>  
 -- output = 1 if x < y   
 -- output = 0 otherwise  
 -- “000...MSB” of adder\_subtract  
 output <= "0000000000000000000000000000000" & adder\_subtract\_output(31);  
 **when** "10" =>  
 output <= adder\_subtract\_output; -- output of adder\_subtract  
 **when** **others** =>  
 output <= logic\_unit\_output; -- output of logic unit  
 **end** **case**;  
 **end** **process**;  
  
 -- zero  
 **process**(adder\_subtract\_output)  
 **begin**  
 -- zero = 1 when output of the adder\_subtract unit is all 0s  
 -- zero = 0 otherwise  
 **if** adder\_subtract\_output = "00000000000000000000000000000000" **then**  
 zero <= '1';  
 **else**  
 zero <= '0';  
 **end** **if**;  
 **end** **process**;  
  
 -- overflow  
 **process**(adder\_subtract\_output, add\_sub, x, y)  
 **begin**  
 -- overflow = 1 when:   
 -- 1. Adding two positive num (x + y) and a negative result is obtained  
 -- 2. Adding two negative numbers (-x + -y) and a possitive result is obtained  
 -- 3. Substracting two operands of opposite sign (-x - y)   
 -- 4. Substracting two operands of opposite sign (x - -y)  
   
 -- 1. and 2. Addition  
 **if** add\_sub = '0' **then**  
 **if** (x(31) = '0' **and** y(31) = '0' **and** adder\_subtract\_output(31) = '1') **or**  
 (x(31) = '1' **and** y(31) = '1' **and** adder\_subtract\_output(31) = '0') **then**  
 overflow <= '1'; -- Overflow detected  
 **else**  
 overflow <= '0'; -- No overflow  
 **end** **if**;  
 --overflow <= (not(x(31)) AND not(y(31)) AND adder\_subtract\_output(31)) OR (x(31) AND y(31) AND not(adder\_subtract\_output(31)));  
   
 -- 3. and 4. Substraction  
 **elsif** add\_sub = '1' **then**  
 **if** (x(31) = '0' **and** y(31) = '1' **and** adder\_subtract\_output(31) = '1') **or**  
 (x(31) = '1' **and** y(31) = '0' **and** adder\_subtract\_output(31) = '0') **then**  
 overflow <= '1'; -- Overflow detected  
 **else**  
 overflow <= '0'; -- No overflow  
 **end** **if**;  
 --overflow <= (x(31) AND not(y(31)) AND not(adder\_subtract\_output(31))) OR (not(x(31)) AND y(31) AND adder\_subtract\_output(31));  
 **end** **if**;  
 **end** **process**;  
**end** arith\_logic\_unit;

5.1.6) lab2\_register\_file.vhd

-- coen 316 lab 2  
-- Andre Hei Wang Law  
-- 4017 5600  
  
**library** IEEE;  
**use** IEEE.std\_logic\_1164.**all**;  
**use** IEEE.std\_logic\_unsigned.**all**;  
**use** IEEE.numeric\_std.**all**;  
  
**entity** regfile **is**  
 **port** (  
 din: **in** std\_logic\_vector(31 **downto** 0); -- data written to specific register  
 reset: **in** std\_logic; -- asynchronous active-high reset input  
 clk: **in** std\_logic; -- clock input  
 write: **in** std\_logic; -- write control signal  
 read\_a: **in** std\_logic\_vector(4 **downto** 0); -- address for read port A  
 read\_b: **in** std\_logic\_vector(4 **downto** 0); -- address for read port B  
 write\_address: **in** std\_logic\_vector(4 **downto** 0); -- address for write port  
 out\_a: **out** std\_logic\_vector(31 **downto** 0); -- data output for read port A  
 out\_b: **out** std\_logic\_vector(31 **downto** 0)); -- data output for read port B  
**end** regfile;  
  
**architecture** reg\_arch **of** regfile **is**  
 **type** reg\_array **is** **array** (0 **to** 31) **of** std\_logic\_vector(31 **downto** 0); -- 32 reg, each 32 bits  
 **signal** registers : reg\_array; -- register file, all zeros  
**begin**  
 **process**(reset, clk, write)  
 **begin**  
 **if** (reset = '1') **then** -- reset (asynchronous)   
 registers <= (**others** => (**others** => '0')); -- clear all reg. zeros  
 **elsif** (clk'event **and** clk='1') **then** -- click (synchronous), rising edge  
 **if** (write = '1') **then** -- check for active write signal  
 registers(to\_integer(unsigned(write\_address))) <= din; -- write   
 **end** **if**;  
 **end** **if**;  
 **end** **process**;  
 -- reading (asynchronous)  
 **process**(read\_a, read\_b, registers)  
 **begin**  
 out\_a <= registers(to\_integer(unsigned(read\_a))); -- read data from read\_a  
 out\_b <= registers(to\_integer(unsigned(read\_b))); -- read data from read\_b  
 **end** **process**;  
**end** **architecture** reg\_arch;

5.1.7) lab3\_next\_addr.vhd

-- coen 316 lab 3  
-- Andre Hei Wang Law  
-- 4017 5600  
  
**library** IEEE;  
**use** IEEE.std\_logic\_1164.**all**;  
**use** IEEE.std\_logic\_signed.**all**;  
  
**entity** next\_address **is**  
**port**(  
 -- inputs  
 rt, rs: **in** std\_logic\_vector(31 **downto** 0);  
 pc: **in** std\_logic\_vector(31 **downto** 0);  
 target\_address: **in** std\_logic\_vector(25 **downto** 0);  
 branch\_type: **in** std\_logic\_vector(1 **downto** 0);  
 pc\_sel: **in** std\_logic\_vector(1 **downto** 0);  
 -- output  
 next\_pc: **out** std\_logic\_vector(31 **downto** 0));  
**end** next\_address;  
  
**architecture** unit **of** next\_address **is**  
  
-- signal  
**signal** tar\_addr\_signed\_32: std\_logic\_vector(31 **downto** 0);  
**signal** branch\_offset\_signed\_32: std\_logic\_vector(31 **downto** 0);  
**signal** branch\_offset: std\_logic\_vector(31 **downto** 0);  
  
**begin**  
 -- calculate "pseudo-direct" addressing to fill entire 32 bit  
 -- target address for "jump" instructions  
 tar\_addr\_signed\_32(31 **downto** 26) <= (**others** => target\_address(25)); -- fill with ones or zeros  
 tar\_addr\_signed\_32(25 **downto** 0) <= target\_address; -- fill the rest   
   
 -- branch offset for no unconditional jump instructions  
 branch\_offset\_signed\_32(31 **downto** 16) <= (**others** => target\_address(15)); -- fill with ones or zeros  
 branch\_offset\_signed\_32(15 **downto** 0) <= target\_address(15 **downto** 0); -- fill the rest   
  
 -- PC\_sel functionality  
 **process**(pc\_sel, rs, branch\_offset, pc, tar\_addr\_signed\_32)  
 **begin**  
 **if** (pc\_sel = "00") **then** -- no unconditional jump  
 next\_pc <= branch\_offset + pc + 1;  
 **elsif** (pc\_sel = "01") **then** -- jump  
 next\_pc <= tar\_addr\_signed\_32;  
 **elsif** (pc\_sel = "10") **then** -- jump register  
 next\_pc <= rs;  
 **elsif** (pc\_sel = "11") **then** -- not used  
 -- do nothing  
 **end** **if**;  
 **end** **process**;  
   
 -- branch\_type functionality  
 **process**(branch\_type, rs, rt, branch\_offset, branch\_offset\_signed\_32)  
 **begin**  
 **if** (branch\_type = "00") **then** -- no branch  
 branch\_offset <= (**others** => '0');  
 **elsif** (branch\_type = "01") **then** -- beq (equal to 0)  
 **if** (rs = rt) **then**  
 branch\_offset <= branch\_offset\_signed\_32;  
 **else**  
 branch\_offset <= (**others** => '0');  
 **end** **if**;  
 **elsif** (branch\_type = "10") **then** -- bne (not equal to 0)  
 **if** (rs /= rt) **then**  
 branch\_offset <= branch\_offset\_signed\_32;  
 **else**  
 branch\_offset <= (**others** => '0');  
 **end** **if**;  
 **elsif** (branch\_type = "11") **then** -- bltz (less then 0)  
 **if** (rs(31) = '1') **then** -- means rs is negative, or < 0  
 branch\_offset <= branch\_offset\_signed\_32;  
 **else**  
 branch\_offset <= (**others** => '0');  
 **end** **if**;  
 **end** **if**;  
 **end** **process**;  
**end** unit;

5.1.8) pc.vhd

**library** IEEE;  
**use** IEEE.std\_logic\_1164.**all**;  
**use** IEEE.std\_logic\_signed.**all**;  
  
**entity** pc **is**  
**port**(  
 reset: **in** std\_logic;  
 clk: **in** std\_logic;  
 d\_in: **in** std\_logic\_vector(31 **downto** 0);  
 q\_out: **out** std\_logic\_vector(31 **downto** 0));  
**end** pc;  
  
**architecture** pc\_arch **of** pc **is**  
**begin**  
 **process**(reset, clk)  
 **begin**  
 **if** (reset = '1') **then** -- reset (asynchronous)   
 q\_out <= (**others** => '0'); -- clear all   
 **elsif** (clk'event **and** clk='1') **then** -- click (synchronous), rising edge  
 q\_out <= d\_in;  
 **end** **if**;  
 **end** **process**;  
**end** pc\_arch;

5.1.9) sign\_extended.vhd

**library** IEEE;  
**use** IEEE.std\_logic\_1164.**all**;  
**use** IEEE.std\_logic\_signed.**all**;  
  
**entity** sign\_extended **is**  
**port**(  
 func: **in** std\_logic\_vector(1 **downto** 0);  
 sign\_in: **in** std\_logic\_vector(15 **downto** 0);  
 sign\_out: **out** std\_logic\_vector(31 **downto** 0));  
**end** sign\_extended;  
  
**architecture** sign\_extended\_arch **of** sign\_extended **is**  
  
**begin**  
 -- mux (func)  
 **process**(sign\_in, func)  
 **begin**  
 **case**(func) **is**  
 **when** "00" =>   
 sign\_out(31 **downto** 16) <= sign\_in; -- load upper immediate  
 sign\_out(15 **downto** 0) <= (**others** => '0');  
 **when** "01" =>   
 sign\_out(31 **downto** 16) <= (**others** => sign\_in(15)); -- sign extend  
 sign\_out(15 **downto** 0) <= sign\_in; -- fill rest  
 **when** "10" =>   
 sign\_out(31 **downto** 16) <= (**others** => sign\_in(15)); -- sign extend  
 sign\_out(15 **downto** 0) <= sign\_in; -- fill rest  
 **when** **others** =>   
 sign\_out(31 **downto** 16) <= (**others** => '0'); -- logical  
 sign\_out(15 **downto** 0) <= sign\_in;  
 **end** **case**;  
 **end** **process**;  
   
**end** sign\_extended\_arch;

**5.2) Constrain .xdc File**

# Ted Obuchowicz  
# XDC file for complete CPU  
  
set\_property **CLOCK\_DEDICATED\_ROUTE**  FALSE [ get\_nets clk ] ;  
  
# set the reset to the left most switch  
  
set\_property -**dict** { PACKAGE\_PIN V10 IOSTANDARD LVCMOS33 } [ get\_ports { reset } ] ;  
  
# use the centre pushbutton as the clock  
  
set\_property -**dict** { PACKAGE\_PIN N17 IOSTANDARD LVCMOS33 } [ get\_ports { clk } ] ;  
  
  
# set pc\_out to left hand LEDS   
  
set\_property -**dict** { PACKAGE\_PIN V11 IOSTANDARD LVCMOS33 } [ get\_ports { pc\_out[3] } ] ;  
set\_property -**dict** { PACKAGE\_PIN V12 IOSTANDARD LVCMOS33 } [ get\_ports { pc\_out[2] } ] ;  
set\_property -**dict** { PACKAGE\_PIN V14 IOSTANDARD LVCMOS33 } [ get\_ports { pc\_out[1] } ] ;  
set\_property -**dict** { PACKAGE\_PIN V15 IOSTANDARD LVCMOS33 } [ get\_ports { pc\_out[0] } ] ;  
  
# set overflow and zero immediately after pc\_out  
  
set\_property -**dict** { PACKAGE\_PIN T16 IOSTANDARD LVCMOS33 } [ get\_ports { overflow } ] ;  
set\_property -**dict** { PACKAGE\_PIN U14 IOSTANDARD LVCMOS33 } [ get\_ports { zero } ] ;  
  
  
# set rs\_out and rt\_out to the right hand LEDS with a gap between the two  
  
# rs\_out  
set\_property -**dict** { PACKAGE\_PIN V16 IOSTANDARD LVCMOS33 } [ get\_ports { rs\_out[3] } ] ;  
set\_property -**dict** { PACKAGE\_PIN U16 IOSTANDARD LVCMOS33 } [ get\_ports { rs\_out[2] } ] ;  
set\_property -**dict** { PACKAGE\_PIN U17 IOSTANDARD LVCMOS33 } [ get\_ports { rs\_out[1] } ] ;  
set\_property -**dict** { PACKAGE\_PIN V17 IOSTANDARD LVCMOS33 } [ get\_ports { rs\_out[0] } ] ;  
  
# rt\_out  
set\_property -**dict** { PACKAGE\_PIN N14 IOSTANDARD LVCMOS33 } [ get\_ports { rt\_out[3] } ] ;  
set\_property -**dict** { PACKAGE\_PIN **J13** IOSTANDARD LVCMOS33 } [ get\_ports { rt\_out[2] } ] ;  
set\_property -**dict** { PACKAGE\_PIN K15 IOSTANDARD LVCMOS33 } [ get\_ports { rt\_out[1] } ] ;  
set\_property -**dict** { PACKAGE\_PIN H17 IOSTANDARD LVCMOS33 } [ get\_ports { rt\_out[0] } ] ;

**5.3) DO File**

5.3.1) Do File Control Unit

# 3.1.1 Data Cache  
  
add wave \*  
  
# 3.2.1.1) -- add  
force op "000000"  
force func\_in "100000"  
run 2  
examine reg\_write reg\_dst reg\_in\_src alu\_src add\_sub data\_write logic\_func func branch\_type pc\_sel  
  
# 3.2.1.2) -- sub  
force op "000000"  
force func\_in "100010"  
run 2  
examine reg\_write reg\_dst reg\_in\_src alu\_src add\_sub data\_write logic\_func func branch\_type pc\_sel  
  
# 3.2.1.3) -- slt  
force op "000000"  
force func\_in "101010"  
run 2  
examine reg\_write reg\_dst reg\_in\_src alu\_src add\_sub data\_write logic\_func func branch\_type pc\_sel  
  
# 3.2.1.4) -- and  
force op "000000"  
force func\_in "100100"  
run 2  
examine reg\_write reg\_dst reg\_in\_src alu\_src add\_sub data\_write logic\_func func branch\_type pc\_sel  
  
# 3.2.1.5) -- or  
force op "000000"  
force func\_in "100101"  
run 2  
examine reg\_write reg\_dst reg\_in\_src alu\_src add\_sub data\_write logic\_func func branch\_type pc\_sel  
  
# 3.2.1.6) -- xor  
force op "000000"  
force func\_in "100110"  
run 2  
examine reg\_write reg\_dst reg\_in\_src alu\_src add\_sub data\_write logic\_func func branch\_type pc\_sel  
  
# 3.2.1.7) -- nor  
force op "000000"  
force func\_in "100111"  
run 2  
examine reg\_write reg\_dst reg\_in\_src alu\_src add\_sub data\_write logic\_func func branch\_type pc\_sel  
  
# 3.2.1.8) -- jr  
force op "000000"  
force func\_in "001000"  
run 2  
examine reg\_write reg\_dst reg\_in\_src alu\_src add\_sub data\_write logic\_func func branch\_type pc\_sel  
  
# 3.2.1.9) -- lui  
force op "001111"  
run 2  
examine reg\_write reg\_dst reg\_in\_src alu\_src add\_sub data\_write logic\_func func branch\_type pc\_sel  
  
# 3.2.1.10) -- addi  
force op "001000"  
run 2  
examine reg\_write reg\_dst reg\_in\_src alu\_src add\_sub data\_write logic\_func func branch\_type pc\_sel  
  
# 3.2.1.11) -- slti  
force op "001010"  
run 2  
examine reg\_write reg\_dst reg\_in\_src alu\_src add\_sub data\_write logic\_func func branch\_type pc\_sel  
  
# 3.2.1.12) -- andi  
force op "001100"  
run 2  
examine reg\_write reg\_dst reg\_in\_src alu\_src add\_sub data\_write logic\_func func branch\_type pc\_sel  
  
# 3.2.1.13) -- ori  
force op "001101"  
run 2  
examine reg\_write reg\_dst reg\_in\_src alu\_src add\_sub data\_write logic\_func func branch\_type pc\_sel  
  
# 3.2.1.14) -- xori  
force op "001110"  
run 2  
examine reg\_write reg\_dst reg\_in\_src alu\_src add\_sub data\_write logic\_func func branch\_type pc\_sel  
  
# 3.2.1.15) -- lw  
force op "100011"  
run 2  
examine reg\_write reg\_dst reg\_in\_src alu\_src add\_sub data\_write logic\_func func branch\_type pc\_sel  
  
# 3.2.1.16) -- sw  
force op "101011"  
run 2  
examine reg\_write reg\_dst reg\_in\_src alu\_src add\_sub data\_write logic\_func func branch\_type pc\_sel  
  
# 3.2.1.17) -- j  
force op "000010"  
run 2  
examine reg\_write reg\_dst reg\_in\_src alu\_src add\_sub data\_write logic\_func func branch\_type pc\_sel  
  
# 3.2.1.18) -- bltz  
force op "000001"  
run 2  
examine reg\_write reg\_dst reg\_in\_src alu\_src add\_sub data\_write logic\_func func branch\_type pc\_sel  
  
# 3.2.1.19) -- beq  
force op "000100"  
run 2  
examine reg\_write reg\_dst reg\_in\_src alu\_src add\_sub data\_write logic\_func func branch\_type pc\_sel  
  
# 3.2.1.20) -- bne  
force op "000101"  
run 2  
examine reg\_write reg\_dst reg\_in\_src alu\_src add\_sub data\_write logic\_func func branch\_type pc\_sel

5.3.2) Do File CPU Unit

**add** wave reset  
**add** wave clk  
**add** wave -radix unsigned pc\_out  
**add** wave -radix unsigned rs\_out  
**add** wave -radix unsigned rt\_out  
  
force reset 1  
force clk 0  
**run** 2  
examine rs\_out rt\_out pc\_out overflow zero s\_inst  
  
force reset 0  
**run** 2  
force clk 1  
**run** 2  
examine rs\_out rt\_out pc\_out overflow zero s\_inst  
  
force clk 0  
**run** 2  
force clk 1   
**run** 2  
examine rs\_out rt\_out pc\_out overflow zero s\_inst  
  
force clk 0  
**run** 2  
force clk 1   
**run** 2  
examine rs\_out rt\_out pc\_out overflow zero s\_inst  
  
force clk 0  
**run** 2  
force clk 1   
**run** 2  
examine rs\_out rt\_out pc\_out overflow zero s\_inst  
  
force clk 0  
**run** 2  
force clk 1   
**run** 2  
examine rs\_out rt\_out pc\_out overflow zero s\_inst  
  
force clk 0  
**run** 2  
force clk 1   
**run** 2  
examine rs\_out rt\_out pc\_out overflow zero s\_inst  
  
force clk 0  
**run** 2  
force clk 1   
**run** 2  
examine rs\_out rt\_out pc\_out overflow zero s\_inst  
  
force clk 0  
**run** 2  
force clk 1   
**run** 2  
examine rs\_out rt\_out pc\_out overflow zero s\_inst  
  
force clk 0  
**run** 2  
force clk 1   
**run** 2  
examine rs\_out rt\_out pc\_out overflow zero s\_inst

5.3.3) Do File d\_cache

# 3.1.1 Data Cache  
  
add wave \*  
  
# 3.1.1.1 initialize value  
force d\_in x"AAAAAAAA"  
force reset 0  
force clk 1  
force data\_write 1  
force addr "00000"  
run 2  
examine -radix hex d\_out  
  
# 3.1.1.2 reset 1, clk 0 and data\_write 0  
force d\_in x"AAAAAAAA"  
force reset 1  
force clk 0  
force data\_write 0  
force addr "00000"  
run 2  
examine -radix hex d\_out  
  
# 3.1.1.3 data\_write 1, reset 0 and clk 0  
force d\_in x"AAAAAAAA"  
force reset 0  
force clk 0  
force data\_write 1  
force addr "00000"  
run 2  
examine -radix hex d\_out  
  
# 3.1.1.4 data\_write 0, reset 0 and clk 1  
force clk 0  
run 2  
force d\_in x"AAAAAAAA"  
force reset 0  
force clk 1  
force data\_write 0  
force addr "00000"  
run 2  
examine -radix hex d\_out  
  
# 3.1.1.5 data\_write 1, reset 0 and clk 1  
force clk 0  
run 2  
force d\_in x"AAAAAAAA"  
force reset 0  
force clk 1  
force data\_write 1  
force addr "00000"  
run 2  
examine -radix hex d\_out

5.3.4) Do File i\_cache

# 3.1.2 Instructions Cache  
  
add wave \*  
  
# 3.1.2.1 addi r1, r0, 1  
force addr\_in "00000"  
run 2  
examine -radix hex inst\_out  
  
# 3.1.2.2 addi r2, r0, 2  
force addr\_in "00001"  
run 2  
examine -radix hex inst\_out  
  
# 3.1.2.3 add r2, r2, r1  
force addr\_in "00010"  
run 2  
examine -radix hex inst\_out  
  
# 3.1.2.4 jump 00010  
force addr\_in "00011"  
run 2  
examine -radix hex inst\_out  
  
# 3.1.2.5 don’t care  
force addr\_in "01101"  
run 2  
examine -radix hex inst\_out

5.3.5) Do File pc

# 3.1.3 Pc  
  
add wave \*  
  
# 3.1.3.1 initialize value  
force reset 0  
force clk 1  
force d\_in x"AAAAAAAA"  
run 2  
examine -radix hex q\_out  
  
# 3.1.3.2 reset 1, clk 0  
force clk 0  
run 2  
force reset 1  
force d\_in x"AAAAAAAA"  
run 2  
examine -radix hex q\_out  
  
# 3.1.3.3 reset 0, clk 1  
force clk 0  
run 2  
force reset 0  
force clk 1  
force d\_in x"AAAAAAAA"  
run 2  
examine -radix hex q\_out

5.3.6) Do File sign\_ext

# 3.1.4 Sign extended  
  
add wave \*  
  
# 3.1.4.1 load upper immediate  
force func "00"  
force sign\_in x"ABCD"  
run 2  
examine -radix hex sign\_out  
  
# 3.1.4.2 set less immediate  
force func "01"  
force sign\_in x"ABCD"  
run 2  
examine -radix hex sign\_out  
  
# 3.1.4.3 arithmetic  
force func "10"  
force sign\_in x"0BCD"  
run 2  
examine -radix hex sign\_out  
  
# 3.1.4.4 logical  
force func "11"  
force sign\_in x"ABCD"  
run 2  
examine -radix hex sign\_out

**5.3) Synthesis Log**

*\*\*\** Running vivado  
 with args -log cpu.vds -m64 -product Vivado -mode batch -messageDb vivado.pb -notrace -source cpu.tcl  
  
  
**\*\*\*\*\***\* Vivado v2018.2 (64-bit)  
 *\*\*\**\* SW Build 2258646 on Thu Jun 14 20:02:38 MDT 2018  
 *\*\*\**\* IP Build 2256618 on Thu Jun 14 22:10:49 MDT 2018  
 \*\* Copyright 1986-2018 Xilinx, Inc. All Rights Reserved.  
  
source cpu.tcl -notrace  
Command: synth\_design -top cpu -part xc7a100tcsg324-1  
Starting synth\_design  
Attempting to get a license for feature 'Synthesis' and/or device 'xc7a100t'  
INFO: [Common 17-349] Got license for feature 'Synthesis' and/or device 'xc7a100t'  
INFO: Launching helper process for spawning children vivado processes  
INFO: Helper process launched with PID 421   
---------------------------------------------------------------------------------  
Starting RTL Elaboration : Time (s): cpu = 00:00:02 ; elapsed = 00:00:04 . Memory (MB): peak = 1468.590 ; gain = 86.727 ; free physical = 71004 ; free virtual = 153913  
---------------------------------------------------------------------------------  
WARNING: [Synth 8-2489] overwriting existing secondary unit i*\_cache\_*arch [/nfs/home/l/l*\_heiwan/coen316/lab4/i\_*cache\_quiz.vhd:10]  
INFO: [Synth 8-638] synthesizing module 'cpu' [/nfs/home/l/l*\_heiwan/coen316/lab4/cpu\_*entity.vhd:17]  
INFO: [Synth 8-3491] module 'pc' declared at '/nfs/home/l/l*\_heiwan/coen316/lab4/pc.vhd:5' bound to instance 'pm\_*pc' of component 'pc' [/nfs/home/l/l*\_heiwan/coen316/lab4/cpu\_*entity.vhd:165]  
INFO: [Synth 8-638] synthesizing module 'pc' [/nfs/home/l/l\_heiwan/coen316/lab4/pc.vhd:13]  
INFO: [Synth 8-256] done synthesizing module 'pc' (1#1) [/nfs/home/l/l\_heiwan/coen316/lab4/pc.vhd:13]  
INFO: [Synth 8-3491] module 'i*\_cache' declared at '/nfs/home/l/l\_*heiwan/coen316/lab4/i*\_cache.vhd:4' bound to instance 'pm\_*i*\_cache' of component 'i\_*cache' [/nfs/home/l/l*\_heiwan/coen316/lab4/cpu\_*entity.vhd:172]  
INFO: [Synth 8-638] synthesizing module 'i*\_cache' [/nfs/home/l/l\_*heiwan/coen316/lab4/i*\_cache\_*quiz.vhd:10]  
INFO: [Synth 8-256] done synthesizing module 'i*\_cache' (2#1) [/nfs/home/l/l\_*heiwan/coen316/lab4/i*\_cache\_*quiz.vhd:10]  
INFO: [Synth 8-3491] module 'regfile' declared at '/nfs/home/l/l*\_heiwan/coen316/lab4/lab2\_*register*\_file.vhd:10' bound to instance 'pm\_*reg*\_file' of component 'reg\_*file' [/nfs/home/l/l*\_heiwan/coen316/lab4/cpu\_*entity.vhd:177]  
INFO: [Synth 8-638] synthesizing module 'regfile' [/nfs/home/l/l*\_heiwan/coen316/lab4/lab2\_*register\_file.vhd:23]  
INFO: [Synth 8-256] done synthesizing module 'regfile' (3#1) [/nfs/home/l/l*\_heiwan/coen316/lab4/lab2\_*register\_file.vhd:23]  
INFO: [Synth 8-3491] module 'alu' declared at '/nfs/home/l/l*\_heiwan/coen316/lab4/lab1\_*alu.vhd:9' bound to instance 'pm*\_alu' of component 'alu' [/nfs/home/l/l\_*heiwan/coen316/lab4/cpu\_entity.vhd:189]  
INFO: [Synth 8-638] synthesizing module 'alu' [/nfs/home/l/l*\_heiwan/coen316/lab4/lab1\_*alu.vhd:20]  
INFO: [Synth 8-256] done synthesizing module 'alu' (4#1) [/nfs/home/l/l*\_heiwan/coen316/lab4/lab1\_*alu.vhd:20]  
INFO: [Synth 8-3491] module 'd*\_cache' declared at '/nfs/home/l/l\_*heiwan/coen316/lab4/d*\_cache.vhd:5' bound to instance 'pm\_*d*\_cache' of component 'd\_*cache' [/nfs/home/l/l*\_heiwan/coen316/lab4/cpu\_*entity.vhd:200]  
INFO: [Synth 8-638] synthesizing module 'd*\_cache' [/nfs/home/l/l\_*heiwan/coen316/lab4/d\_cache.vhd:15]  
WARNING: [Synth 8-614] signal 'data*\_write' is read in the process but is not in the sensitivity list [/nfs/home/l/l\_*heiwan/coen316/lab4/d\_cache.vhd:21]  
INFO: [Synth 8-256] done synthesizing module 'd*\_cache' (5#1) [/nfs/home/l/l\_*heiwan/coen316/lab4/d\_cache.vhd:15]  
INFO: [Synth 8-3491] module 'sign*\_extended' declared at '/nfs/home/l/l\_*heiwan/coen316/lab4/sign*\_extended.vhd:5' bound to instance 'pm\_*sign*\_ext' of component 'sign\_*ext' [/nfs/home/l/l*\_heiwan/coen316/lab4/cpu\_*entity.vhd:209]  
INFO: [Synth 8-638] synthesizing module 'sign*\_extended' [/nfs/home/l/l\_*heiwan/coen316/lab4/sign\_extended.vhd:12]  
INFO: [Synth 8-256] done synthesizing module 'sign*\_extended' (6#1) [/nfs/home/l/l\_*heiwan/coen316/lab4/sign\_extended.vhd:12]  
INFO: [Synth 8-3491] module 'next*\_address' declared at '/nfs/home/l/l\_*heiwan/coen316/lab4/lab3*\_next\_*addr.vhd:9' bound to instance 'pm*\_next\_*address' of component 'next*\_address' [/nfs/home/l/l\_*heiwan/coen316/lab4/cpu\_entity.vhd:215]  
INFO: [Synth 8-638] synthesizing module 'next*\_address' [/nfs/home/l/l\_*heiwan/coen316/lab4/lab3*\_next\_*addr.vhd:22]  
INFO: [Synth 8-256] done synthesizing module 'next*\_address' (7#1) [/nfs/home/l/l\_*heiwan/coen316/lab4/lab3*\_next\_*addr.vhd:22]  
INFO: [Synth 8-3491] module 'control*\_unit' declared at '/nfs/home/l/l\_*heiwan/coen316/lab4/control*\_unit.vhd:4' bound to instance 'pm\_*control*\_unit' of component 'control\_*unit' [/nfs/home/l/l*\_heiwan/coen316/lab4/cpu\_*entity.vhd:225]  
INFO: [Synth 8-638] synthesizing module 'control*\_unit' [/nfs/home/l/l\_*heiwan/coen316/lab4/control\_unit.vhd:20]  
INFO: [Synth 8-256] done synthesizing module 'control*\_unit' (8#1) [/nfs/home/l/l\_*heiwan/coen316/lab4/control\_unit.vhd:20]  
INFO: [Synth 8-256] done synthesizing module 'cpu' (9#1) [/nfs/home/l/l*\_heiwan/coen316/lab4/cpu\_*entity.vhd:17]  
---------------------------------------------------------------------------------  
Finished RTL Elaboration : Time (s): cpu = 00:00:03 ; elapsed = 00:00:06 . Memory (MB): peak = 1512.230 ; gain = 130.367 ; free physical = 71016 ; free virtual = 153924  
---------------------------------------------------------------------------------  
  
Report Check Netlist:   
+------+------------------+-------+---------+-------+------------------+  
| |Item |Errors |Warnings |Status |Description |  
+------+------------------+-------+---------+-------+------------------+  
|1 |multi*\_driven\_*nets | 0| 0|Passed |Multi driven nets |  
+------+------------------+-------+---------+-------+------------------+  
---------------------------------------------------------------------------------  
Start Handling Custom Attributes  
---------------------------------------------------------------------------------  
---------------------------------------------------------------------------------  
Finished Handling Custom Attributes : Time (s): cpu = 00:00:03 ; elapsed = 00:00:06 . Memory (MB): peak = 1512.230 ; gain = 130.367 ; free physical = 71015 ; free virtual = 153923  
---------------------------------------------------------------------------------  
---------------------------------------------------------------------------------  
Finished RTL Optimization Phase 1 : Time (s): cpu = 00:00:03 ; elapsed = 00:00:06 . Memory (MB): peak = 1512.230 ; gain = 130.367 ; free physical = 71015 ; free virtual = 153923  
---------------------------------------------------------------------------------  
INFO: [Device 21-403] Loading part xc7a100tcsg324-1  
INFO: [Project 1-570] Preparing netlist for logic optimization  
  
Processing XDC Constraints  
Initializing timing engine  
Parsing XDC File [/nfs/home/l/l\_heiwan/coen316/lab4/givenToUs/cpu.xdc]  
Finished Parsing XDC File [/nfs/home/l/l\_heiwan/coen316/lab4/givenToUs/cpu.xdc]  
INFO: [Project 1-236] Implementation specific constraints were found while reading constraint file [/nfs/home/l/l*\_heiwan/coen316/lab4/givenToUs/cpu.xdc]. These constraints will be ignored for synthesis but will be used in implementation. Impacted constraints are listed in the file [.Xil/cpu\_*propImpl.xdc].  
Resolution: To avoid this warning, move constraints listed in [.Xil/cpu*\_propImpl.xdc] to another XDC file and exclude this new file from synthesis with the used\_*in\_synthesis property (File Properties dialog in GUI) and re-run elaboration/synthesis.  
Completed Processing XDC Constraints  
  
INFO: [Project 1-111] Unisim Transformation Summary:  
No Unisim elements were transformed.  
  
Constraint Validation Runtime : Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 1892.141 ; gain = 0.000 ; free physical = 70673 ; free virtual = 153582  
---------------------------------------------------------------------------------  
Finished Constraint Validation : Time (s): cpu = 00:00:15 ; elapsed = 00:01:06 . Memory (MB): peak = 1892.141 ; gain = 510.277 ; free physical = 70824 ; free virtual = 153732  
---------------------------------------------------------------------------------  
---------------------------------------------------------------------------------  
Start Loading Part and Timing Information  
---------------------------------------------------------------------------------  
Loading part: xc7a100tcsg324-1  
---------------------------------------------------------------------------------  
Finished Loading Part and Timing Information : Time (s): cpu = 00:00:15 ; elapsed = 00:01:06 . Memory (MB): peak = 1892.141 ; gain = 510.277 ; free physical = 70824 ; free virtual = 153732  
---------------------------------------------------------------------------------  
---------------------------------------------------------------------------------  
Start Applying 'set\_property' XDC Constraints  
---------------------------------------------------------------------------------  
---------------------------------------------------------------------------------  
Finished applying 'set\_property' XDC Constraints : Time (s): cpu = 00:00:15 ; elapsed = 00:01:06 . Memory (MB): peak = 1892.141 ; gain = 510.277 ; free physical = 70825 ; free virtual = 153734  
---------------------------------------------------------------------------------  
INFO: [Synth 8-5546] ROM "inst\_out" won't be mapped to RAM because it is too sparse  
INFO: [Synth 8-5546] ROM "registers\_reg[0]" won't be mapped to RAM because it is too sparse  
INFO: [Synth 8-5546] ROM "registers\_reg[1]" won't be mapped to RAM because it is too sparse  
INFO: [Synth 8-5546] ROM "registers\_reg[2]" won't be mapped to RAM because it is too sparse  
INFO: [Synth 8-5546] ROM "registers\_reg[3]" won't be mapped to RAM because it is too sparse  
INFO: [Synth 8-5546] ROM "registers\_reg[4]" won't be mapped to RAM because it is too sparse  
INFO: [Synth 8-5546] ROM "registers\_reg[5]" won't be mapped to RAM because it is too sparse  
INFO: [Synth 8-5546] ROM "registers\_reg[6]" won't be mapped to RAM because it is too sparse  
INFO: [Synth 8-5546] ROM "registers\_reg[7]" won't be mapped to RAM because it is too sparse  
INFO: [Synth 8-5546] ROM "registers\_reg[8]" won't be mapped to RAM because it is too sparse  
INFO: [Synth 8-5546] ROM "registers\_reg[9]" won't be mapped to RAM because it is too sparse  
INFO: [Synth 8-5546] ROM "registers\_reg[10]" won't be mapped to RAM because it is too sparse  
INFO: [Synth 8-5546] ROM "registers\_reg[11]" won't be mapped to RAM because it is too sparse  
INFO: [Synth 8-5546] ROM "registers\_reg[12]" won't be mapped to RAM because it is too sparse  
INFO: [Synth 8-5546] ROM "registers\_reg[13]" won't be mapped to RAM because it is too sparse  
INFO: [Synth 8-5546] ROM "registers\_reg[14]" won't be mapped to RAM because it is too sparse  
INFO: [Synth 8-5546] ROM "registers\_reg[15]" won't be mapped to RAM because it is too sparse  
INFO: [Synth 8-5546] ROM "registers\_reg[16]" won't be mapped to RAM because it is too sparse  
INFO: [Synth 8-5546] ROM "registers\_reg[17]" won't be mapped to RAM because it is too sparse  
INFO: [Synth 8-5546] ROM "registers\_reg[18]" won't be mapped to RAM because it is too sparse  
INFO: [Synth 8-5546] ROM "registers\_reg[19]" won't be mapped to RAM because it is too sparse  
INFO: [Synth 8-5546] ROM "registers\_reg[20]" won't be mapped to RAM because it is too sparse  
INFO: [Synth 8-5546] ROM "registers\_reg[21]" won't be mapped to RAM because it is too sparse  
INFO: [Synth 8-5546] ROM "registers\_reg[22]" won't be mapped to RAM because it is too sparse  
INFO: [Synth 8-5546] ROM "registers\_reg[23]" won't be mapped to RAM because it is too sparse  
INFO: [Synth 8-5546] ROM "registers\_reg[24]" won't be mapped to RAM because it is too sparse  
INFO: [Synth 8-5546] ROM "registers\_reg[25]" won't be mapped to RAM because it is too sparse  
INFO: [Synth 8-5546] ROM "registers\_reg[26]" won't be mapped to RAM because it is too sparse  
INFO: [Synth 8-5546] ROM "registers\_reg[27]" won't be mapped to RAM because it is too sparse  
INFO: [Synth 8-5546] ROM "registers\_reg[28]" won't be mapped to RAM because it is too sparse  
INFO: [Synth 8-5546] ROM "registers\_reg[29]" won't be mapped to RAM because it is too sparse  
INFO: [Synth 8-5546] ROM "registers\_reg[30]" won't be mapped to RAM because it is too sparse  
INFO: [Synth 8-5546] ROM "registers\_reg[31]" won't be mapped to RAM because it is too sparse  
INFO: [Synth 8-5818] HDL ADVISOR - The operator resource <**adder**> is shared. To prevent sharing consider applying a KEEP on the output of the operator [/nfs/home/l/l*\_heiwan/coen316/lab4/lab1\_*alu.vhd:30]  
INFO: [Synth 8-5546] ROM "registers\_reg[0]" won't be mapped to RAM because it is too sparse  
INFO: [Synth 8-5546] ROM "registers\_reg[1]" won't be mapped to RAM because it is too sparse  
INFO: [Synth 8-5546] ROM "registers\_reg[2]" won't be mapped to RAM because it is too sparse  
INFO: [Synth 8-5546] ROM "registers\_reg[3]" won't be mapped to RAM because it is too sparse  
INFO: [Synth 8-5546] ROM "registers\_reg[4]" won't be mapped to RAM because it is too sparse  
INFO: [Synth 8-5546] ROM "registers\_reg[5]" won't be mapped to RAM because it is too sparse  
INFO: [Synth 8-5546] ROM "registers\_reg[6]" won't be mapped to RAM because it is too sparse  
INFO: [Synth 8-5546] ROM "registers\_reg[7]" won't be mapped to RAM because it is too sparse  
INFO: [Synth 8-5546] ROM "registers\_reg[8]" won't be mapped to RAM because it is too sparse  
INFO: [Synth 8-5546] ROM "registers\_reg[9]" won't be mapped to RAM because it is too sparse  
INFO: [Synth 8-5546] ROM "registers\_reg[10]" won't be mapped to RAM because it is too sparse  
INFO: [Synth 8-5546] ROM "registers\_reg[11]" won't be mapped to RAM because it is too sparse  
INFO: [Synth 8-5546] ROM "registers\_reg[12]" won't be mapped to RAM because it is too sparse  
INFO: [Synth 8-5546] ROM "registers\_reg[13]" won't be mapped to RAM because it is too sparse  
INFO: [Synth 8-5546] ROM "registers\_reg[14]" won't be mapped to RAM because it is too sparse  
INFO: [Synth 8-5546] ROM "registers\_reg[15]" won't be mapped to RAM because it is too sparse  
INFO: [Synth 8-5546] ROM "registers\_reg[16]" won't be mapped to RAM because it is too sparse  
INFO: [Synth 8-5546] ROM "registers\_reg[17]" won't be mapped to RAM because it is too sparse  
INFO: [Synth 8-5546] ROM "registers\_reg[18]" won't be mapped to RAM because it is too sparse  
INFO: [Synth 8-5546] ROM "registers\_reg[19]" won't be mapped to RAM because it is too sparse  
INFO: [Synth 8-5546] ROM "registers\_reg[20]" won't be mapped to RAM because it is too sparse  
INFO: [Synth 8-5546] ROM "registers\_reg[21]" won't be mapped to RAM because it is too sparse  
INFO: [Synth 8-5546] ROM "registers\_reg[22]" won't be mapped to RAM because it is too sparse  
INFO: [Synth 8-5546] ROM "registers\_reg[23]" won't be mapped to RAM because it is too sparse  
INFO: [Synth 8-5546] ROM "registers\_reg[24]" won't be mapped to RAM because it is too sparse  
INFO: [Synth 8-5546] ROM "registers\_reg[25]" won't be mapped to RAM because it is too sparse  
INFO: [Synth 8-5546] ROM "registers\_reg[26]" won't be mapped to RAM because it is too sparse  
INFO: [Synth 8-5546] ROM "registers\_reg[27]" won't be mapped to RAM because it is too sparse  
INFO: [Synth 8-5546] ROM "registers\_reg[28]" won't be mapped to RAM because it is too sparse  
INFO: [Synth 8-5546] ROM "registers\_reg[29]" won't be mapped to RAM because it is too sparse  
INFO: [Synth 8-5546] ROM "registers\_reg[30]" won't be mapped to RAM because it is too sparse  
INFO: [Synth 8-5546] ROM "registers\_reg[31]" won't be mapped to RAM because it is too sparse  
INFO: [Synth 8-5546] ROM "control\_signals" won't be mapped to RAM because it is too sparse  
WARNING: [Synth 8-327] inferring latch for variable 'next*\_pc\_*reg' [/nfs/home/l/l*\_heiwan/coen316/lab4/lab3\_*next\_addr.vhd:43]  
WARNING: [Synth 8-327] inferring latch for variable 'branch*\_offset\_*reg' [/nfs/home/l/l*\_heiwan/coen316/lab4/lab3\_*next\_addr.vhd:57]  
---------------------------------------------------------------------------------  
Finished RTL Optimization Phase 2 : Time (s): cpu = 00:00:16 ; elapsed = 00:01:07 . Memory (MB): peak = 1892.141 ; gain = 510.277 ; free physical = 70815 ; free virtual = 153724  
---------------------------------------------------------------------------------  
  
Report RTL Partitions:   
+-+--------------+------------+----------+  
| |RTL Partition |Replication |Instances |  
+-+--------------+------------+----------+  
+-+--------------+------------+----------+  
---------------------------------------------------------------------------------  
Start RTL Component Statistics   
---------------------------------------------------------------------------------  
Detailed RTL Component Info :   
+---Adders :   
 3 Input 32 Bit Adders := 2   
+---XORs :   
 2 Input 32 Bit XORs := 1   
+---Registers :   
 32 Bit Registers := 65   
+---Muxes :   
 2 Input 32 Bit Muxes := 12   
 4 Input 32 Bit Muxes := 3   
 9 Input 14 Bit Muxes := 1   
 14 Input 14 Bit Muxes := 1   
 2 Input 5 Bit Muxes := 1   
 2 Input 1 Bit Muxes := 67   
 4 Input 1 Bit Muxes := 1   
---------------------------------------------------------------------------------  
Finished RTL Component Statistics   
---------------------------------------------------------------------------------  
---------------------------------------------------------------------------------  
Start RTL Hierarchical Component Statistics   
---------------------------------------------------------------------------------  
Hierarchical RTL Component report   
Module cpu   
Detailed RTL Component Info :   
+---Muxes :   
 2 Input 32 Bit Muxes := 2   
 2 Input 5 Bit Muxes := 1   
Module pc   
Detailed RTL Component Info :   
+---Registers :   
 32 Bit Registers := 1   
Module i\_cache   
Detailed RTL Component Info :   
+---Muxes :   
 2 Input 32 Bit Muxes := 1   
Module regfile   
Detailed RTL Component Info :   
+---Registers :   
 32 Bit Registers := 32   
+---Muxes :   
 2 Input 1 Bit Muxes := 32   
Module alu   
Detailed RTL Component Info :   
+---Adders :   
 3 Input 32 Bit Adders := 1   
+---XORs :   
 2 Input 32 Bit XORs := 1   
+---Muxes :   
 4 Input 32 Bit Muxes := 2   
 2 Input 32 Bit Muxes := 1   
 2 Input 1 Bit Muxes := 1   
Module d\_cache   
Detailed RTL Component Info :   
+---Registers :   
 32 Bit Registers := 32   
+---Muxes :   
 2 Input 1 Bit Muxes := 32   
Module sign\_extended   
Detailed RTL Component Info :   
+---Muxes :   
 4 Input 32 Bit Muxes := 1   
Module next\_address   
Detailed RTL Component Info :   
+---Adders :   
 3 Input 32 Bit Adders := 1   
+---Muxes :   
 2 Input 32 Bit Muxes := 8   
 2 Input 1 Bit Muxes := 2   
 4 Input 1 Bit Muxes := 1   
Module control\_unit   
Detailed RTL Component Info :   
+---Muxes :   
 9 Input 14 Bit Muxes := 1   
 14 Input 14 Bit Muxes := 1   
---------------------------------------------------------------------------------  
Finished RTL Hierarchical Component Statistics  
---------------------------------------------------------------------------------  
---------------------------------------------------------------------------------  
Start Part Resource Summary  
---------------------------------------------------------------------------------  
Part Resources:  
DSPs: 240 (col length:80)  
BRAMs: 270 (col length: RAMB18 80 RAMB36 40)  
---------------------------------------------------------------------------------  
Finished Part Resource Summary  
---------------------------------------------------------------------------------  
---------------------------------------------------------------------------------  
Start Cross Boundary and Area Optimization  
---------------------------------------------------------------------------------  
Warning: Parallel synthesis criteria is not met   
INFO: [Synth 8-5546] ROM "pm*\_control\_*unit/control\_signals" won't be mapped to RAM because it is too sparse  
INFO: [Synth 8-3886] merging instance 'pm*\_reg\_*file/registers*\_reg[14][4]' (FDCE) to 'pm\_*reg*\_file/registers\_*reg[13][4]'  
INFO: [Synth 8-3886] merging instance 'pm*\_reg\_*file/registers*\_reg[13][4]' (FDCE) to 'pm\_*reg*\_file/registers\_*reg[11][4]'  
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\pm*\_reg\_*file/registers\_reg[11][4] )  
INFO: [Synth 8-3886] merging instance 'pm*\_reg\_*file/registers*\_reg[14][5]' (FDCE) to 'pm\_*reg*\_file/registers\_*reg[13][5]'  
INFO: [Synth 8-3886] merging instance 'pm*\_reg\_*file/registers*\_reg[13][5]' (FDCE) to 'pm\_*reg*\_file/registers\_*reg[11][5]'  
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\pm*\_reg\_*file/registers\_reg[11][5] )  
INFO: [Synth 8-3886] merging instance 'pm*\_reg\_*file/registers*\_reg[14][6]' (FDCE) to 'pm\_*reg*\_file/registers\_*reg[13][6]'  
INFO: [Synth 8-3886] merging instance 'pm*\_reg\_*file/registers*\_reg[13][6]' (FDCE) to 'pm\_*reg*\_file/registers\_*reg[11][6]'  
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\pm*\_reg\_*file/registers\_reg[11][6] )  
INFO: [Synth 8-3886] merging instance 'pm*\_reg\_*file/registers*\_reg[14][7]' (FDCE) to 'pm\_*reg*\_file/registers\_*reg[13][7]'  
INFO: [Synth 8-3886] merging instance 'pm*\_reg\_*file/registers*\_reg[13][7]' (FDCE) to 'pm\_*reg*\_file/registers\_*reg[11][7]'  
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\pm*\_reg\_*file/registers\_reg[11][7] )  
INFO: [Synth 8-3886] merging instance 'pm*\_reg\_*file/registers*\_reg[14][8]' (FDCE) to 'pm\_*reg*\_file/registers\_*reg[13][8]'  
INFO: [Synth 8-3886] merging instance 'pm*\_reg\_*file/registers*\_reg[13][8]' (FDCE) to 'pm\_*reg*\_file/registers\_*reg[11][8]'  
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\pm*\_reg\_*file/registers\_reg[11][8] )  
INFO: [Synth 8-3886] merging instance 'pm*\_reg\_*file/registers*\_reg[14][9]' (FDCE) to 'pm\_*reg*\_file/registers\_*reg[13][9]'  
INFO: [Synth 8-3886] merging instance 'pm*\_reg\_*file/registers*\_reg[13][9]' (FDCE) to 'pm\_*reg*\_file/registers\_*reg[11][9]'  
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\pm*\_reg\_*file/registers\_reg[11][9] )  
INFO: [Synth 8-3886] merging instance 'pm*\_reg\_*file/registers*\_reg[14][10]' (FDCE) to 'pm\_*reg*\_file/registers\_*reg[13][10]'  
INFO: [Synth 8-3886] merging instance 'pm*\_reg\_*file/registers*\_reg[13][10]' (FDCE) to 'pm\_*reg*\_file/registers\_*reg[11][10]'  
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\pm*\_reg\_*file/registers\_reg[11][10] )  
INFO: [Synth 8-3886] merging instance 'pm*\_reg\_*file/registers*\_reg[14][11]' (FDCE) to 'pm\_*reg*\_file/registers\_*reg[13][11]'  
INFO: [Synth 8-3886] merging instance 'pm*\_reg\_*file/registers*\_reg[13][11]' (FDCE) to 'pm\_*reg*\_file/registers\_*reg[11][11]'  
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\pm*\_reg\_*file/registers\_reg[11][11] )  
INFO: [Synth 8-3886] merging instance 'pm*\_reg\_*file/registers*\_reg[14][12]' (FDCE) to 'pm\_*reg*\_file/registers\_*reg[13][12]'  
INFO: [Synth 8-3886] merging instance 'pm*\_reg\_*file/registers*\_reg[13][12]' (FDCE) to 'pm\_*reg*\_file/registers\_*reg[11][12]'  
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\pm*\_reg\_*file/registers\_reg[11][12] )  
INFO: [Synth 8-3886] merging instance 'pm*\_reg\_*file/registers*\_reg[14][13]' (FDCE) to 'pm\_*reg*\_file/registers\_*reg[13][13]'  
INFO: [Synth 8-3886] merging instance 'pm*\_reg\_*file/registers*\_reg[13][13]' (FDCE) to 'pm\_*reg*\_file/registers\_*reg[11][13]'  
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\pm*\_reg\_*file/registers\_reg[11][13] )  
INFO: [Synth 8-3886] merging instance 'pm*\_reg\_*file/registers*\_reg[14][14]' (FDCE) to 'pm\_*reg*\_file/registers\_*reg[13][14]'  
INFO: [Synth 8-3886] merging instance 'pm*\_reg\_*file/registers*\_reg[13][14]' (FDCE) to 'pm\_*reg*\_file/registers\_*reg[11][14]'  
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\pm*\_reg\_*file/registers\_reg[11][14] )  
INFO: [Synth 8-3886] merging instance 'pm*\_reg\_*file/registers*\_reg[14][15]' (FDCE) to 'pm\_*reg*\_file/registers\_*reg[13][15]'  
INFO: [Synth 8-3886] merging instance 'pm*\_reg\_*file/registers*\_reg[13][15]' (FDCE) to 'pm\_*reg*\_file/registers\_*reg[11][15]'  
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\pm*\_reg\_*file/registers\_reg[11][15] )  
INFO: [Synth 8-3886] merging instance 'pm*\_reg\_*file/registers*\_reg[14][16]' (FDCE) to 'pm\_*reg*\_file/registers\_*reg[13][16]'  
INFO: [Synth 8-3886] merging instance 'pm*\_reg\_*file/registers*\_reg[13][16]' (FDCE) to 'pm\_*reg*\_file/registers\_*reg[11][16]'  
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\pm*\_reg\_*file/registers\_reg[11][16] )  
INFO: [Synth 8-3886] merging instance 'pm*\_reg\_*file/registers*\_reg[14][17]' (FDCE) to 'pm\_*reg*\_file/registers\_*reg[13][17]'  
INFO: [Synth 8-3886] merging instance 'pm*\_reg\_*file/registers*\_reg[13][17]' (FDCE) to 'pm\_*reg*\_file/registers\_*reg[11][17]'  
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\pm*\_reg\_*file/registers\_reg[11][17] )  
INFO: [Synth 8-3886] merging instance 'pm*\_reg\_*file/registers*\_reg[14][18]' (FDCE) to 'pm\_*reg*\_file/registers\_*reg[13][18]'  
INFO: [Synth 8-3886] merging instance 'pm*\_reg\_*file/registers*\_reg[13][18]' (FDCE) to 'pm\_*reg*\_file/registers\_*reg[11][18]'  
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\pm*\_reg\_*file/registers\_reg[11][18] )  
INFO: [Synth 8-3886] merging instance 'pm*\_reg\_*file/registers*\_reg[14][19]' (FDCE) to 'pm\_*reg*\_file/registers\_*reg[13][19]'  
INFO: [Synth 8-3886] merging instance 'pm*\_reg\_*file/registers*\_reg[13][19]' (FDCE) to 'pm\_*reg*\_file/registers\_*reg[11][19]'  
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\pm*\_reg\_*file/registers\_reg[11][19] )  
INFO: [Synth 8-3886] merging instance 'pm*\_reg\_*file/registers*\_reg[14][20]' (FDCE) to 'pm\_*reg*\_file/registers\_*reg[13][20]'  
INFO: [Synth 8-3886] merging instance 'pm*\_reg\_*file/registers*\_reg[13][20]' (FDCE) to 'pm\_*reg*\_file/registers\_*reg[11][20]'  
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\pm*\_reg\_*file/registers\_reg[11][20] )  
INFO: [Synth 8-3886] merging instance 'pm*\_reg\_*file/registers*\_reg[14][21]' (FDCE) to 'pm\_*reg*\_file/registers\_*reg[13][21]'  
INFO: [Synth 8-3886] merging instance 'pm*\_reg\_*file/registers*\_reg[13][21]' (FDCE) to 'pm\_*reg*\_file/registers\_*reg[11][21]'  
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\pm*\_reg\_*file/registers\_reg[11][21] )  
INFO: [Synth 8-3886] merging instance 'pm*\_reg\_*file/registers*\_reg[14][22]' (FDCE) to 'pm\_*reg*\_file/registers\_*reg[13][22]'  
INFO: [Synth 8-3886] merging instance 'pm*\_reg\_*file/registers*\_reg[13][22]' (FDCE) to 'pm\_*reg*\_file/registers\_*reg[11][22]'  
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\pm*\_reg\_*file/registers\_reg[11][22] )  
INFO: [Synth 8-3886] merging instance 'pm*\_reg\_*file/registers*\_reg[14][23]' (FDCE) to 'pm\_*reg*\_file/registers\_*reg[13][23]'  
INFO: [Synth 8-3886] merging instance 'pm*\_reg\_*file/registers*\_reg[13][23]' (FDCE) to 'pm\_*reg*\_file/registers\_*reg[11][23]'  
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\pm*\_reg\_*file/registers\_reg[11][23] )  
INFO: [Synth 8-3886] merging instance 'pm*\_reg\_*file/registers*\_reg[14][24]' (FDCE) to 'pm\_*reg*\_file/registers\_*reg[13][24]'  
INFO: [Synth 8-3886] merging instance 'pm*\_reg\_*file/registers*\_reg[13][24]' (FDCE) to 'pm\_*reg*\_file/registers\_*reg[11][24]'  
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\pm*\_reg\_*file/registers\_reg[11][24] )  
INFO: [Synth 8-3886] merging instance 'pm*\_reg\_*file/registers*\_reg[14][25]' (FDCE) to 'pm\_*reg*\_file/registers\_*reg[13][25]'  
INFO: [Synth 8-3886] merging instance 'pm*\_reg\_*file/registers*\_reg[13][25]' (FDCE) to 'pm\_*reg*\_file/registers\_*reg[11][25]'  
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\pm*\_reg\_*file/registers\_reg[11][25] )  
INFO: [Synth 8-3886] merging instance 'pm*\_reg\_*file/registers*\_reg[14][26]' (FDCE) to 'pm\_*reg*\_file/registers\_*reg[13][26]'  
INFO: [Synth 8-3886] merging instance 'pm*\_reg\_*file/registers*\_reg[13][26]' (FDCE) to 'pm\_*reg*\_file/registers\_*reg[11][26]'  
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\pm*\_reg\_*file/registers\_reg[11][26] )  
INFO: [Synth 8-3886] merging instance 'pm*\_reg\_*file/registers*\_reg[14][27]' (FDCE) to 'pm\_*reg*\_file/registers\_*reg[13][27]'  
INFO: [Synth 8-3886] merging instance 'pm*\_reg\_*file/registers*\_reg[13][27]' (FDCE) to 'pm\_*reg*\_file/registers\_*reg[11][27]'  
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\pm*\_reg\_*file/registers\_reg[11][27] )  
INFO: [Synth 8-3886] merging instance 'pm*\_reg\_*file/registers*\_reg[14][28]' (FDCE) to 'pm\_*reg*\_file/registers\_*reg[13][28]'  
INFO: [Synth 8-3886] merging instance 'pm*\_reg\_*file/registers*\_reg[13][28]' (FDCE) to 'pm\_*reg*\_file/registers\_*reg[11][28]'  
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\pm*\_reg\_*file/registers\_reg[11][28] )  
INFO: [Synth 8-3886] merging instance 'pm*\_reg\_*file/registers*\_reg[14][29]' (FDCE) to 'pm\_*reg*\_file/registers\_*reg[13][29]'  
INFO: [Synth 8-3886] merging instance 'pm*\_reg\_*file/registers*\_reg[13][29]' (FDCE) to 'pm\_*reg*\_file/registers\_*reg[11][29]'  
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\pm*\_reg\_*file/registers\_reg[11][29] )  
INFO: [Synth 8-3886] merging instance 'pm*\_reg\_*file/registers*\_reg[14][30]' (FDCE) to 'pm\_*reg*\_file/registers\_*reg[13][30]'  
INFO: [Synth 8-3886] merging instance 'pm*\_reg\_*file/registers*\_reg[13][30]' (FDCE) to 'pm\_*reg*\_file/registers\_*reg[11][30]'  
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\pm*\_reg\_*file/registers\_reg[11][30] )  
INFO: [Synth 8-3886] merging instance 'pm*\_reg\_*file/registers*\_reg[14][31]' (FDCE) to 'pm\_*reg*\_file/registers\_*reg[13][31]'  
INFO: [Synth 8-3886] merging instance 'pm*\_reg\_*file/registers*\_reg[13][31]' (FDCE) to 'pm\_*reg*\_file/registers\_*reg[11][31]'  
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\pm*\_reg\_*file/registers\_reg[11][31] )  
INFO: [Synth 8-3886] merging instance 'pm*\_reg\_*file/registers*\_reg[14][0]' (FDCE) to 'pm\_*reg*\_file/registers\_*reg[13][0]'  
INFO: [Synth 8-3886] merging instance 'pm*\_reg\_*file/registers*\_reg[13][0]' (FDCE) to 'pm\_*reg*\_file/registers\_*reg[11][0]'  
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\pm*\_reg\_*file/registers\_reg[11][0] )  
INFO: [Synth 8-3886] merging instance 'pm*\_reg\_*file/registers*\_reg[14][1]' (FDCE) to 'pm\_*reg*\_file/registers\_*reg[13][1]'  
INFO: [Synth 8-3886] merging instance 'pm*\_reg\_*file/registers*\_reg[13][1]' (FDCE) to 'pm\_*reg*\_file/registers\_*reg[11][1]'  
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\pm*\_reg\_*file/registers\_reg[11][1] )  
INFO: [Synth 8-3886] merging instance 'pm*\_reg\_*file/registers*\_reg[14][2]' (FDCE) to 'pm\_*reg*\_file/registers\_*reg[13][2]'  
INFO: [Synth 8-3886] merging instance 'pm*\_reg\_*file/registers*\_reg[13][2]' (FDCE) to 'pm\_*reg*\_file/registers\_*reg[11][2]'  
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\pm*\_reg\_*file/registers\_reg[11][2] )  
INFO: [Synth 8-3886] merging instance 'pm*\_reg\_*file/registers*\_reg[14][3]' (FDCE) to 'pm\_*reg*\_file/registers\_*reg[13][3]'  
INFO: [Synth 8-3886] merging instance 'pm*\_reg\_*file/registers*\_reg[13][3]' (FDCE) to 'pm\_*reg*\_file/registers\_*reg[11][3]'  
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\pm*\_reg\_*file/registers\_reg[11][3] )  
WARNING: [Synth 8-3332] Sequential element (pm*\_reg\_*file/registers\_reg[8][31]) is unused and will be removed from module cpu.  
WARNING: [Synth 8-3332] Sequential element (pm*\_reg\_*file/registers\_reg[8][30]) is unused and will be removed from module cpu.  
WARNING: [Synth 8-3332] Sequential element (pm*\_reg\_*file/registers\_reg[8][29]) is unused and will be removed from module cpu.  
WARNING: [Synth 8-3332] Sequential element (pm*\_reg\_*file/registers\_reg[8][28]) is unused and will be removed from module cpu.  
WARNING: [Synth 8-3332] Sequential element (pm*\_reg\_*file/registers\_reg[8][27]) is unused and will be removed from module cpu.  
WARNING: [Synth 8-3332] Sequential element (pm*\_reg\_*file/registers\_reg[8][26]) is unused and will be removed from module cpu.  
WARNING: [Synth 8-3332] Sequential element (pm*\_reg\_*file/registers\_reg[8][25]) is unused and will be removed from module cpu.  
WARNING: [Synth 8-3332] Sequential element (pm*\_reg\_*file/registers\_reg[8][24]) is unused and will be removed from module cpu.  
WARNING: [Synth 8-3332] Sequential element (pm*\_reg\_*file/registers\_reg[8][23]) is unused and will be removed from module cpu.  
WARNING: [Synth 8-3332] Sequential element (pm*\_reg\_*file/registers\_reg[8][22]) is unused and will be removed from module cpu.  
WARNING: [Synth 8-3332] Sequential element (pm*\_reg\_*file/registers\_reg[8][21]) is unused and will be removed from module cpu.  
WARNING: [Synth 8-3332] Sequential element (pm*\_reg\_*file/registers\_reg[8][20]) is unused and will be removed from module cpu.  
WARNING: [Synth 8-3332] Sequential element (pm*\_reg\_*file/registers\_reg[8][19]) is unused and will be removed from module cpu.  
WARNING: [Synth 8-3332] Sequential element (pm*\_reg\_*file/registers\_reg[8][18]) is unused and will be removed from module cpu.  
WARNING: [Synth 8-3332] Sequential element (pm*\_reg\_*file/registers\_reg[8][17]) is unused and will be removed from module cpu.  
WARNING: [Synth 8-3332] Sequential element (pm*\_reg\_*file/registers\_reg[8][16]) is unused and will be removed from module cpu.  
WARNING: [Synth 8-3332] Sequential element (pm*\_reg\_*file/registers\_reg[8][15]) is unused and will be removed from module cpu.  
WARNING: [Synth 8-3332] Sequential element (pm*\_reg\_*file/registers\_reg[8][14]) is unused and will be removed from module cpu.  
WARNING: [Synth 8-3332] Sequential element (pm*\_reg\_*file/registers\_reg[8][13]) is unused and will be removed from module cpu.  
WARNING: [Synth 8-3332] Sequential element (pm*\_reg\_*file/registers\_reg[8][12]) is unused and will be removed from module cpu.  
WARNING: [Synth 8-3332] Sequential element (pm*\_reg\_*file/registers\_reg[8][11]) is unused and will be removed from module cpu.  
WARNING: [Synth 8-3332] Sequential element (pm*\_reg\_*file/registers\_reg[8][10]) is unused and will be removed from module cpu.  
WARNING: [Synth 8-3332] Sequential element (pm*\_reg\_*file/registers\_reg[8][9]) is unused and will be removed from module cpu.  
WARNING: [Synth 8-3332] Sequential element (pm*\_reg\_*file/registers\_reg[8][8]) is unused and will be removed from module cpu.  
WARNING: [Synth 8-3332] Sequential element (pm*\_reg\_*file/registers\_reg[8][7]) is unused and will be removed from module cpu.  
WARNING: [Synth 8-3332] Sequential element (pm*\_reg\_*file/registers\_reg[8][6]) is unused and will be removed from module cpu.  
WARNING: [Synth 8-3332] Sequential element (pm*\_reg\_*file/registers\_reg[8][5]) is unused and will be removed from module cpu.  
WARNING: [Synth 8-3332] Sequential element (pm*\_reg\_*file/registers\_reg[8][4]) is unused and will be removed from module cpu.  
WARNING: [Synth 8-3332] Sequential element (pm*\_reg\_*file/registers\_reg[8][3]) is unused and will be removed from module cpu.  
WARNING: [Synth 8-3332] Sequential element (pm*\_reg\_*file/registers\_reg[8][2]) is unused and will be removed from module cpu.  
WARNING: [Synth 8-3332] Sequential element (pm*\_reg\_*file/registers\_reg[8][1]) is unused and will be removed from module cpu.  
WARNING: [Synth 8-3332] Sequential element (pm*\_reg\_*file/registers\_reg[8][0]) is unused and will be removed from module cpu.  
WARNING: [Synth 8-3332] Sequential element (pm*\_reg\_*file/registers\_reg[9][31]) is unused and will be removed from module cpu.  
WARNING: [Synth 8-3332] Sequential element (pm*\_reg\_*file/registers\_reg[9][30]) is unused and will be removed from module cpu.  
WARNING: [Synth 8-3332] Sequential element (pm*\_reg\_*file/registers\_reg[9][29]) is unused and will be removed from module cpu.  
WARNING: [Synth 8-3332] Sequential element (pm*\_reg\_*file/registers\_reg[9][28]) is unused and will be removed from module cpu.  
WARNING: [Synth 8-3332] Sequential element (pm*\_reg\_*file/registers\_reg[9][27]) is unused and will be removed from module cpu.  
WARNING: [Synth 8-3332] Sequential element (pm*\_reg\_*file/registers\_reg[9][26]) is unused and will be removed from module cpu.  
WARNING: [Synth 8-3332] Sequential element (pm*\_reg\_*file/registers\_reg[9][25]) is unused and will be removed from module cpu.  
WARNING: [Synth 8-3332] Sequential element (pm*\_reg\_*file/registers\_reg[9][24]) is unused and will be removed from module cpu.  
WARNING: [Synth 8-3332] Sequential element (pm*\_reg\_*file/registers\_reg[9][23]) is unused and will be removed from module cpu.  
WARNING: [Synth 8-3332] Sequential element (pm*\_reg\_*file/registers\_reg[9][22]) is unused and will be removed from module cpu.  
WARNING: [Synth 8-3332] Sequential element (pm*\_reg\_*file/registers\_reg[9][21]) is unused and will be removed from module cpu.  
WARNING: [Synth 8-3332] Sequential element (pm*\_reg\_*file/registers\_reg[9][20]) is unused and will be removed from module cpu.  
WARNING: [Synth 8-3332] Sequential element (pm*\_reg\_*file/registers\_reg[9][19]) is unused and will be removed from module cpu.  
WARNING: [Synth 8-3332] Sequential element (pm*\_reg\_*file/registers\_reg[9][18]) is unused and will be removed from module cpu.  
WARNING: [Synth 8-3332] Sequential element (pm*\_reg\_*file/registers\_reg[9][17]) is unused and will be removed from module cpu.  
WARNING: [Synth 8-3332] Sequential element (pm*\_reg\_*file/registers\_reg[9][16]) is unused and will be removed from module cpu.  
WARNING: [Synth 8-3332] Sequential element (pm*\_reg\_*file/registers\_reg[9][15]) is unused and will be removed from module cpu.  
WARNING: [Synth 8-3332] Sequential element (pm*\_reg\_*file/registers\_reg[9][14]) is unused and will be removed from module cpu.  
WARNING: [Synth 8-3332] Sequential element (pm*\_reg\_*file/registers\_reg[9][13]) is unused and will be removed from module cpu.  
WARNING: [Synth 8-3332] Sequential element (pm*\_reg\_*file/registers\_reg[9][12]) is unused and will be removed from module cpu.  
WARNING: [Synth 8-3332] Sequential element (pm*\_reg\_*file/registers\_reg[9][11]) is unused and will be removed from module cpu.  
WARNING: [Synth 8-3332] Sequential element (pm*\_reg\_*file/registers\_reg[9][10]) is unused and will be removed from module cpu.  
WARNING: [Synth 8-3332] Sequential element (pm*\_reg\_*file/registers\_reg[9][9]) is unused and will be removed from module cpu.  
WARNING: [Synth 8-3332] Sequential element (pm*\_reg\_*file/registers\_reg[9][8]) is unused and will be removed from module cpu.  
WARNING: [Synth 8-3332] Sequential element (pm*\_reg\_*file/registers\_reg[9][7]) is unused and will be removed from module cpu.  
WARNING: [Synth 8-3332] Sequential element (pm*\_reg\_*file/registers\_reg[9][6]) is unused and will be removed from module cpu.  
WARNING: [Synth 8-3332] Sequential element (pm*\_reg\_*file/registers\_reg[9][5]) is unused and will be removed from module cpu.  
WARNING: [Synth 8-3332] Sequential element (pm*\_reg\_*file/registers\_reg[9][4]) is unused and will be removed from module cpu.  
WARNING: [Synth 8-3332] Sequential element (pm*\_reg\_*file/registers\_reg[9][3]) is unused and will be removed from module cpu.  
WARNING: [Synth 8-3332] Sequential element (pm*\_reg\_*file/registers\_reg[9][2]) is unused and will be removed from module cpu.  
WARNING: [Synth 8-3332] Sequential element (pm*\_reg\_*file/registers\_reg[9][1]) is unused and will be removed from module cpu.  
WARNING: [Synth 8-3332] Sequential element (pm*\_reg\_*file/registers\_reg[9][0]) is unused and will be removed from module cpu.  
WARNING: [Synth 8-3332] Sequential element (pm*\_reg\_*file/registers\_reg[10][31]) is unused and will be removed from module cpu.  
WARNING: [Synth 8-3332] Sequential element (pm*\_reg\_*file/registers\_reg[10][30]) is unused and will be removed from module cpu.  
WARNING: [Synth 8-3332] Sequential element (pm*\_reg\_*file/registers\_reg[10][29]) is unused and will be removed from module cpu.  
WARNING: [Synth 8-3332] Sequential element (pm*\_reg\_*file/registers\_reg[10][28]) is unused and will be removed from module cpu.  
WARNING: [Synth 8-3332] Sequential element (pm*\_reg\_*file/registers\_reg[10][27]) is unused and will be removed from module cpu.  
WARNING: [Synth 8-3332] Sequential element (pm*\_reg\_*file/registers\_reg[10][26]) is unused and will be removed from module cpu.  
WARNING: [Synth 8-3332] Sequential element (pm*\_reg\_*file/registers\_reg[10][25]) is unused and will be removed from module cpu.  
WARNING: [Synth 8-3332] Sequential element (pm*\_reg\_*file/registers\_reg[10][24]) is unused and will be removed from module cpu.  
WARNING: [Synth 8-3332] Sequential element (pm*\_reg\_*file/registers\_reg[10][23]) is unused and will be removed from module cpu.  
WARNING: [Synth 8-3332] Sequential element (pm*\_reg\_*file/registers\_reg[10][22]) is unused and will be removed from module cpu.  
WARNING: [Synth 8-3332] Sequential element (pm*\_reg\_*file/registers\_reg[10][21]) is unused and will be removed from module cpu.  
WARNING: [Synth 8-3332] Sequential element (pm*\_reg\_*file/registers\_reg[10][20]) is unused and will be removed from module cpu.  
WARNING: [Synth 8-3332] Sequential element (pm*\_reg\_*file/registers\_reg[10][19]) is unused and will be removed from module cpu.  
WARNING: [Synth 8-3332] Sequential element (pm*\_reg\_*file/registers\_reg[10][18]) is unused and will be removed from module cpu.  
WARNING: [Synth 8-3332] Sequential element (pm*\_reg\_*file/registers\_reg[10][17]) is unused and will be removed from module cpu.  
WARNING: [Synth 8-3332] Sequential element (pm*\_reg\_*file/registers\_reg[10][16]) is unused and will be removed from module cpu.  
WARNING: [Synth 8-3332] Sequential element (pm*\_reg\_*file/registers\_reg[10][15]) is unused and will be removed from module cpu.  
WARNING: [Synth 8-3332] Sequential element (pm*\_reg\_*file/registers\_reg[10][14]) is unused and will be removed from module cpu.  
WARNING: [Synth 8-3332] Sequential element (pm*\_reg\_*file/registers\_reg[10][13]) is unused and will be removed from module cpu.  
WARNING: [Synth 8-3332] Sequential element (pm*\_reg\_*file/registers\_reg[10][12]) is unused and will be removed from module cpu.  
WARNING: [Synth 8-3332] Sequential element (pm*\_reg\_*file/registers\_reg[10][11]) is unused and will be removed from module cpu.  
WARNING: [Synth 8-3332] Sequential element (pm*\_reg\_*file/registers\_reg[10][10]) is unused and will be removed from module cpu.  
WARNING: [Synth 8-3332] Sequential element (pm*\_reg\_*file/registers\_reg[10][9]) is unused and will be removed from module cpu.  
WARNING: [Synth 8-3332] Sequential element (pm*\_reg\_*file/registers\_reg[10][8]) is unused and will be removed from module cpu.  
WARNING: [Synth 8-3332] Sequential element (pm*\_reg\_*file/registers\_reg[10][7]) is unused and will be removed from module cpu.  
WARNING: [Synth 8-3332] Sequential element (pm*\_reg\_*file/registers\_reg[10][6]) is unused and will be removed from module cpu.  
WARNING: [Synth 8-3332] Sequential element (pm*\_reg\_*file/registers\_reg[10][5]) is unused and will be removed from module cpu.  
WARNING: [Synth 8-3332] Sequential element (pm*\_reg\_*file/registers\_reg[10][4]) is unused and will be removed from module cpu.  
WARNING: [Synth 8-3332] Sequential element (pm*\_reg\_*file/registers\_reg[10][3]) is unused and will be removed from module cpu.  
WARNING: [Synth 8-3332] Sequential element (pm*\_reg\_*file/registers\_reg[10][2]) is unused and will be removed from module cpu.  
WARNING: [Synth 8-3332] Sequential element (pm*\_reg\_*file/registers\_reg[10][1]) is unused and will be removed from module cpu.  
WARNING: [Synth 8-3332] Sequential element (pm*\_reg\_*file/registers\_reg[10][0]) is unused and will be removed from module cpu.  
WARNING: [Synth 8-3332] Sequential element (pm*\_reg\_*file/registers\_reg[12][31]) is unused and will be removed from module cpu.  
WARNING: [Synth 8-3332] Sequential element (pm*\_reg\_*file/registers\_reg[12][30]) is unused and will be removed from module cpu.  
WARNING: [Synth 8-3332] Sequential element (pm*\_reg\_*file/registers\_reg[12][29]) is unused and will be removed from module cpu.  
WARNING: [Synth 8-3332] Sequential element (pm*\_reg\_*file/registers\_reg[12][28]) is unused and will be removed from module cpu.  
INFO: [Common 17-14] Message 'Synth 8-3332' appears 100 times and further instances of the messages will be disabled. Use the Tcl command set*\_msg\_*config to change the current settings.  
---------------------------------------------------------------------------------  
Finished Cross Boundary and Area Optimization : Time (s): cpu = 00:00:28 ; elapsed = 00:01:20 . Memory (MB): peak = 1908.156 ; gain = 526.293 ; free physical = 70786 ; free virtual = 153698  
---------------------------------------------------------------------------------  
  
Report RTL Partitions:   
+-+--------------+------------+----------+  
| |RTL Partition |Replication |Instances |  
+-+--------------+------------+----------+  
+-+--------------+------------+----------+  
---------------------------------------------------------------------------------  
Start Applying XDC Timing Constraints  
---------------------------------------------------------------------------------  
---------------------------------------------------------------------------------  
Finished Applying XDC Timing Constraints : Time (s): cpu = 00:00:35 ; elapsed = 00:01:39 . Memory (MB): peak = 1908.156 ; gain = 526.293 ; free physical = 70656 ; free virtual = 153568  
---------------------------------------------------------------------------------  
---------------------------------------------------------------------------------  
Start Timing Optimization  
---------------------------------------------------------------------------------  
---------------------------------------------------------------------------------  
Finished Timing Optimization : Time (s): cpu = 00:00:37 ; elapsed = 00:01:40 . Memory (MB): peak = 1908.156 ; gain = 526.293 ; free physical = 70658 ; free virtual = 153570  
---------------------------------------------------------------------------------  
  
Report RTL Partitions:   
+-+--------------+------------+----------+  
| |RTL Partition |Replication |Instances |  
+-+--------------+------------+----------+  
+-+--------------+------------+----------+  
---------------------------------------------------------------------------------  
Start Technology Mapping  
---------------------------------------------------------------------------------  
INFO: [Synth 8-3886] merging instance 'pm*\_reg\_*file/registers*\_reg[6][8]' (FDCE) to 'pm\_*reg*\_file/registers\_*reg[7][8]'  
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\pm*\_reg\_*file/registers\_reg[7][8] )  
INFO: [Synth 8-3886] merging instance 'pm*\_reg\_*file/registers*\_reg[6][9]' (FDCE) to 'pm\_*reg*\_file/registers\_*reg[7][9]'  
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\pm*\_reg\_*file/registers\_reg[7][9] )  
INFO: [Synth 8-3886] merging instance 'pm*\_reg\_*file/registers*\_reg[6][10]' (FDCE) to 'pm\_*reg*\_file/registers\_*reg[7][10]'  
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\pm*\_reg\_*file/registers\_reg[7][10] )  
INFO: [Synth 8-3886] merging instance 'pm*\_reg\_*file/registers*\_reg[6][11]' (FDCE) to 'pm\_*reg*\_file/registers\_*reg[7][11]'  
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\pm*\_reg\_*file/registers\_reg[7][11] )  
INFO: [Synth 8-3886] merging instance 'pm*\_reg\_*file/registers*\_reg[6][20]' (FDCE) to 'pm\_*reg*\_file/registers\_*reg[7][20]'  
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\pm*\_reg\_*file/registers\_reg[7][20] )  
INFO: [Synth 8-3886] merging instance 'pm*\_reg\_*file/registers*\_reg[6][21]' (FDCE) to 'pm\_*reg*\_file/registers\_*reg[7][21]'  
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\pm*\_reg\_*file/registers\_reg[7][21] )  
INFO: [Synth 8-3886] merging instance 'pm*\_reg\_*file/registers*\_reg[6][22]' (FDCE) to 'pm\_*reg*\_file/registers\_*reg[7][22]'  
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\pm*\_reg\_*file/registers\_reg[7][22] )  
INFO: [Synth 8-3886] merging instance 'pm*\_reg\_*file/registers*\_reg[6][23]' (FDCE) to 'pm\_*reg*\_file/registers\_*reg[7][23]'  
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\pm*\_reg\_*file/registers\_reg[7][23] )  
INFO: [Synth 8-3886] merging instance 'pm*\_reg\_*file/registers*\_reg[6][4]' (FDCE) to 'pm\_*reg*\_file/registers\_*reg[7][4]'  
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\pm*\_reg\_*file/registers\_reg[7][4] )  
INFO: [Synth 8-3886] merging instance 'pm*\_reg\_*file/registers*\_reg[6][5]' (FDCE) to 'pm\_*reg*\_file/registers\_*reg[7][5]'  
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\pm*\_reg\_*file/registers\_reg[7][5] )  
INFO: [Synth 8-3886] merging instance 'pm*\_reg\_*file/registers*\_reg[6][6]' (FDCE) to 'pm\_*reg*\_file/registers\_*reg[7][6]'  
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\pm*\_reg\_*file/registers\_reg[7][6] )  
INFO: [Synth 8-3886] merging instance 'pm*\_reg\_*file/registers*\_reg[6][7]' (FDCE) to 'pm\_*reg*\_file/registers\_*reg[7][7]'  
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\pm*\_reg\_*file/registers\_reg[7][7] )  
INFO: [Synth 8-3886] merging instance 'pm*\_reg\_*file/registers*\_reg[6][12]' (FDCE) to 'pm\_*reg*\_file/registers\_*reg[7][12]'  
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\pm*\_reg\_*file/registers\_reg[7][12] )  
INFO: [Synth 8-3886] merging instance 'pm*\_reg\_*file/registers*\_reg[6][13]' (FDCE) to 'pm\_*reg*\_file/registers\_*reg[7][13]'  
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\pm*\_reg\_*file/registers\_reg[7][13] )  
INFO: [Synth 8-3886] merging instance 'pm*\_reg\_*file/registers*\_reg[6][14]' (FDCE) to 'pm\_*reg*\_file/registers\_*reg[7][14]'  
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\pm*\_reg\_*file/registers\_reg[7][14] )  
INFO: [Synth 8-3886] merging instance 'pm*\_reg\_*file/registers*\_reg[6][15]' (FDCE) to 'pm\_*reg*\_file/registers\_*reg[7][15]'  
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\pm*\_reg\_*file/registers\_reg[7][15] )  
INFO: [Synth 8-3886] merging instance 'pm*\_reg\_*file/registers*\_reg[6][16]' (FDCE) to 'pm\_*reg*\_file/registers\_*reg[7][16]'  
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\pm*\_reg\_*file/registers\_reg[7][16] )  
INFO: [Synth 8-3886] merging instance 'pm*\_reg\_*file/registers*\_reg[6][17]' (FDCE) to 'pm\_*reg*\_file/registers\_*reg[7][17]'  
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\pm*\_reg\_*file/registers\_reg[7][17] )  
INFO: [Synth 8-3886] merging instance 'pm*\_reg\_*file/registers*\_reg[6][18]' (FDCE) to 'pm\_*reg*\_file/registers\_*reg[7][18]'  
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\pm*\_reg\_*file/registers\_reg[7][18] )  
INFO: [Synth 8-3886] merging instance 'pm*\_reg\_*file/registers*\_reg[6][19]' (FDCE) to 'pm\_*reg*\_file/registers\_*reg[7][19]'  
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\pm*\_reg\_*file/registers\_reg[7][19] )  
INFO: [Synth 8-3886] merging instance 'pm*\_reg\_*file/registers*\_reg[6][24]' (FDCE) to 'pm\_*reg*\_file/registers\_*reg[7][24]'  
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\pm*\_reg\_*file/registers\_reg[7][24] )  
INFO: [Synth 8-3886] merging instance 'pm*\_reg\_*file/registers*\_reg[6][25]' (FDCE) to 'pm\_*reg*\_file/registers\_*reg[7][25]'  
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\pm*\_reg\_*file/registers\_reg[7][25] )  
INFO: [Synth 8-3886] merging instance 'pm*\_reg\_*file/registers*\_reg[6][26]' (FDCE) to 'pm\_*reg*\_file/registers\_*reg[7][26]'  
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\pm*\_reg\_*file/registers\_reg[7][26] )  
INFO: [Synth 8-3886] merging instance 'pm*\_reg\_*file/registers*\_reg[6][27]' (FDCE) to 'pm\_*reg*\_file/registers\_*reg[7][27]'  
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\pm*\_reg\_*file/registers\_reg[7][27] )  
INFO: [Synth 8-3886] merging instance 'pm*\_reg\_*file/registers*\_reg[6][28]' (FDCE) to 'pm\_*reg*\_file/registers\_*reg[7][28]'  
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\pm*\_reg\_*file/registers\_reg[7][28] )  
INFO: [Synth 8-3886] merging instance 'pm*\_reg\_*file/registers*\_reg[6][29]' (FDCE) to 'pm\_*reg*\_file/registers\_*reg[7][29]'  
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\pm*\_reg\_*file/registers\_reg[7][29] )  
INFO: [Synth 8-3886] merging instance 'pm*\_reg\_*file/registers*\_reg[6][30]' (FDCE) to 'pm\_*reg*\_file/registers\_*reg[7][30]'  
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\pm*\_reg\_*file/registers\_reg[7][30] )  
INFO: [Synth 8-3886] merging instance 'pm*\_reg\_*file/registers*\_reg[6][31]' (FDCE) to 'pm\_*reg*\_file/registers\_*reg[7][31]'  
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\pm*\_reg\_*file/registers\_reg[7][31] )  
INFO: [Synth 8-3886] merging instance 'pm*\_reg\_*file/registers*\_reg[6][0]' (FDCE) to 'pm\_*reg*\_file/registers\_*reg[7][0]'  
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\pm*\_reg\_*file/registers\_reg[7][0] )  
INFO: [Synth 8-3886] merging instance 'pm*\_reg\_*file/registers*\_reg[6][1]' (FDCE) to 'pm\_*reg*\_file/registers\_*reg[7][1]'  
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\pm*\_reg\_*file/registers\_reg[7][1] )  
INFO: [Synth 8-3886] merging instance 'pm*\_reg\_*file/registers*\_reg[6][2]' (FDCE) to 'pm\_*reg*\_file/registers\_*reg[7][2]'  
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\pm*\_reg\_*file/registers\_reg[7][2] )  
INFO: [Synth 8-3886] merging instance 'pm*\_reg\_*file/registers*\_reg[6][3]' (FDCE) to 'pm\_*reg*\_file/registers\_*reg[7][3]'  
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\pm*\_reg\_*file/registers\_reg[7][3] )  
---------------------------------------------------------------------------------  
Finished Technology Mapping : Time (s): cpu = 00:00:38 ; elapsed = 00:01:41 . Memory (MB): peak = 1923.773 ; gain = 541.910 ; free physical = 70658 ; free virtual = 153570  
---------------------------------------------------------------------------------  
  
Report RTL Partitions:   
+-+--------------+------------+----------+  
| |RTL Partition |Replication |Instances |  
+-+--------------+------------+----------+  
+-+--------------+------------+----------+  
---------------------------------------------------------------------------------  
Start IO Insertion  
---------------------------------------------------------------------------------  
---------------------------------------------------------------------------------  
Start Flattening Before IO Insertion  
---------------------------------------------------------------------------------  
---------------------------------------------------------------------------------  
Finished Flattening Before IO Insertion  
---------------------------------------------------------------------------------  
---------------------------------------------------------------------------------  
Start Final Netlist Cleanup  
---------------------------------------------------------------------------------  
---------------------------------------------------------------------------------  
Finished Final Netlist Cleanup  
---------------------------------------------------------------------------------  
---------------------------------------------------------------------------------  
Finished IO Insertion : Time (s): cpu = 00:00:38 ; elapsed = 00:01:42 . Memory (MB): peak = 1923.777 ; gain = 541.914 ; free physical = 70658 ; free virtual = 153570  
---------------------------------------------------------------------------------  
  
Report Check Netlist:   
+------+------------------+-------+---------+-------+------------------+  
| |Item |Errors |Warnings |Status |Description |  
+------+------------------+-------+---------+-------+------------------+  
|1 |multi*\_driven\_*nets | 0| 0|Passed |Multi driven nets |  
+------+------------------+-------+---------+-------+------------------+  
---------------------------------------------------------------------------------  
Start Renaming Generated Instances  
---------------------------------------------------------------------------------  
---------------------------------------------------------------------------------  
Finished Renaming Generated Instances : Time (s): cpu = 00:00:38 ; elapsed = 00:01:42 . Memory (MB): peak = 1923.777 ; gain = 541.914 ; free physical = 70658 ; free virtual = 153570  
---------------------------------------------------------------------------------  
  
Report RTL Partitions:   
+-+--------------+------------+----------+  
| |RTL Partition |Replication |Instances |  
+-+--------------+------------+----------+  
+-+--------------+------------+----------+  
---------------------------------------------------------------------------------  
Start Rebuilding User Hierarchy  
---------------------------------------------------------------------------------  
---------------------------------------------------------------------------------  
Finished Rebuilding User Hierarchy : Time (s): cpu = 00:00:38 ; elapsed = 00:01:42 . Memory (MB): peak = 1923.777 ; gain = 541.914 ; free physical = 70658 ; free virtual = 153570  
---------------------------------------------------------------------------------  
---------------------------------------------------------------------------------  
Start Renaming Generated Ports  
---------------------------------------------------------------------------------  
---------------------------------------------------------------------------------  
Finished Renaming Generated Ports : Time (s): cpu = 00:00:38 ; elapsed = 00:01:42 . Memory (MB): peak = 1923.777 ; gain = 541.914 ; free physical = 70658 ; free virtual = 153570  
---------------------------------------------------------------------------------  
---------------------------------------------------------------------------------  
Start Handling Custom Attributes  
---------------------------------------------------------------------------------  
---------------------------------------------------------------------------------  
Finished Handling Custom Attributes : Time (s): cpu = 00:00:38 ; elapsed = 00:01:42 . Memory (MB): peak = 1923.777 ; gain = 541.914 ; free physical = 70658 ; free virtual = 153570  
---------------------------------------------------------------------------------  
---------------------------------------------------------------------------------  
Start Renaming Generated Nets  
---------------------------------------------------------------------------------  
---------------------------------------------------------------------------------  
Finished Renaming Generated Nets : Time (s): cpu = 00:00:38 ; elapsed = 00:01:42 . Memory (MB): peak = 1923.777 ; gain = 541.914 ; free physical = 70658 ; free virtual = 153570  
---------------------------------------------------------------------------------  
---------------------------------------------------------------------------------  
Start Writing Synthesis Report  
---------------------------------------------------------------------------------  
  
Report BlackBoxes:   
+-+--------------+----------+  
| |BlackBox name |Instances |  
+-+--------------+----------+  
+-+--------------+----------+  
  
Report Cell Usage:   
+------+-------+------+  
| |Cell |Count |  
+------+-------+------+  
|1 |BUFG | 1|  
|2 |CARRY4 | 13|  
|3 |LUT2 | 13|  
|4 |LUT3 | 1|  
|5 |LUT4 | 65|  
|6 |LUT5 | 125|  
|7 |LUT6 | 451|  
|8 |MUXF7 | 163|  
|9 |MUXF8 | 62|  
|10 |FDCE | 1221|  
|11 |IBUF | 2|  
|12 |OBUF | 14|  
+------+-------+------+  
  
Report Instance Areas:   
+------+------------------+-------------+------+  
| |Instance |Module |Cells |  
+------+------------------+-------------+------+  
|1 |top | | 2131|  
|2 | pm\_alu |alu | 17|  
|3 | pm*\_d\_*cache |d\_cache | 1470|  
|4 | pm*\_next\_*address |next\_address | 2|  
|5 | pm\_pc |pc | 369|  
|6 | pm*\_reg\_*file |regfile | 256|  
+------+------------------+-------------+------+  
---------------------------------------------------------------------------------  
Finished Writing Synthesis Report : Time (s): cpu = 00:00:38 ; elapsed = 00:01:42 . Memory (MB): peak = 1923.777 ; gain = 541.914 ; free physical = 70658 ; free virtual = 153570  
---------------------------------------------------------------------------------  
Synthesis finished with 0 errors, 0 critical warnings and 829 warnings.  
Synthesis Optimization Runtime : Time (s): cpu = 00:00:28 ; elapsed = 00:00:46 . Memory (MB): peak = 1923.777 ; gain = 162.004 ; free physical = 70712 ; free virtual = 153624  
Synthesis Optimization Complete : Time (s): cpu = 00:00:38 ; elapsed = 00:01:42 . Memory (MB): peak = 1923.781 ; gain = 541.914 ; free physical = 70723 ; free virtual = 153635  
INFO: [Project 1-571] Translating synthesized netlist  
INFO: [Netlist 29-17] Analyzing 240 Unisim elements for replacement  
INFO: [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds  
INFO: [Project 1-570] Preparing netlist for logic optimization  
INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).  
INFO: [Project 1-111] Unisim Transformation Summary:  
No Unisim elements were transformed.  
  
INFO: [Common 17-83] Releasing license: Synthesis  
267 Infos, 104 Warnings, 0 Critical Warnings and 0 Errors encountered.  
synth\_design completed successfully  
synth\_design: Time (s): cpu = 00:00:40 ; elapsed = 00:01:44 . Memory (MB): peak = 1955.793 ; gain = 586.656 ; free physical = 70709 ; free virtual = 153621  
WARNING: [Constraints 18-5210] No constraint will be written out.  
INFO: [Common 17-1381] The checkpoint '/nfs/home/l/l*\_heiwan/coen316/lab4/vivado/part2/lab4\_*part2/lab4*\_part2.runs/synth\_*1/cpu.dcp' has been generated.  
INFO: [runtcl-4] Executing : report*\_utilization -file cpu\_*utilization*\_synth.rpt -pb cpu\_*utilization\_synth.pb  
report\_utilization: Time (s): cpu = 00:00:00.07 ; elapsed = 00:00:00.14 . Memory (MB): peak = 1979.812 ; gain = 0.000 ; free physical = 70708 ; free virtual = 153620  
INFO: [Common 17-206] Exiting Vivado at Wed Nov 22 20:05:28 2023...

**5.4) Implementation Log**

\*\*\* Running vivado  
 with args -log cpu.vdi -applog -m64 -product Vivado -messageDb vivado.pb -mode batch -source cpu.tcl -notrace  
  
  
\*\*\*\*\*\* Vivado v2018.2 (64-bit)  
 \*\*\*\* SW Build 2258646 on Thu Jun 14 20:02:38 MDT 2018  
 \*\*\*\* IP Build 2256618 on Thu Jun 14 22:10:49 MDT 2018  
 \*\* Copyright 1986-2018 Xilinx, Inc. All Rights Reserved.  
  
source cpu.tcl -notrace  
Command: link\_design -top cpu -part xc7a100tcsg324-1  
Design **is** defaulting to srcset: sources\_1  
Design **is** defaulting to constrset: constrs\_1  
INFO: [Netlist 29-17] Analyzing 240 Unisim elements **for** replacement  
INFO: [Netlist 29-28] Unisim Transformation completed **in** 0 CPU seconds  
INFO: [Project 1-479] Netlist was created with Vivado 2018.2  
INFO: [Device 21-403] Loading part xc7a100tcsg324-1  
INFO: [Project 1-570] Preparing netlist **for** logic optimization  
Parsing XDC File [/nfs/home/l/l\_heiwan/coen316/lab4/givenToUs/cpu.xdc]  
Finished Parsing XDC File [/nfs/home/l/l\_heiwan/coen316/lab4/givenToUs/cpu.xdc]  
INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).  
INFO: [Project 1-111] Unisim Transformation Summary:  
No Unisim elements were transformed.  
  
7 Infos, 0 Warnings, 0 Critical Warnings **and** 0 Errors encountered.  
link\_design completed successfully  
link\_design: Time (s): cpu = 00:00:11 ; elapsed = 00:00:58 . Memory (MB): peak = 1704.566 ; gain = 330.414 ; free physical = 70839 ; free virtual = 153748  
Command: opt\_design  
Attempting to **get** a license **for** feature 'Implementation' **and**/**or** device 'xc7a100t'  
INFO: [Common 17-349] Got license **for** feature 'Implementation' **and**/**or** device 'xc7a100t'  
Running DRC as a precondition to command opt\_design  
  
Starting DRC Task  
INFO: [DRC 23-27] Running DRC with 8 threads  
INFO: [Project 1-461] DRC finished with 0 Errors  
INFO: [Project 1-462] Please refer to the DRC report (report\_drc) **for** more information.  
  
Time (s): cpu = 00:00:02 ; elapsed = 00:00:04 . Memory (MB): peak = 1778.594 ; gain = 74.027 ; free physical = 70828 ; free virtual = 153737  
  
Starting Cache Timing Information Task  
INFO: [Timing 38-35] Done setting XDC timing constraints.  
Ending Cache Timing Information Task | Checksum: 132e5b778  
  
Time (s): cpu = 00:00:15 ; elapsed = 00:01:08 . Memory (MB): peak = 2251.094 ; gain = 472.500 ; free physical = 70383 ; free virtual = 153292  
  
Starting Logic Optimization Task  
  
Phase 1 Retarget  
INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).  
INFO: [Opt 31-49] Retargeted 0 cell(s).  
Phase 1 Retarget | Checksum: 132e5b778  
  
Time (s): cpu = 00:00:00.14 ; elapsed = 00:00:00.09 . Memory (MB): peak = 2251.094 ; gain = 0.000 ; free physical = 70399 ; free virtual = 153308  
INFO: [Opt 31-389] Phase Retarget created 0 cells **and** removed 0 cells  
  
Phase 2 Constant propagation  
INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).  
Phase 2 Constant propagation | Checksum: 132e5b778  
  
Time (s): cpu = 00:00:00.18 ; elapsed = 00:00:00.12 . Memory (MB): peak = 2251.094 ; gain = 0.000 ; free physical = 70399 ; free virtual = 153308  
INFO: [Opt 31-389] Phase Constant propagation created 0 cells **and** removed 0 cells  
  
Phase 3 Sweep  
Phase 3 Sweep | Checksum: 120e2a9de  
  
Time (s): cpu = 00:00:00.20 ; elapsed = 00:00:00.15 . Memory (MB): peak = 2251.094 ; gain = 0.000 ; free physical = 70399 ; free virtual = 153308  
INFO: [Opt 31-389] Phase Sweep created 0 cells **and** removed 0 cells  
  
Phase 4 BUFG optimization  
Phase 4 BUFG optimization | Checksum: 120e2a9de  
  
Time (s): cpu = 00:00:00.23 ; elapsed = 00:00:00.18 . Memory (MB): peak = 2251.094 ; gain = 0.000 ; free physical = 70399 ; free virtual = 153308  
INFO: [Opt 31-662] Phase BUFG optimization created 0 cells of which 0 are BUFGs **and** removed 0 cells.  
  
Phase 5 Shift Register Optimization  
Phase 5 Shift Register Optimization | Checksum: 15f26dba6  
  
Time (s): cpu = 00:00:00.26 ; elapsed = 00:00:00.21 . Memory (MB): peak = 2251.094 ; gain = 0.000 ; free physical = 70399 ; free virtual = 153308  
INFO: [Opt 31-389] Phase Shift Register Optimization created 0 cells **and** removed 0 cells  
  
Phase 6 Post Processing Netlist  
Phase 6 Post Processing Netlist | Checksum: 15f26dba6  
  
Time (s): cpu = 00:00:00.27 ; elapsed = 00:00:00.22 . Memory (MB): peak = 2251.094 ; gain = 0.000 ; free physical = 70399 ; free virtual = 153308  
INFO: [Opt 31-389] Phase Post Processing Netlist created 0 cells **and** removed 0 cells  
  
Starting Connectivity Check Task  
  
Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2251.094 ; gain = 0.000 ; free physical = 70399 ; free virtual = 153308  
Ending Logic Optimization Task | Checksum: 15f26dba6  
  
Time (s): cpu = 00:00:00.28 ; elapsed = 00:00:00.23 . Memory (MB): peak = 2251.094 ; gain = 0.000 ; free physical = 70399 ; free virtual = 153308  
  
Starting Power Optimization Task  
INFO: [Pwropt 34-132] Skipping clock gating **for** clocks with a period < 2.00 ns.  
Ending Power Optimization Task | Checksum: 15f26dba6  
  
Time (s): cpu = 00:00:00.02 ; elapsed = 00:00:00.06 . Memory (MB): peak = 2251.094 ; gain = 0.000 ; free physical = 70399 ; free virtual = 153308  
  
Starting Final Cleanup Task  
Ending Final Cleanup Task | Checksum: 15f26dba6  
  
Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2251.094 ; gain = 0.000 ; free physical = 70399 ; free virtual = 153308  
INFO: [Common 17-83] Releasing license: Implementation  
23 Infos, 0 Warnings, 0 Critical Warnings **and** 0 Errors encountered.  
opt\_design completed successfully  
opt\_design: Time (s): cpu = 00:00:17 ; elapsed = 00:01:12 . Memory (MB): peak = 2251.094 ; gain = 546.527 ; free physical = 70399 ; free virtual = 153308  
INFO: [Timing 38-480] Writing timing data to binary archive.  
Writing placer database...  
Writing XDEF routing.  
Writing XDEF routing logical nets.  
Writing XDEF routing special nets.  
Write XDEF Complete: Time (s): cpu = 00:00:00.06 ; elapsed = 00:00:00.02 . Memory (MB): peak = 2283.105 ; gain = 0.000 ; free physical = 70395 ; free virtual = 153305  
INFO: [Common 17-1381] The checkpoint '/nfs/home/l/l\_heiwan/coen316/lab4/vivado/part2/lab4\_part2/lab4\_part2.runs/impl\_1/cpu\_opt.dcp' has been generated.  
INFO: [runtcl-4] Executing : report\_drc -file cpu\_drc\_opted.rpt -pb cpu\_drc\_opted.pb -rpx cpu\_drc\_opted.rpx  
Command: report\_drc -file cpu\_drc\_opted.rpt -pb cpu\_drc\_opted.pb -rpx cpu\_drc\_opted.rpx  
INFO: [IP\_Flow 19-234] Refreshing IP repositories  
INFO: [IP\_Flow 19-1704] No user IP repositories specified  
INFO: [IP\_Flow 19-2313] Loaded Vivado IP repository '/CMC/tools/xilinx/Vivado\_2018.2/Vivado/2018.2/data/ip'.  
INFO: [DRC 23-27] Running DRC with 8 threads  
INFO: [Coretcl 2-168] The results of DRC are **in** file /nfs/home/l/l\_heiwan/coen316/lab4/vivado/part2/lab4\_part2/lab4\_part2.runs/impl\_1/cpu\_drc\_opted.rpt.  
report\_drc completed successfully  
report\_drc: Time (s): cpu = 00:00:04 ; elapsed = 00:00:07 . Memory (MB): peak = 2363.148 ; gain = 80.031 ; free physical = 70401 ; free virtual = 153310  
Command: place\_design  
Attempting to **get** a license **for** feature 'Implementation' **and**/**or** device 'xc7a100t'  
INFO: [Common 17-349] Got license **for** feature 'Implementation' **and**/**or** device 'xc7a100t'  
INFO: [DRC 23-27] Running DRC with 8 threads  
INFO: [Vivado\_Tcl 4-198] DRC finished with 0 Errors  
INFO: [Vivado\_Tcl 4-199] Please refer to the DRC report (report\_drc) **for** more information.  
Running DRC as a precondition to command place\_design  
INFO: [DRC 23-27] Running DRC with 8 threads  
INFO: [Vivado\_Tcl 4-198] DRC finished with 0 Errors  
INFO: [Vivado\_Tcl 4-199] Please refer to the DRC report (report\_drc) **for** more information.  
  
Starting Placer Task  
INFO: [Place 30-611] Multithreading enabled **for** place\_design using a maximum of 8 CPUs  
  
Phase 1 Placer Initialization  
  
Phase 1.1 Placer Initialization Netlist Sorting  
Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2363.148 ; gain = 0.000 ; free physical = 70392 ; free virtual = 153302  
Phase 1.1 Placer Initialization Netlist Sorting | Checksum: ca97ba35  
  
Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00.02 . Memory (MB): peak = 2363.148 ; gain = 0.000 ; free physical = 70392 ; free virtual = 153302  
Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.01 . Memory (MB): peak = 2363.148 ; gain = 0.000 ; free physical = 70392 ; free virtual = 153302  
  
Phase 1.2 IO Placement/ Clock Placement/ Build Placer Device  
INFO: [Timing 38-35] Done setting XDC timing constraints.  
WARNING: [Place 30-574] Poor placement **for** routing between an IO pin **and** BUFG. This **is** normally an ERROR but the CLOCK\_DEDICATED\_ROUTE constraint **is** **set** to FALSE allowing your design to **continue**. The use of **this** **override** **is** highly discouraged as it may lead to very poor timing results. It **is** recommended that **this** error condition be corrected **in** the design.  
  
 clk\_IBUF\_inst (IBUF.O) **is** locked to IOB\_X0Y82  
 clk\_IBUF\_BUFG\_inst (BUFG.I) **is** provisionally placed by clockplacer on BUFGCTRL\_X0Y0  
Resolution: Poor placement of an IO pin **and** a BUFG has resulted **in** the router using a non-dedicated path between the two. There are several things that could trigger **this** DRC, each of which can cause unpredictable clock insertion delays that result **in** poor timing. This DRC could be caused by any of the following: (a) a clock port was placed on a pin that **is** **not** a CCIO-pin (b)the BUFG has **not** been placed **in** the same half of the device **or** SLR as the CCIO-pin (c) a single ended clock has been placed on the N-Side of a differential pair CCIO-pin.  
Phase 1.2 IO Placement/ Clock Placement/ Build Placer Device | Checksum: 4eb80967  
  
Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.85 . Memory (MB): peak = 2363.148 ; gain = 0.000 ; free physical = 70390 ; free virtual = 153300  
  
Phase 1.3 Build Placer Netlist Model  
Phase 1.3 Build Placer Netlist Model | Checksum: 14e35c75a  
  
Time (s): cpu = 00:00:02 ; elapsed = 00:00:00.92 . Memory (MB): peak = 2363.148 ; gain = 0.000 ; free physical = 70391 ; free virtual = 153301  
  
Phase 1.4 Constrain Clocks/Macros  
Phase 1.4 Constrain Clocks/Macros | Checksum: 14e35c75a  
  
Time (s): cpu = 00:00:02 ; elapsed = 00:00:00.92 . Memory (MB): peak = 2363.148 ; gain = 0.000 ; free physical = 70391 ; free virtual = 153301  
Phase 1 Placer Initialization | Checksum: 14e35c75a  
  
Time (s): cpu = 00:00:02 ; elapsed = 00:00:00.93 . Memory (MB): peak = 2363.148 ; gain = 0.000 ; free physical = 70391 ; free virtual = 153301  
  
Phase 2 Global Placement  
  
Phase 2.1 Floorplanning  
Phase 2.1 Floorplanning | Checksum: 14e35c75a  
  
Time (s): cpu = 00:00:02 ; elapsed = 00:00:00.95 . Memory (MB): peak = 2363.148 ; gain = 0.000 ; free physical = 70395 ; free virtual = 153304  
WARNING: [Place 46-29] place\_design **is** **not** **in** timing mode. Skip physical synthesis **in** placer  
Phase 2 Global Placement | Checksum: fc646420  
  
Time (s): cpu = 00:00:09 ; elapsed = 00:00:03 . Memory (MB): peak = 2418.168 ; gain = 55.020 ; free physical = 70353 ; free virtual = 153262  
  
Phase 3 Detail Placement  
  
Phase 3.1 Commit Multi Column Macros  
Phase 3.1 Commit Multi Column Macros | Checksum: fc646420  
  
Time (s): cpu = 00:00:09 ; elapsed = 00:00:03 . Memory (MB): peak = 2418.168 ; gain = 55.020 ; free physical = 70353 ; free virtual = 153262  
  
Phase 3.2 Commit Most Macros & LUTRAMs  
Phase 3.2 Commit Most Macros & LUTRAMs | Checksum: 120db6594  
  
Time (s): cpu = 00:00:09 ; elapsed = 00:00:03 . Memory (MB): peak = 2418.168 ; gain = 55.020 ; free physical = 70352 ; free virtual = 153262  
  
Phase 3.3 Area Swap Optimization  
Phase 3.3 Area Swap Optimization | Checksum: 12cbbff89  
  
Time (s): cpu = 00:00:09 ; elapsed = 00:00:03 . Memory (MB): peak = 2418.168 ; gain = 55.020 ; free physical = 70352 ; free virtual = 153262  
  
Phase 3.4 Pipeline Register Optimization  
Phase 3.4 Pipeline Register Optimization | Checksum: 12cbbff89  
  
Time (s): cpu = 00:00:09 ; elapsed = 00:00:03 . Memory (MB): peak = 2418.168 ; gain = 55.020 ; free physical = 70352 ; free virtual = 153262  
  
Phase 3.5 Small Shape Detail Placement  
Phase 3.5 Small Shape Detail Placement | Checksum: 144f226f7  
  
Time (s): cpu = 00:00:10 ; elapsed = 00:00:04 . Memory (MB): peak = 2418.168 ; gain = 55.020 ; free physical = 70354 ; free virtual = 153264  
  
Phase 3.6 Re-assign LUT pins  
Phase 3.6 Re-assign LUT pins | Checksum: 144f226f7  
  
Time (s): cpu = 00:00:10 ; elapsed = 00:00:04 . Memory (MB): peak = 2418.168 ; gain = 55.020 ; free physical = 70354 ; free virtual = 153264  
  
Phase 3.7 Pipeline Register Optimization  
Phase 3.7 Pipeline Register Optimization | Checksum: 144f226f7  
  
Time (s): cpu = 00:00:10 ; elapsed = 00:00:04 . Memory (MB): peak = 2418.168 ; gain = 55.020 ; free physical = 70354 ; free virtual = 153264  
Phase 3 Detail Placement | Checksum: 144f226f7  
  
Time (s): cpu = 00:00:10 ; elapsed = 00:00:04 . Memory (MB): peak = 2418.168 ; gain = 55.020 ; free physical = 70354 ; free virtual = 153264  
  
Phase 4 Post Placement Optimization **and** Clean-Up  
  
Phase 4.1 Post Commit Optimization  
Phase 4.1 Post Commit Optimization | Checksum: 144f226f7  
  
Time (s): cpu = 00:00:10 ; elapsed = 00:00:04 . Memory (MB): peak = 2418.168 ; gain = 55.020 ; free physical = 70354 ; free virtual = 153264  
  
Phase 4.2 Post Placement Cleanup  
Phase 4.2 Post Placement Cleanup | Checksum: 144f226f7  
  
Time (s): cpu = 00:00:10 ; elapsed = 00:00:04 . Memory (MB): peak = 2418.168 ; gain = 55.020 ; free physical = 70354 ; free virtual = 153263  
  
Phase 4.3 Placer Reporting  
Phase 4.3 Placer Reporting | Checksum: 144f226f7  
  
Time (s): cpu = 00:00:10 ; elapsed = 00:00:04 . Memory (MB): peak = 2418.168 ; gain = 55.020 ; free physical = 70354 ; free virtual = 153263  
  
Phase 4.4 Final Placement Cleanup  
Phase 4.4 Final Placement Cleanup | Checksum: 1b809c133  
  
Time (s): cpu = 00:00:10 ; elapsed = 00:00:04 . Memory (MB): peak = 2418.168 ; gain = 55.020 ; free physical = 70354 ; free virtual = 153263  
Phase 4 Post Placement Optimization **and** Clean-Up | Checksum: 1b809c133  
  
Time (s): cpu = 00:00:10 ; elapsed = 00:00:04 . Memory (MB): peak = 2418.168 ; gain = 55.020 ; free physical = 70354 ; free virtual = 153263  
Ending Placer Task | Checksum: f6ad9808  
  
Time (s): cpu = 00:00:10 ; elapsed = 00:00:04 . Memory (MB): peak = 2418.168 ; gain = 55.020 ; free physical = 70372 ; free virtual = 153282  
INFO: [Common 17-83] Releasing license: Implementation  
41 Infos, 2 Warnings, 0 Critical Warnings **and** 0 Errors encountered.  
place\_design completed successfully  
place\_design: Time (s): cpu = 00:00:12 ; elapsed = 00:00:08 . Memory (MB): peak = 2418.168 ; gain = 55.020 ; free physical = 70372 ; free virtual = 153282  
INFO: [Timing 38-480] Writing timing data to binary archive.  
Writing placer database...  
Writing XDEF routing.  
Writing XDEF routing logical nets.  
Writing XDEF routing special nets.  
Write XDEF Complete: Time (s): cpu = 00:00:00.37 ; elapsed = 00:00:00.13 . Memory (MB): peak = 2418.168 ; gain = 0.000 ; free physical = 70366 ; free virtual = 153278  
INFO: [Common 17-1381] The checkpoint '/nfs/home/l/l\_heiwan/coen316/lab4/vivado/part2/lab4\_part2/lab4\_part2.runs/impl\_1/cpu\_placed.dcp' has been generated.  
INFO: [runtcl-4] Executing : report\_io -file cpu\_io\_placed.rpt  
report\_io: Time (s): cpu = 00:00:00.07 ; elapsed = 00:00:00.17 . Memory (MB): peak = 2418.168 ; gain = 0.000 ; free physical = 70366 ; free virtual = 153276  
INFO: [runtcl-4] Executing : report\_utilization -file cpu\_utilization\_placed.rpt -pb cpu\_utilization\_placed.pb  
report\_utilization: Time (s): cpu = 00:00:00.07 ; elapsed = 00:00:00.14 . Memory (MB): peak = 2418.168 ; gain = 0.000 ; free physical = 70370 ; free virtual = 153281  
INFO: [runtcl-4] Executing : report\_control\_sets -verbose -file cpu\_control\_sets\_placed.rpt  
report\_control\_sets: Time (s): cpu = 00:00:00.03 ; elapsed = 00:00:00.10 . Memory (MB): peak = 2418.168 ; gain = 0.000 ; free physical = 70369 ; free virtual = 153279  
Command: route\_design  
Attempting to **get** a license **for** feature 'Implementation' **and**/**or** device 'xc7a100t'  
INFO: [Common 17-349] Got license **for** feature 'Implementation' **and**/**or** device 'xc7a100t'  
Running DRC as a precondition to command route\_design  
INFO: [DRC 23-27] Running DRC with 8 threads  
WARNING: [DRC PLCK-12] Clock Placer Checks: Poor placement **for** routing between an IO pin **and** BUFG.   
Resolution: Poor placement of an IO pin **and** a BUFG has resulted **in** the router using a non-dedicated path between the two. There are several things that could trigger **this** DRC, each of which can cause unpredictable clock insertion delays that result **in** poor timing. This DRC could be caused by any of the following: (a) a clock port was placed on a pin that **is** **not** a CCIO-pin (b)the BUFG has **not** been placed **in** the same half of the device **or** SLR as the CCIO-pin (c) a single ended clock has been placed on the N-Side of a differential pair CCIO-pin.  
 This **is** normally an ERROR but the CLOCK\_DEDICATED\_ROUTE constraint **is** **set** to FALSE allowing your design to **continue**. The use of **this** **override** **is** highly discouraged as it may lead to very poor timing results. It **is** recommended that **this** error condition be corrected **in** the design.  
  
 clk\_IBUF\_inst (IBUF.O) **is** locked to IOB\_X0Y82  
 clk\_IBUF\_BUFG\_inst (BUFG.I) **is** provisionally placed by clockplacer on BUFGCTRL\_X0Y0  
INFO: [Vivado\_Tcl 4-198] DRC finished with 0 Errors, 1 Warnings  
INFO: [Vivado\_Tcl 4-199] Please refer to the DRC report (report\_drc) **for** more information.  
  
  
Starting Routing Task  
INFO: [Route 35-254] Multithreading enabled **for** route\_design using a maximum of 8 CPUs  
Checksum: PlaceDB: 53719dcc ConstDB: 0 ShapeSum: a33bfa3c RouteDB: 0  
  
Phase 1 Build RT Design  
Phase 1 Build RT Design | Checksum: 12884b526  
  
Time (s): cpu = 00:00:24 ; elapsed = 00:00:21 . Memory (MB): peak = 2460.773 ; gain = 42.605 ; free physical = 70210 ; free virtual = 153121  
Post Restoration Checksum: NetGraph: 2b6571ad NumContArr: fd1f4379 Constraints: 0 Timing: 0  
  
Phase 2 Router Initialization  
INFO: [Route 35-64] No timing constraints were detected. The router will operate **in** resource-optimization mode.  
  
Phase 2.1 Fix Topology Constraints  
Phase 2.1 Fix Topology Constraints | Checksum: 12884b526  
  
Time (s): cpu = 00:00:24 ; elapsed = 00:00:21 . Memory (MB): peak = 2466.762 ; gain = 48.594 ; free physical = 70179 ; free virtual = 153089  
  
Phase 2.2 Pre Route Cleanup  
Phase 2.2 Pre Route Cleanup | Checksum: 12884b526  
  
Time (s): cpu = 00:00:24 ; elapsed = 00:00:21 . Memory (MB): peak = 2466.762 ; gain = 48.594 ; free physical = 70179 ; free virtual = 153089  
 Number of Nodes with overlaps = 0  
Phase 2 Router Initialization | Checksum: 1612e7d2a  
  
Time (s): cpu = 00:00:25 ; elapsed = 00:00:21 . Memory (MB): peak = 2476.027 ; gain = 57.859 ; free physical = 70169 ; free virtual = 153080  
  
Phase 3 Initial Routing  
Phase 3 Initial Routing | Checksum: f5895377  
  
Time (s): cpu = 00:00:26 ; elapsed = 00:00:21 . Memory (MB): peak = 2480.027 ; gain = 61.859 ; free physical = 70169 ; free virtual = 153080  
  
Phase 4 Rip-up And Reroute  
  
Phase 4.1 Global Iteration 0  
 Number of Nodes with overlaps = 150  
 Number of Nodes with overlaps = 1  
 Number of Nodes with overlaps = 0  
Phase 4.1 Global Iteration 0 | Checksum: 14242920f  
  
Time (s): cpu = 00:00:28 ; elapsed = 00:00:22 . Memory (MB): peak = 2480.027 ; gain = 61.859 ; free physical = 70168 ; free virtual = 153079  
Phase 4 Rip-up And Reroute | Checksum: 14242920f  
  
Time (s): cpu = 00:00:28 ; elapsed = 00:00:22 . Memory (MB): peak = 2480.027 ; gain = 61.859 ; free physical = 70168 ; free virtual = 153079  
  
Phase 5 Delay **and** Skew Optimization  
Phase 5 Delay **and** Skew Optimization | Checksum: 14242920f  
  
Time (s): cpu = 00:00:28 ; elapsed = 00:00:22 . Memory (MB): peak = 2480.027 ; gain = 61.859 ; free physical = 70168 ; free virtual = 153079  
  
Phase 6 Post Hold Fix  
  
Phase 6.1 Hold Fix Iter  
Phase 6.1 Hold Fix Iter | Checksum: 14242920f  
  
Time (s): cpu = 00:00:28 ; elapsed = 00:00:22 . Memory (MB): peak = 2480.027 ; gain = 61.859 ; free physical = 70168 ; free virtual = 153079  
Phase 6 Post Hold Fix | Checksum: 14242920f  
  
Time (s): cpu = 00:00:28 ; elapsed = 00:00:22 . Memory (MB): peak = 2480.027 ; gain = 61.859 ; free physical = 70168 ; free virtual = 153079  
  
Phase 7 Route finalize  
  
Router Utilization Summary  
 Global Vertical Routing Utilization = 0.296644 %  
 Global Horizontal Routing Utilization = 0.356067 %  
 Routable Net Status\*  
 \*Does **not** include unroutable nets such as driverless **and** loadless.  
 Run report\_route\_status **for** detailed report.  
 Number of Failed Nets = 0  
 Number of Unrouted Nets = 0  
 Number of Partially Routed Nets = 0  
 Number of Node Overlaps = 0  
  
Congestion Report  
North Dir 1x1 Area, Max Cong = 34.2342%, No Congested Regions.  
South Dir 1x1 Area, Max Cong = 44.1441%, No Congested Regions.  
East Dir 1x1 Area, Max Cong = 42.6471%, No Congested Regions.  
West Dir 1x1 Area, Max Cong = 38.2353%, No Congested Regions.  
  
------------------------------  
Reporting congestion hotspots  
------------------------------  
Direction: North  
----------------  
Congested clusters found at Level 0  
Effective congestion level: 0 Aspect Ratio: 1 Sparse Ratio: 0  
Direction: South  
----------------  
Congested clusters found at Level 0  
Effective congestion level: 0 Aspect Ratio: 1 Sparse Ratio: 0  
Direction: East  
----------------  
Congested clusters found at Level 0  
Effective congestion level: 0 Aspect Ratio: 1 Sparse Ratio: 0  
Direction: West  
----------------  
Congested clusters found at Level 0  
Effective congestion level: 0 Aspect Ratio: 1 Sparse Ratio: 0  
  
Phase 7 Route finalize | Checksum: 14242920f  
  
Time (s): cpu = 00:00:28 ; elapsed = 00:00:22 . Memory (MB): peak = 2480.027 ; gain = 61.859 ; free physical = 70169 ; free virtual = 153079  
  
Phase 8 Verifying routed nets  
  
 Verification completed successfully  
Phase 8 Verifying routed nets | Checksum: 14242920f  
  
Time (s): cpu = 00:00:28 ; elapsed = 00:00:22 . Memory (MB): peak = 2482.027 ; gain = 63.859 ; free physical = 70168 ; free virtual = 153079  
  
Phase 9 Depositing Routes  
Phase 9 Depositing Routes | Checksum: 16ee01053  
  
Time (s): cpu = 00:00:28 ; elapsed = 00:00:22 . Memory (MB): peak = 2482.027 ; gain = 63.859 ; free physical = 70169 ; free virtual = 153079  
INFO: [Route 35-16] Router Completed Successfully  
  
Time (s): cpu = 00:00:28 ; elapsed = 00:00:22 . Memory (MB): peak = 2482.027 ; gain = 63.859 ; free physical = 70203 ; free virtual = 153113  
  
Routing Is Done.  
INFO: [Common 17-83] Releasing license: Implementation  
54 Infos, 3 Warnings, 0 Critical Warnings **and** 0 Errors encountered.  
route\_design completed successfully  
route\_design: Time (s): cpu = 00:00:30 ; elapsed = 00:00:26 . Memory (MB): peak = 2482.027 ; gain = 63.859 ; free physical = 70203 ; free virtual = 153113  
INFO: [Timing 38-480] Writing timing data to binary archive.  
Writing placer database...  
Writing XDEF routing.  
Writing XDEF routing logical nets.  
Writing XDEF routing special nets.  
Write XDEF Complete: Time (s): cpu = 00:00:00.34 ; elapsed = 00:00:00.13 . Memory (MB): peak = 2482.027 ; gain = 0.000 ; free physical = 70196 ; free virtual = 153110  
INFO: [Common 17-1381] The checkpoint '/nfs/home/l/l\_heiwan/coen316/lab4/vivado/part2/lab4\_part2/lab4\_part2.runs/impl\_1/cpu\_routed.dcp' has been generated.  
INFO: [runtcl-4] Executing : report\_drc -file cpu\_drc\_routed.rpt -pb cpu\_drc\_routed.pb -rpx cpu\_drc\_routed.rpx  
Command: report\_drc -file cpu\_drc\_routed.rpt -pb cpu\_drc\_routed.pb -rpx cpu\_drc\_routed.rpx  
INFO: [DRC 23-27] Running DRC with 8 threads  
INFO: [Coretcl 2-168] The results of DRC are **in** file /nfs/home/l/l\_heiwan/coen316/lab4/vivado/part2/lab4\_part2/lab4\_part2.runs/impl\_1/cpu\_drc\_routed.rpt.  
report\_drc completed successfully  
INFO: [runtcl-4] Executing : report\_methodology -file cpu\_methodology\_drc\_routed.rpt -pb cpu\_methodology\_drc\_routed.pb -rpx cpu\_methodology\_drc\_routed.rpx  
Command: report\_methodology -file cpu\_methodology\_drc\_routed.rpt -pb cpu\_methodology\_drc\_routed.pb -rpx cpu\_methodology\_drc\_routed.rpx  
INFO: [Timing 38-35] Done setting XDC timing constraints.  
INFO: [Timing 38-35] Done setting XDC timing constraints.  
INFO: [DRC 23-133] Running Methodology with 8 threads  
INFO: [Coretcl 2-1520] The results of Report Methodology are **in** file /nfs/home/l/l\_heiwan/coen316/lab4/vivado/part2/lab4\_part2/lab4\_part2.runs/impl\_1/cpu\_methodology\_drc\_routed.rpt.  
report\_methodology completed successfully  
INFO: [runtcl-4] Executing : report\_power -file cpu\_power\_routed.rpt -pb cpu\_power\_summary\_routed.pb -rpx cpu\_power\_routed.rpx  
Command: report\_power -file cpu\_power\_routed.rpt -pb cpu\_power\_summary\_routed.pb -rpx cpu\_power\_routed.rpx  
WARNING: [Power 33-232] No user defined clocks were found **in** the design!  
Resolution: Please specify clocks using create\_clock/create\_generated\_clock **for** sequential elements. For pure combinatorial circuits, please specify a virtual clock, otherwise the vectorless estimation might be inaccurate  
INFO: [Timing 38-35] Done setting XDC timing constraints.  
Running Vector-less Activity Propagation...  
  
Finished Running Vector-less Activity Propagation  
Invalid argument  
66 Infos, 4 Warnings, 0 Critical Warnings **and** 0 Errors encountered.  
report\_power failed  
INFO: [runtcl-4] Executing : report\_route\_status -file cpu\_route\_status.rpt -pb cpu\_route\_status.pb  
INFO: [runtcl-4] Executing : report\_timing\_summary -max\_paths 10 -file cpu\_timing\_summary\_routed.rpt -pb cpu\_timing\_summary\_routed.pb -rpx cpu\_timing\_summary\_routed.rpx -warn\_on\_violation   
INFO: [Timing 38-91] UpdateTimingParams: Speed grade: -1, Delay Type: min\_max, Timing Stage: Requireds.  
INFO: [Timing 38-191] Multithreading enabled **for** timing update using a maximum of 8 CPUs  
WARNING: [Timing 38-313] There are no user specified timing constraints. Timing constraints are needed **for** proper timing analysis.  
INFO: [runtcl-4] Executing : report\_incremental\_reuse -file cpu\_incremental\_reuse\_routed.rpt  
INFO: [Vivado\_Tcl 4-545] No incremental reuse to report, no incremental placement **and** routing data was found.  
INFO: [runtcl-4] Executing : report\_clock\_utilization -file cpu\_clock\_utilization\_routed.rpt  
INFO: [runtcl-4] Executing : report\_bus\_skew -warn\_on\_violation -file cpu\_bus\_skew\_routed.rpt -pb cpu\_bus\_skew\_routed.pb -rpx cpu\_bus\_skew\_routed.rpx  
INFO: [Timing 38-91] UpdateTimingParams: Speed grade: -1, Delay Type: min\_max, Timing Stage: Requireds.  
INFO: [Timing 38-191] Multithreading enabled **for** timing update using a maximum of 8 CPUs  
INFO: [Common 17-206] Exiting Vivado at Wed Nov 22 20:09:27 2023...  
  
\*\*\* Running vivado  
 with args -log cpu.vdi -applog -m64 -product Vivado -messageDb vivado.pb -mode batch -source cpu.tcl -notrace  
  
  
\*\*\*\*\*\* Vivado v2018.2 (64-bit)  
 \*\*\*\* SW Build 2258646 on Thu Jun 14 20:02:38 MDT 2018  
 \*\*\*\* IP Build 2256618 on Thu Jun 14 22:10:49 MDT 2018  
 \*\* Copyright 1986-2018 Xilinx, Inc. All Rights Reserved.  
  
source cpu.tcl -notrace  
Command: open\_checkpoint cpu\_routed.dcp  
  
Starting open\_checkpoint Task  
  
Time (s): cpu = 00:00:00.07 ; elapsed = 00:00:00.24 . Memory (MB): peak = 1343.125 ; gain = 0.000 ; free physical = 71120 ; free virtual = 154032  
INFO: [Netlist 29-17] Analyzing 240 Unisim elements **for** replacement  
INFO: [Netlist 29-28] Unisim Transformation completed **in** 0 CPU seconds  
INFO: [Project 1-479] Netlist was created with Vivado 2018.2  
INFO: [Device 21-403] Loading part xc7a100tcsg324-1  
INFO: [Project 1-570] Preparing netlist **for** logic optimization  
INFO: [Timing 38-478] Restoring timing data **from** binary archive.

