CE219881 - PSoC 6 MCU Switching Between Power Modes

Objective

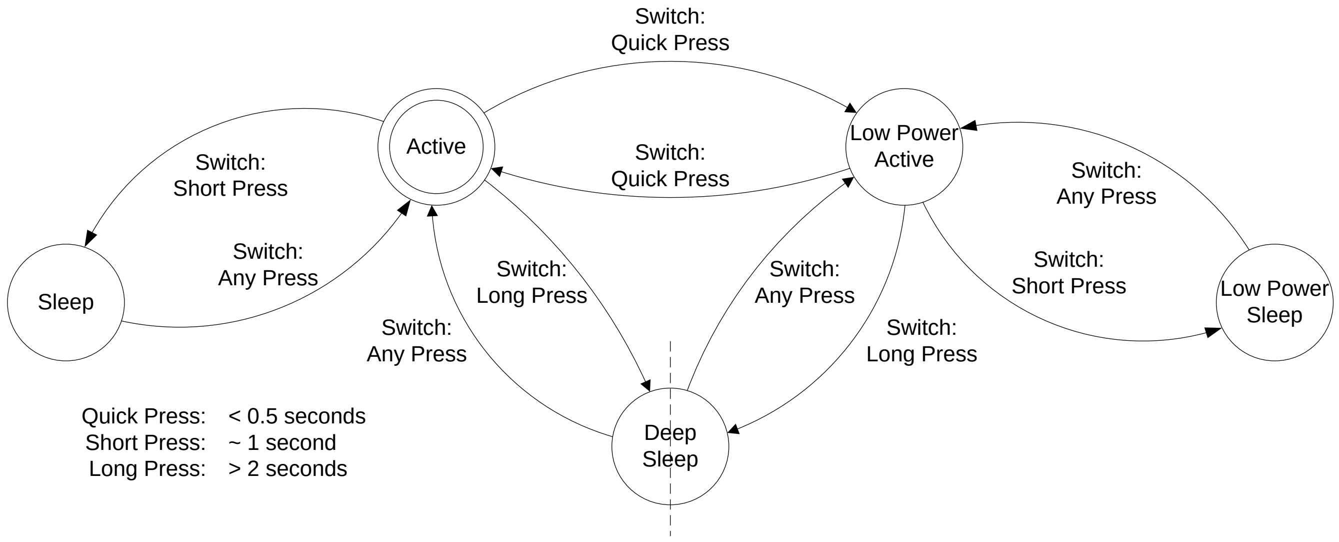
This example demonstrates how to transition PSoC 6 between the following power modes - Active, Sleep, Low Power Active, Low Power Sleep and Deep Sleep.

Overview

This code example shows how to enter and exit low power modes, and transition from Active to Deep Sleep or Sleep. Once in either mode, the example also shows how to wake up and return to one of the Active modes.

The project uses a switch to transition among the power modes. Figure 1 shows the state machine implemented in the firmware to execute the transitions.

Figure 1. Power mode state machine



The project also uses two LEDs to indicate the power mode selected. Table 1 shows the state of the LEDs for each mode.

Table 1. Power Mode Versus LEDs State

Power Mode	LEDs State
Active	Red Full Bright
Sleep	Red Low Bright
Low Power Active	Blue Full Bright
Low Power Sleep	Blue Low Bright
Deep Sleep	Both Turned OFF

Requirements

Tool: PSoC® Creator™ 4.2

Programming Language: C (ARM® GCC 5.4-2016-q2-update)

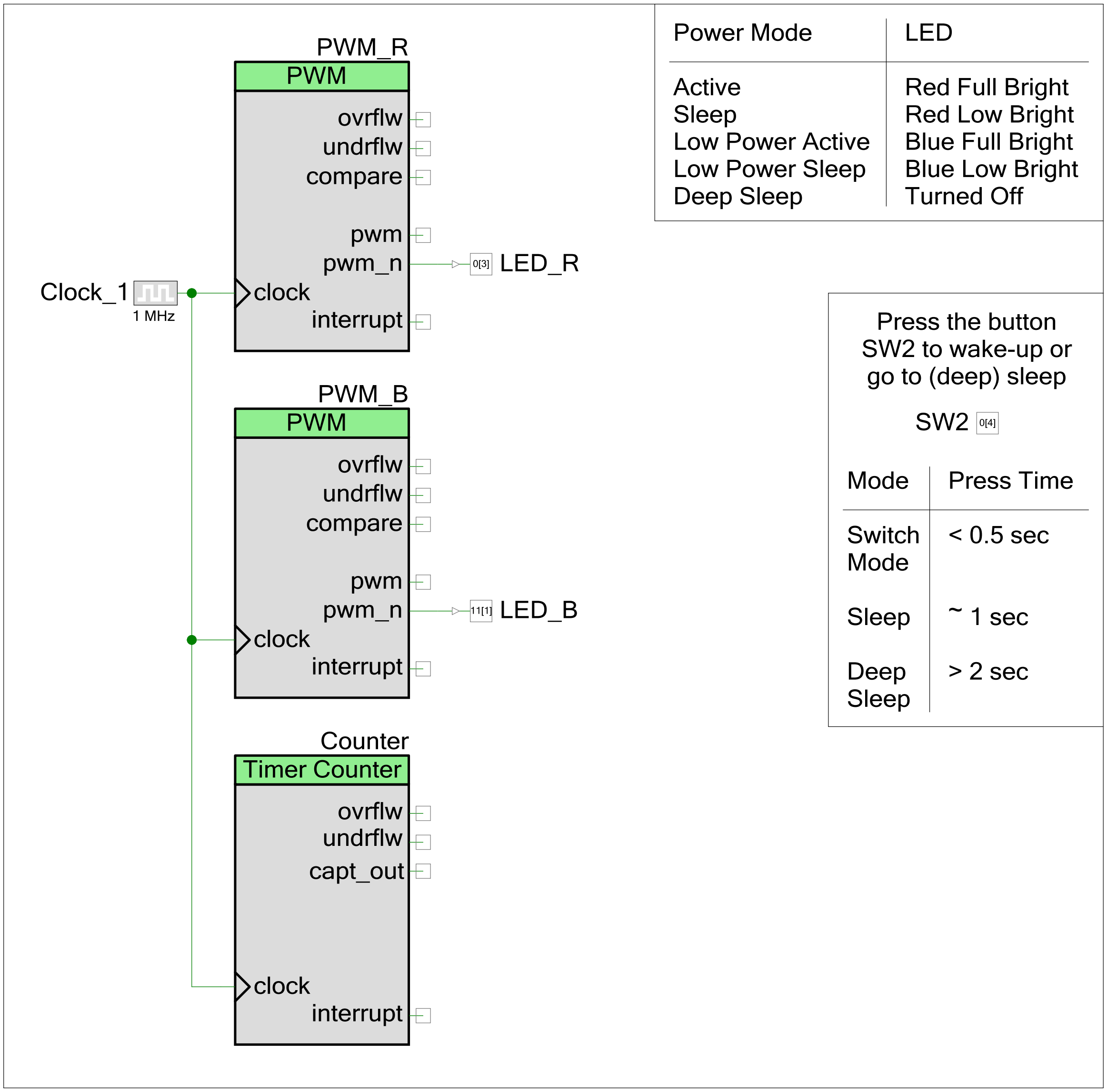
Associated Parts: All PSoC 6 parts

Related Hardware: CY8CKIT-062 or CY8CKIT-062-BLE

Design

Figure 2 shows the PSoC Creator schematic for this project. Two PWM blocks control the intensity of the kit Red and Blue LEDs. The Counter block counts the time that SW2 is pressed.

Figure 2. Project Schematics



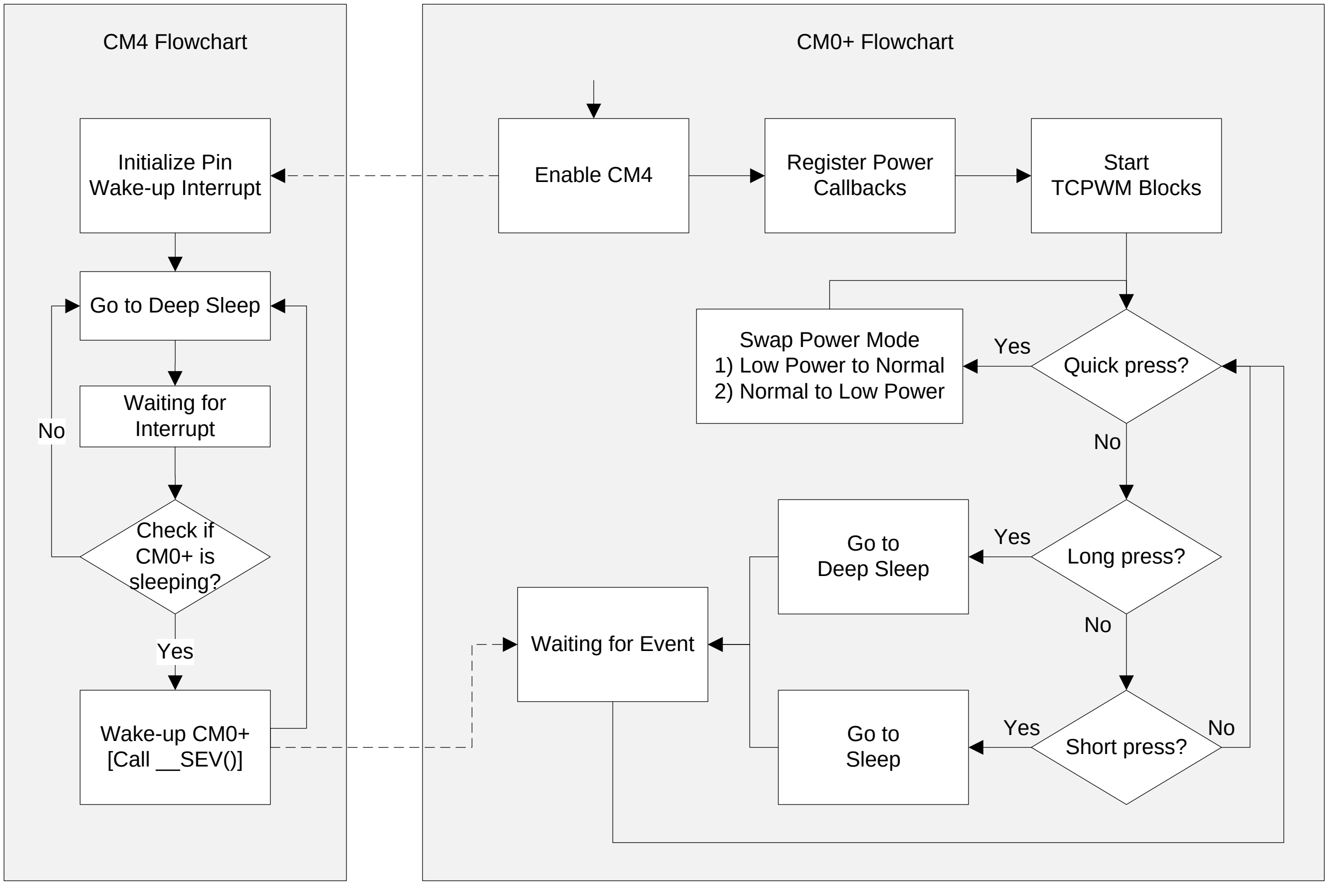
Power Mode	LED
Active	Red Full Bright
Sleep	Red Low Bright
Low Power Active	Blue Full Bright
Low Power Sleep	Blue Low Bright
Deep Sleep	Turned Off

Press the button SW2 to wake-up or go to (deep) sleep

Mode	Press Time
Switch Mode	< 0.5 sec
Sleep	~ 1 sec
Deep Sleep	> 2 sec

This example uses both CPU cores of PSoC 6. ARM Cortex® M0+ (CM0+) handles the state machine shown in Figure 1 and controls the duty cycle of the PWM block. ARM Cortex M4 (CM4) wakes up CM0+ when a switch press is detected. Figure 3 shows the firmware flow of both cores.

Figure 3. Firmware Flowchart



Six power callback functions are registered. Table 2 shows the actions of each callback function. For more information on power callbacks, refer to the PDL Driver – System Power Management (SysPm).

Table 2. Power Callback Actions

Power Callback Functions	State Modes (CY_SYSPM_*)			
	CHECK_READY	CHECK_FAIL	BEFORE_TRANSITION	AFTER_TRANSITION
TCPWM Sleep Callback	Nothing	Nothing	Drop the selected LED PWM duty cycle and disable the Counter.	Set the selected LED PWM duty cycle to 100% and re-enable the Counter.
TCPWM Deep Sleep Callback	Nothing	Nothing	Disable all TCPWM blocks	Re-enable all TCPWM blocks and set the selected LED PWM duty cycle to 100%.
TCPWM Enter Low Power Callback	Nothing	Nothing	Set the Blue LED PWM duty cycle to 100% and Red LED PWM duty cycle to 0%. Re-init the Counter with new clock prescaler.	Nothing
TCPWM Exit Low Power Callback	Nothing	Nothing	Nothing	Set the Red LED PWM duty cycle to 100% and Blue LED PWM duty cycle to

Power Callback Functions	State Modes (CY_SYSPM_*)			
	CHECK_READY	CHECK_FAIL	BEFORE_TRANSITION	AFTER_TRANSITION
				0%. Re-init the Counter with the original clock prescaler.
Clock Enter Low Power Callback	Nothing	Nothing	Drop the internal LDO voltage to 0.9 Volts. Reconfigure the FLL frequency to half of the original value.	Nothing
Clock Exit Low Power Callback	Nothing	Nothing	Nothing	Increase the internal LDO voltage to 1.1 Volts. Reconfigure the FLL frequency to its original value.

Design Considerations

This code example runs on CY8CKIT-062-BLE or CY8CKIT-062, which have a PSoC 6 device. To port the design to other PSoC 6 devices and kits, change the target device using PSoC Creator **Project** > **Device Selector**, and pin assignments in the Design Wide Resources window.

Hardware Setup

This example does not require any additional hardware to run. However, you can connect an ammeter to measure the current consumed by the CM0+ and CM4. Simply remove the jumper PWR_MON from the PSoC 6 kit and connect the ammeter on the header pins. This jumper is located in the backside of the PSoC 6 kit. Refer to the kit guide for the exact location.

Operation

Follow the instructions that came with your kit to make sure that it is connected to your PC.

1. If observation of the current is desired, remove the PWR_MON jumper on CY8CKIT-062 and connect an ammeter to the header pins.
2. Build the “CE219881_PowerModes” project and program CY8CKIT-062. For more information on building projects and device programming, see PSoC Creator Help.
3. Confirm that the Red LED is ON and take note of the current consumption. The device is in Active mode at this moment.
4. Press the SW2 switch for approximately one second and release it. Observe that the Red LED dims and the current consumption drops by a few microamperes. The device is in Sleep mode at this moment.
5. Quickly press SW2 to return to Active mode. Observe that the Red LED is fully ON again.
6. Press the SW2 switch for at least two seconds and release it. Observe that the Red LED is OFF and the current consumption drops to under 100 µA. The device is in Deep Sleep mode at this moment.
7. Quickly press SW2 to return to Active mode. Observe that the Red LED is fully ON again and the current consumption increases to the same level measured before.
8. Quickly press SW2 again to enter Low Power Active mode. Observe that the Blue LED is ON and the current consumption drops significantly when comparing to Active mode. You can quickly press SW2 to switch between the two modes.
9. Keep the device in Low Power Active mode and press SW2 for around one second and release it. Observe that the Blue LED dims and the current consumption drops by a few microamperes. The device is in the Low Power Sleep mode at this moment.
10. Quickly press SW2 to return to Low Power Active mode. Observe that the Blue LED is fully ON again.
11. Press SW2 switch for at least two seconds and release it. Observe that the Blue LED is OFF and the current consumption drops to under 100 µA. The device is in Deep Sleep mode at this moment.

12. Quickly press SW2 to return to Low Power Active mode. Observe that the Blue LED is fully ON again and the current consumption increases to the same level measured before.

Components

Table 3 lists the PSoC Creator Components used in this example, as well as the hardware resources used by each.

Table 3. List of PSoC Creator Components

Component	Instance Name	Hardware Resources
TCPWM	PWM_R	1 TCPWM block
TCPWM	PWM_B	1 TCPWM block
TCPWM	Counter	1 TCPWM block
Digital Output Pin	LED_R	1 GPIO
Digital Output Pin	LED_B	1 GPIO
Digital Input Pin	SW2	1 GPIO

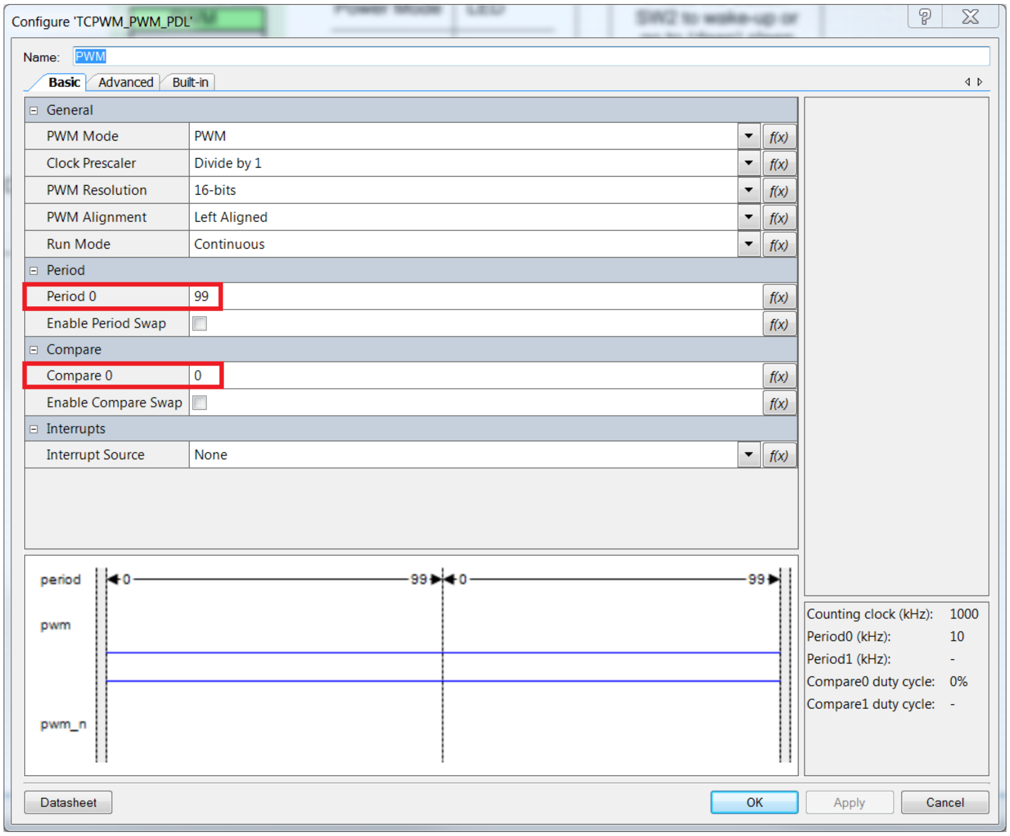
Parameter Settings

This section shows the changed settings for various Components as well as the system clocks.

PWM_R / PWM_B

Both PWM Components are configured to have a period of 99 counts and the initial duty cycle (compare register) is set to zero. Figure 4 shows the PWM Component configuration window.

Figure 4. PDM_PCM Component Configuration Window



Configure 'TCPWM_PWM_PDL'

Name: PWM

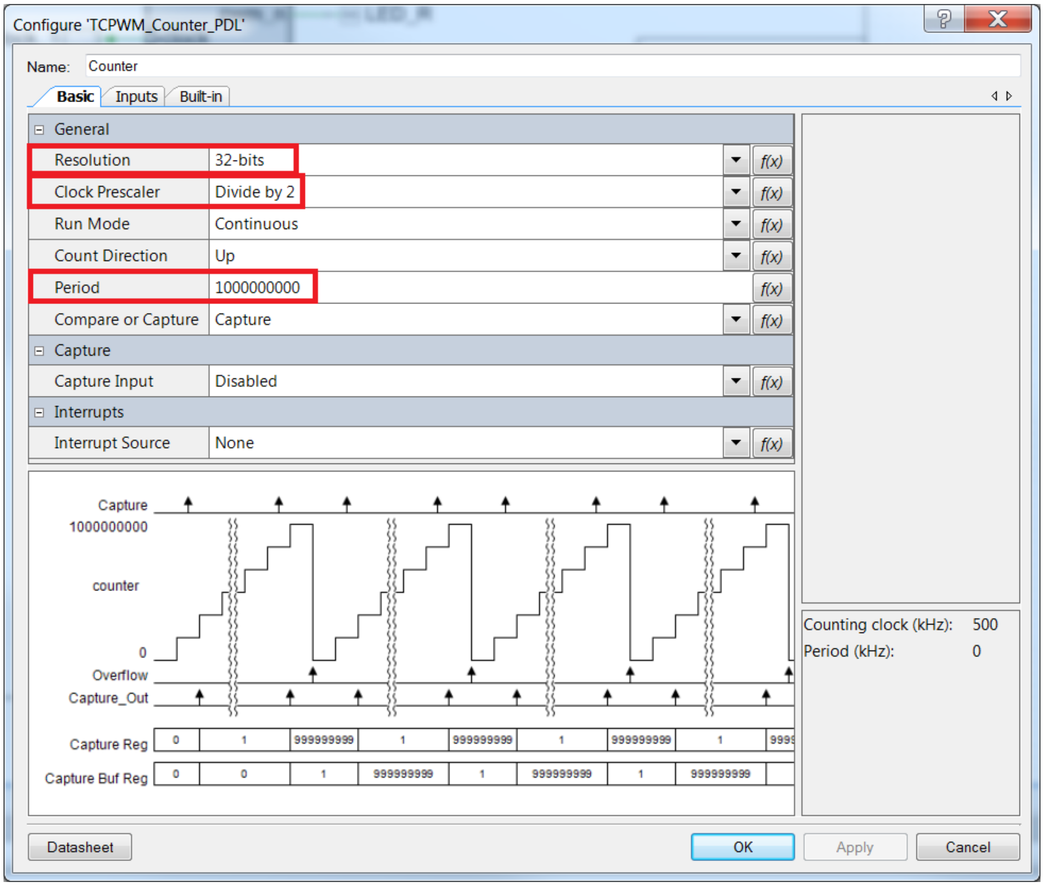
General	
PWM Mode	PWM
Clock Prescaler	Divide by 1
PWM Resolution	16-bits
PWM Alignment	Left Aligned
Run Mode	Continuous
Period	
Period 0	99
Enable Period Swap	□
Compare	
Compare 0	0
Enable Compare Swap	□
Interrupts	
Interrupt Source	None

Counting clock (kHz):	1000
Period0 (kHz):	10
Period1 (kHz):	-
Compare0 duty cycle:	0%
Compare1 duty cycle:	-

Counter

The counter is configured to have a resolution of 32 bits and Clock Prescaler to “Divide by 2”. Figure 5 shows the Counter Component configuration window.

Figure 5. Counter Configuration Window



Configure 'TCPWM_Counter_PDL'

Name: Counter

General

Resolution	32-bits
Clock Prescaler	Divide by 2
Run Mode	Continuous
Count Direction	Up
Period	1000000000
Compare or Capture	Capture

Capture

Capture Input	Disabled

Interrupts

Interrupt Source	None

Counting clock (kHz): 500

Period (kHz): 0

SW2

The pin drive mode is configured to be **Resistive Pull Up**.

LED_R / LED_B

Both pin drive modes are configured to be **Strong Drive**.

Related Documents

Table 4 lists all relevant application notes, code examples, knowledge base articles, device datasheets, and Component / user module datasheets.

Table 4. Related Documents

Application Notes	
AN210781 Getting Started with PSoC 6 MCU with BLE Connectivity	Describes the PSoC 6 BLE, and how to build this code example
AN215656 PSoC 6 MCU Dual-Core CPU System Design	Describes the dual-core CPU architecture in the PSoC 6 MCU
PSoC Creator Component Datasheets	
Clock (SYSCLK) Component	Provides an interface to the programmable peripheral clock dividers
General Purpose Input / Output (GPIO) Component	Allows hardware resources to connect to a physical port-pin
Pulse Width Modulator (TCPWM_PWM)	Allows to configure the TCPWM hardware for PWM functionality
Timer / Counter (TCPWM_COUNTER)	Allows to configure the TCPWM hardware for Timer/Counter functionality
Device Documentation	
PSoC 6 MCU: PSoC 63 with BLE Datasheet (PRELIMINARY)	
PSoC 6 MCU: PSoC 62 Datasheet	
PSoC 6 MCU: PSoC 63 with BLE Architecture Technical Reference Manual	
PSoC 6 MCU: PSoC 63 with BLE Register Technical Reference Manual	
PSoC 6 MCU Programming Specifications	
Development Kit (DVK) Documentation	
CY8CKIT-062-BLE PSoC 6 BLE Pioneer Kit	

Document History

Document Title: CE219881 - PSoC 6 MCU Switching Between Power Modes

Document Number: 002-19881

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	5777742	RLOS	06/19/2017	New Code Example
*A	5848138	RLOS	08/08/2017	Updated Project to PSoC Creator 4.2
*B	6002595	RLOS	12/22/2017	Removed figure of the CY8CKIT-062 BLE kit and added description of the location of the PWR_MON jumper.

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at Cypress Locations.

Products

ARM® Cortex® Microcontrollers	cypress.com/arm
Automotive	cypress.com/automotive
Clocks & Buffers	cypress.com/clocks
Interface	cypress.com/interface
Internet of Things	cypress.com/iot
Memory	cypress.com/memory
Microcontrollers	cypress.com/mcu
PSoC	cypress.com/psoc
Power Management ICs	cypress.com/pmic
Touch Sensing	cypress.com/touch
USB Controllers	cypress.com/usb
Wireless Connectivity	cypress.com/wireless

PSoC® Solutions

PSoC 1 | PSoC 3 | PSoC 4 | PSoC 5LP | PSoC 6

Cypress Developer Community

Forums | WICED IOT Forums | Projects | Videos | Blogs | Training | Components

Technical Support

cypress.com/support

All other trademarks or registered trademarks referenced herein are the property of their respective owners.

Cypress Semiconductor
198 Champion Court
San Jose, CA 95134-1709

TO THE EXTENT PERMITTED BY APPLICABLE LAW, CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS DOCUMENT OR ANY SOFTWARE OR ACCOMPANYING HARDWARE, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. To the extent permitted by applicable law, Cypress reserves the right to make changes to this document without further notice. Cypress does not assume any liability arising out of the application or use of any product or circuit described in this document. Any information provided in this document, including any sample design information or programming code, is provided only for reference purposes. It is the responsibility of the user of this document to properly design, program, and test the functionality and safety of any application made of this information and any resulting product. Cypress products are not designed, intended, or authorized for use as critical components in systems designed or intended for the operation of weapons, weapons systems, nuclear installations, life-support devices or systems, other medical devices or systems (including resuscitation equipment and surgical implants), pollution control or hazardous substances management, or other uses where the failure of the device or system could cause personal injury, death, or property damage ("Unintended Uses"). A critical component is any component of a device or system whose failure to perform can be reasonably expected to cause the failure of the device or system, or to affect its safety or effectiveness. Cypress is not liable, in whole or in part, and you shall and hereby do release Cypress from any claim, damage, or other liability arising from or related to all Unintended Uses of Cypress products. You shall indemnify and hold Cypress harmless from and against all claims, costs, damages, and other liabilities, including claims for personal injury or death, arising from or related to any Unintended Uses of Cypress products.

Cypress, the Cypress logo, Spansion, the Spansion logo, and combinations thereof, WICED, PSoC, CapSense, EZ-USB, F-RAM, and Traveo are trademarks or registered trademarks of Cypress in the United States and other countries. For a more complete list of Cypress trademarks, visit cypress.com. Other names and brands may be claimed as property of their respective owners.