

Objective

This example demonstrates the write and read operations to the Serial Memory Interface (SMIF) in PSoC® 6 MCU.

Overview

This example writes and reads 256 bytes of data to external memory using SMIF quad mode. The example also checks the integrity of read data against written data.

Requirements

Tool: [PSoC Creator™ 4.2](#)

Programming Language: C (Arm® GCC 5.4-2016-q2-update, Arm MDK 5.22)

Associated Parts: All [PSoC 6 MCU](#) parts

Related Hardware: [CY8CKIT-062-BLE PSoC 6 BLE Pioneer Kit](#)

Design

[Figure 1](#) shows the design for this code example. The SMIF Component implements a SPI-based communication for interfacing external memory devices with PSoC. SMIF Component is configured with four data lines and single slave select line. The UART Component outputs debug information to a terminal window. It is configured for 8N1, transmit only, at 115.2 kbps. The design also uses two digital output pins to drive the RGB LED to indicate the status of data transfer.

Figure 1. SMIF Memory Write and Read Example Schematic

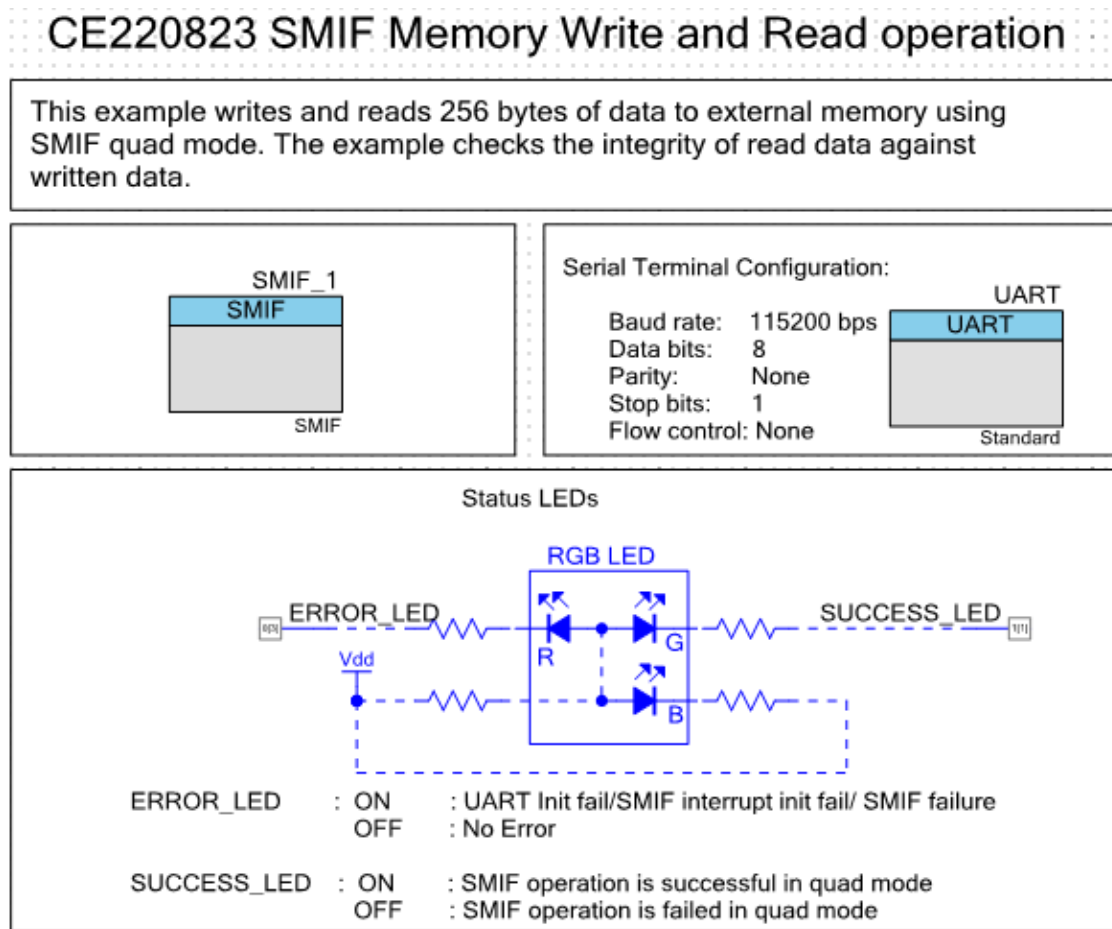


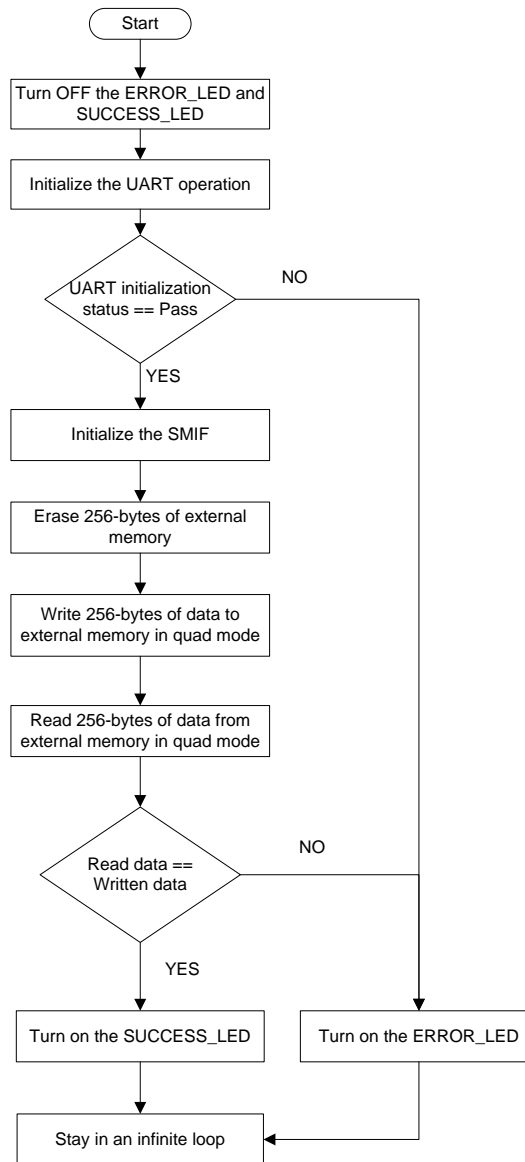
Table 1 explains the LED status indication.

Table 1. LED Status Indication

LED name	LED Status	Indication
ERROR_LED	ON	UART initialization failure or SMIF interrupt initialization failure or SMIF initialization failure or SMIF operation failure
	OFF	No Error
SUCCESS_LED	ON	SMIF operation succeeded in quad mode
	OFF	SMIF operation failed in quad mode

Figure 2 shows the firmware flow chart.

Figure 2. Firmware Flow Chart



The firmware uses source code (*cy_smif_memconfig.c* and *cy_smif_memconfig.h* files) generated from the SMIF Configuration Tool. This source code provides declarations for the SMIF driver memory configuration. For more information on the SMIF Configuration Tool, see [Appendix A: SMIF Configuration Tool](#).

Design Considerations

This code example is designed to run on CY8CKIT-062-BLE with the PSoC 6 MCU device. To port the design to other PSoC 6 MCU family devices and kits, you must change the target device in Device Selector, and change the pin assignments in the *cydwr* settings. For single-core PSoC 6 MCU devices, port the code from *main_cm4.c* to *main.c* file as CM0+ CPU is not used in this code example.

Hardware Setup

The code example works with the default settings on the CY8CKIT-062-BLE PSoC 6 BLE Pioneer Kit. If the settings are different from the default values, see the “Selection Switches” table in the [kit guide](#) to reset to the default settings.

Operation

1. Connect CY8CKIT-062-BLE to a USB port on your PC.
2. Open a serial port communication program, such as Tera Term and select the corresponding COM port. Configure the terminal to match UART: 115200 baud rate, 8N1, and Flow control – None. These settings must match the configuration of the PSoC Creator UART Component in the project.
3. Build and program the application into CY8CKIT-062-BLE. For more information on building a project or programming a device, see PSoC Creator Help.
4. Observe the LEDs to determine the status of the SMIF operation.
5. Make sure that debug messages display in the terminal window as expected.

Figure 3 is a snapshot of the debug UART terminal output.

Figure 3. Debug UART Terminal Output

[illegible]

Components

Table 2 lists the PSoC Creator Components used in this example and the hardware resources used by each Component.

Table 2. PSoC Creator Components

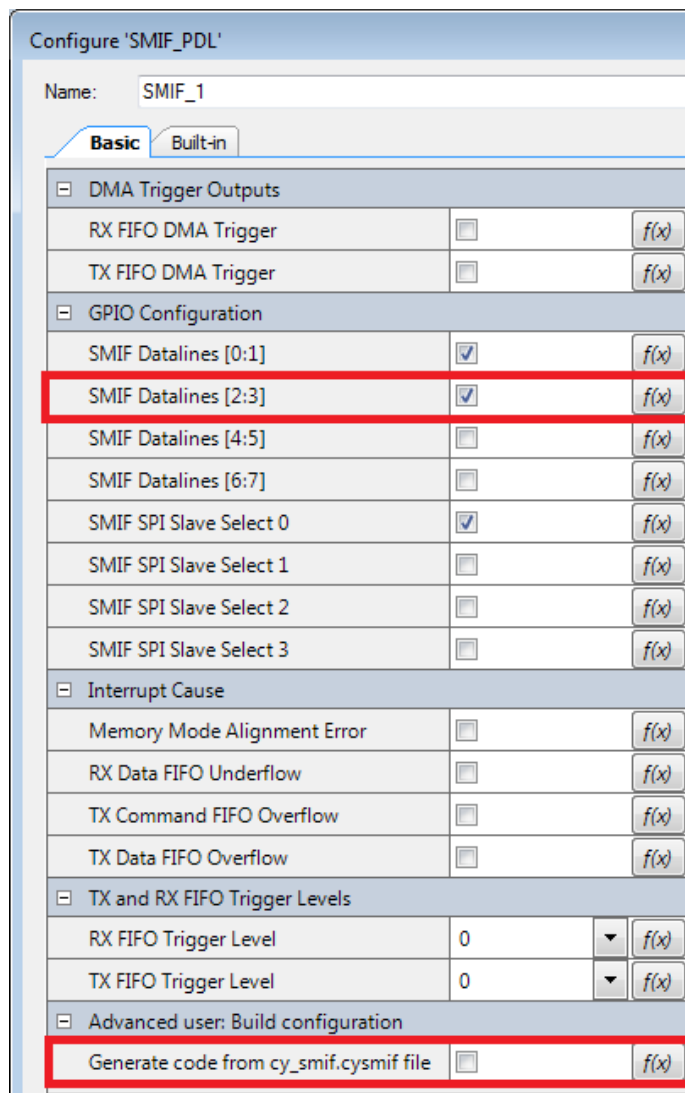
Component	Instance Name	Hardware Resources
Serial Memory Interface (SMIF_PDL)	SMIF_1	The mxsmif peripheral block
UART (SCB_UART_PDL)	UART	Single SCB peripheral block
General Purpose Input / Output (GPIO)	ERROR_LED, SUCCESS_LED	2 physical pins

Parameter Settings

Non-default settings for each Component is outlined in red in the following figures.

Figure 4 shows the SMIF_1 Component parameter settings.

Figure 4. SMIF Component Parameter Settings



Configure 'SMIF_PDL'

Name: SMIF_1

Basic Built-in

☐ DMA Trigger Outputs

RX FIFO DMA Trigger ☐ f(x)

TX FIFO DMA Trigger ☐ f(x)

☐ GPIO Configuration

SMIF Datalines [0:1] ☒ f(x)

SMIF Datalines [2:3] ☒ f(x)

SMIF Datalines [4:5] ☐ f(x)

SMIF Datalines [6:7] ☐ f(x)

SMIF SPI Slave Select 0 ☒ f(x)

SMIF SPI Slave Select 1 ☐ f(x)

SMIF SPI Slave Select 2 ☐ f(x)

SMIF SPI Slave Select 3 ☐ f(x)

☐ Interrupt Cause

Memory Mode Alignment Error ☐ f(x)

RX Data FIFO Underflow ☐ f(x)

TX Command FIFO Overflow ☐ f(x)

TX Data FIFO Overflow ☐ f(x)

☐ TX and RX FIFO Trigger Levels

RX FIFO Trigger Level 0 ▼ f(x)

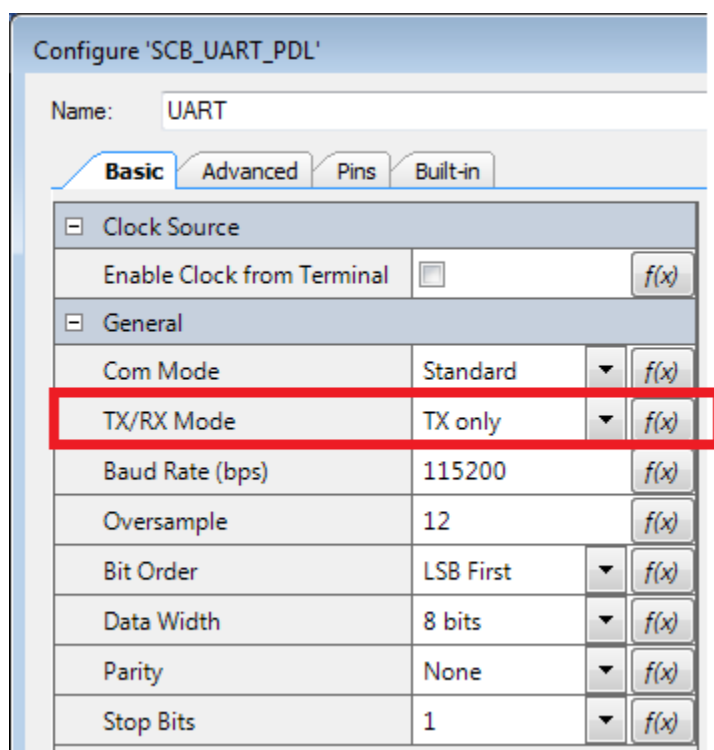
TX FIFO Trigger Level 0 ▼ f(x)

☐ Advanced user: Build configuration

Generate code from cy_smif.cysmif file ☒ f(x)

Figure 5 shows the UART Component parameter settings.

Figure 5. UART Component Parameter Settings



Design-Wide Resources

Make sure that V_{DD} (PSoC Creator > Design Wide Resources tab > System tab) is set to 2.7 V or more to use SUCCESS_LED.

Table 3 lists the pin assignment for the code example.

Table 3. Pin Names and Location

Pin Name	Location
SMIF_1:spi_clk	P11[7]
SMIF_1:spi_data_0	P11[6]
SMIF_1:spi_data_1	P11[5]
SMIF_1:spi_data_2	P11[4]
SMIF_1:spi_data_3	P11[3]
SMIF_1:spi_select0	P11[2]
UART:tx	P5[1]
ERROR_LED	P0[3]
SUCCESS_LED	P1[1]

Appendix A: SMIF Configuration Tool

PSoC Creator supports a stand-alone application, SMIF Configuration Tool, which enables a user to configure the SMIF through a GUI-based interface. This application is invoked from the SMIF Component in PSoC Creator. Figure 6 and Figure 7 show how to configure the memory device interfaced with SMIF. This tool will generate a *.cysmif file with these configuration details. Follow these steps to generate SMIF driver memory configuration (*.cysmif, cy_smif_memconfig.c, and cy_smif_memconfig.h) files from the SMIF Configuration Tool.

1. Make sure that the "Generate code from cymem file" parameter is selected in the SMIF Component
2. Remove cy_smif_memconfig.c and cy_smif_memconfig.h files from the project workspace.
3. Right-click the SMIF Component in **PSoC Creator schematics** window and click **SMIF Configuration Tool**.
4. Configure the memory part number to match the device on the kit.
5. Click **File** and save *.cysmif in the **example** root folder.
6. Click **Options > Configurations...** to select the example root folder as the output folder.
7. Click **Run > Generate Source Code** to generate the cy_smif_memconfig.c and cy_smif_memconfig.h files. These files provide definitions of the SMIF driver memory configuration.
8. Close the SMIF Configuration Tool.
9. Build the application. PSoC Creator generates the cy_smif_memslot.c and cy_smif_memslot.h files, the source code for the memory-level API of the SMIF driver. These APIs are used by the firmware to implement SMIF operation.

Figure 6. SMIF Configuration 1

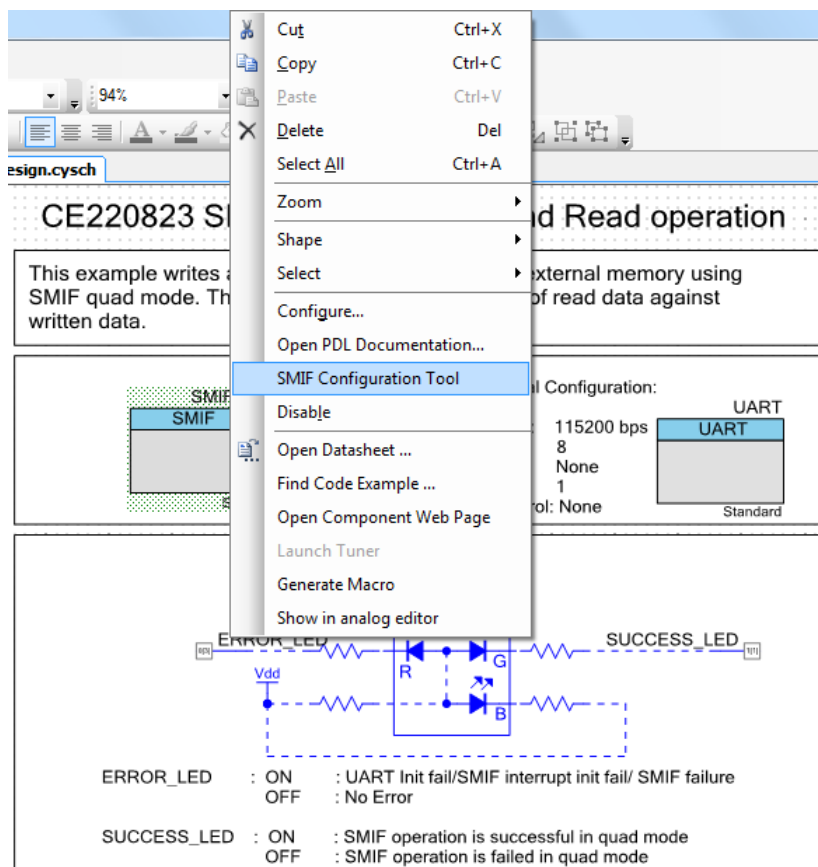


Figure 7. SMIF Configuration 2

SMIF Configuration Tool: E:\Ashwath\Q4_CEs\CE220823\SMIF_Memory_Write_and_Read_Operation.cydsn\cy_smif.cysmif

File Run Options Help

PSoC 6

Slave slot	Memory part number	Data select	Memory mapped	Pair with slot	Start address	Size	End address	Write enable	Config data in flash	Encrypt
0	S25FL512S	Quad SPI-Data[0:3]	<input type="checkbox"/>	None	0x18000000	0x10000	0x1800FFFF	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
1	Not used	SPI-MOSI:MISO Data[0:1]	<input type="checkbox"/>	None	0x18010000	0x10000	0x1801FFFF	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
2	Not used	SPI-MOSI:MISO Data[0:1]	<input type="checkbox"/>	None	0x18020000	0x10000	0x1802FFFF	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
3	Not used	SPI-MOSI:MISO Data[0:1]	<input type="checkbox"/>	None	0x18030000	0x10000	0x1803FFFF	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>

Location: C:\Program Files (x86)\Cypress\PD\3.0.1\tools\win\smif_config\memory\S2

User part number: S25FL512S

Erase time: 520 ms

Status register busy mask: 0x01

Chip erase time: 134 s

Status register quad enable mask: 0x02

Program time (us): 340

Size of memory: 0x04000000

Program page size: 0x00000200

Erase block size (bytes): 0x00040000

Description: 64Mbytes 3V serial Flash memory

Number of address bytes for SMIF transactions: 0x03

Description	Number	Command width	Address width	Mode	Mode width	Dummy cycles	Data width
Read command format	0xEB	Single	Quad	0x01	Quad	4	Quad
Write enable command format	0x06	Single	Single	NA	Single	NA	Single
Write disable command format	0x04	Single	Single	NA	Single	NA	Single
Erase command format	0xD8	Single	Single	NA	Single	NA	Single
Chip erase command format	0x60	Single	Single	NA	Single	NA	Single
Program command format	0x38	Single	Single	NA	Quad	NA	Quad
Read status register command (containing QE bit)	0x35	Single	Single	NA	Single	NA	Single
Read status register command (containing WIP bit)	0x05	Single	Single	NA	Single	NA	Single
Write status register command (containing QE bit)	0x01	Single	Single	NA	Single	NA	Single

Related Documents

Table 4 lists all relevant application notes, code examples, knowledge base articles, device datasheets, and Component/user module datasheets.

Table 4. Related Documents

Application Notes	
AN210781 Getting Started with PSoC 6 MCU with Bluetooth Low Energy (BLE) Connectivity	Describes PSoC 63 with Bluetooth Low Energy (BLE) Connectivity and how to build your first PSoC Creator project
PSoC Creator Component Datasheets	
Serial Memory Interface	Supports Single/Dual/Quad/Octal SPI Memories
UART	Supports UART communication
General-Purpose Input / Output	Supports Analog, Digital I/O and Bidirectional signal types
Device Documentation	
PSoC 6 MCU: PSoC 63 with BLE Datasheet	PSoC 6 MCU: PSoC 63 with BLE Architecture Technical Reference Manual
Development Kit (DK) Documentation	
CY8CKIT-062-BLE PSoC 6 BLE Pioneer Kit	

Document History

Document Title: CE220823 - PSoC 6 MCU SMIF Memory Write and Read Operation

Document Number: 002-20823

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	5856613	VJYA	08/17/2017	Initial public release
*A	5918188	VJYA	11/03/2017	Updated project name
*B	6003180	VJYA	12/22/2017	Updated Figure 6 and Figure 7

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