CE220061 – PSoC 6 MCU: Multi-Counter Watchdog Interrupts

Objective

This example demonstrates the operation of multi-counter watchdog timer (MCWDT) counters and interrupts in PSoC® 6 MCU.

Overview

This example uses two MCWDT PSoC Creator™ Components available in the PSoC 6 MCU devices to generate periodic events. These periodic events are used to drive GPIO pins.

Requirements

Tool: PSoC Creator™ 4.2

Programming Language: C (Arm® GCC 5.4-2016-q2-update, Arm MDK 5.22)

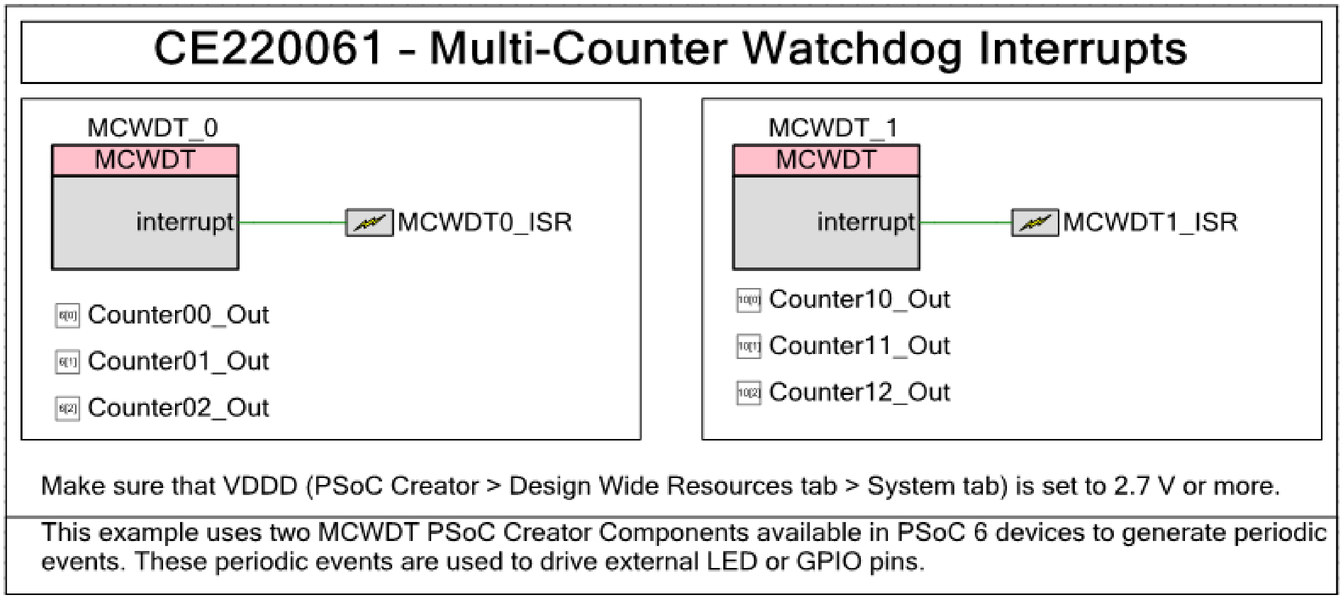
Associated Parts: All PSoC 6 MCU parts

Related Hardware: CY8CKIT-062-BLE PSoC 6 BLE Pioneer Kit

Design

The design shown in Figure 1 consists of two MCWDT_PDL PSoC Creator Components namely MCWDT_0 and MCWDT_1. Each MCWDT block has two 16-bit counters (Counter0 and Counter1) and one 32-bit counter (Counter2). All counters are clocked by either LFCLK (nominal 32 kHz) or by a cascaded counter.

Figure 1. MCWDT Interrupts Example Schematic



Make sure that VDDD (PSoC Creator > Design Wide Resources tab > System tab) is set to 2.7 V or more.

This example uses two MCWDT PSoC Creator Components available in PSoC 6 devices to generate periodic events. These periodic events are used to drive external LED or GPIO pins.

Table 1 shows the configuration of each counter in both the MCWDTs.

Table 1. MCWDT_0 and MCWDT_1 Configuration

	Counter0	Counter1	Counter2
MCWDT_0	• 16-bit counter • Clocked by LFCLK (32 kHz) • Free-running with a period of 65,536 counts • Interrupt mode (generates an interrupt when count reaches 65,536) • Drives Counter00_Out • Period of event = 2 s	• 16-bit counter • Clocked by LFCLK (32 kHz) • Clears on match with period 15,999+1 • Interrupt mode (generates an interrupt when count reaches 16,000) • Drives Counter01_Out • Period of event = 488 ms	• 32-bit counter • Clocked by MCWDT_0 - Counter1 interrupt • Interrupt mode (generates an interrupt when bit position 1 of counter toggles) • Drives Counter02_Out • Period of event = 976 ms
MCWDT_1	• 16-bit counter • Clocked by LFCLK (32 kHz) • Free-running with a period of 65,536 counts • Interrupt mode (generates an interrupt when count reaches 65,536) • Drives Counter10_Out • Period of event = 2 s	• 16-bit counter • Clocked by LFCLK (32 kHz) • Clear on match with period 32,768+1 • Interrupt mode (generates an interrupt when count reaches 32,769) • Drives Counter11_Out • Period of event = 1 s	• 32-bit counter • Clocked by LFCLK (32 kHz) • Interrupt mode (generates an interrupt when bit position 15 of counter toggles) • Drives Counter12_Out • Period of event = 1 s

Figure 2 shows the MCWDT_0 timing diagram.

Figure 2. MCWDT_0 Timing Diagram

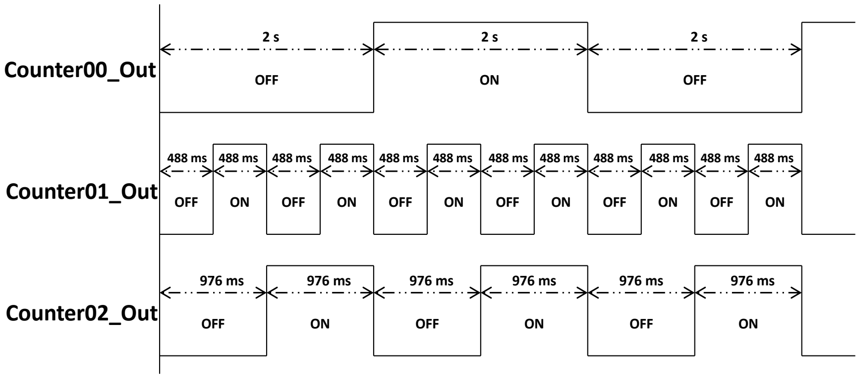
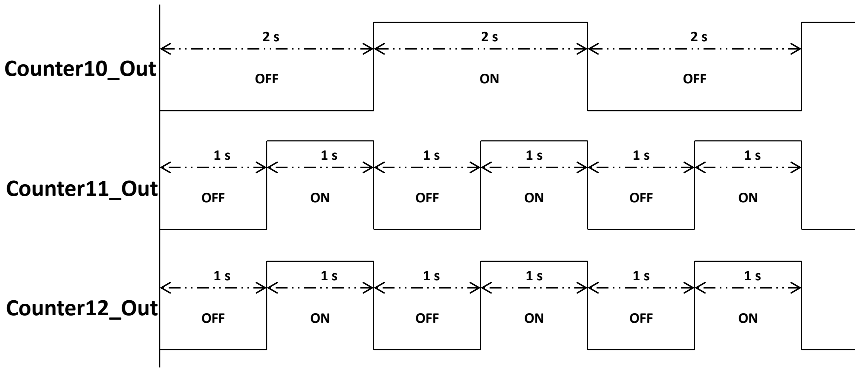


Figure 3 shows the MCWDT_1 timing diagram.

Figure 3. MCWDT_1 Timing Diagram



The firmware performs the following in the `main` function:

1. Initializes the interrupts for MCWDT_0 and MCWDT_1.
2. Configures the MCWDT_0 and MCWDT_1 Components.
3. Waits for the MCWDT_0 or MCWDT_1 interrupt in an infinite loop.

The firmware performs the following in the `MCWDT_0` ISR function:

1. Toggles the Counter00_Out pin for interrupt from MCWDT_0 Counter0.
2. Toggles the Counter01_Out pin for interrupt from MCWDT_0 Counter1.
3. Toggles the Counter02_Out pin for interrupt from MCWDT_0 Counter2.

The firmware performs the following in the `MCWDT_1` ISR function:

1. Toggles the Counter10_Out pin for interrupt from MCWDT_1 Counter0.
2. Toggles the Counter11_Out pin for interrupt from MCWDT_1 Counter1.
3. Toggles the Counter12_Out pin for interrupt from MCWDT_1 Counter2.

Design Considerations

This code example is designed to run on CY8CKIT-062-BLE with the PSoC 6 MCU. To port the design to other PSoC 6 MCU and kits, you must change the target device in Device Selector, and change the pin assignments in the ***cydwr*** settings. For single-core PSoC 6 MCU devices, port the code from *main_cm4.c* to *main.c* file as CM0+ CPU is not used in this code example.

This code example does not work at 1.8V (VDD) out of the box. Make sure that the switch "SW5" is set to select "3.3V" as VDD on the CY8CKIT-062-BLE PSoC 6 BLE Pioneer Kit.

Hardware Setup

The code example works with the default settings on the CY8CKIT-062-BLE PSoC 6 BLE Pioneer Kit. If the settings are different from the default values, see the “Selection Switches” table in the kit guide to reset to the default settings.

Operation

1. Connect CY8CKIT-062 BLE to a USB port on your PC.
2. Build and program the application into CY8CKIT-062 BLE. For more information on building a project or programming a device, see PSoC Creator Help.
3. Probe the following signals on a logic analyzer - Counter00_Out (P6[0]), Counter01_Out (P6[1]), Counter02_Out (P6[2]), Counter10_Out (P10[0]), Counter11_Out (P10[1]), Counter12_Out (P10[2]). Make sure that signal waveforms match the waveforms in Figure 2 and Figure 3.

Components

Table 2 lists the PSoC Creator Components used in this example and the hardware resources used by each Component.

Table 2. PSoC Creator Components

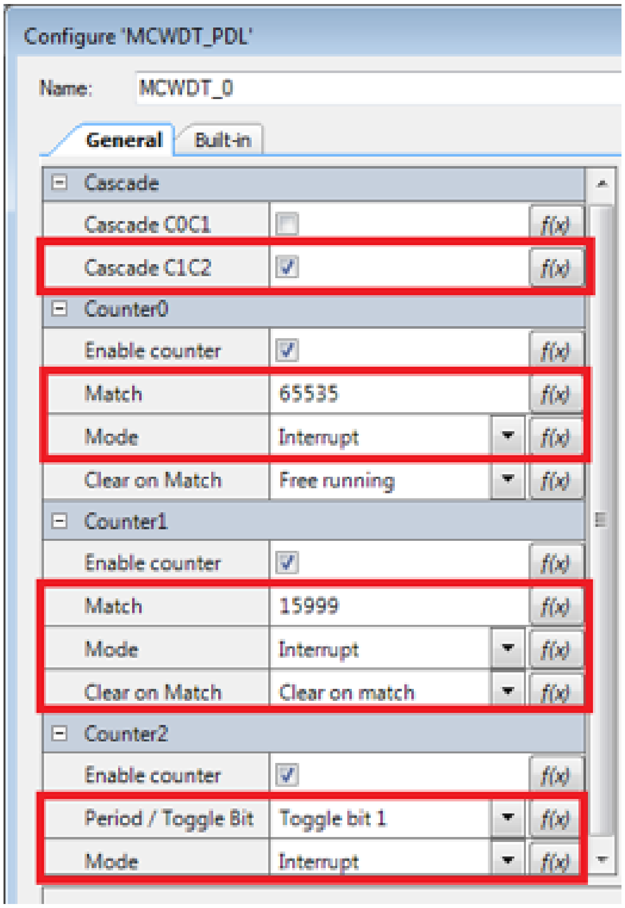
Component	Instance Name	Hardware Resources
Multi-Counter Watchdog (MCWDT_PDL)	MCWDT_0, MCWDT_1	Two MCWDT blocks of the System Resources Sub-System (SRSS)
System Interrupt (SysInt)	MCWDT0_ISR, MCWDT1_ISR	Two entries in the device interrupt vector table

Parameter Settings

Non-default settings for each Component is outlined in red in the following figure.

MCWDT_0 Component parameter settings are shown in Figure 4.

Figure 4. MCWDT_0 Component Parameter Settings



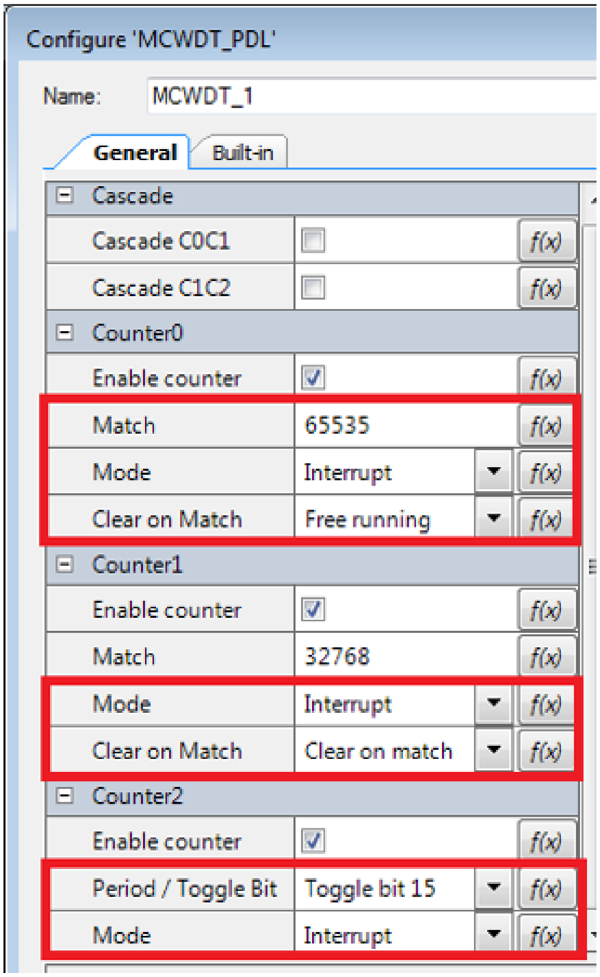
Configure 'MCWDT_PDL'

Name: MCWDT_0

⊟ Cascade		
Cascade C0C1	☐	f(x)
Cascade C1C2	☑	f(x)
⊟ Counter0		
Enable counter	☑	f(x)
Match	65535	f(x)
Mode	Interrupt	f(x)
Clear on Match	Free running	f(x)
⊟ Counter1		
Enable counter	☑	f(x)
Match	15999	f(x)
Mode	Interrupt	f(x)
Clear on Match	Clear on match	f(x)
⊟ Counter2		
Enable counter	☑	f(x)
Period / Toggle Bit	Toggle bit 1	f(x)
Mode	Interrupt	f(x)

MCWDT_1 Component parameter settings are shown in Figure 5.

Figure 5. MCWDT_1 Component Parameter Settings



Configure 'MCWDT_PDL'

Name: MCWDT_1

⊟ Cascade

- Cascade C0C1: □
- Cascade C1C2: □

⊟ Counter0

- Enable counter: ☑
- Match: 65535
- Mode: Interrupt
- Clear on Match: Free running

⊟ Counter1

- Enable counter: ☑
- Match: 32768
- Mode: Interrupt
- Clear on Match: Clear on match

⊟ Counter2

- Enable counter: ☑
- Period / Toggle Bit: Toggle bit 15
- Mode: Interrupt

Design-Wide Resources

Table 3 shows the pin assignment for the code example.

Table 3. Pin Names and Location

Pin Name	Location
Counter00_Out	P6[0]
Counter01_Out	P6[1]
Counter02_Out	P6[2]
Counter10_Out	P10[0]
Counter11_Out	P10[1]
Counter12_Out	P10[2]

Related Documents

Application Notes	
AN210781 – Getting Started with PSoC 6 MCU with Bluetooth Low Energy (BLE) Connectivity	Describes PSoC 63 with Bluetooth Low Energy (BLE) Connectivity and how to build your first PSoC Creator project
PSoC Creator Component Datasheets	
MCWDT_PDL	Supports Multi-Counter Watchdog with two 16-bit counters and one 32-bit counter
System Interrupt	Interrupt vectoring and control
Device Documentation	
PSoC 6 MCU: PSoC 63 with BLE Datasheet	PSoC 6 MCU: PSoC 63 with BLE Architecture Technical Reference Manual
Development Kit (DVK) Documentation	
CY8CKIT-062-BLE PSoC 6 BLE Pioneer Kit	

Document History

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Document Number: 002-20061

Revision	ECN	Orig. of Change	Submission Date	Description of Change
*A	5858250	VJYA	08/22/2017	Initial public release
*B	5918161	VJYA	11/03/2017	Updated project name
*C	6003197	VJYA	12/22/2017	Updated to latest PSoC Creator build

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