

Circuitos e Sistemas Integrados - Introdução ao Projeto VLSI

Prof. Fabian L. Cabrera & Prof. José L. Güntzel
fabian.cabrera.r@gmail.com



Universidade Federal de Santa Catarina
Florianópolis

2019



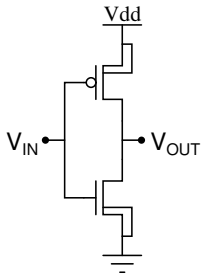
- ▶ Entregar o desenho do layout do inversor (feito a mão) em folha de papel. (pode usar diferentes cores)
- ▶ Entregar a biblioteca criada no Cadence comprimida. Se o nome da biblioteca é aula1 então pode usar o comando para comprimir:
`tar cvfz aula1.tar.gz aula1`
- ▶ Mostrar em sala de aula o resultado correto do DRC e LVS.

Critérios de avaliação da folha a ser entregue

- ▶ Representação física correta do layout.
- ▶ Identificação de todas as camadas e nós.



Substrato-P e Poço-N



NMOS

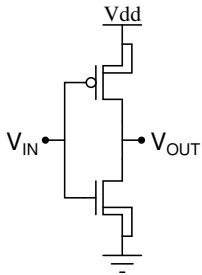
PMOS

P-sub

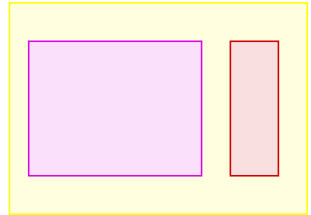
N-Well



Difusões n+ e p+



NMOS



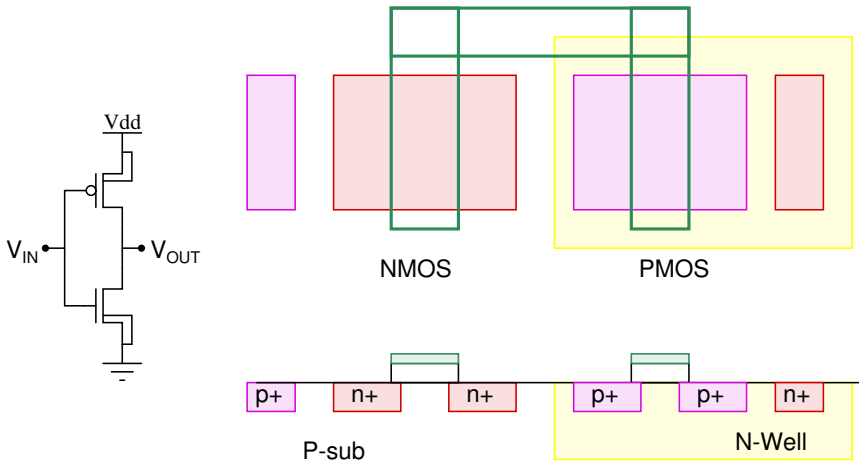
PMOS

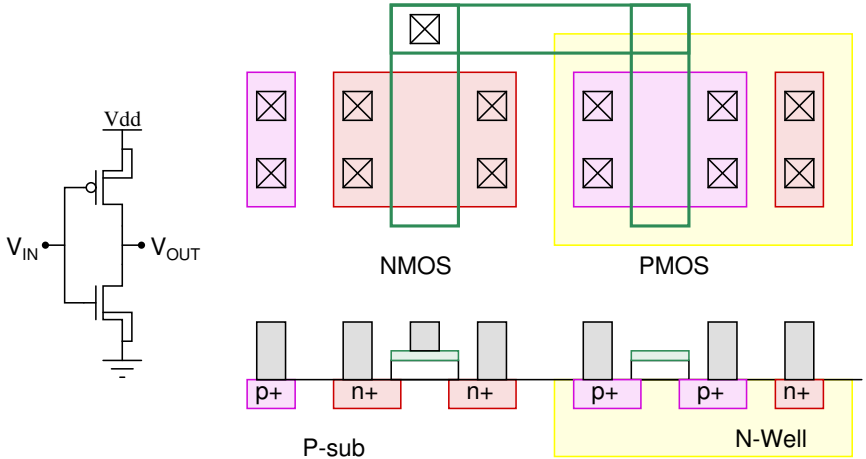


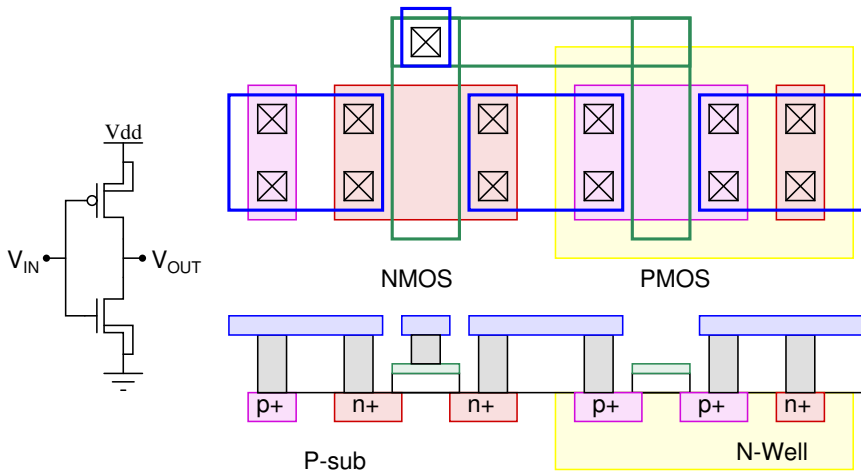
P-sub

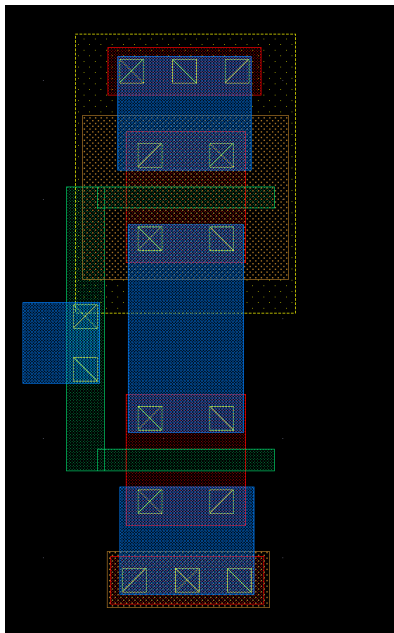


N-Well









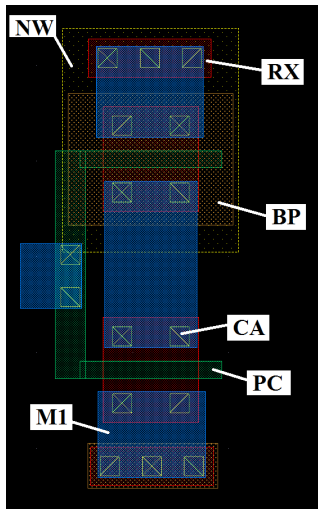
Na janela do esquemático:
Launch > Layout XL

Alguns atalhos:

f	Full view
m	Move
r	Draw rectangle
z	Zoom
shift+o	Rotate
s	Stretch
q	Properties



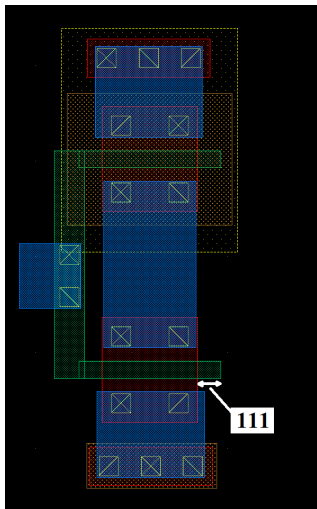
Nome das camadas (layers)



Na janela do esquemático:
Launch > Layout XL

Alguns atalhos:

f	Full view
m	Move
r	Draw rectangle
z	Zoom
shift+o	Rotate
s	Stretch
q	Properties



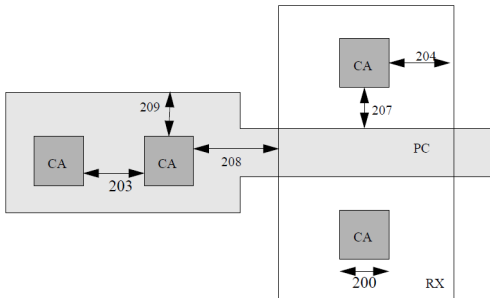
Arquivo de regras (Confidencial):
work/doc/cmrf7sf.design_manual.pdf

Por exemplo:

$$111 \left| \begin{array}{l} \text{(PC overlap past RX), when (PC intersect RX) to} \\ \text{RX corner} \geq 0.08 \end{array} \right| \geq \left| 0.240 \right|$$



Exemplos de regras



200	CA width and length (exact)	≡	0.200
203a	CA to CA	≥	0.240
204	CA within RX	≥	0.100
207	CA(over RX) to adj PC	≥	0.160
208	CA(over PC) to adj RX	≥	0.160
209	CA within PC	≥	0.060



Criar os pinos no layout, para isso procure o menu:

Create > Pin ...

- Deve colocar os mesmos nomes do esquemático.
- escolher corretamente input ou output.
- Desenhar na mesma camada do metal.



Para verificar as regras:

IBM.PDK > Checking > Assura > DRC

Run Assura DRC

Layout Design Source: **DFI** Compare two layouts: ☐ Generate Lvl Compare Rules...

Library: **aula1** Cell: **inversor1** View: **layout** Browse...

Save Extracted View: ☐ View Name: **drc_extracted**

Area To Be Checked: **Full**

Run Name: **drc1** Run Directory: **.drc1**

Run Location: **local**

View Rules Files: ☒ Technology: **-undefined-** Rule Set: **default**

Rules File: **ibm/cmr7sf/v2.0.0.0AM/Assura/DRC/drc.rul** View... Edit... Reload

Switch Names: **GridCheck** Set Switches

RSF Include: View... Edit...

Variable: **None** Value: Default: Description:

View avParameters: ☐ Modify avParameters... 1 avParameter is set.

View Additional Functions: ☐ No additional functions are set.

Enable limitDrcCheck: ☐

OK Cancel Apply Defaults Load State Save State View RSF Help



Layout vs. Schematic (LVS)

IBM_PDK > Checking > Assura > LVS

Run Assura LVS

Schematic Design Source: Use Existing Netlist: ☐ Netlisting Options...
Use Verilog Top Cell: ☐

Library: Cell: View: Browse...

Layout Design Source: Use Existing Extracted Netlist: ☐

Library: Cell: View: Browse...

Run Name: Run Directory: ...

Run Location:

View Rules Files: ☒ Technology: Rule Set:

Extract Rules: View... Edit... Reload

Compare Rules: View... Edit...

Switch Names: Set Switches

Binding File(s): View... Edit...

RSF Include: View... Edit...

Variable: Value: Default: Description:

View avParameters: ☐ Modify avParameters... 1 avParameter is set.

View avCompareRules: ☐ Modify avCompareRules... No avCompare rules are set.

View Additional Functions: ☐ No additional functions are set.

OK Cancel Apply Defaults Load State Save State View RSF Help

Run: "lvs1"

Run: "lvs1" from
/home/fabian/Desktop/cnrf/lvs1

Schematic and Layout Match.
You currently have an open run (project).

Do you want to close current project and view the results of new run?

Summary of LVS Issues

Extraction Information:

- 0 cells have 0 mal-formed device problems
- 0 cells have 0 label short problems
- 0 cells have 0 label open problems

Comparison Information:

- 0 cells have 0 Net mismatches
- 0 cells have 0 Device mismatches
- 0 cells have 0 Pin mismatches
- 0 cells have 0 Parameter mismatches

Yes No Help



- Fazer o layout das portas NAND e NOR.