Circuitos e Sistemas Integrados - Introdução ao Projeto VLSI

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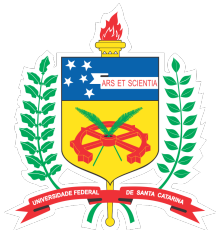


Universidade Federal de Santa Catarina
Florianópolis

2019

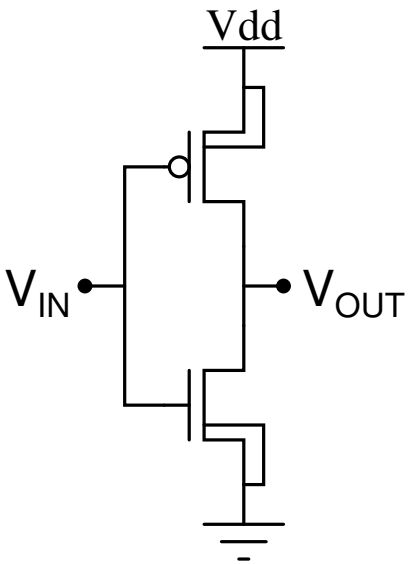
Forma de avaliação

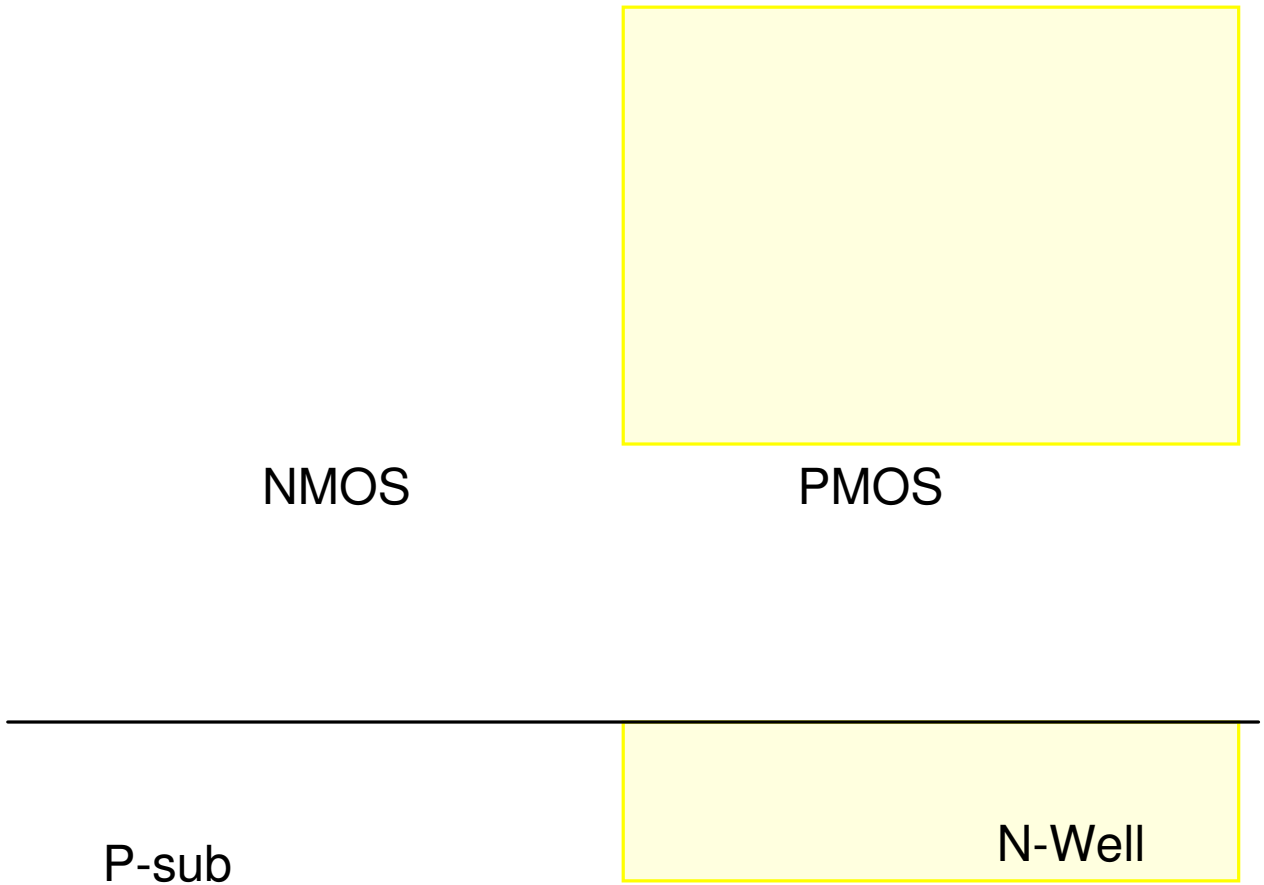
- Entregar o desenho do layout do inversor (feito a mão) em folha de papel. (pode usar diferentes cores)
- Entregar a biblioteca criada no Cadence comprimida. Se o nome da biblioteca é aula1 então pode usar o comando para comprimir: tar cvfz aula1.tar.gz aula1
- Mostrar em sala de aula o resultado correto do DRC e LVS.

Critérios de avaliação da folha a ser entregue

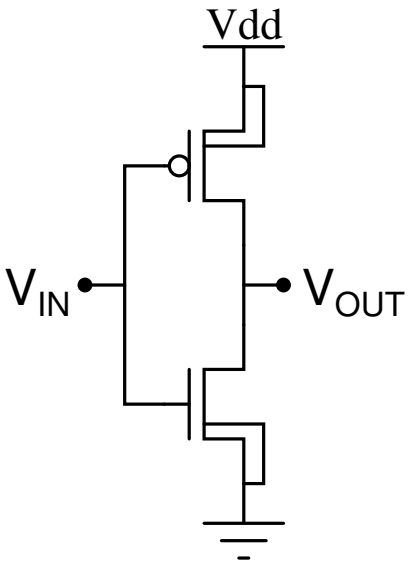
- Representação física correta do layout.
- Identificação de todas as camadas e nós.

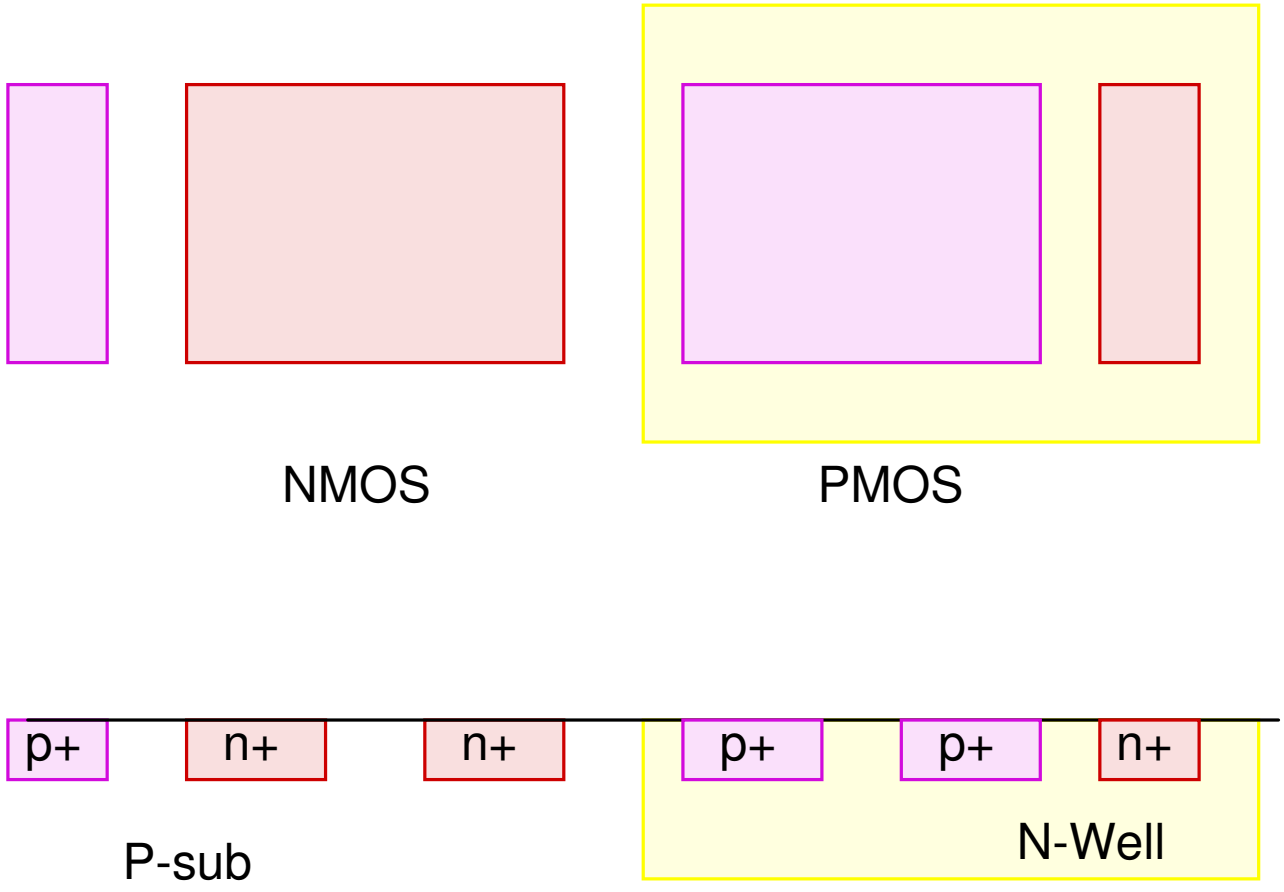
Substrato-P e Poço-N



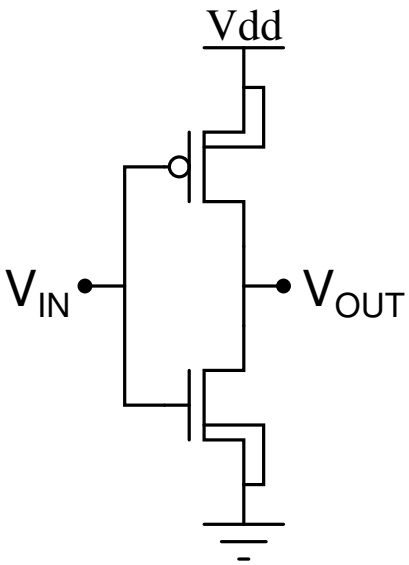


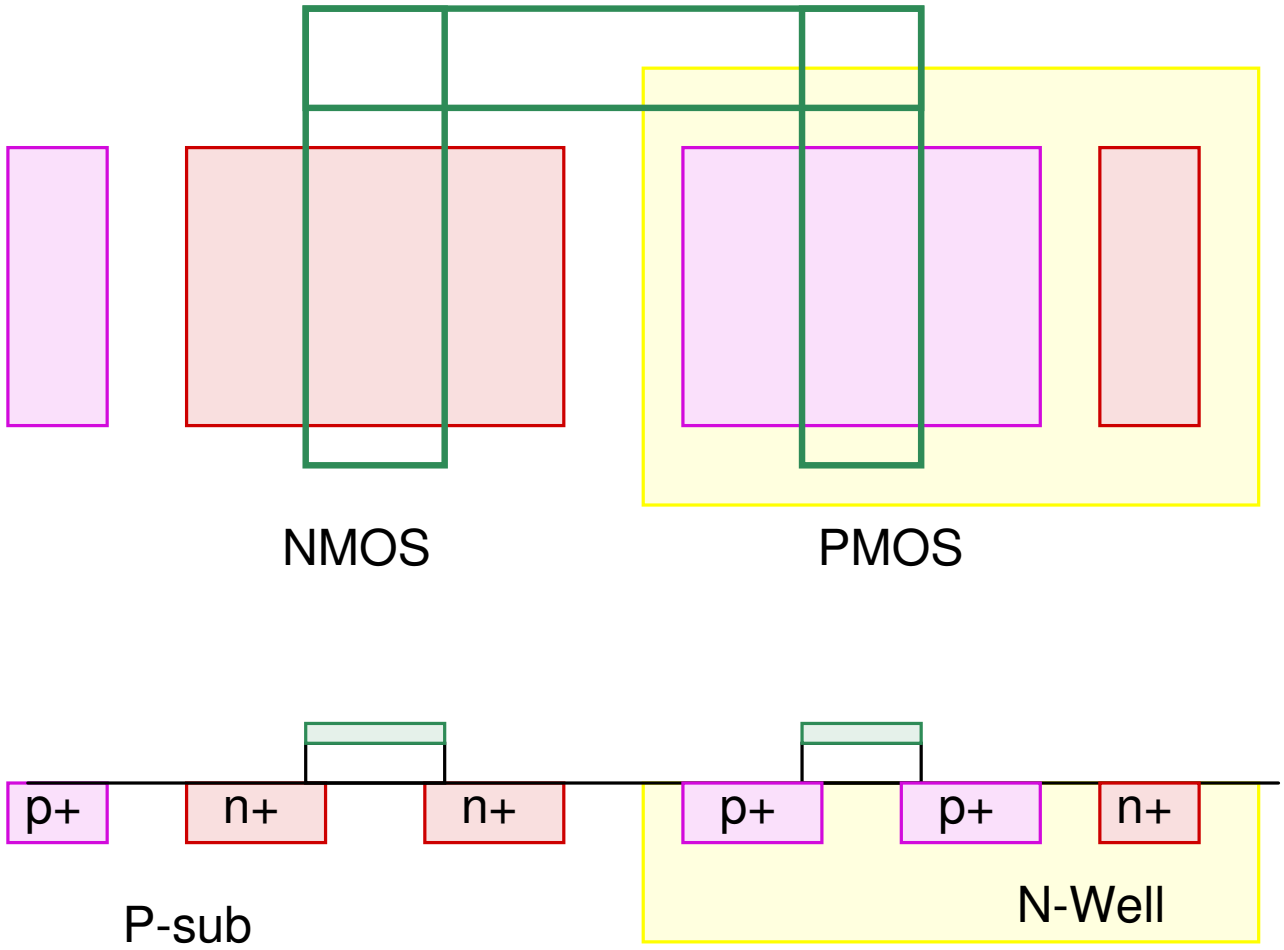
Difussões n+ e p+



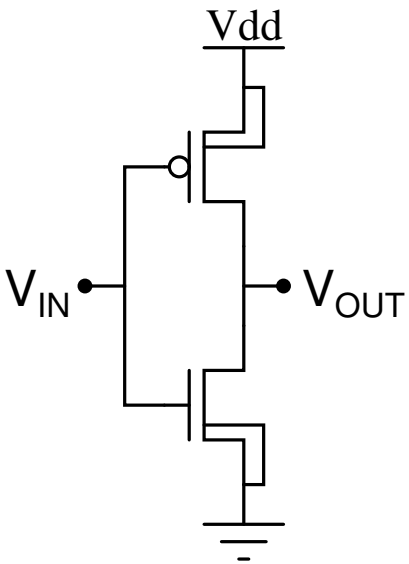


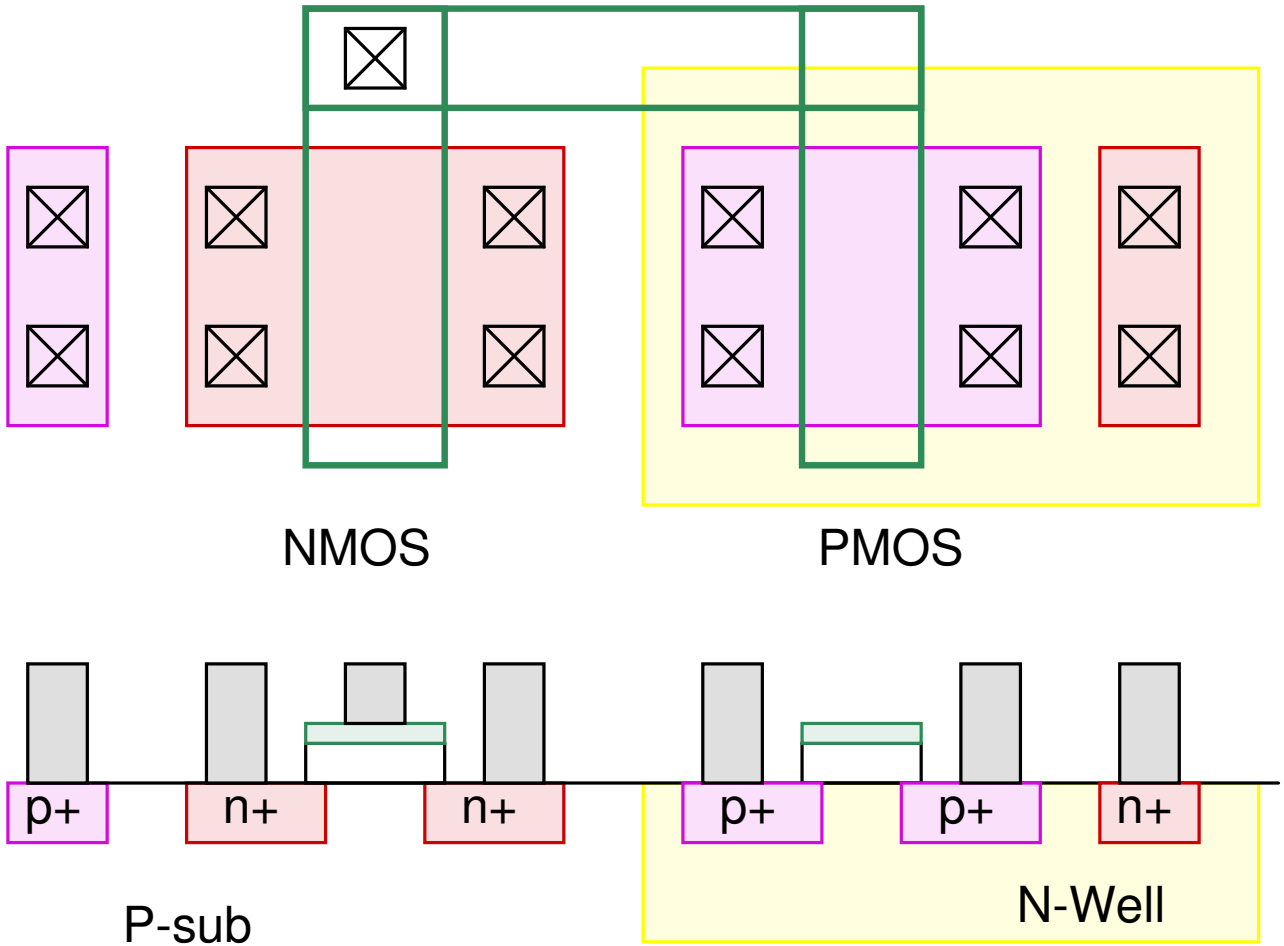
Polisilício



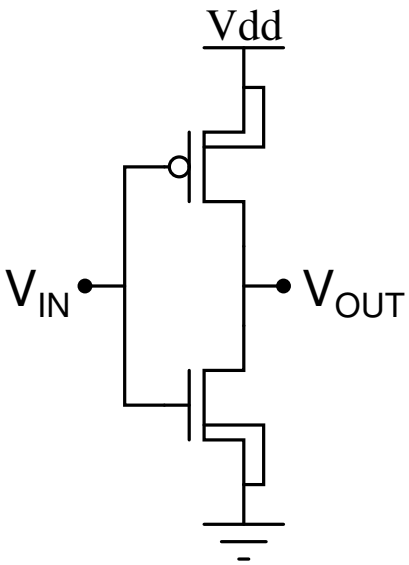


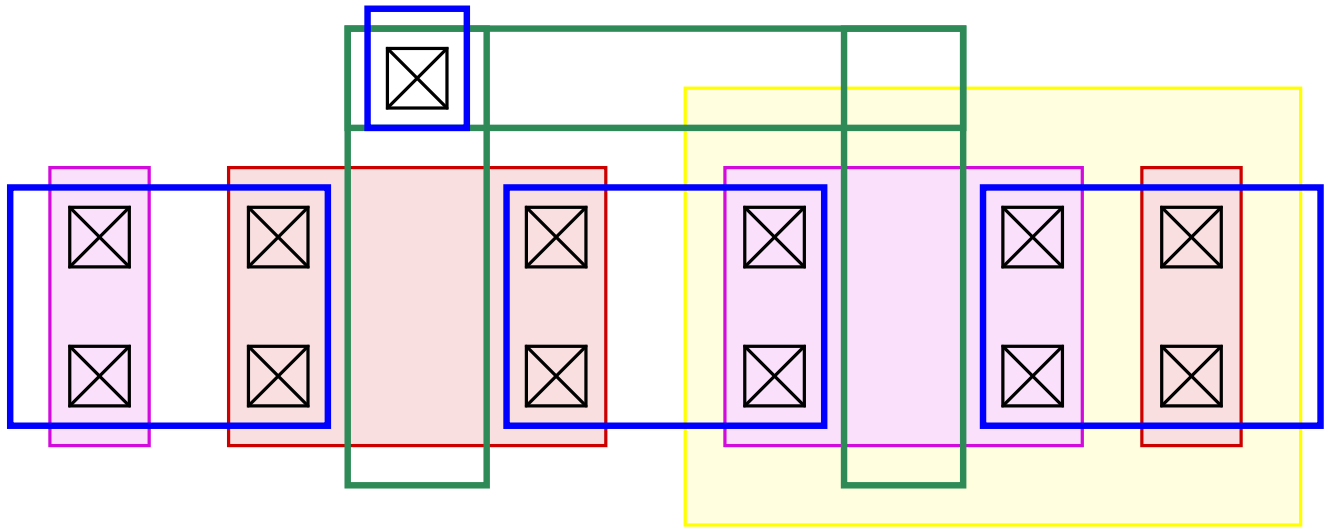
Contatos

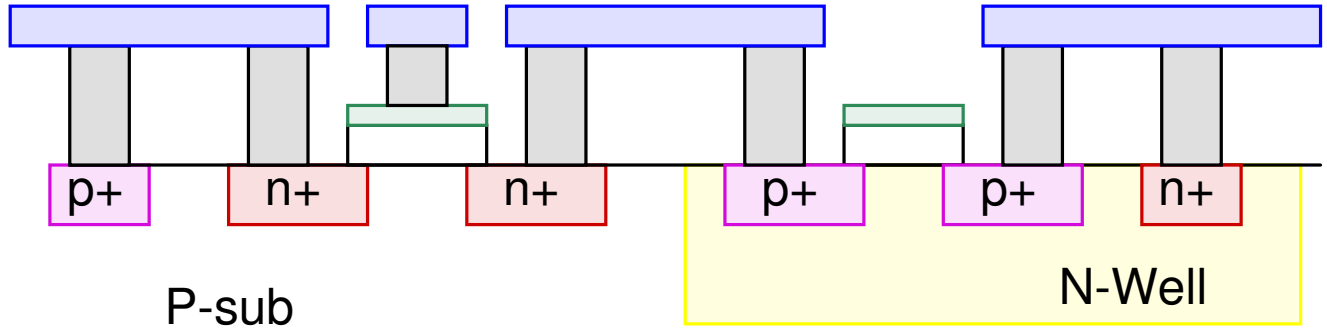




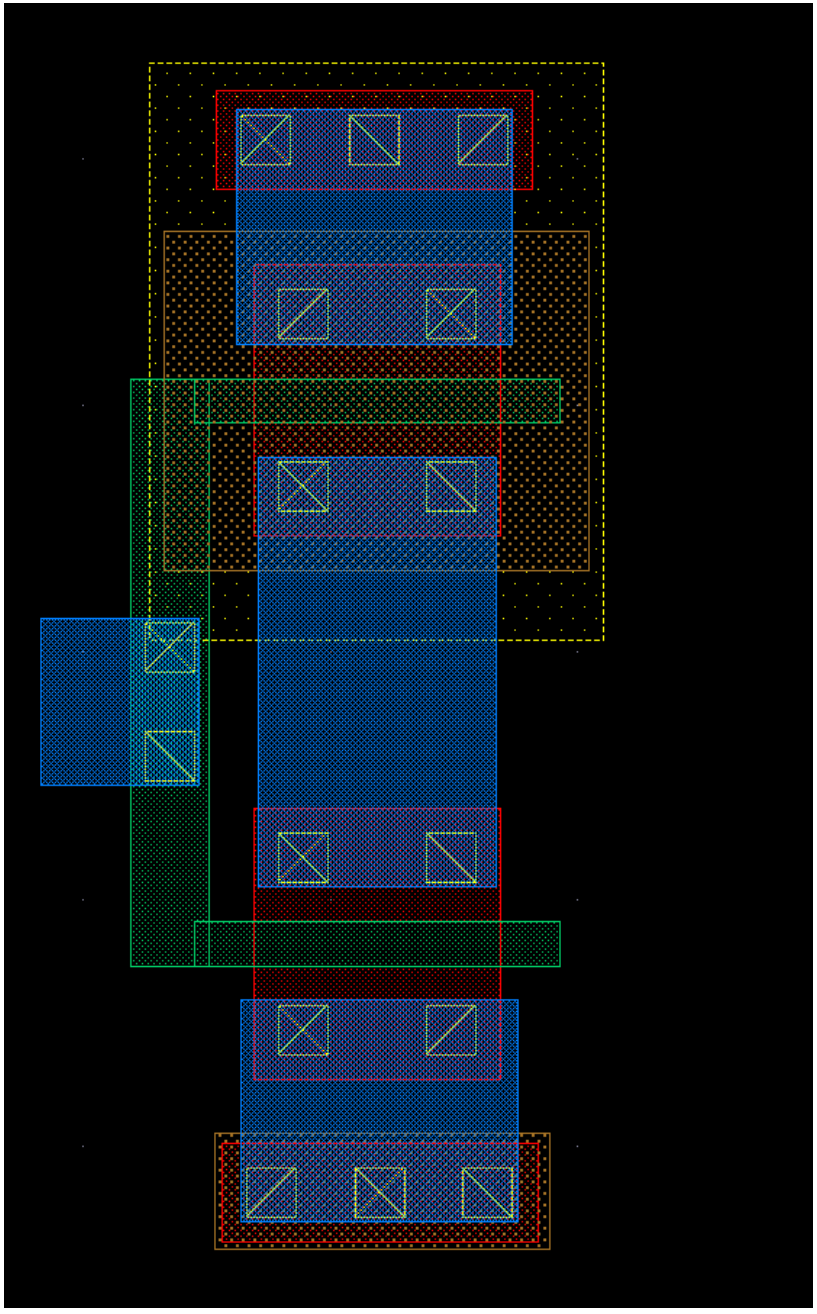
Metal 1







Layout no Cadence

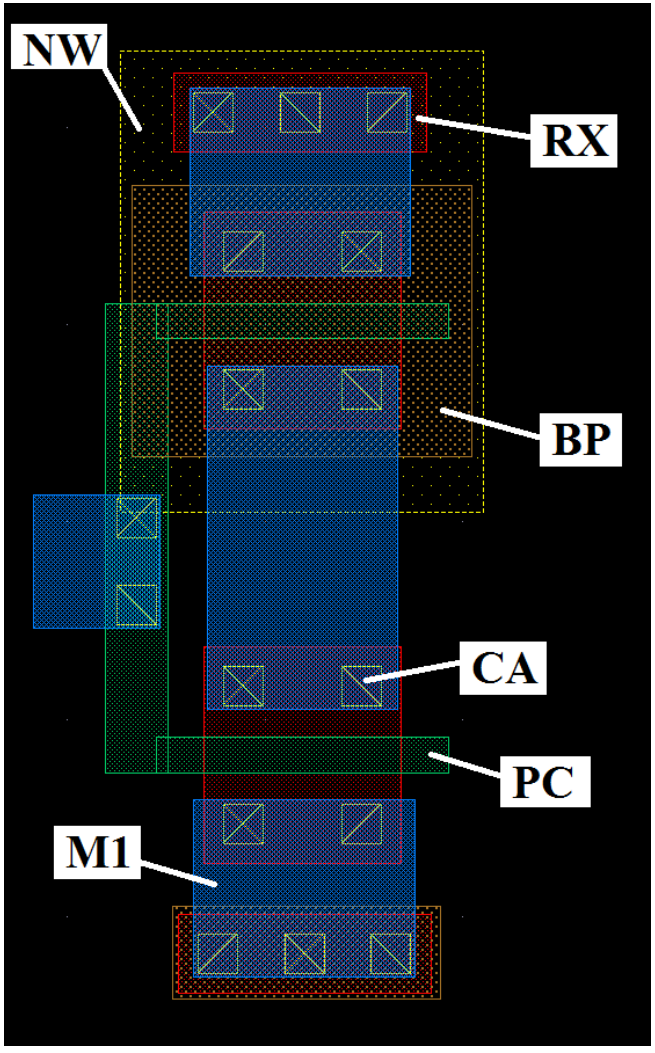


Na janela do esquemático:
Launch > Layout XL

Alguns atalhos:

f	Full view
m	Move
r	Draw rectangle
z	Zoom
shift+o	Rotate
s	Stretch
q	Properties

Nome das camadas (layers)



Na janela do esquemático:
Launch > Layout XL

Alguns atalhos:

f	Full view
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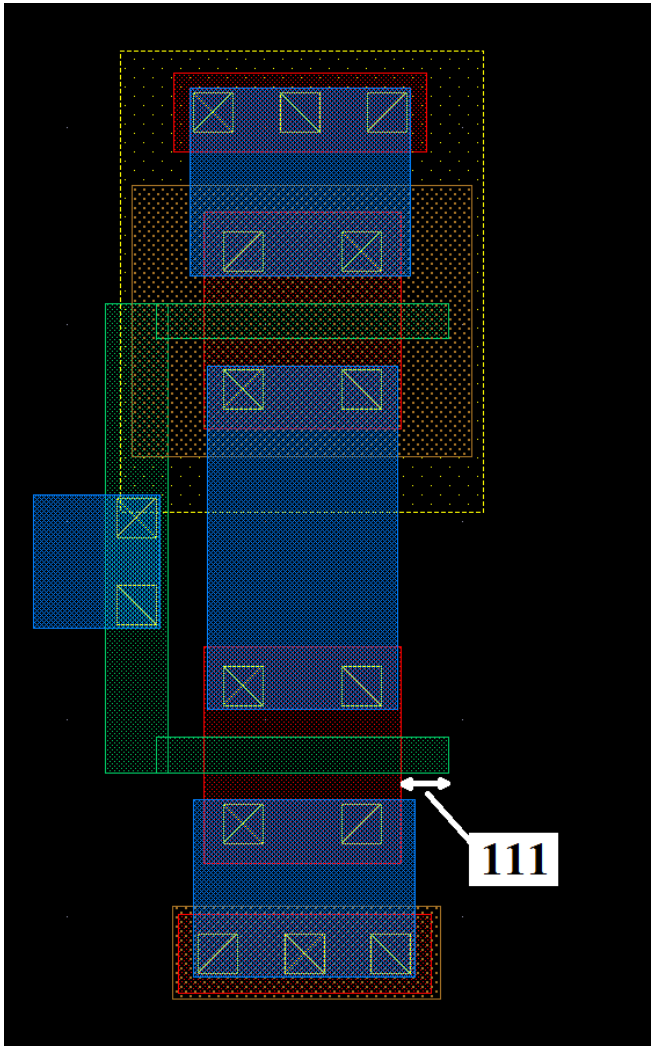
shift+o	Rotate
s	Stretch
q	Properties

Design Rule Check (DRC)

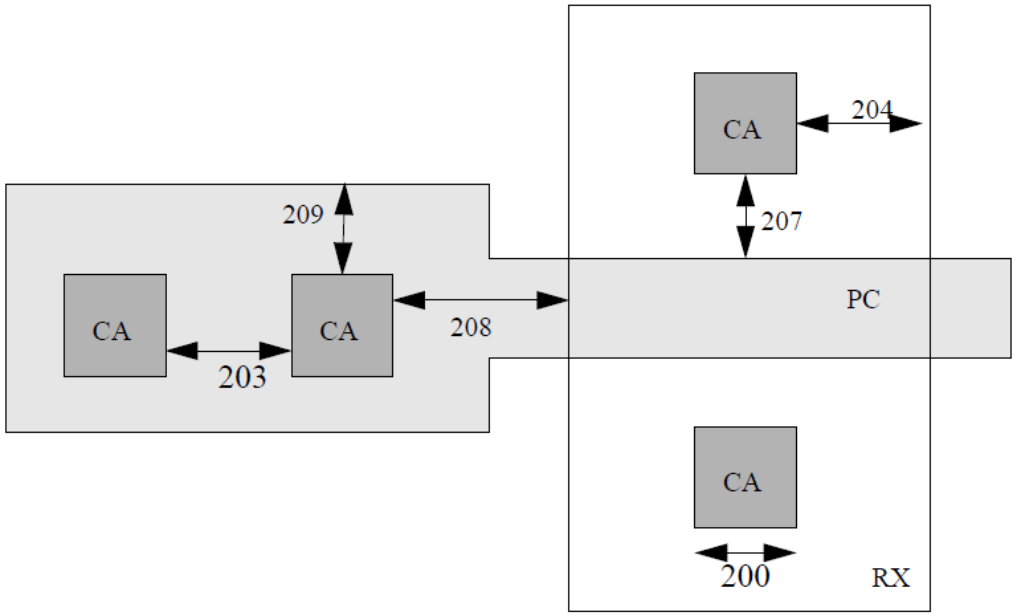


Arquivo de regras (Confidencial):
work/doc/cmrf7sf.design_manual.pdf

Por exemplo:

111	(PC overlap past RX), when (PC intersect RX) to RX corner ≥ 0.08	≥	0.240

Exemplos de regras



200	CA width and length (exact)	≡	0.200
203a	CA to CA	≥	0.240
204	CA within RX	≥	0.100
207	CA(over RX) to adj PC	≥	0.160
208	CA(over PC) to adj RX	≥	0.160
209	CA within PC	≥	0.060

Pinos no layout

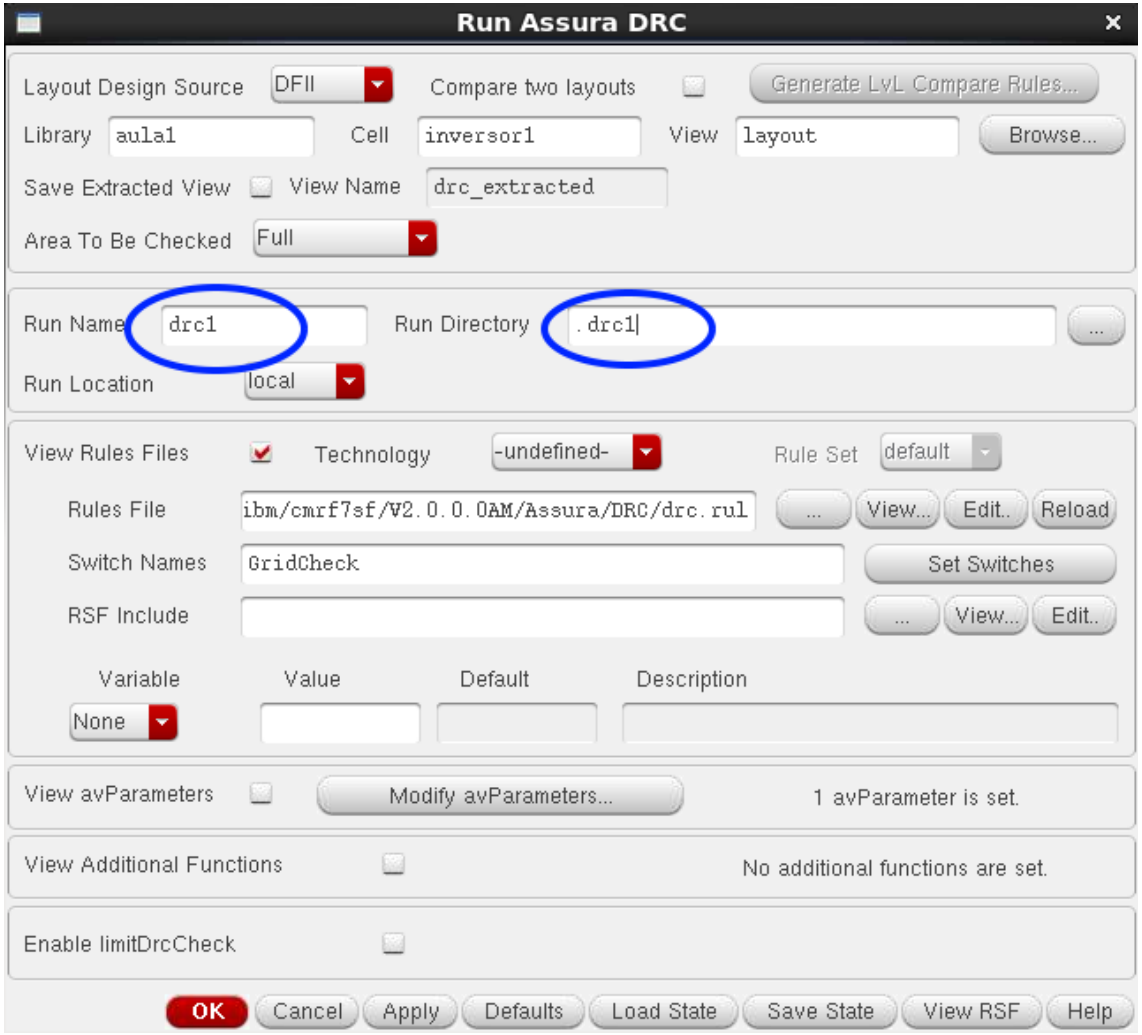
Criar os pinos no layout, para isso procure o menu:

Create > Pin ...

- Deve colocar os mesmos nomes do esquemático.
- escolher corretamente input ou output.
- Desenhar na mesma camada do metal.

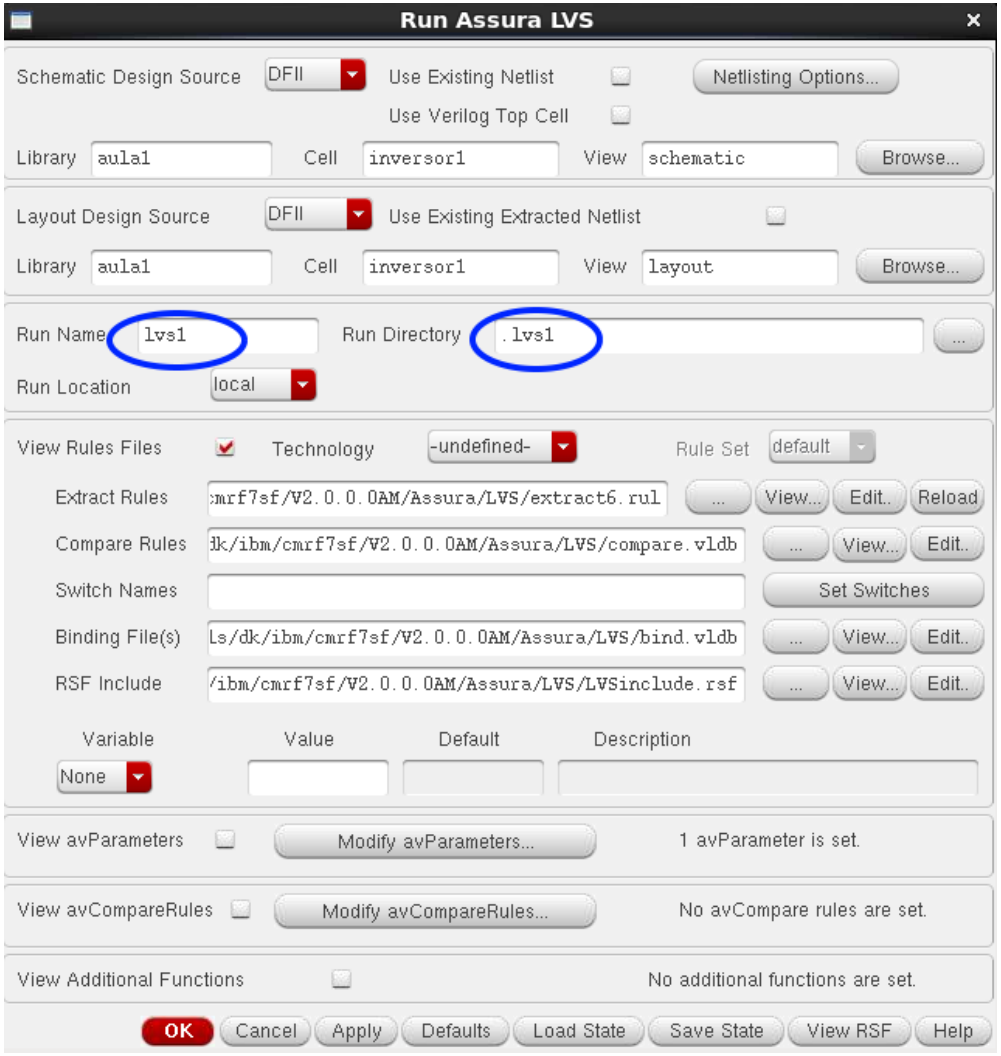
Verificando as regras

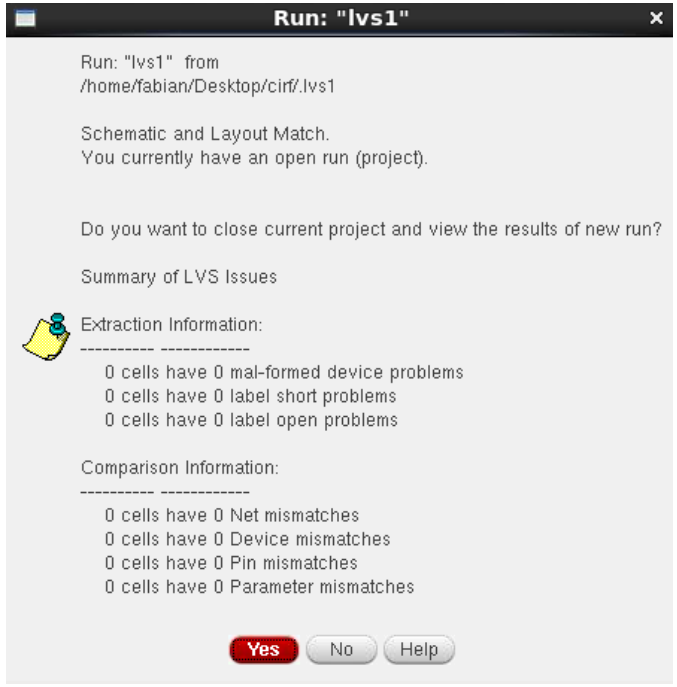
Para verificar as regras:
IBM_PDK > Checking > Assura > DRC



Layout vs. Schematic (LVS)

IBM_PDK > Checking > Assura > LVS





Tarefa opcional

- Fazer o layout das portas NAND e NOR.