IObundle 2ES MP3 Encoder

User Guide

IOB-2ES-MP3-E, Version 0.21 , Build 84e1e30

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Revision History

Date	Author	Summary of changes
15/06/2018	J. Sousa	Initial draft
19/06/2018	J. Sousa	Added revision history. Added second mute signal in Table 4. Improved Table 12, removed direct setting or getting of Control Word. Added Table 13. Added Table 3. Added Timing column to Table 16.
20/06/2018	J. Sousa	Improved Fig. 6, Table 20, removed FIFO status bits and improved table 16, added Table 4, improved Fig. 5, added section.
21/06/2018	J. Sousa	Changed document category to User Guide, improved Fig. 6, added signals in Table 16, added Fig. 4, UART reference, second watchdog timer for system stall.
22/06/2018	J. Sousa	Hided hyperlink color borders, improved Fig. 2, Added RS232 and channel mode to features. Improved Fig. 4. Removed white spaces. Added HW and SW hard coded version parameters. Improved Table 21.
23/06/2018	J. Sousa	Pause mode added. Fixed tables 7, 12, 9 13, 16, 17, 21. Table 22 added. Fixed Figs. 2 and 6.
25/06/2018	J. Sousa	Stop command removed. Reset and pause commands improved. Fixed tables 4, 10, 13, 17, 21. Explanation added in section 9.2. Fixed Figs. 5, 6. Replaced T_com with T_cmd.
27/06/2018	J. Sousa	Improved Fig. 5. Added conversion formula after Table 3. Created a clear separation in Table 13. Added explanation in Table 12. Created split tables 16 and 17. Added section 4.4 that describes the mask bits. Added section 5. Added section 6. Added Table 6. Updated RS232 usage.
28/06/2018	J. Sousa	Improved Fig. 3 and 2, Tables 17 and 22, section 5, 6, 4.3.4.
29/06/2018	J. Sousa	Added Table 14 and improved Table 7, Table 16, Table 17, Table 10, Table 21, Table 7, Fig. 4, Fig. 6, Table 20, Table 9, Table 12.
09/07/2018	J. Sousa	Removed 24-bit support and added sample rate conversion table.
11/07/2018	J. Sousa	Fixed Fig. 2, Table 7, Table 20.
12/07/2018	J. Sousa	Improved tables 4, 4, 4, 14, 16, 17, 23. Added tables 5,15. Replaced watchdog timer table with plain text explanation. Removed fixed sample rate from Fig. 4

Table 1: Revision history

Date	Author	Summary of changes
23/07/2018	J. Sousa	Fixed Table 23 and Table 20. Added clarification on latency. Added correct part number to block diagram.
25/07/2018	J. Sousa	Added symbol in Fig. 1. Added Ethernet interface signals and explanations. All SPI operation material grouped in section 4 and detailed comments to each subsection. Added Ethernet testing.
26/07/2018	J. Sousa	Fixed this table. Fixed section 4.4. Improved Fig. 2. Added section 2.1. Added correct part number to Table 20.
28/07/2018	J. Sousa	Replaced Intel Ethernet core with IObundle 2-port UDP core. Improved explanation for Reset command and recommended action on Stall. Renamed InvalidCommand to cmdFail and moved this interrupt flag from CPU1/2 to CPU0.
31/07/2018	J. Sousa	Replaced Ethernet IP in features and its section.
27/08/2018	J. Sousa	Changed Fig. 2, Fig. 5, section 2, section 4
09/09/2018	J. Sousa	Updates figures: 2, 3, 4, 6. Updated tables: 3, 4, 5, 6, 7, 12, 13, 17, 19, 20. Added section 11
17/09/2018	J. Sousa	Added test section. Updated sections 2.1.
01/05/2019	J. Sousa	Complete userguide upgrade. Removed Ethernet and testing sections.
09/06/2019	J. Sousa	Changed timeout and interrupt mask defaults and changed returned SIW upon RUN, RESET and PAUSE.

Table 2: Revision history (continued)

Constants

Symbol	Value	Unit	Description
f_{sys_clk}	User specified	Hz	System clock frequency
f_{sample}	48	kHz	Sample rate frequency
f_{i2s_lrclk}	48	kHz	Audio input I2S word clock frequency
f_{spi_sclk}	User specified	Hz	SPI interface clock frequency
f_{out_clk}	User specified	kHz	Audio output parallel interface clock
l_{frame}	576 or 1152	none	PCM frame length in samples. 576 samples for 32 and 64 kbps bitrates due to internal sample rate conversion to 16 and 24 kHz, respectively
T_{cmd}	10000	System clock cycles	Guaranteed max time to process a command

Table 3: Table of constants

1 Introduction

The IOB-2ES-MP3-E is an IP core for independent and simultaneously encoding 2 audio PCM streams into 2 MPEG 1/2 Layer III (MP3) audio streams. The IP is currently supported in Intel FPGAs.

1.1 Symbol

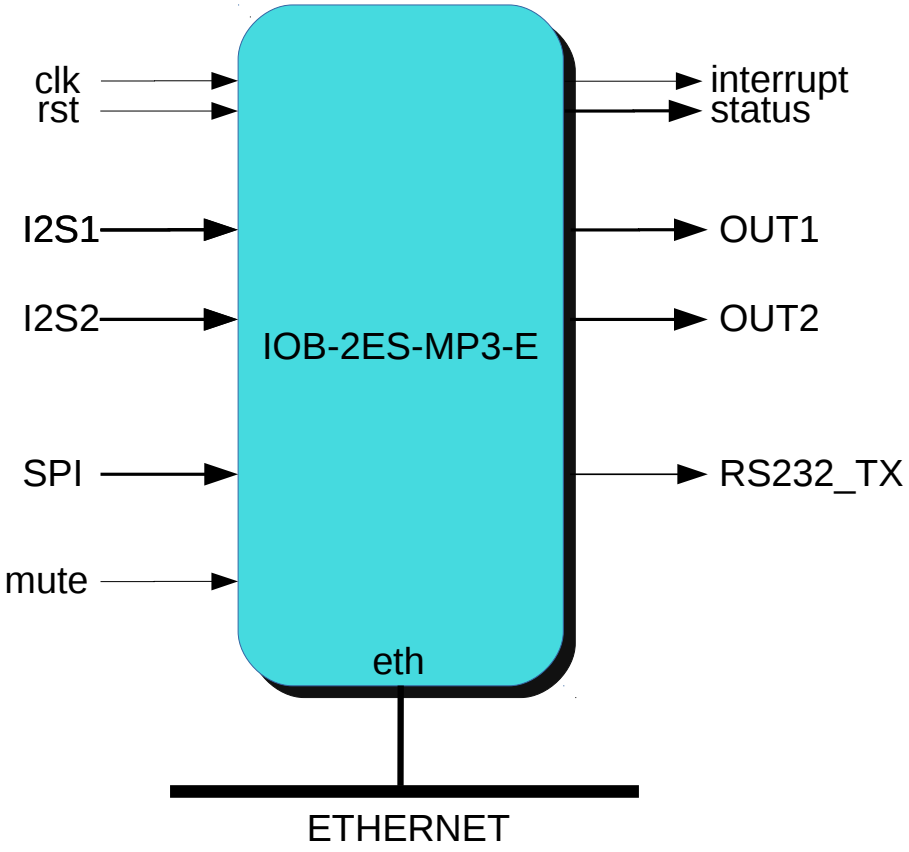

Figure 1: IP symbol

1.2 Features

- ISO/IEC 11172-3 MPEG 1 Layer III standard
- SPI slave interface for configuration, control and status information
- RS232 interfaces for viewing runtime messages
- 2 encoder CPUs
- 1 control CPU
- 2 Audio input I2S slave interfaces
- 2 Audio output parallel master interfaces
- 48KHz audio sample rate frequency
- 16-bit audio sample size
- Fixed stereo audio channel mode
- Guaranteed 2-frame latency and real time operation
- 3 watchdog timers to detect stall in each CPU

1.3 Benefits

- Compact hardware implementation
- Can be integrated with other functions in the same FPGA
- Low operation frequency
- Low power consumption

2 Block Diagram

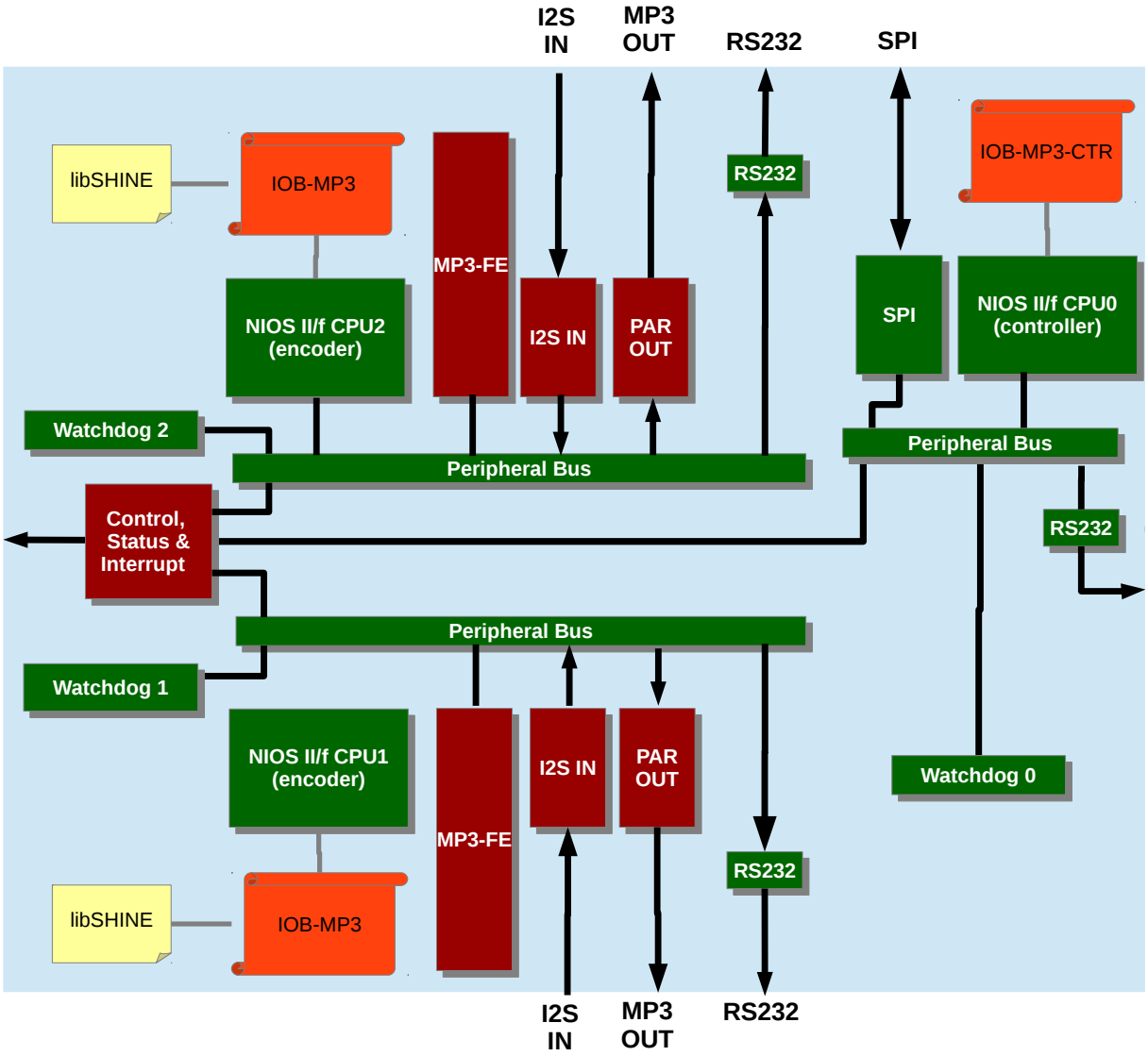

Figure 2: Block diagram

2.1 Functional Description

2.1.1 Hardware Components

NIOS II/f CPU0: Used for system control and test. Controls CPU1 and CPU2 according to user commands. Receives commands and sends responses via SPI. In test mode, receives audio data from Ethernet, sends audio data to CPU1 and CPU2 via I2S output, collects encoded data via Audio PAR IN. Updates its status and interrupt bits.

NIOS II/f CPU1 and CPU2: Used for encoding audio data in the MP3 format. Receive commands and encoding parameters from CPU0 via Control Reg. Receive data from Audio IN I2S and send encoded data through Audio OUT PAR. Update their status and interrupt bits.

RS232: Used for displaying runtime messages, errors and status information.

SPI slave: Used for receiving commands from host machine.

I2S IN: Used by CPU1 and CPU2 to input PCM audio data.

I2S OUT: Used by CPU0 to produce a test I2S interface

PAR OUT: Used by CPU1 and CPU2 to output MP3 audio data.

PAR IN: Used by CPU0 to input MP3 audio data for testing.

MP3-FE: MP3 front-end (sample rate conversion, sub-band filter bank and MDCT) implemented in hardware.

Watchdog: Used to monitor if the respective host CPU has stalled.

Control, Status & Interrupt: Used by CPU0 to send commands to CPU1 and CPU2, used by the 3 CPUs to update status and interrupt bits.

2.1.2 Software Components

IOB-MP3: MP3 encoder wrapper: controls and configures the libSHINE encoder library according to commands received from IOB-MP3-CTR. Runs on CPU1 and CPU2.

libSHINE: MP3 encoder library. Called by IOB-MP3.

IOB-MP3-CTR: Runs on CPU0 and controls and configures the encoders running on CPU1 and CPU2.

IOB-MP3-TEST: Runs on a personal computer and exercises a board containg an FPGA configured with the IOB-2ES-MP3-E system for test and demonstration purposes.

3 Interface Signals

3.1 General Interface Signals

Signal	Direction	Description
sys_clk	IN	Main system clock
sys_rst	IN	Asynchronous active high reset signal.
mute_1	IN	When high mutes encoder on CPU1. I2S input data is ignored and a muted MP3 stream is produced at the output.
mute_2	IN	When high mutes encoder on CPU2. I2S input data is ignored and a muted MP3 stream is produced at the output.
interrupt	OUT	Interrupt signal; goes high if any unmasked interrupt bit is high.
status[31:0]	OUT	Status and Interrupt Word as in Table 14.

Table 4: General interface signals

3.2 RS232 Interface Signals

The RS232 IP core used in the *Intel FPGA UART Core* described in Chapter 9 of the following document accessed in June/20/2018 from

https://www.altera.com/en_US/pdfs/literature/ug/ug_embedded_ip.pdf.

Three instances of this IP are being used, one for each CPU. However, only one RS232 pin is used, according to the table below:

Signal	Direction	Description
rs232_tx	OUT	Serial transmit signal from CPU0
rs232_tx_1	OUT	Serial transmit signal from CPU1
rs232_tx_2	OUT	Serial transmit signal CPU2

Table 5: RS232 interface signals

3.3 Audio Input I2S Slave Interface

Signal	Direction	Description
i2s_bclk_1	IN	Bit clock for encoder on CPU1. Samples data at rising edge.
i2s_lrclk_1	IN	Word clock for encoder on CPU1. Left channel when 0, right when 1.
i2s_data_1	IN	I2S serial data for encoder on CPU1.
i2s_bclk_2	IN	Bit clock for encoder on CPU2. Samples data at rising edge.
i2s_lrclk_2	IN	Word clock for encoder on CPU2. Left channel when 0, right when 1.
i2s_data_2	IN	I2S serial data for encoder on CPU2.

Table 6: Audio input I2S slave interface

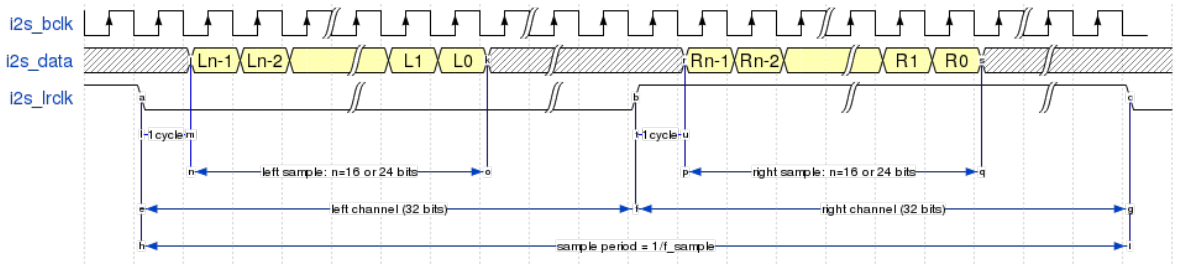

Figure 3: Audio input I2S slave interface timing diagram

3.4 Audio Output Parallel Interface

Signal	Direction	Description
out_clk	IN	Audio output clock.
out_valid_1	OUT	Audio output valid for CPU1.
out_frame_start_1	OUT	High when the first stream byte is output by CPU1, low otherwise.
out_frame_end_1	OUT	High when the last stream byte is output by CPU1, low otherwise.
out_bitrate_1[1:0]	OUT	Audio output bit rate for CPU1: 00=32kbps, 01=64kbps, 10=128kbps, 11=192kbps.
out_samplerate_1[1:0]	OUT	Audio output sample rate by CPU1: 00=16kHz, 01=24kHz, 10=48kHz, 11=unused.
out_data_1[7:0]	OUT	Audio output bistream data from CPU1 organized in bytes.
out_valid	OUT	Audio output valid for CPU2.
out_frame_start_2[1:0]	OUT	High when the first stream byte is output by CPU2, low otherwise.
out_frame_end_2[1:0]	OUT	High when the last stream byte is output by CPU2, low otherwise.
out_bitrate_2[1:0]	OUT	Audio output bit rate for CPU2: 00=32kbps, 01=64kbps, 10=128kbps, 11=192kbps.
out_samplerate_2[1:0]	OUT	Audio output sample rate for CPU2: 00=16kHz, 01=24kHz, 10=48kHz, 11=unused.
out_data_2[7:0]	OUT	Audio output bistream data from CPU2 organized in bytes.

Table 7: Audio Output parallel interface signals

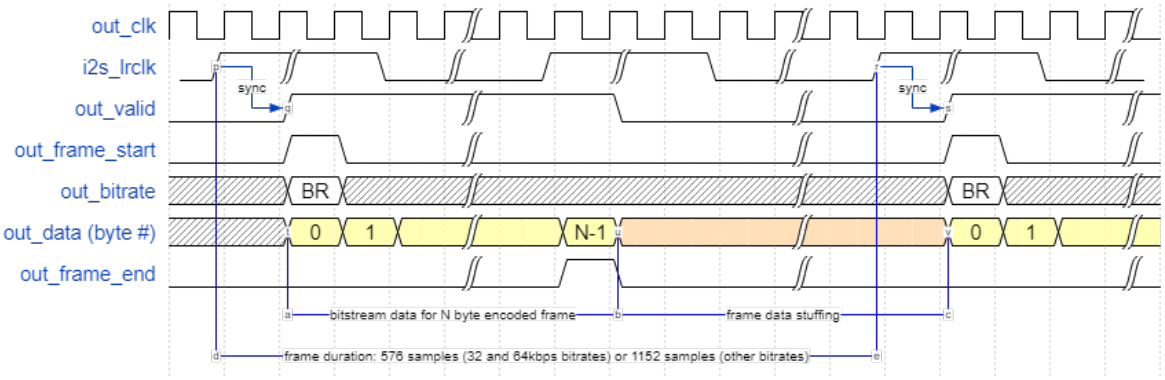

Figure 4: Audio output parallel interface timing diagram

3.5 SPI Slave Interface

Signal	Direction	Description
spi_sclk	IN	SPI serial (bit) clock.
spi_mosi	IN	SPI master output / slave input.
spi_miso	OUT	SPI master input / slave output.
spi_ss	IN	SPI slave select.

Table 8: SPI slave interface

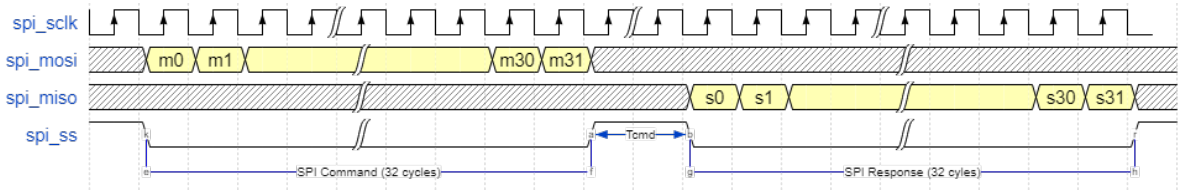

Figure 5: SPI slave interface timing diagram

4 SPI Operation

4.1 Master Control Word

The Master Control Word (MCW) is sent by the SPI master to CPU0, in order to control the operation of the IOB-2ES-MP3-E core. The structure of the MCW is detailed in Fig. 9.

Command[31:28]	Processors[27:24]	Argument[23:0]

Table 9: Master Control Word

The MCW fields are described in the next subsections.

4.1.1 Command Field

The list of commands that can be sent to the IOB-2ES-MP3-E core is detailed in Table 10 below.

Command	Code	Description
Get	0010	Gets parameters according to the Argument field for the selected processor in the Processors field. It is possible to Get parameters for a running, paused or idle processor. The Processors field must select a single processor or otherwise the command is invalid and will raise the cmdFail interrupt bit.
Set	0001	Sets parameters according to the Argument field for the selected processors in the Processors field. It is possible to Set parameters for an idle processor. Additionally, it is possible to Set the BIT_RATE parameter for a running or paused processor, which becomes effective for encoding the next frame after the Set command is executed.
Run	0011	Runs the encoder processors selected in the Processors field. The command will enable the I2S input previously disabled. It is still possible to Get parameters for a running processor; however only the BIT_RATE parameter can be set and any attempt to Set other parameters will raise the cmdFail interrupt bit. Argument field ignored.
Pause	0100	Pauses the processors selected in the Processors field after finishing encoding the current frame. Settings, internal data buffers, input and output FIFOs are preserved. Data input is ignored. Argument field ignored.
Reset	0000	Sends a hardware reset to the processors selected in the Processors field. Restores parameters to default values. Flushes internal data buffers, input and output FIFOs. Resets the program counter. Status and interrupt bits are cleared. Namely, the Ready status bit of the selected processors goes low until this command has completed after which it goes high again. Argument field ignored.

Table 10: Command field

4.1.2 Processors Field

It is possible to send the same command to multiple processors by simultaneously activating multiple bits of the Processors field.

Bit#	Description
27	Reserved.
26	When high selects processor CPU2.
25	When high selects processor CPU1.
24	When high selects processor CPU0.

Table 11: Processors field

4.1.3 Argument Field

The Argument field is used to send command options as explained in Table 12 below.

Command	Parameter	Argument[23:16]	Argument[15:0]
Get	BIT_RATE(1)	0x04	Don't Care.
Get	INTRRPT_MASK	0x05	Don't Care.
Get	STATUS_INTRRPT	0x0D	Don't Care.
Get	TIMEOUT	0x13	Don't Care.
Get	VERSION	0x09	Don't Care.
Get	LAST_COMMAND	0x12	Don't Care.
Get	HALF_VOLUME	0x0C	Don't Care.
Set	HALF_VOLUME	0x0C	0 means full scale volume, non-zero means half scale volume (-6dB)
Set	TIMEOUT_H	0x01	16-bit high part of 32-bit system wait time limit to activate Stall in Table 15 and Table 17 given in system clock cycles.
Set	TIMEOUT_L	0x02	16-bit low part of 32-bit TIMEOUT parameter.
Set	BIT_RATE	0x04	Output bitstream bit rate in kbps. Valid settings are 0x0020 (32kpbs), 0x0040 (64kbps), 0x0080 (128kbps) and 0x00C0 (192kbps).
Set	INTRRPT_MASK_H	0x06	16-bit high part of 32-bit Interrupt Mask Word. A bit is masked if its mask is 1 and unmasked otherwise.
Set	INTRRPT_MASK_L	0x07	16-bit low part of 32-bit Interrupt Mask Word. A bit is masked if its mask is 1 and unmasked otherwise.
Set	INTRRPT_CLR	0x0F	Don't Care; clears the Interrupt Bits.
Run(2)	NA	Don't Care	Don't Care.
Pause	NA	Don't Care	Don't Care.
Reset	NA	Don't Care	Don't Care.

Table 12: Argument field

(1) This Get command can only select one CPU, either CPU1 or CPU2. Otherwise the command will fail.
(2) The Run command can only select CPU1, CPU2 or both but not CPU0. Selecting CPU0 will raise the CmdFail flag.

4.2 Slave Response Word

The Slave Response Word (SRW) is sent by CPU0 to the SPI master as response to the previous command. For that the SPI master can optionally perform an SPI read cycle after the write cycle to send the command. See the timing diagram in Fig. 5. The structure of the SRW is detailed in Table 13.

Command	Argument	Description	Default
Get	BIT_RATE	Returns the output bitstream bit rate in kbps. Valid responses are 0x0020 (32kpbs), 0x0040 (64kbps), 0x0080 (128kbps) and 0x00C0 (192kbps).	0x00000080
Get	INTRRPT_MASK	Returns the Interrupt Mask Word.	0x1F7F1F74
Get	STATUS_INTRRPT	Returns Status and Interrupt Word.	0x00000000
Get	VERSION	Returns the product version in format 8Q8.	NA
Get	LAST_COMMAND	Returns the last command sent.	0x00000000
Get	TIMEOUT	Returns the TIMEOUT parameter. Either TIMEOUT_H or TIMEOUT_L can be used as argument.	0x09000000
Get	HALF_VOLUME	Returns the HALF_VOLUME parameter.	0x00000000
Set	HALF_VOLUME	Returns the just set HALF_VOLUME parameter.	NA
Set	BIT_RATE	Returns the just set BIT_RATE parameter.	NA
Set	INTRRPT_MASK_H	Returns the just set INTRRPT_MASK Word.	NA
Set	INTRRPT_MASK_L	Returns the just set INTRRPT_MASK Word	NA
Set	INTRRPT_CLR	Returns the previous Status and Interrupt Word before clearing.	NA
Set	TIMEOUT_H	Returns the just set TIMEOUT parameter.	NA
Set	TIMEOUT_L	Returns the just set TIMEOUT parameter.	NA
Run	NA	Returns the previous Status and Interrupt Word.	0x00000000
Pause	NA	Returns the previous Status and Interrupt Word.	0x00000000
Reset	NA	Returns the previous Status and Interrupt Word.	0x00000000

Table 13: Slave Response Word

4.3 Status and Interrupt Word

The Status and Interrupt Word (SIW) is present at the core interface as described in Table 4. The SIW is also accessible via SPI by means of a Get command and as explained in Table 12.

CPU2		RESERVED	CPU1		RESERVED	CPU0		
STATUS [31:29]	INTERRUPT [28:23]	[22:16]	STATUS [15:13]	INTERRUPT [12:7]	[6:3]	CmdFail [2]	Stall [1]	Ready [0]

Table 14: Status and Interrupt Word

The fields of the SIW are detailed in the next subsections.

4.3.1 Status and Interrupt Bits for CPU0

Bit#	Type	Name	Description	Timing
2	Interrupt	cmdFail	1 if last command sent is unrecognized and 0 otherwise	0-1 transition occurs at most T_{cmd} system clock cycles after an invalid command is issued; cleared on next command.
1	Interrupt	Stall	1 if CPU0 watchdog timer goes off and 0 otherwise; reveals a system or software issue	0-1 transition occurs if the watchdog timer counts to TIMEOUT system clock cycles; and remains 1 until cleared by HW reset or *Reset* command.
0	Status	Ready	1 if CPU ready or 0 otherwise; send commands if CPU ready.	0-1 transition occurs when the control sofware in CPU0 has initialized correctly and is ready to take commands; remains high until the HW is reset.

Table 15: Status and Interrupt Bits for CPU0 as in Table 14

4.3.2 Status Bits for CPU1 and CPU2

CPU 2 Bit#	CPU 1 Bit#	Name	Description	Timing
31	15	Ready	1 if encoder ready or 0 otherwise; send commands if encoder ready.	0-1 transition occurs when the sofware in both the Control CPU and the encoder CPU have initialized correctly and are ready to take commands; remains high until the HW is reset.
30:29	14:13	State	10 if running, 01 if paused and 00 if idle	Transition to running state occurs at most T_{cmd} system clock cycles after the *Run* command is issued; transitions from running state occurs at most $T_{cmd} + l_{frame}/f_{sample}$ seconds after the *Pause* command is issued.

Table 16: Status Bits for CPU1 and CPU2 as in Table 14

4.3.3 Interrupt Bits for CPU1 and CPU2

Bit# (CPU 2)	Bit# (CPU 1)	Name	Description	Timing
28	12	LatencyFail	1 if latency violated and 0 otherwise	Occurs if encoding the first frame takes more than $2 \times l_{frame}/f_{sample}$ seconds; remains high until the HW is reset or the *Reset* command is issued.
27	11	RealTimeFail	1 if real-time is violated and 0 otherwise	Occurs if encoding of a frame takes more than $\times l_{frame}/f_{sample}$ seconds; remains high until the HW is reset or the *Reset* command is issued.
25	9	InputOverflow	1 if internal I2S FIFO is ever full and 0 otherwise; happens if CPU is not fast enough or I2S is faster than f_{sample}	0-1 transition occurs while the encoder is running and condition happens and remains 1 until cleared by HW reset or *Reset* command.
24	8	I2SError	1 if the number of *bclk* cycles in a *lrclk* period I2S is different from 64 and 0 otherwise;	0-1 transition happens right after the negative edge of *lrclk* if the I2S period is short or if the bclk cycle count exceeds 64 if the I2S period is long. This flag remains 1 until cleared by HW reset or the *Reset* or *Set INTRRPT_CLR* commands are issued. ((This flag will mute the I2S input.))
23	7	Stall	1 if encoder watchdog timer goes off and 0 otherwise; reveals a system or software issue	0-1 transition occurs if the watchdog timer counts to TIMEOUT system clock cycles; and remains 1 until cleared by HW reset or *Reset* command.

Table 17: Interrupt Bits for CPU1 and CPU2 as in Table 14

4.3.4 Recommended Action on Interrupt

Name	Description
LatencyFail	Make sure the system clock and/or I2S frequencies are correct to prevent this condition. If they are correct attempt to reproduce the problem in the provided test environment. Collect RS232 logs and contact IObundle's customer support.
RealTimeFail	Make sure the system clock and/or I2S frequencies are correct to prevent this condition. If they are correct attempt to reproduce the problem in the provided test environment.
CmdFail	Invalid command. Fix the command and resend.
InputUnderflow	Make sure I2S is running and its frequency is not slower than f_{sample}.
InputOverflow	Make sure system clock is not slow and/or I2S clock is not faster than f_{sample}.
I2SError	Make sure I2S is sending the right number of bits per sample.
Stall	If CPU1 and/or CPU2 are stalled then reset the stalled processor(s) using the *Reset* command. If CPU0 is stalled perform a hardware reset on the system. Make sure the system clock and/or I2S frequencies are correct to prevent this condition. If they are correct attempt to reproduce the problem in the provided test environment.

Table 18: Recommended Action on Interrupt

In a situation the problem cannot be diagnosed or solved using the above, collect RS232 logs and contact IObundle's customer support.

4.4 Interrupt Mask Word

The Interrupt Mask Word (IMW) is accessible via SPI by means of Get/Set commands and as explained in Table 12. Refer to Table 12 for an explanation on how to set the bits of this word.

don't care[31:29]	**CPU2[28:23]**	don't care[21:13]	**CPU1[12:7]**	don't care[5:2]	**CPU0[2:1]**	don't care[0]

Table 19: Interrupt Mask Word to apply to the interrupt bits as in Table 14

5 Watchdog Timer Operation

5.1 Watchdog Timer Operation for CPU0

CPU0 continuously resets its watchdog timer and checks for commands in a polling loop.

If CPU0 stalls it can no longer do the above and its watchdog timer will count up to the user set TIMEOUT value and go off.

It is recommended that the TIMEOUT parameter is set so that the watchdog timer counts for at least 5 ms.

5.2 Watchdog Timer Operation for CPU1 and CPU2

CPU1 and CPU2 continuously reset their watchdog timer and encodes frames and in a loop.

If CPU1 and/or CPU2 stall they can no longer do the above and their watchdog timer will count up to the user set TIMEOUT value and go off.

It is recommended that the TIMEOUT parameter is set so that the watchdog timer counts for at least 30 ms.

6 Latency

Definition. *Latency (L) is the time from enabling the input of the core, upon receiving the Run command, to the output of the last byte of the first encoded frame as given by the following equation:*

$$L = 640/f_{sample} + T_1 + \frac{l_{frame} BIT\_RATE}{8 f_{sample} f_{out\_clk}}$$

where T_1 is the processing time for the first frame.

Note that encoding starts after 640 samples are received, since 512 zero-samples are automatically inserted by the encoder after it is started (algorithmic latency, which is not included in the above definition), takes T_1 seconds to process the frame thus formed and outputs $\frac{l_{frame} BIT\_RATE}{8 f_{sample}}$ bytes at frequency f_{out_clk}.

Example. *Let BIT_RATE = 64kbps, $f_{out\_clk} = 50\ MHz$ and $T_1 = l_{frame}/f_{sample}$.*
Then, using the above equation L=37.337 ms, which is about 1.56 the time of a frame.

7 Operation Flowchart

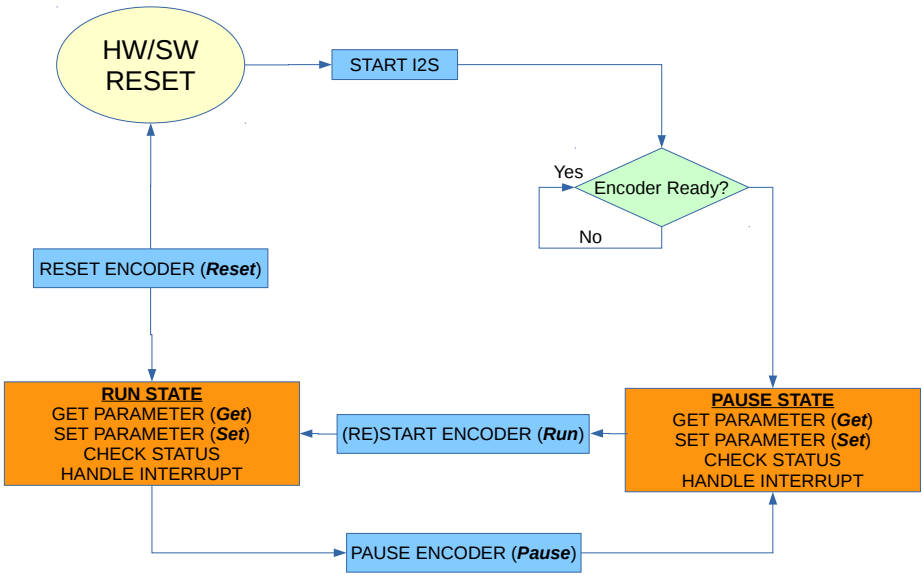

Figure 6: Operation flowchart for each selected processor

8 Implementation Results

Resource	Used	Available	Usage ratio
ALMs	17,256	56,484	31%
FFs	19,059	225,920	8%
BLOCK RAM bits	4,582,528	7,692	65%
BLOCK RAM blocks	570	686	83%
DSPs	16	156	10%

Table 20: Implementation Resources for the 5CGXFC7D6F27I7NSC device

9 Operation Frequencies and Clock Domains

9.1 Operation Frequencies

Signal	Value	Comment
f_{sys_clk}	$80 - 120MHz$	Estimated before fitting.
f_{i2s_lrclk}	$f_{sample} = 48$ kHz	Supports this sample rate only.
f_{i2s_bclk}	$64 \times f_{sample} = 3.072MHz$	Must support 48 kHz sample rate frequency.
f_{spi_sclk}	$40MHz$	Verified.
f_{out_clk}	$40 - 80MHz$	Need not be synchronous to $i2s\_lrclk$.

Table 21: Operation frequencies

9.2 Clock Domains

All clock signals expected to be clean, glitch-free signals.

Domain	Clock signal	Comment
System clock	sys_clk	CPUs and CPU side of peripherals.
I2S clock	$i2s\_bclk$	Audio Input I2S clock domain. Crosses to system clock domain by means of asynchronous FIFO inside Audio Input I2S module.
SPI clock	spi_sclk	SPI front-end clock domain. Crosses to system clock domain by means of synchronizer inside SPI module.
OUT clock	out_clk	Audio Output clock domain. Crosses from system clock domain by means of asynchronous FIFO inside Audio Output Parallel Interface module.

Table 22: Clock domains

10 Internal Sample Rate Conversion

FSin (kHz)	FSout (kHz)	BR (kbps)	FL (samples)	FD (ms)
48	16	32	576	36
48	24	64	576	24
48	48	128	1152	24
48	48	192	1152	24

Table 23: Input sample rate (FSin), output sample rate (FSout), bit rate (BR), frame length (FL) and frame duration (FD)

11 Supported Rates for each MPEG Version in Layer III

Version	Bit rates (kbps)	Sample rates (kHz)	Samples per frame
1	32, 64, 128, 192	48	1152
2	32, 64, 128	16(*), 24(*)	576, 1152
2.5	32, 64, 128, 192	NA	576, 1152

Table 24: Supported rates for each MPEG version in layer III

(*) After internal conversion from 48KHz input sample rate.