Overview

The MPEG1/2 Layer I/II Audio Decoder (IOB-MP2-D) is an audio engine IP core powered by the IObundle proprietary IOB-RV32-X processor, which supports the standard RISC-V instruction set architecture. This IP core is capable of real-time decoding of 1 Elementary Stream of MPEG1/2 Layer I/II encoded audio data.

The compressed audio stream can be input using either an I2S or parallel interface. The parallel interface data is organized in a burst/stuffing format, where useful data is transmitted during the burst period and don't care data is transmitted during the stuffing period. This way, the data interfaces can use fast clocks whose frequency is unrelated to the sample rate. Additionally, the parallel output requires an audio sample clock for synchronization. The system, input, output and word clocks may all be asynchronous for maximum flexibility but synchronous operation is also supported.

The IP core uses a UART for outputting messages useful during the IP integration phase. The UART can also be used to receive configuration and control data from a host. Configuration and control can also be exerted via a dedicated AXI Lite interface.

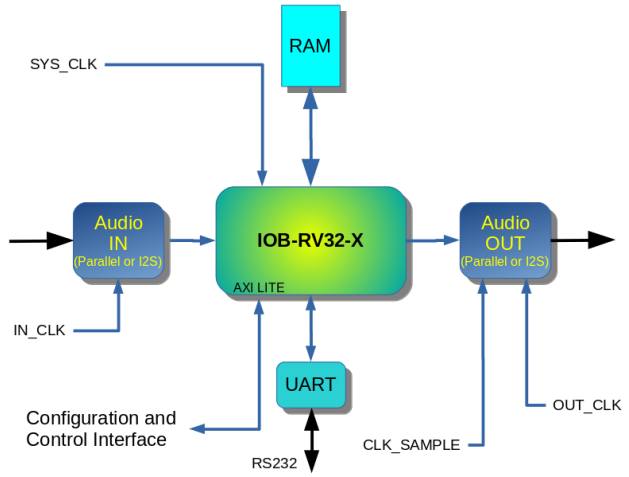
Features

- Compliant with the ISO/IEC 11172-3 and the ISO/IEC 13818-3 standards
- Real time decoding of 1 stereo audio stream at 100 MHz.
- I2S and par audio interface
- I2S and par audio with PCM-like compressed data
- Sample rates: 16 to 48KHz
- Bitrates: 32 to 448/384kbps (Layer I/II)
- 16-bit output audio resolution
- Required memory size: 128kByte
- Configuration, Control and Status register file with APB slave interface
- Channel modes: Mono, joint stereo and stereo
- Latency: 384 (Layer I) or 1152 (Layer II) audio sample periods
- AXI Lite interface for control and configuration
- Asynchronous or synchronous system, input, output and sample clocks

Benefits

- Compact hardware implementation
- Can fit many instances in low cost FPGAs
- Can fit many instances in small ASICs
- Low power consumption

Block Diagram



FPGA Resources

FPGA	LUT-6	BRAM-18 kb	BRAM-36 kb	DSPs
KU040	3539	2	32	3

Table 1: Xilinx Kintex Ultrascale

Deliverables

- FPGA netlist or source code (optional)
- Example testbench
- Implementation constraints for map, place and route
- Demo on commercial board with Ethernet realtime MPEG 1 Layer II decoding
- Datasheet and user documentation for system integration

Contact information

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Disclaimer: IObundle reserves the right to modify the current technical specifications without notice.