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A trigger–time–event system for the W7-X experiment

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Abstract

All control and data acquisition systems of the WENDELSTEIN 7-X (W7-X) fusion experiment need to be perfectly synchronised with an accuracy of $\leqslant 10$ ns. Another essential requirement is to process and record events and trigger signals in such a way that they can be used for real-time control. This paper describes the architecture of a trigger–time–event (TTE) system for the W7-X experiment and gives an overview of the characteristics of the special board of the local TTE units. The main components of the board are a local oscillator synchronised by a central timing unit, and a field programmable gate array (FPGA). The FPGA comprises an event and trigger command receiver/decoder, a local 64-bit time counter, time capture registers, delay devices, a programmable state machine, trigger generators, and a programmable switch matrix, which allows output and input signals of the devices to be interconnected. The time, fast trigger, and event information are distributed from the central timing unit to the local TTE boards via a tree-type optical network. For hardware trigger signals an electrical network may be used. The board has configurable I/O ports for trigger signals and a 64-bit time port.

Keywords: Timing system; Trigger–time–event system; Special PCI-card; Fusion; Experiment control

1. Introduction

The WENDELSTEIN 7-X (W7-X) stellarator experiment is a large experimental device, now being constructed in Greifswald at Max-Planck-Institut für Plasmaphysik. W7-X is integrated in the European Fusion Programme and is aimed at exploring and demonstrating the potential of the stellarator principle for a nuclear fusion power reactor. Unlike most fusion devices, W7-X can operate in steady state. This means that the experiment can produce discharges with a duration of up to 30 min. The experiment has the following main parameters [1]:

- major radius of the vacuum chamber 5.5 m,
- coil system with 50 non-planar and 20 planar super-conducting coils,
- maximum magnet field on axis 3 Tesla,
- installation of 10 MW ECR, 4 MW ICR and 5 MW NBI heating.

The W7-X control system consists of a master control unit and local controllers for all subsys-

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tems such as diagnostics, data acquisition, magnetic system, heating units, and cryogenic units. All periods of operation will be subdivided into segments of variable duration. A segment programme defines the operational rules and parameters of each unit in use. Well in advance the information for each segment is stored in a database. Before the start of an experiment cycle all defined segments for this cycle are sorted in a segment sequence. After each unit has loaded its specific information and generated the necessary control objects, the master control system can start the cycle. Segment processing and fast feedback control will run under the VxWorks real-time operation system. Programmable logic controllers (PLCs) will be used mainly to control the technical components and diagnostic systems. Some parts of the device have to be monitored continuously in order to control the segment processing. All data acquired from the diagnostic and control systems are matched by precise time stamps and will be stored in a centralised data archive. A distribution system for trigger, timing and synchronisation information, event messages, and accurate timing is therefore a key component of the control system.

2. Structure of the trigger–time–event system

The trigger–time–event (TTE) system is an independent system, which closely interacts with the control systems of the experiment. It consists of one central and many local TTE systems. The requirements for the response time and precision of time stamps of the local systems are very different. Short response times with data processing in real-time and a time resolution in a range of 10 ns are essential for data acquisition systems, segment processing, and fast feedback control. Most control systems for the technical components and diagnostic systems, based on PLCs, are less demanding. Because the cycle time of a PLC often exceeds 10–50 ms, time resolution and time accuracy can be much lower than for real-time computer systems. The local TTE system, consisting of a computer board and software components for trigger, time, and event message tasks, is integrated into the control systems of the technical components. The time, trigger, and event-related messages are broadcast from the central TTE system to the local units through a unidirectional fibre network. Units not equipped with a local TTE board, such as PLCs or computers with low requirements for the precision of time stamps, can receive the same information through a dedicated Ethernet. Trigger signals with high requirements for the response time or reliability will be distributed with hardware trigger lines. The number of TTE connected units is flexible and not limited. Fig. 1 shows the structure of the TTE system.

The central TTE system operate as follows:

A very stable oscillator produces a 100 MHz reference clock signal, which will be used to clock the central 64-bit time counter. If necessary, the central time counter can be synchronised with the time information from a Global Position System receiver or other time information systems. Redundancy is necessary within the central TTE unit in order to achieve the very high reliability necessary for the central clock of the experiment. For synchronisation of the local components the clock signal and the time information are distributed over the fibre-optic network, the time information additionally over the Ethernet. Event messages such as information about the current status of the experiment (e.g. plasma events, control status, safety status) are received from the central control

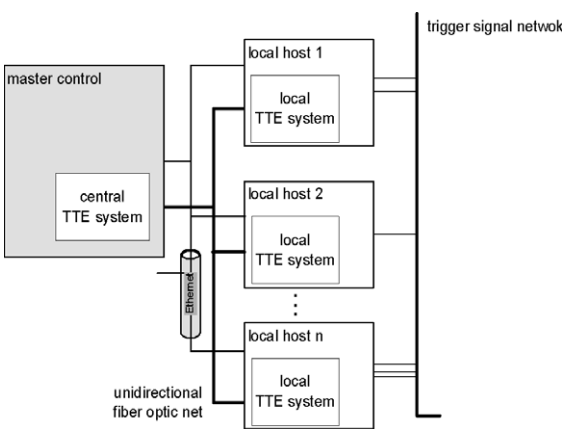

Fig. 1. Structure of the W7-X TTE system.

system and distributed via the fibre-optic network to all local systems. Across the lines of the trigger network the central timer can receive or transmit fast trigger signals.

For real-time computer systems a special card is being developed. These local TTE units have the following properties:

A quartz-stabilised oscillator of the local TTE system drives a 64-bit time counter. By means of the clock signal distributed with the fibre network it can be phase-locked to the oscillator of the central timer. At regular intervals the value of the local counter is compared with that of the central counter transmitted on the fibre network and set to these values if the two differ. The transmission time on the network is compensated by a special technique. Event messages will be received and decoded. The reaction of the card to an event message is defined by the user. The local TTE unit has several ports to transmit signals. Hardware ports can be configured as inputs or outputs of triggers. A 64-bit time port allows transmission of the actual time counter value. The local TTE unit consists of special units for digital signal processing. These units include a timer/counter, time capture registers, pulse generators, a programmable state machine, and I/O triggers. The properties of these signal-processing units and the structure of the signal processing are programmable.

3. Trigger–time–event card overview

The prototype of the TTE card was developed as a PCI bus computer card. Fig. 2 shows the main components of the card. AMCC's S5933 is a powerful flexible PCI controller and serves as a PCI bus target. Bus transactions between the host and the TTE core are executed across the S5933 pass-through interface. All TTE system functions are integrated into a field programmable gate array (FPGA) Xilinx Virtex 1000E. This combination in one chip allows a simple update for other bus interface types in connection with further developments. By implementing the complex function of the device in a FPGA, production time and costs for the integrated circuit are minimised. Design may be carried out very fast, because the Virtex FPGA is re-programmable. The TTE devices are functional units for special time, trigger or event message tasks. They can be configured through registers and can be controlled both with device hardware signals and/or software commands through the PCI interface. All TTE devices types and their functions are summarised in Table 1.

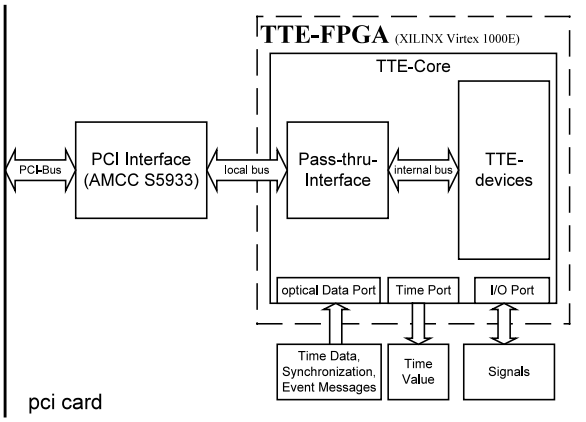

Fig. 2. Functional design of a local TTE (PCI) card.

Fig. 3 depicts a generic TTE device model. Over the bus interface the user chooses the desired device behaviour by setting flags of the device configuration register.

The configuration register values determine, for example, the active input and output signals, the pulse frequency, the trigger mode, and the trigger signal length.

Either device can initiate a bus interrupt when its status is active. The input status of a device is determined by both the hardware input signal and the control flags.

The device transfer function defines the type of TTE device (alarm timer, pulse generator,) and is not changeable. If the conditions for an active output signal are fulfilled, the output signal switches from inactive to active. The status of output signals (device active, output signal active) is determined by the output register status. For tests the user can set both the input and output status with the bus interface. This permits the complex TTE card functions to be evaluated in a simple manner.

4. Trigger–time–event device properties

4.1. Time counter

The time counter device consists of a 64-bit counter. Bit 1 of time counter is clocked with a 100 MHz clock signal (prototype board: Bit 2 with 50 MHz). Bit 0 is reserved for future extensions. The time counter works with three different time modes.

1. *Time Mode 0:* The time counter works with a free-running local oscillator without clock and time value synchronisation from the central TTE unit.

Table 1
TTE device overview

Device type	Number of devices	Function
64 Bit time counter	1	Local timer with 10 ns resolution (prototype: 20 ns)
Alarm timer	1	Generates alarm signals in a absolute or relative alarm time mode
Time capture	4	Latch time value for an event (signal or set a control flag)
Pulse generator	2	Generates pulses with variable rates
Delay timer/counter	4	Delay timer mode: generates a delayed trigger pulse with programmable shape counter mode: count pulses
I/O trigger	8	Input or output pulses with programmable shapes
Programmable logic	4	Resolves a free programmable Boolean function with four input and one output signals
Finite state machine	1	A free programmable state machine with max. 16 states
Event trigger	8	Received event messages can generate max. 8 trigger signals

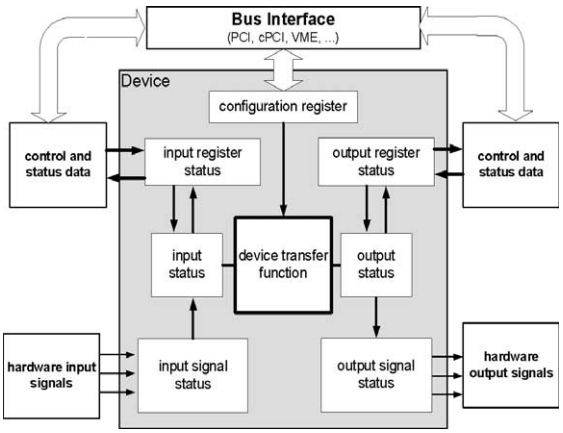

Fig. 3. Generic model of TTE device.

2. *Time Mode 1:* The local oscillator is synchronised with signals from the master oscillator of the central TTE unit.
3. *Time Mode 2:* The local oscillator and the time value are synchronised with signals from the master oscillator and time counter of the central TTE unit. If a time value error occurs, the right value will be set automatically. The error range for the time value is user-defined.

Because of the different path lengths of the optical transmission the time counter values arrive at different times in the TTE units. In order to compensate for this the reference time for comparison with the local counter is delayed after the time of arrival by means of a variable-delay compensation unit so that the total delay is the same for all TTE units and all local clocks run exactly synchronously.

4.2. Alarm timer

The alarm timer device generates a signal at the *Alarm* Q/Q_{neg} output, if the current time value equals the preset alarm time value. The alarm time has to be written in the *Alarm Set Value* register. The alarm timer works with two different time modes.

1. *Alarm Mode 0:* The *Alarm Set Value* is an absolute 64-bit value for the alarm time.
2. *Alarm Mode 1:* The *Alarm Set Value* is a relative 64-bit value for the alarm time. When

the alarm timer is starting, the absolute alarm value is calculated by adding *Alarm Set Value* to the current time counter value.

After starting the alarm timer the user can set a new value for the alarm time for the next alarm cycle without interfering with the current alarm function.

4.3. Time port

The local time value can be written out through this 65-bit port (64-bit time value and 1 bit for control: *Time Port Ready*). The update frequency is variable. The TTE board is closely connected to a time-to-digital converter (TDC) [2]. Over this time port the TDC reads out the current time information from the TTE time counter. A combination of TDC and ADC (analogue-to-digital converter) data is fed into a base system [3].

4.4. Time capture

The use of the time capture devices allows a time stamp to be generated when an event occurs. An event can be a hardware signal or flag set operation. The current time value is written in a 64-bit register named *TCValue*.

4.5. Delay timer/counter

The delay timer/counter supports two modes:

1. *Delay timer mode:* When the delay timer is started, a single trigger signal or a periodic pulse chain will be generated after a delay time depending on the setting of a flag. The 48-bit value *DTCSetValue* defines the delay time.
2. *Counter mode:* Incoming pulses on the input port are counted. The number of pulses is written in the register *DTCCountValue*. The value *DTCSetValue* in counter mode is the value for the overflow of a counter. A trigger signal is generated when an overflow occurs.

4.6. Pulse generator

The pulse generator provides a periodic pulse signal. The frequency can be programmed with the value *PGSetValue*. It is possible to synchronise the phase of this generator with a time mark signal from the master time unit by setting a flag *PGPhaseSychCtr*.

4.7. I/O device

The connections between the TTE devices and external electronics can be used by the I/O devices. The flag *I/ODir* sets the signal direction of the device. The user can change between 5 modes of input signal processing. Table 2 describes these modes. When desired, the input signal can be filtered. The filter value is stored in the *I/OFilterValue* register. In mode 2 an I/O device can work with or without re-trigger attributes.

Table 2
I/O device modes

Mode	Description	Means
I/OMode0	Pass through mode	Input signals are put through directly from input to output
I/OMode1	Latch mode	Active input signals set the output signal to active. The status of the output can only be reset by setting flags I/O to Reset or I/OoutStat Reset
I/OMode2	Trigger mode	When an active input signal occurs the output to the signal is set to the active status for a predefined time (register I/Otrigger-SignLength
I/OMode3	Start/stop mode	The first active signal edge set the output to the active state. The next active input signal reset this signal
I/OMode4	Edge detector mode	Every signal edge sets the output signal for a duration of one clock cycle

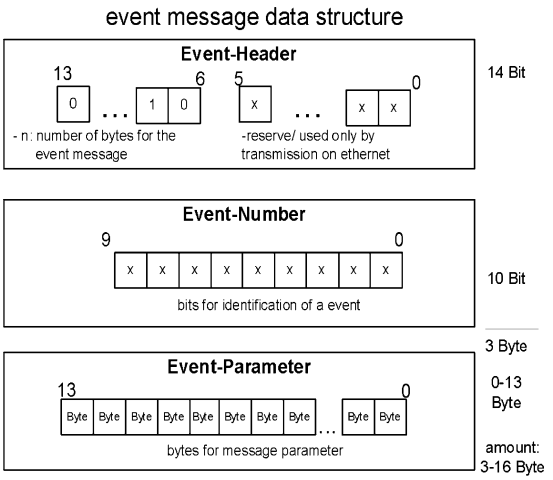

Fig. 4. Event message protocol.

4.8. Event trigger device

Special messages for control tasks, so-called event messages, can be transmitted through (a) the optical network or (b) the Ethernet from the central TTE unit (versions a and b) or every technical component with an Ethernet port (only version b). These messages use the simple protocol shown in Fig. 4. The event is characterised by a predefined event number (0–1023) and can include a maximum amount of 14 parameter bytes. Two stages for event message processing are provided on the TTE board as shown in Fig. 5. The

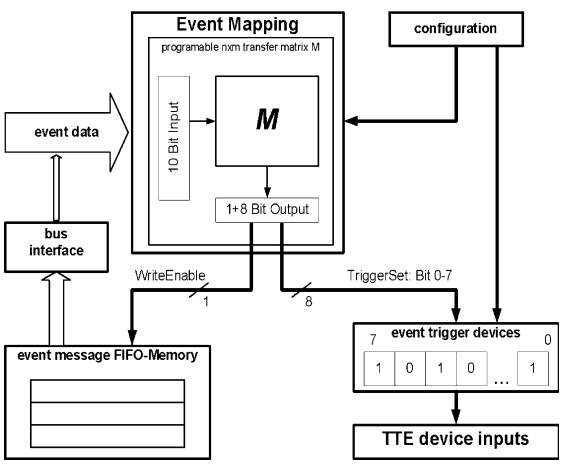

Fig. 5. Event message processing.

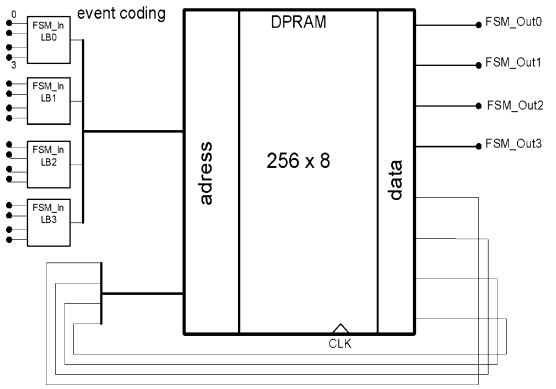

Fig. 6. Structure of FSM device.

user of a TTE card can define the reaction to each of the 1024 event messages. By setting flags in a 1024×9-bit transfer matrix one can allow up to 8 trigger devices and write the message into a FIFO.

Via the bus interface all FIFO entries can be transferred into the host RAM so that very specific reactions depending on the parameters can be programmed in the host. Using the connection matrix (see below) the output of the event trigger devices can be connected with arbitrary TTE device inputs.

4.9. Logic device

The TTE FPGA includes four devices for logical applications. These devices are characterised by four input and one output signals. The free-programmable Boolean transfer function is stored in a memory area of these devices.

4.10. Finite-state machine

In addition to the logical devices the use of the Finite State Machine (FSM) facilitates a very flexible signal connection with time dependencies.

The FSM processes input signals and information about the current state for determining a new state. The FSM works on the principle of a MOORE automate. The on-board FSM allows one to define a state machine with a maximum of 16 states. Fig. 6 depicts the principle of the FSM on the TTE FPGA. The FSM uses a dual-ported RAM area.

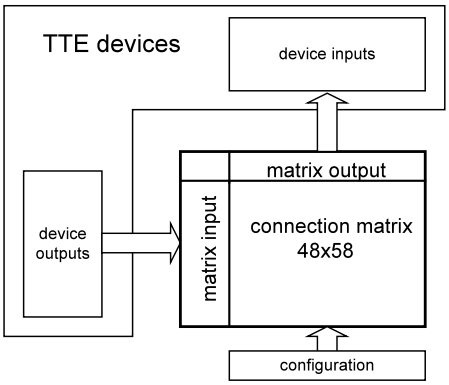

Fig. 7. Connection matrix.

4.11. The connection matrix

Potential users of the TTE card have very different requirements for the signal flow between the devices on the board. A connection matrix permits the output of the TTE devices to be interconnected with the input of another device in a flexible way, making it possible to design complex structures for trigger, time and event-based tasks. The matrix defining the connections between input and output has 48 rows for outputs and 58 columns for inputs (Fig. 7). A device input can be connected to one device output only, but one output can have many connections to inputs.

5. Status

The TTE system for W7-X at the moment is in a state of ongoing development. The program for the FPGA is running faultlessly with a clock frequency of 50 MHz in a simulation and on a prototype board. A standalone version of a PCI board will be available by mid-2001. A basic driver for VxWorks (Wind River Systems Inc.) and an interactive software tool for initialising the very complex unit were developed in co-operation with the University of Applied Sciences at Stralsund, Germany.

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