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The upgrade of KSTAR timing system to support long-pulse operation and high-speed data acquisition

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ABSTRACT

Since the first campaign of KSTAR in 2008, the home-made timing system had run for the synchronized operation of tokamak. The timing board which featured PMC-form factor, giga-bit optical communication, home-made protocol, multi-triggering capability, using GPS time and being integrated to EPICS (Experimental Physics and Industrial Control System), had advantages of compactness, modularity, platform independency and full functionality for the synchronized tokamak operation. However, there was deficiency in timing accuracy resulting from the engagement of software in realization of timing function and timing jitter due to poor isolation in output ports. Moreover, new requirements were on the rise as the plasma pulse length was getting longer and diagnostics operating at the higher frequency were newly installed.

In order to meet new requirements and overcome the problems, the new timing board has been developed. As a result, the performance is remarkably enhanced: timing accuracy less than 5 ns, jitter less than 100 ps, 8 configurable multi-triggering sections, provision of maximum 100 MHz sampling clock. The KSTAR timing system upgraded by introducing the new timing board is participating in the 2011 campaign after calibration and consolidating the established timing system.

This paper describes design, development and commissioning results of the new KSTAR timing system.

1. Introduction

In order to perform properly plasma experiments and obtain precisely engineering and physics data in a tokamak, various and complicated systems which are participating in the experiments should be synchronized in time and operated according to sequences. Also, stamping time on occurred events and acquired data is essential to analyze the experiments. A timing system plays the role to make it. The accuracy required to the timing system can be classified in accordance with objectives as below [1,2]. The accuracy less than ms can be attained only by hardware triggering from a timing system, while the accuracy for synchronizing a global time can be obtained by using NTP (Network Time Protocol).

- Measuring engineering data@max100 Hz ~10 μs
- Measuring scientific data ~order of ns
- Synchronizing global time ~10 ms

The KSTAR timing system is composed of a central timing system, many local timing systems and a dedicated optical timing network between them, and exchanges signals between the central system and the local systems as follows. Additionally, a central timing board is named as CTU (Central Timing Unit) and a local timing board as LTU (Local Timing Unit) [3].

- Current time information referenced on GPS time at every 1 s.
- Shot start pulse according to plasma shot sequence.
- Master clock signal.
- Information for calibration.

In addition to the functions of generating timing signals, we had considered many other aspects in the design of a timing board such as board form-factor to have hardware independency, being fully integrated to EPICS (Experimental Physics and Industrial Control System) which is a middleware of the KSTAR control system, using a GPS time as a reference, and having a multi-triggering function. In the end, the first v.1 timing board had been developed on PMC (PCI Mezzanine Card) form-factor with features of current time referenced on GPS time and 5 pair outputs of trigger and clock, a pair of them having multi-triggering with 3 sections [4].

Although most of timing functions were implemented in a FPGA, software took some roles for the timing generation due to lack of logic cells of the FPGA. This resulted in serious deficiency in timing accuracy and the nominal measured value was 20 μs. Besides, poor isolation between output ports made crosstalk between them

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and it became more severe when clock frequency was high. Not only these drawbacks, but new demands were on the rise as the KSTAR campaigns progressed for carrying out longer plasma experiments and measuring data in diagnostic systems operating at the higher frequency. In order to overcome the problems and meet new requirements, the new timing board has been developed to provide higher timing accuracy, less timing jitter, higher frequency of sampling clock, more multi-triggering sections and more accurate delay compensation.

2. Development of new timing board (V.2)

2.1. Design specifications

The main purposes of the development were to solve the problems rising in the previous operations and to improve the timing performance. First, elimination of the software role and enhancement of the time resolution were conducted by increasing the number of logic cells in a FPGA and the frequency of the master clock. These modifications led to the achievement of timing accuracy and resolution to 5 ns. Then, the overall upgrade of a PCB (Printed Circuit Board) of an output extension module was carried out by separating signal layer and power layer, matching impedance of output patterns, reinforcing isolation between ports, and allotting more ICs to convert level of output signals from LVDS to TTL. These improved the timing jitter greatly.

The next purpose was to support longer pulse experiments and diagnostics operating at higher frequency by adding additional functions and enhancing operability. First, we increased the configurable sections for the multiple triggering and also made every output have this function. In addition, each port became a trigger or a clock by configuration depending on usage, and the maximum frequency of the sampling clock increased up to 100 MHz. For the rest, existing advantages such as compactness, modularity, full integration to EPICS and home-made timing protocol were preserved. The multi-triggering function proves its real merits when the plasma pulse length is getting longer. It facilitates the measurement of data at different frequency during the interesting period of single plasma shot, hence more accurate observation and analysis of experiments can be achieved. Along with this, it is very useful in the view of data management because we can acquire and archive only necessary data.

Table 1
Specification of the new timing board next to the old.

Specification	Old board (v.1)	New board (v.2)
Timing accuracy	–	Max. 5 ns(1tick)
Timing jitter	Typ. 20 μs	<100 ps
Clock frequency	1–5 MHz	1–100 MHz
Master clock	100MHz	200 MHz
Outputs	5 triggers, 5 clocks	8, configurable trigger or clock
Multi-triggering	1 pair of outputs	All outputs
– sections	3	8
Optical comm.	1Gbps	2 Gbps
FPGA	Virtex-4 (20k logic cells)	Spartan-6 (150k logic cells)
IRIG-B T/C	O	O
Form-factor	PMC	PMC
Interface	PCI/PCI-X	PCI/PCI-X
EPICS device driver	Vxworks, Linux 2.4.x/2.6.x	Vxworks, Linux 2.4.x/2.6.x

Table 1 shows the overall specifications of the new timing board next to the v.1 board.

2.2. Development

The KSTAR timing board is divided into CTU and LTU according to its function, and these two boards are identical in hardware only except for a firmware implemented in a FPGA. This feature has an advantage in availability because it can work as CTU or LTU by changing the firmware. Another feature of the timing board is that it was developed in a PMC form-factor, which means the timing board can be installed in any hardware only if it has a PCI interface. Initially, it was highly demanded to develop the timing board as a universal type because the DAQ (Data AcQuisition) systems were implemented in almost every form-factor [4]. Fig. 1 shows a

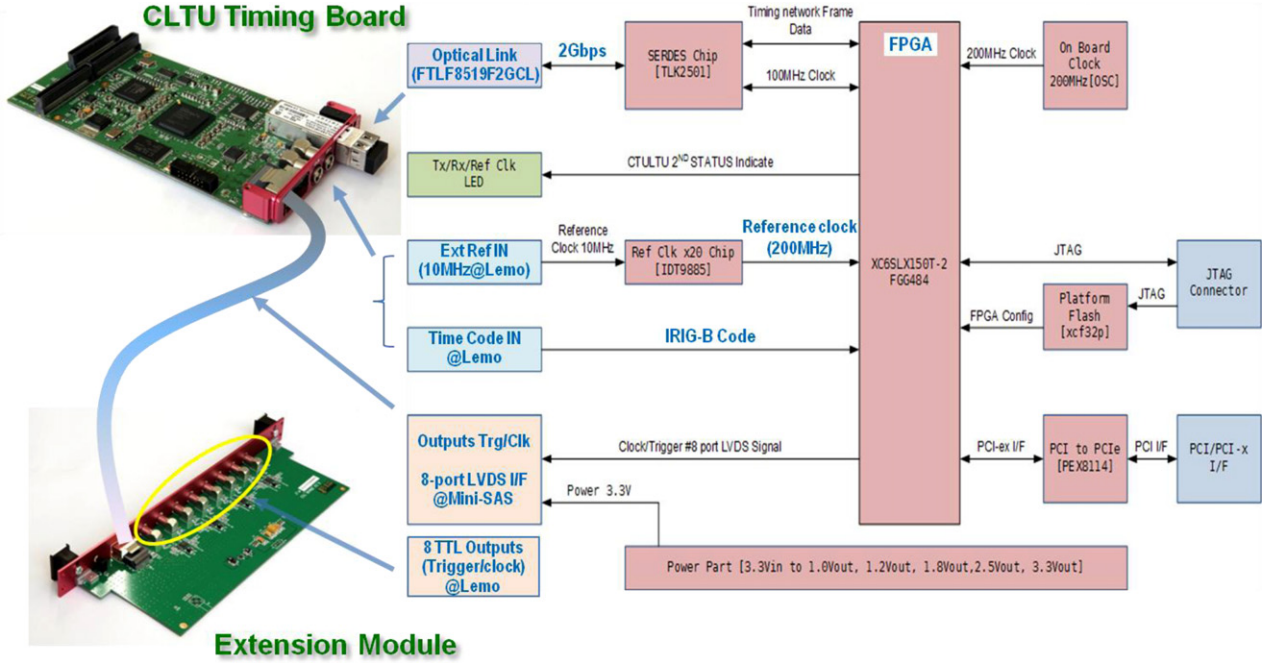

Fig. 1. Photograph of the new timing board and its block diagram (CLTU: Central Local Timing Unit).

composition of the new timing board. We generally call the timing board as CLTU.

The CLTU is composed of a PMC board and an output extension module, and a mini-SAS cable which is connected between them to transfer output signals in 3.3 V LVDS (Low Voltage Differential Signaling). In order to suppress crosstalk between pins of the mini-SAS cable, every pin is isolated with ground connection. The LVDS signals are converted to TTL level in the extension module. The PMC board consists of a FPGA, an optical transceiver, an on-board oscillator, a frequency multiplier, a flash memory and a PCI bridge. In principle, the clock synchronization between CTU and LTUs is achieved by generating LTU clock to be locked in phase with a clock from CTU. However, when the master clock is disconnected, the on-board oscillator is used as a reference for the LTU clock. Also, CTU generates a 200 MHz master clock by multiplying a precise reference signal at 10 MHz from an external source with very high stability. The other difference of CTU from LTU is decoding of the IRIG-B time code from a GPS receiver to make a 53-bit current time data. The message frame formats between CTU and LTU are as follows.

- CTU Tx data packet to LTU:
  SOF (6bytes) – fixed value
  Current Time (4Bytes_Sec)
  Global Shot Start Time (8Bytes_Sec/Tick)
  Global Shot End Time (8Bytes_Sec/Tick)
  Received LTU ID (2Bytes)
  Compensation Time Value (2Bytes)
  CheckSum (2Bytes) – frame check sum field
- LTU Tx data packet to CTU
  SOF (6bytes) – fixed value
  Reserved (20Bytes)
  LTU ID (2Bytes)
  Reserved (2Bytes)
  CheckSum (2Bytes) – frame check sum field

Even though CLTU basically has a PCI/PCI-X interface, it uses PCI express bus with 2.5 Gbps/lane inside the board to interface with the FPGA. Through the 2 Gbps optical link for the dedicated timing network between CTU and all LTUs, the GPS time data, the shot start event and the master clock are transferred in one direction, while calibration data are transmitted in both directions.

The software for CTU and LTU are implemented in different structures as shown in Fig. 2. The central timing system is implemented in a VME bus system; therefore, CTU has EPICS device support and IOC on vxWorks. Otherwise, LTU runs on Linux, KSTAR standard operating system [5].

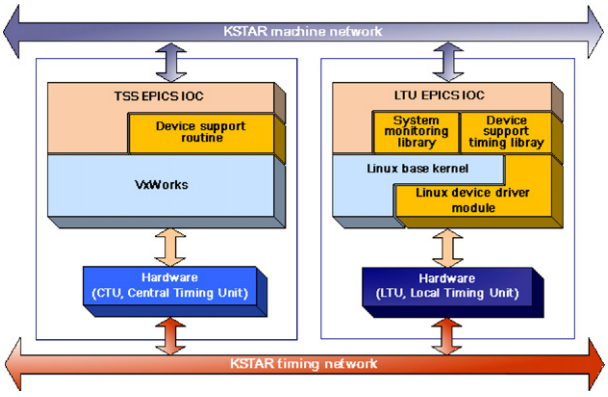

Fig. 2. Software structure.

2.3. IRIG-B time decoding

CTU receives the IRIG-B DCLS (Direct Current Level Shift, Pulse modulated) time code for the GPS receiver and decodes it to 25-bit IRIG-B current time data in second, and then, updates the time data using the master clock until next time code arrives. Also, CTU sends this IRIG-B current time in accompany with the 200 MHz master clock to all LTUs thru the timing network as soon as completion of the decoding. Gradually, the current time in LTU is updated by using the IRIG-B current time, and in the same way of CTU's, it updates the time by using the LTU clock synchronized with the CTU master clock until next time comes from CTU. Total current time to 5 ns [1tick] is represented in 53-bit data.

$$\text{Current time} = \text{25-bit for 1 year in second} + \text{28-bit for sub-second time to 5 ns}$$

2.4. Generation of timing signals

The synchronized operation of KSTAR progresses in accordance with the shot sequence which is pre-configured. In shot preparation stage, LTU first receives the configuration data for timing output through EPICS CA (Channel Access). It is presented in [start time, end time] in second relative to the shot start time and sampling clock frequency. After everything is ready for plasma shot, an operator initiates the shot start event, which is sent in the form of [second, tick] by CTU to all LTUs via the timing network. When the shot start pulse (Global Shot in Fig. 3) arrives, LTU generates trigger or clock signals after the delay of the configured time from the time of the shot start. Fig. 3 shows how to produce an output with maximum 8 multi-triggering sections by summing signals from two control blocks. The generation of timing signals is carried out in the FPGA.

2.5. Performance of the new timing board

The tests were performed to measure the performance of the new timing board itself and confirm the designed functions. For the measurement of jitter, a display persistence mode of a digital oscilloscope with 2GS/s was used. Fig. 4(a) presents a trigger output

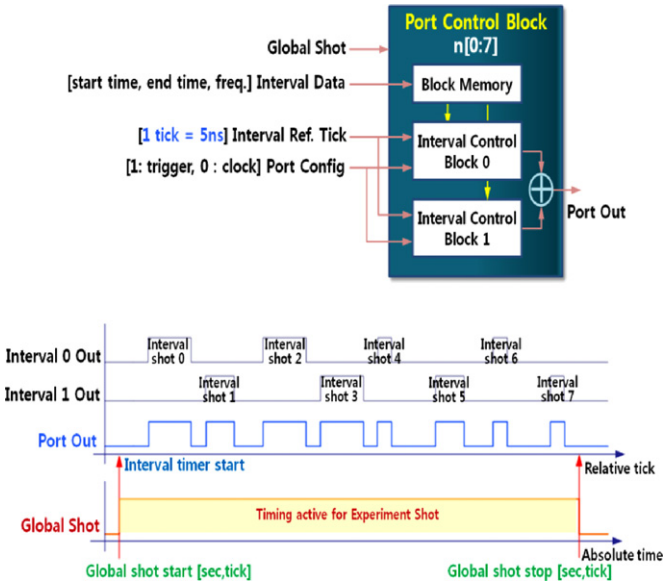

Fig. 3. Trigger output with 8 multi-triggering sections.

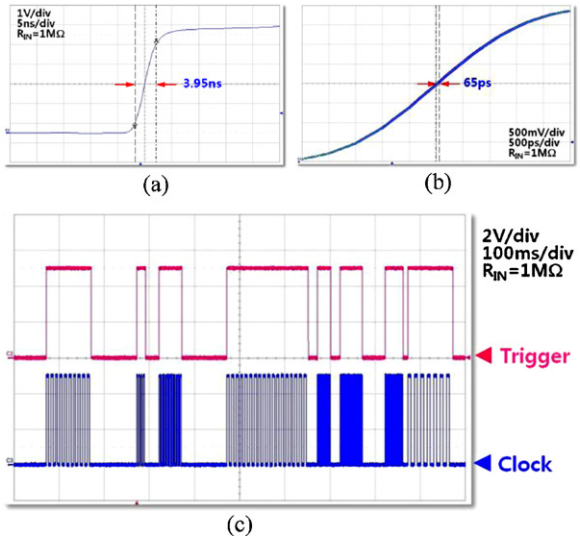

Fig. 4. Performance of the new timing board: (a) rising time, (b) jitter, and (c) multi-triggered output.

in TTL level with a rising time of 3.95 ns that is a typical value of TTL signal. Fig. 4(b) shows the maximum jitter of the trigger output that is 65 ps after accumulation for 13 h. Before this test, we made a simple script to measure jitter continuously by sending a shot start signal repetitively. The last test was carried out to confirm the operation of the timing board. Fig. 4(c) shows a trigger and a clock outputs with 8 configurable sections, especially the clock output has different frequencies in each section. All the parameters were configured via a timing OPI (OPerator Interface) panel which was developed by using Qt, a KSTAR standard open-source tool for the developing GUI (Graphic User Interface). The results presented an excellent performance as well as the satisfaction of the design requirements.

3. Upgrade of the KSTAR timing system

3.1. Consolidation of two timing systems

In the first place, it was intended to compose the upgrade timing system by integrating the existing LTUs(V.1), the new LTUs(V.2) and one CTU(V.2) in order to eliminate the possible out-of-synchronization between two systems. However, we could not make a protocol same to the old one because much more functions than the initial expectation were added into the new board. Finally, we decided to implement two timing systems using the different versions of boards, guaranteeing the one system to be synchronized to the other.

Fig. 5 shows the layout of the upgraded timing system adopting two types of timing boards. In the figure, two CTUs share the GPS signal and the V.2 CTU provides a reference source to the V.1 CTU, consequently the V.1 becomes dependent on the V.2 system in the views of accuracy and synchronization. The configurable optical switches in the central timing system work as multiplexers to dispatch the signals from the CTUs to all LTUs, and 850 nm, multi-mode optical links are connected for the optical timing network.

3.2. Compensation of delay

The target systems that LTUs are installed in are distributed over a wide area around KSTAR, hence the distance between CTU and LTU as well as the distance difference among LTUs are considerably long. Eventually, this degrades the performance of synchronization in the tokamak operation unless compensating it. The delays which

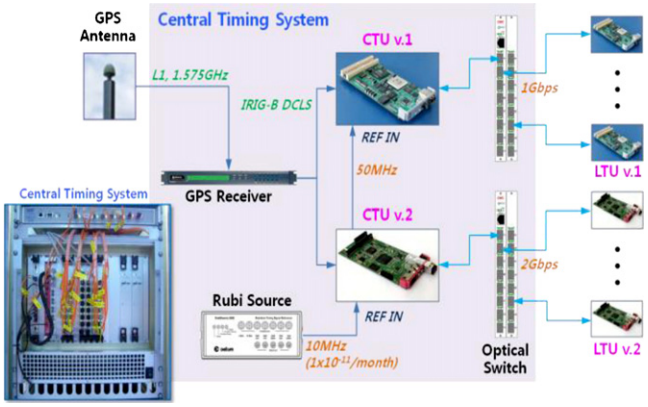

Fig. 5. Integration of the KSTAR timing system.

must be calibrated are the path delay of the optical link including the optical cables and the optical switches, and the process delays inside CTU and LTU. Therefore, the calibration should be carried out in two steps.

In the normal operation, CTU works in Tx only mode by just sending various signals to all LTUs. Otherwise, in the calibration mode, it operates in Tx/Rx mode, that is, the CTU sends to and receives from LTUs. First, the CTU transmits a data packet to LTU, and LTU sends back the received data packet and own ID to CTU as soon as it receives the packet from CTU. Next, CTU calculates the path delay in [tick] by subtracting the time to receive from the time to send and then dividing it by 2. Finally, CTU re-sends the data packet to have the LTU ID and the path delay to let the LTU compensate own delay. This calibration is automatically performed by using the calibration mode in the OPI panel as long as the LTU is installed.

In the second place to compensate the process delays of CTU and LTU, we directly measure output signals from CTU and LTU by using a digital oscilloscope and an optical cable with a known delay, and compensate it by putting the delay value into the LTU in the OPI panel. This calibration is conducted before installing LTU in a test bench. As shown in Fig. 6(b) and (c), the delay of 134 ns was

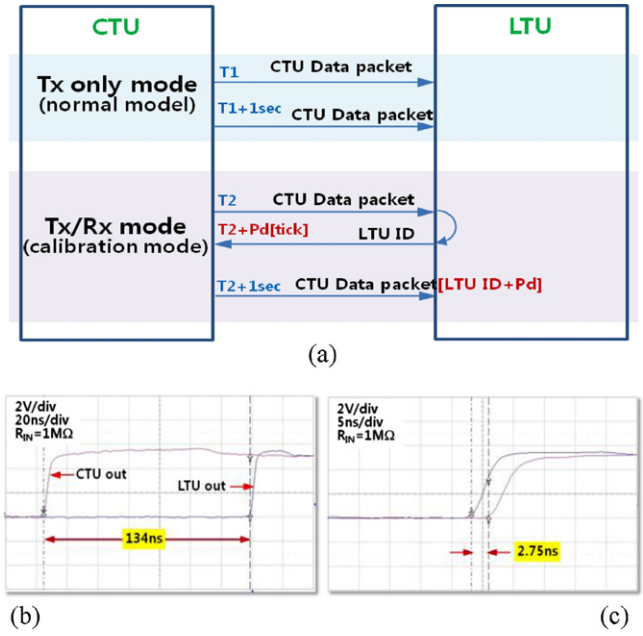

Fig. 6. Compensation of delay between CTU and LTU: (a) calibration sequence, (b) delay before calibration, and (c) after calibration.

decreased to 2.75 ns after calibration. The maximum error range is only restricted to 1 [tick], 5 ns.

3.3. Commissioning

The goal in the early stage was to evaluate the improvement in plasma control and quality of data acquisition by the effects of the enhanced timing performance. However, due to the limitation of experiments time in the 2011 campaign and the influence of the bigger IVC noise than the timing jitter, we could not evaluates the integrated performance in the synchronization, but could confirm the improvements in timing accuracy, operability and availability. Especially, software works for standardization, optimization and user-friendly operation greatly decreased the failure rate in the sequential operation and data acquisition for plasma experiments.

For the next campaign of KSTAR, we will replace all V.1 timing boards with V.2 boards, and introduce a new GPS receiver with a NTP server, which will improve the accuracy of the global time, too.

4. Conclusion

The new timing board for the synchronized operation of KSTAR has been successfully developed to improve the deficiencies appeared in the previous campaigns and satisfy the new requirements to support the longer pulse plasma experiments and data acquisition at the higher frequency. The development has been performed by eliminating the software roles in the generation of timing signals and almost all changing in the extension module to obtain better timing accuracy, jitter, port isolation and higher frequency clock. In addition, many functions have been added for increasing operability and availability, conserving the advantages of the existing timing board such as hardware independency, compactness, modularity, dedicated giga-bit optical communication, home-made protocol, multi-triggering capability, using GPS time and being integrated to EPICS (Experimental Physics and Industrial Control System). Finally, we have innovatively achieved the improvements such as the timing accuracy less than 5 ns, timing jitter less than 100 ps, 8 trigger or clock outputs, maximum 8 configurable multi-triggering.

After replacing all V.1 timing boards with V.2 boards, we will evaluate the improvement in plasma control and quality of data acquisition by the effects of the enhanced timing performance.

Acknowledgment

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