

Processor

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graph LR; Processor[Processor] --> Cache[Cache]; Processor --> WB[Write Buffer]; Cache --> Processor; Memory[Memory] --> Cache; WB --> Memory;
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The diagram illustrates a memory system architecture. On the left is a large box labeled 'Processor'. To its right is a box labeled 'Cache'. Further right is a box labeled 'Memory'. Below the 'Cache' box is a 'Write Buffer', represented as a horizontal row of four small squares. Arrows indicate the flow of data: a bidirectional arrow connects the Processor and the Cache; an arrow points from the Memory to the Cache; an arrow points from the Processor to the Write Buffer; and an arrow points from the Write Buffer to the Memory. The text 'Write Buffer' is written in blue below the four squares.

Cache

Memory

Write Buffer