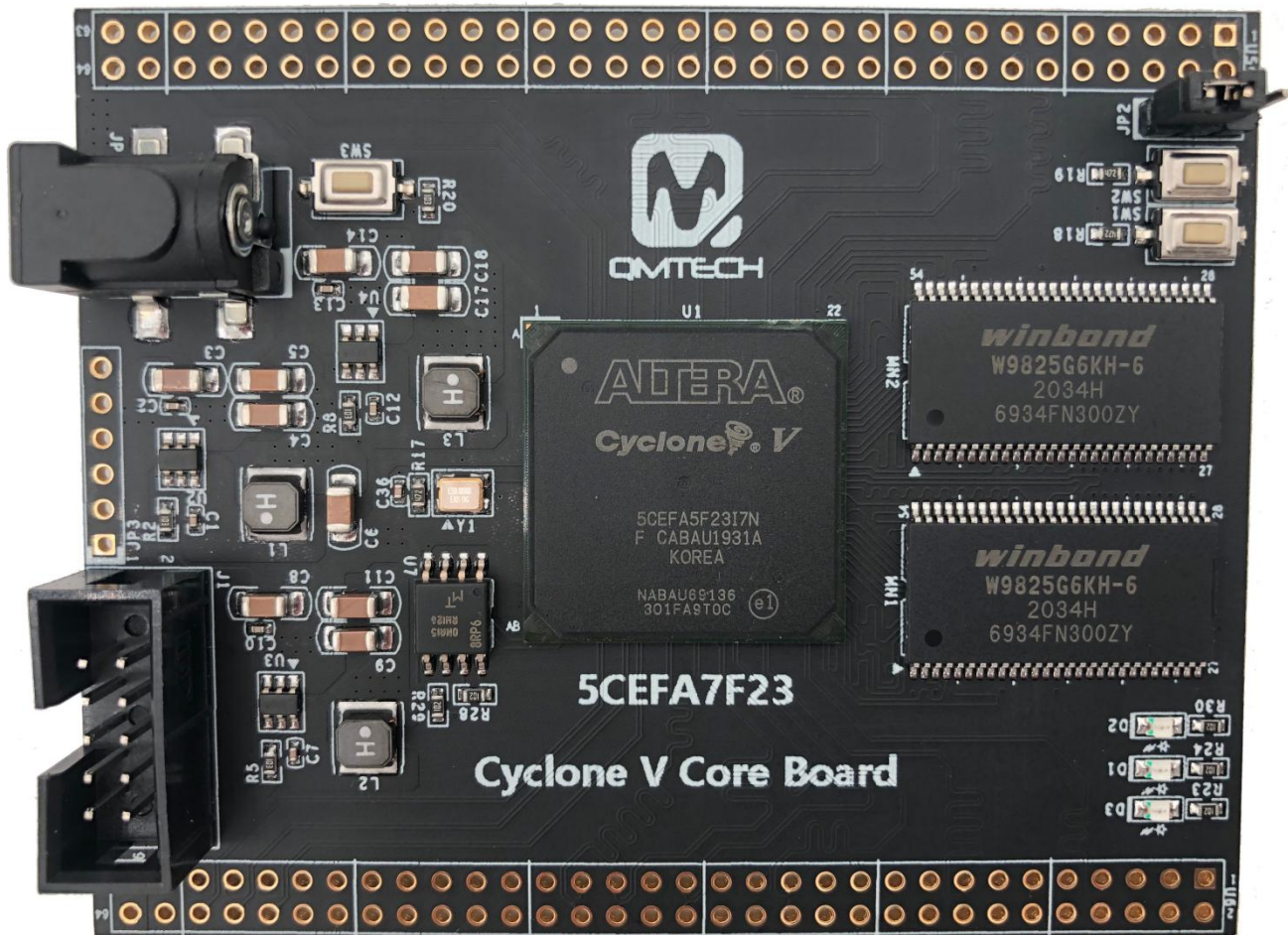# CYCLONEV_5CEFA5 CORE BOARD

## USER MANUAL

## Preface

The QMTech® Cyclone V SDRAM Development Kit uses Intel(Altera) 5CEFA5F23 device to demonstrate the industry's lowest system cost and power, along with performance levels that make the device family ideal for differentiating your high-volume applications. You'll get up to 40% lower total power compared with the previous generation, efficient logic integration capabilities, integrated transceiver variants, and SoC FPGA variants with an ARM®-based hard processor system (HPS).

# Table of Contents

# 1.    Introduction

## 1.1    Document Scope

This demo user manual introduces the QMTECH_CycloneV_5CEFA5 core board and describes how to setup the core board running with application software Altera Quartus II 15.1. Users may employee the on board rich logic resource FPGA 5CEFA5F23I7N and large SDRAM memory W9825G6KH-6 to implement various applications. The core board also has 108 non-multiplexed FPGA IOs for extending customized modules, such as UART module, CMOS/CCD camera module, LCD/HDMI/VGA display module etc.

## 1.2    Kit Overview

Below section lists the parameters of the QMTECH_CycloneV_5CEFA5:
➢   On-Board FPGA: 5CEFA5F23I7N;
➢   On-Board FPGA external crystal frequency: 50MHz;
➢   5CEFA5F23I7N has rich block RAM resource up to 4460Kb;
➢   5CEFA5F23I7N has 77K Logic elements;
➢   On-Board Micron MT25QL128A SPI Flash, 16M bytes for user configuration code;
➢   On-Board 32MB x 2, Winbond SDRAM, W9825G6KH-6;
➢   On-Board power supply for FPGA by using TPS563201 wide input range DC/DC;
➢   QMTECH_CycloneV_5CEFA5 core board has two 64p, 2.54mm pitch headers for extending user IOs. All IOs are precisely designed with length matching;
➢   QMTECH_CycloneV_5CEFA5 core board has 3 user switches;
➢   QMTECH_CycloneV_5CEFA5 core board has 2 user LEDs;
➢   QMTECH_CycloneV_5CEFA5 core board has JTAG interface, by using 10p, 2.54mm pitch header;
➢   QMTECH_CycloneV_5CEFA5 core board PCB size is: 6.7cm x 8.4cm;
➢   Default power source for core board is: 1A@5V DC, the DC header type: DC-050, 5.5mmx2.1mm;
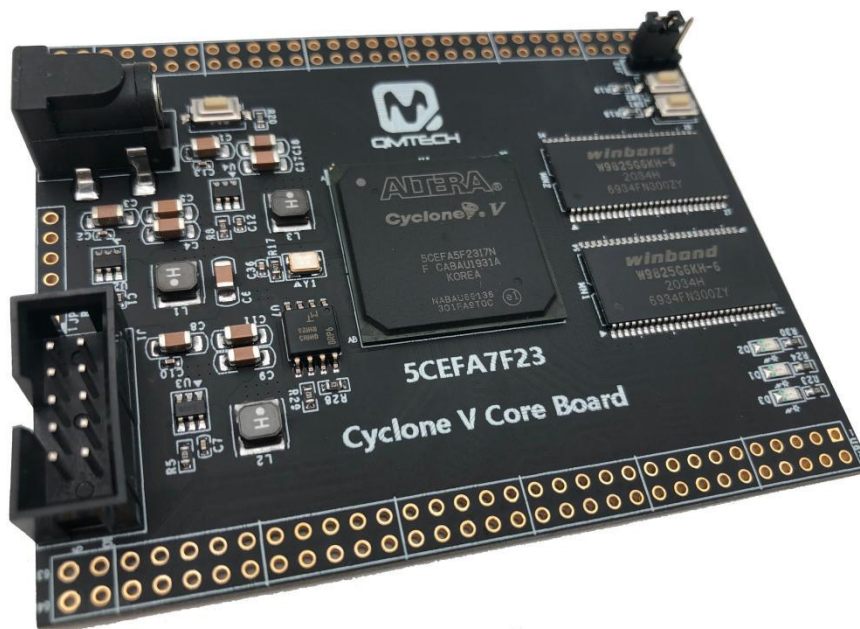
## 1.3    Kit Top View



**Figure 1-1. QMTECH_CycloneV_5CEFA5 Top View**

## 2. Getting Started

Below image shows the dimension of the QMTECH_CycloneV_5CEFA5 core board: 67.1mm x 84.1mm. The unit in below image is millimeter(mm).
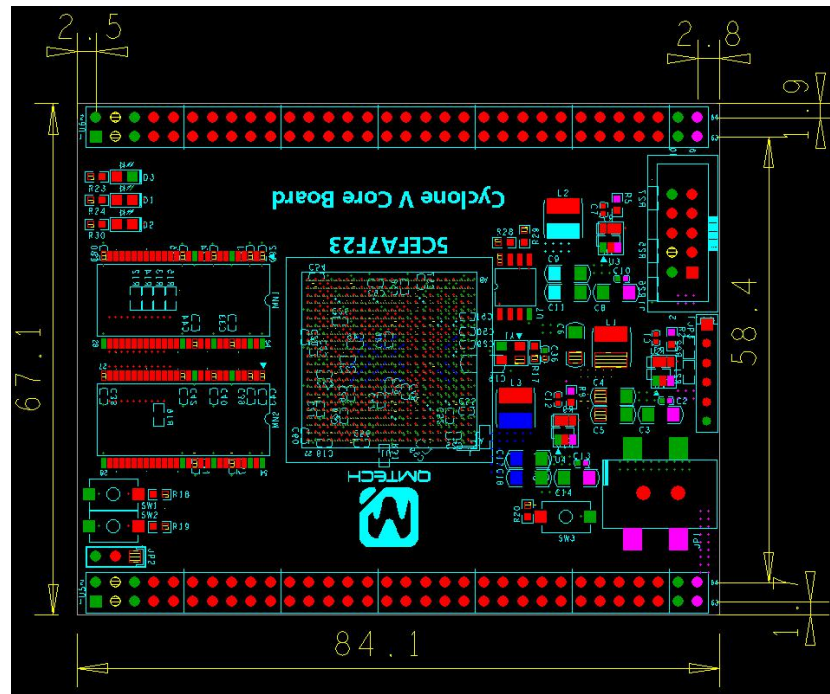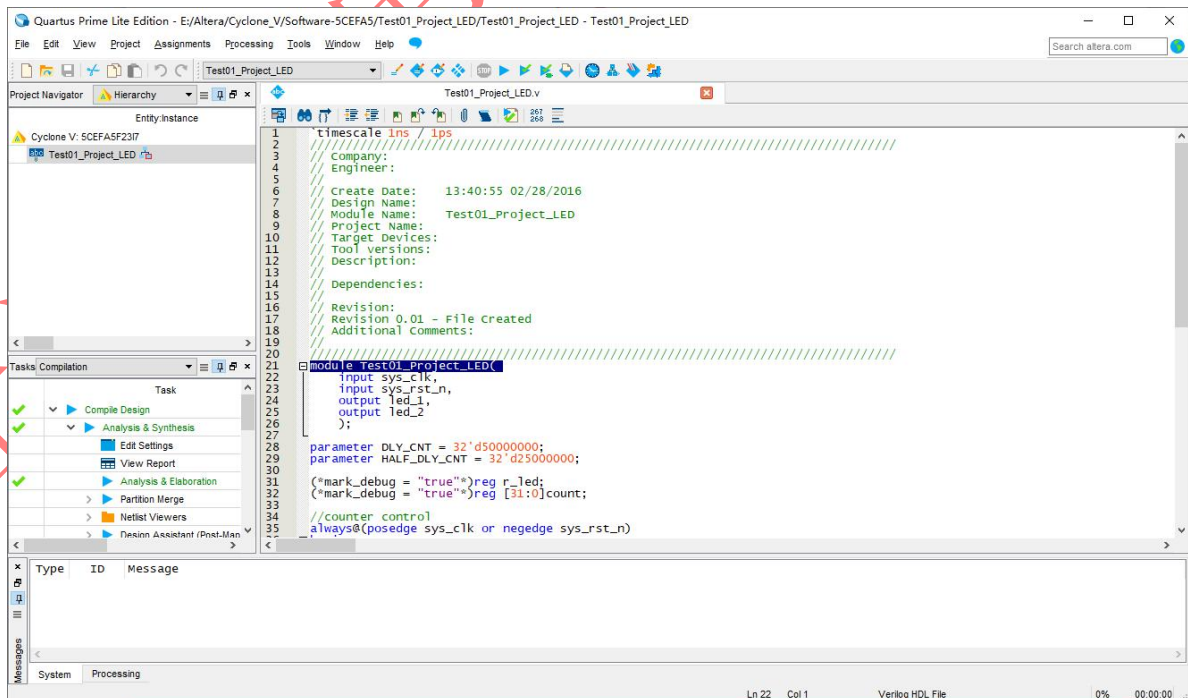


**Figure 2-1. QMTECH_CycloneV_5CEFA5 Dimension**

The QMTECH_CycloneV_5CEFA5 core board tool chain consists of Altera Quartus II 15.1, Altera USB Blaster cable, 5CEFA5F23 core board and 5V DC power supply. Below image shows the Altera Quartus II 15.1 development environment which could be downloaded from Altera(Intel) office website:

## 2.2 QMTECH_CycloneV_5CEFA5 Hardware Design

### 2.2.1 QMTECH_CycloneV_5CEFA5 Power Supply

The core board needs 5V DC input as power supply which could be directly injected from power header or the 64P header U5/U6. Users may refer to the hardware schematic for the detailed design. The on board LED D3 indicates the 3.3V supply, it will be turned on when the 5V power supply is active. In default status, all the FPGA banks IO power level is 3.3V because bank power supply is 3.3V.
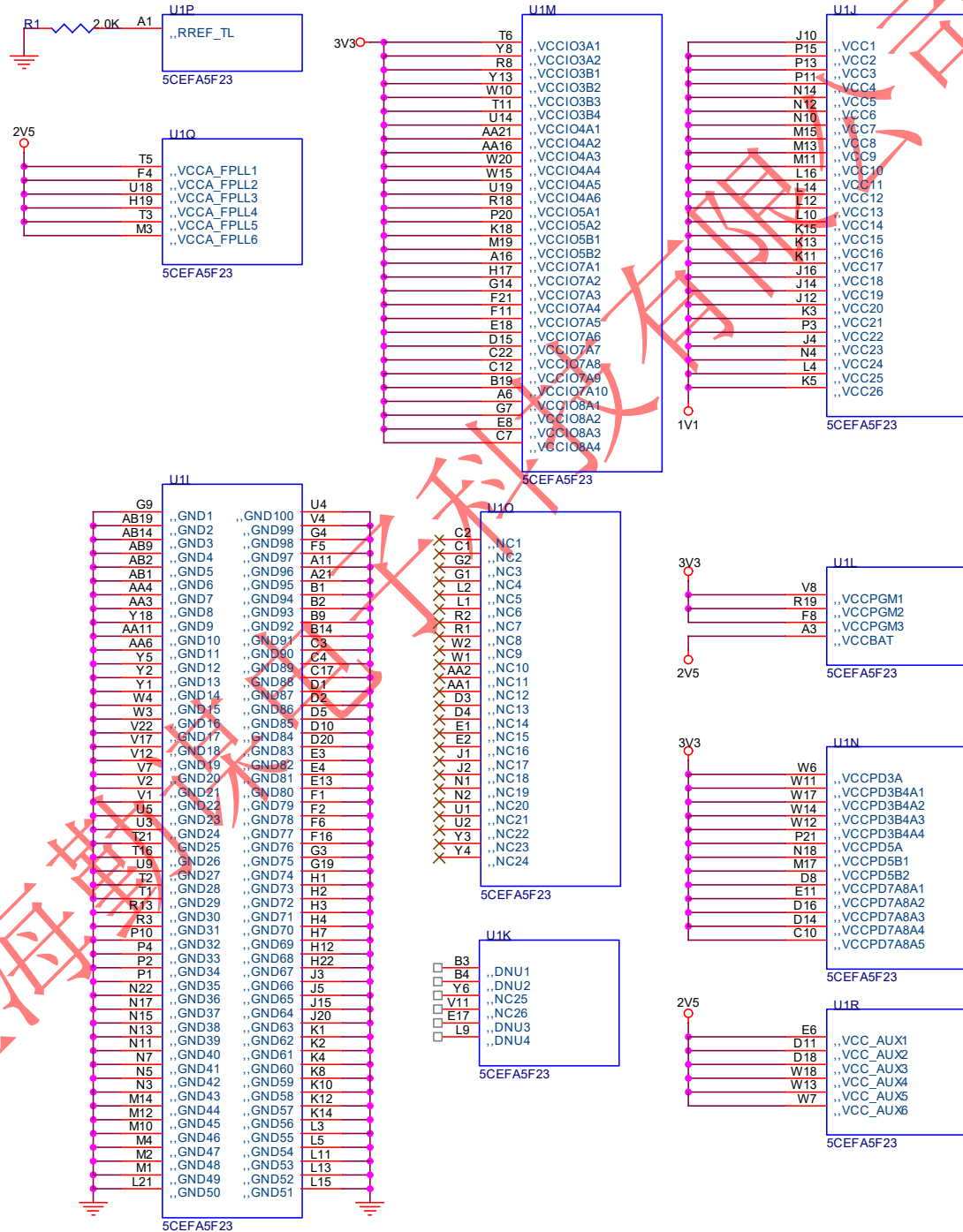


**Figure 2-2. Power Supply for the FPGA**

## 2.2.2 QMTECH_CycloneV_5CEFA5 SDRAM Memory

QMTECH_CycloneV_5CEFA5 has two 32MB SDRAM chips: W9825G6KH-6 SDRAM provided by Winbond. These two SDRAMs are working in a 32bit width mode. Below image shows the detailed hardware design:
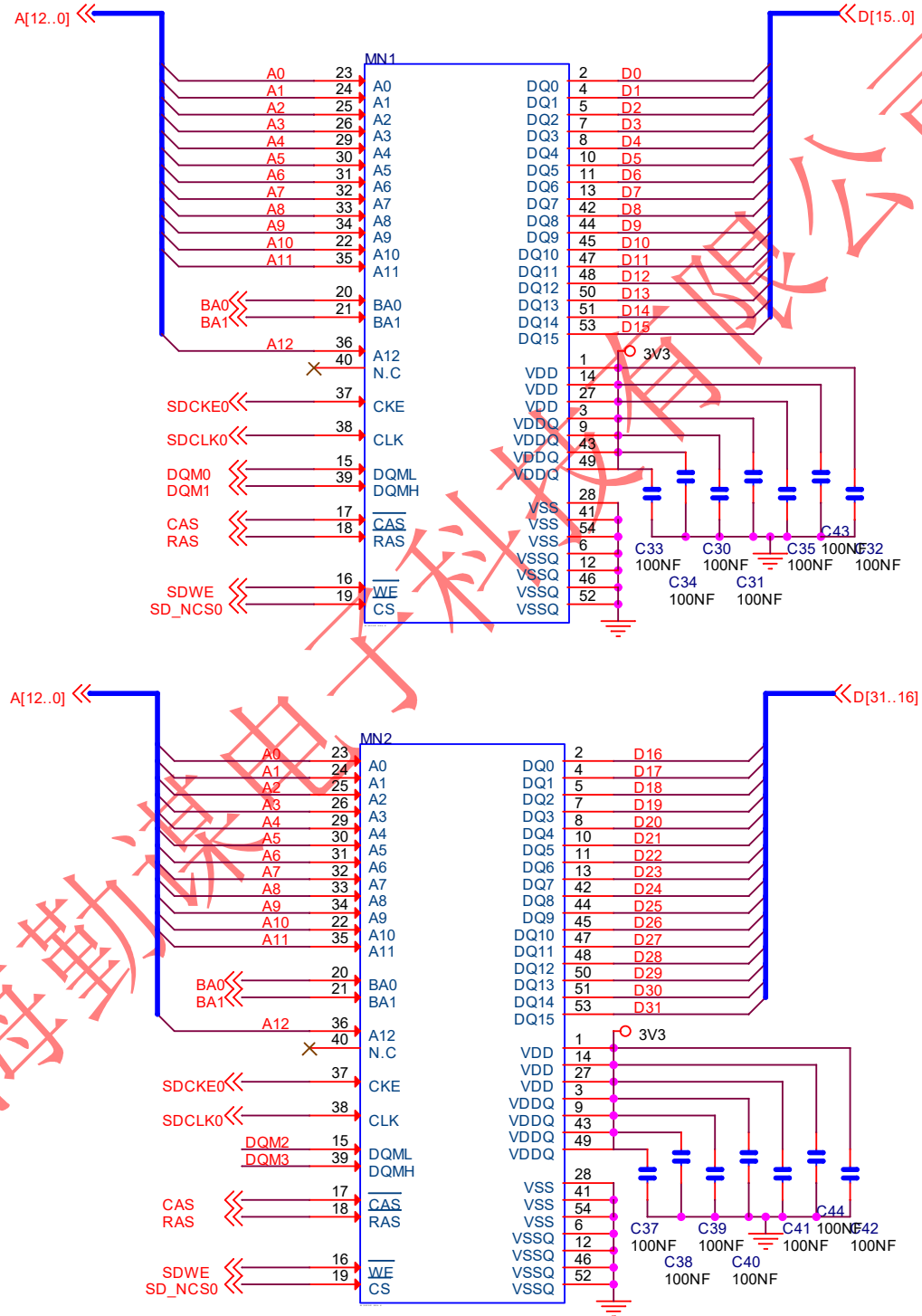


**Figure 2-3. SDRAM**

### 2.2.3 QMTECH_CycloneV_5CEFA5 SPI Boot

QMTECH_CycloneV_5CEFA5 boots from external SPI Flash, detailed hardware design is shown in below figure. The SPI flash is using MT25QL128A manufactured by Micron, with 128Mbit memory storage.
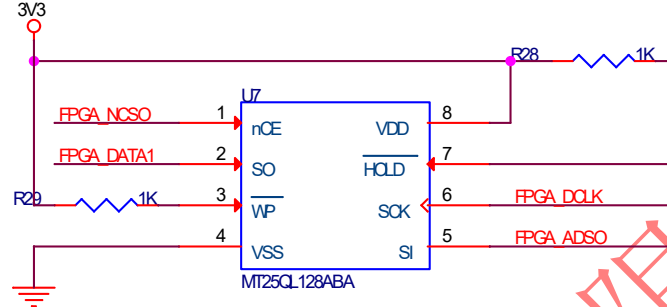
Note: The SPI Flash is designed with x1 mode.



**Figure 2-4. SPI Flash**

Below image shows the hardware configuration of MSEL[4:0]:

(1) 10011 when the jumper is at position PIN1 and PIN2 of Header JP2, in which way will make the FPGA boot from Active Serial (x1 or x4) Standard Mode.

(2) 10001 when the jumper is at position PIN2 and PIN3 pf header JP2, in which way will make the FPGA boot from Passive Serial Mode.
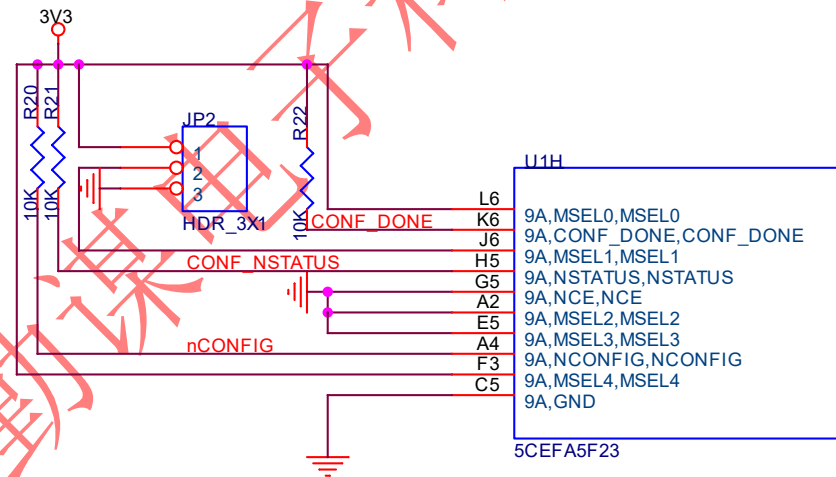


**Figure 2-5. MSEL Settings**

### 2.2.4 QMTECH_CycloneV_5CEFA5 System Clock

The QMTECH_CycloneV_5CEFA5 has system clock frequency 50MHz which is directly provided by external crystal. The crystal is designed with high accuracy and stability with low temperature drift 10ppm/°c. Below image shows the detailed hardware design:
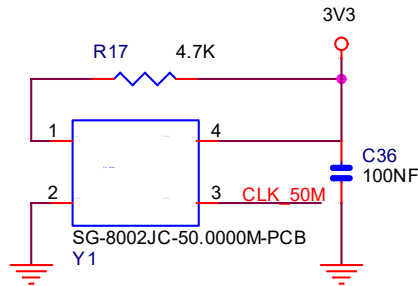
**Figure 2-6. 50MHz System Clock**

### 2.2.1 QMTECH_CycloneV_5CEFA5 JTAG Port

The on board JTAG port uses 10P 2.54mm pitch header which could be easily connected to Altera USB blaster cable. Below image shows the hardware design of the JTAG port:
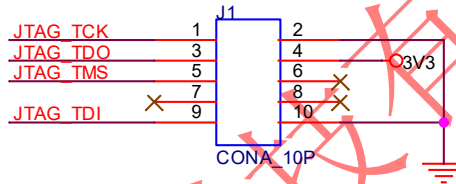


**Figure 2-7. JTAG Port**

### 2.2.2 QMTECH_CycloneV_5CEFA5 Power Supply

The core board's 3.3V power supply is using high efficiency DC/DC chip TPS563201 provided by TI. The TPS563201 supports wide voltage input range from 4.5V to 17V. In normal use case, 5V DC power supply is suggested to be applied on the board. Below image shows the TPS563201 hardware design:
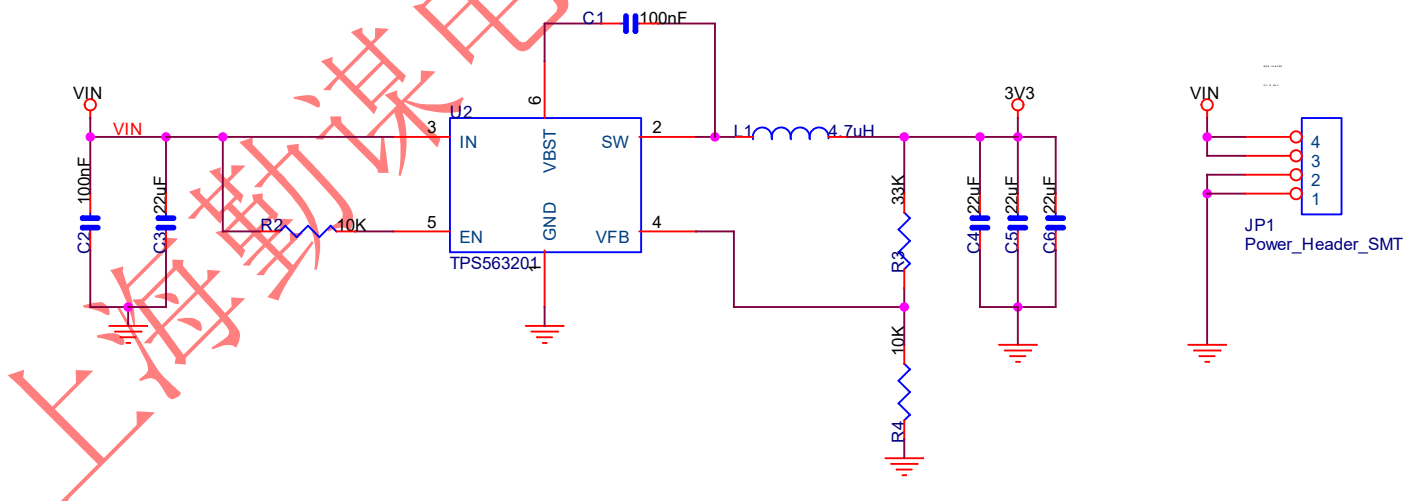


**Figure 2-8. TPS563201 Hardware Design**

The core board's 2.5V and 1.1V FPGA core voltage power supply is also using high efficiency DC/DC chip TPS563201 provided by TI.
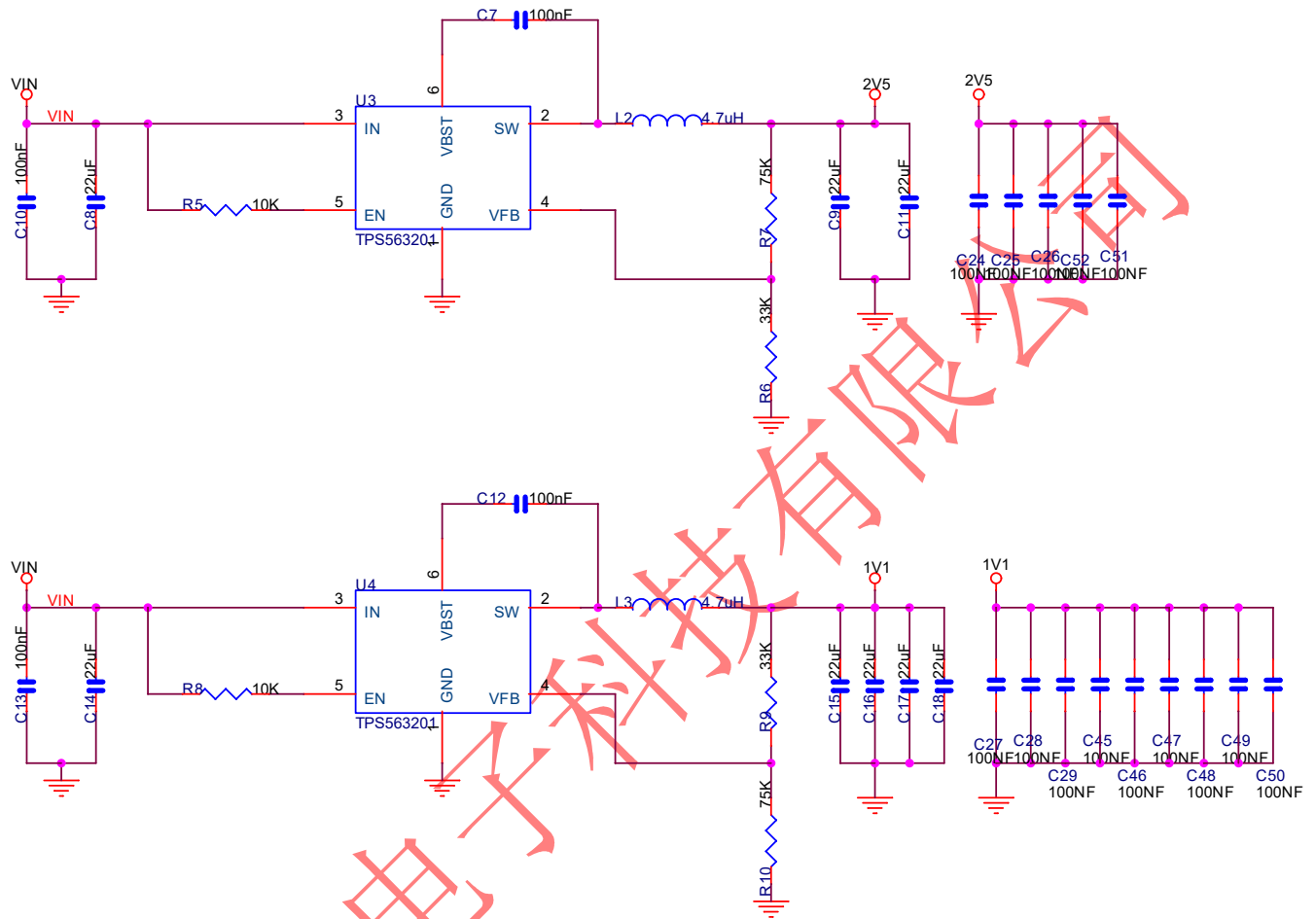


**Figure 2-9. TPS563201 Hardware Design**

### 2.2.3 QMTECH_CycloneV_5CEFA5 Extension IO

The core board has two 64P 2.54mm pitch female headers which are used for extending user modules, such as ADC/DAC module, audio/video module, ethernet module, etc.
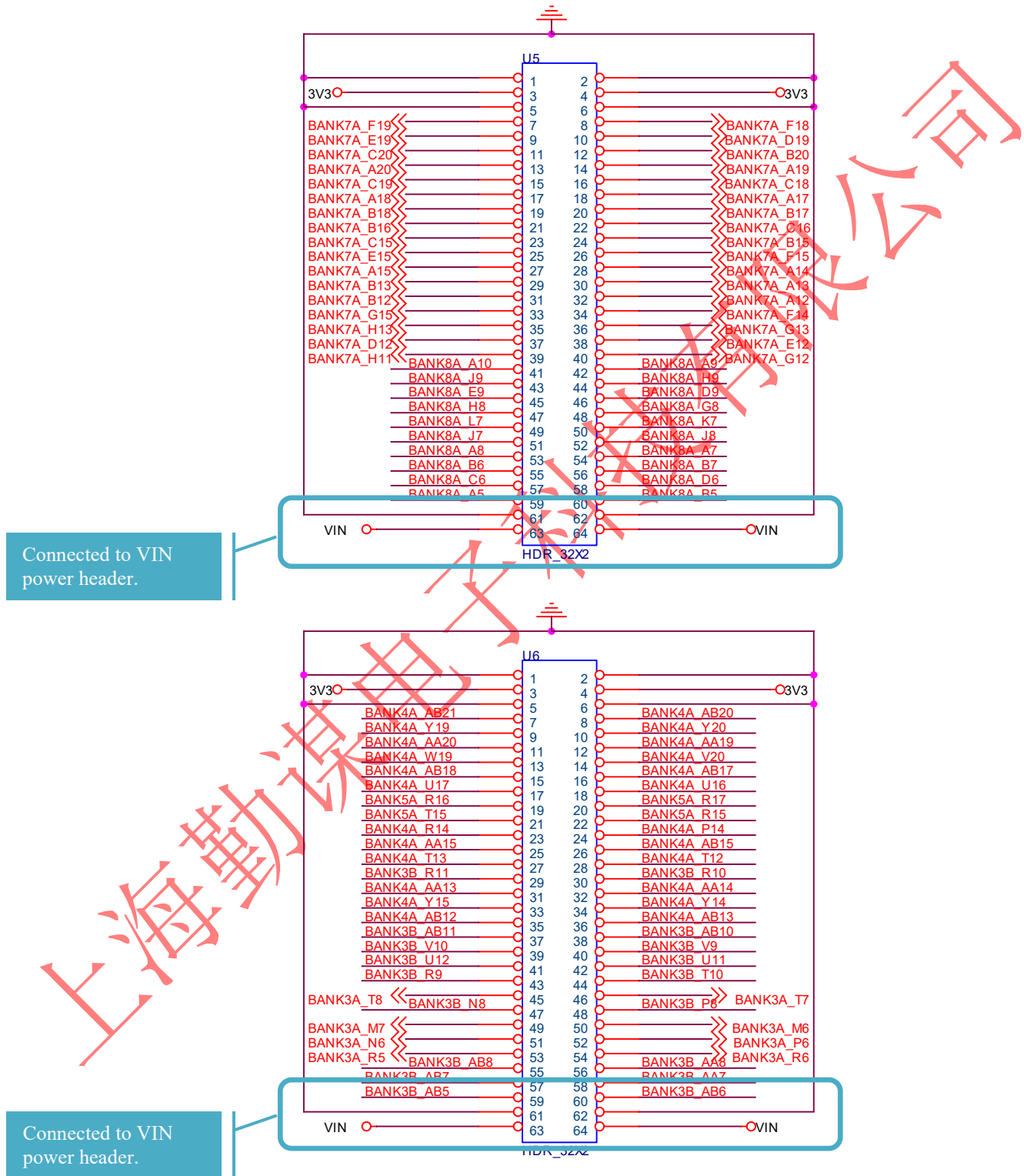


**Figure 2-10.   Extension IO**

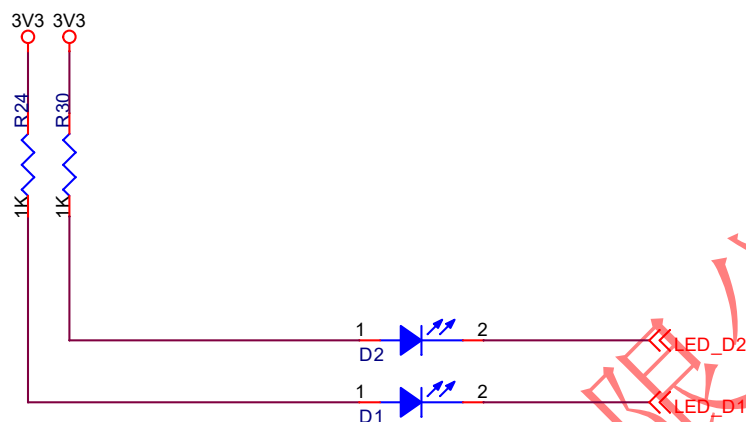### 2.2.4　QMTECH_CycloneV_5CEFA5 User LEDs

Below image shows two user LEDs:



**Figure 2-11.　User LEDs**

### 2.2.5　QMTECH_CycloneV_5CEFA5 User Key

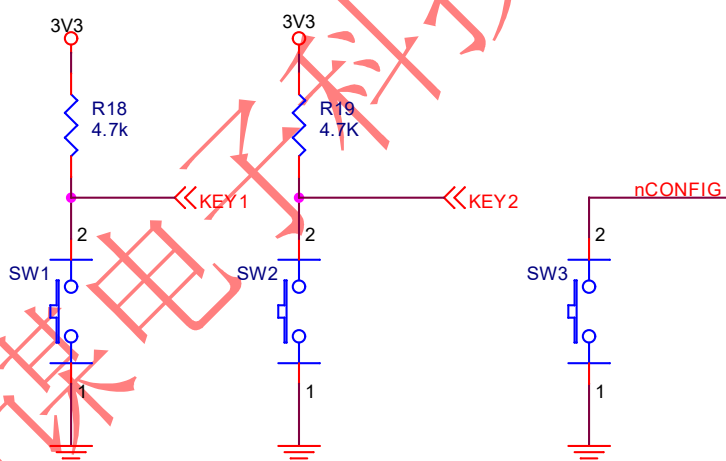Below image shows the nCONFIG key and two user keys:



**Figure 2-12.　User Keys**

# 3.    Reference

[1]  5cefa5-sdram-20200910-V01.pdf
[2]  cv_5v2_Cyclone V Device Handbook.pdf
[3]  an662_Arria V and Cyclone V Design Guidelines.pdf
[4]  cv_51001_Cyclone V Device Overview.pdf
[5]  cv_51002_Cyclone V Device Datasheet.pdf
[6]  pcg-01014_Cyclone® V Device Family Pin Connection Guidelines.pdf

## 4. Revision

| Doc. Rev. | Date | Comments |
|-----------|------|----------|
| 0.1 | 10/09/2020 | Initial Version. |
| 1.0 | 20/11/2020 | V1.0 Formal Release. |
| | | |
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