

# 1. Description

# 1.1. Project

Project Name	F767ZIV1_Bilateral_synchonization
Board Name	NUCLEO-F767ZI
Generated with:	STM32CubeMX 6.1.1
Date	10/10/2021

### 1.2. MCU

MCU Series	STM32F7
MCU Line	STM32F7x7
MCU name	STM32F767ZITx
MCU Package	LQFP144
MCU Pin number	144

# 1.3. Core(s) information

Core(s)	Arm Cortex-M7

# 2. Pinout Configuration

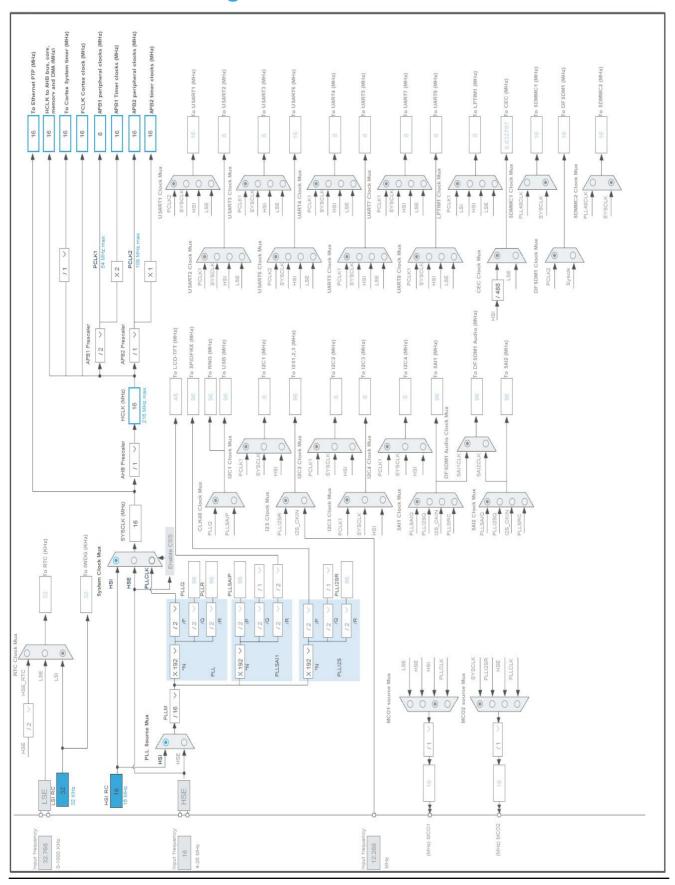


# 3. Pins Configuration

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
6	VBAT	Power		
16	VSS	Power		
17	VDD	Power		
25	NRST	Reset		
26	PC0 *	I/O	GPIO_Output	EBlue
29	PC3 *	I/O	GPIO_Output	ERed
30	VDD	Power		
31	VSSA	Power		
32	VREF+	Power		
33	VDDA	Power		
38	VSS	Power		
39	VDD	Power		
51	VSS	Power		
52	VDD	Power		
61	VSS	Power		
62	VDD	Power		
71	VCAP_1	Power		
72	VDD	Power		
83	VSS	Power		
84	VDD	Power		
94	VSS	Power		
95	VDDUSB	Power		
106	VCAP_2	Power		
107	VSS	Power		
108	VDD	Power		
120	VSS	Power		
121	VDDSDMMC	Power		
130	VSS	Power		
131	VDD	Power		
138	воото	Boot		
143	PDR_ON	Reset		
144	VDD	Power		

<sup>\*</sup> The pin is affected with an I/O function

# 4. Clock Tree Configuration



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# 5. Software Project

### 5.1. Project Settings

Name	Value	
Project Name	F767ZIV1_Bilateral_synchonization	
Project Folder	E:\Mysrc\EmbeddedSystems\RTOS\F767ZIV1_Bilateral_synchonization	
Toolchain / IDE	STM32CubeIDE	
Firmware Package Name and Version	STM32Cube FW_F7 V1.15.0	
Application Structure	Basic	
Generate Under Root	Yes	
Do not generate the main()	No	
Minimum Heap Size	0x200	
Minimum Stack Size	0x400	

## 5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power	No
consumption)	
Enable Full Assert	No

### 5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	MX_GPIO_Init	GPIO
2	SystemClock_Config	RCC

# 6. Power Consumption Calculator report

### 6.1. Microcontroller Selection

Series	STM32F7
Line	STM32F7x7
MCU	STM32F767ZITx
Datasheet	DS11532_Rev4

### 6.2. Parameter Selection

Temperature	25
Vdd	3.3

### 6.3. Battery Selection

Battery	Alkaline(9V)
Capacity	625.0 mAh
Self Discharge	0.3 %/month
Nominal Voltage	9.0 V
Max Cont Current	200.0 mA
Max Pulse Current	0.0 mA
Cells in series	1
Cells in parallel	1

## 6.4. Sequence

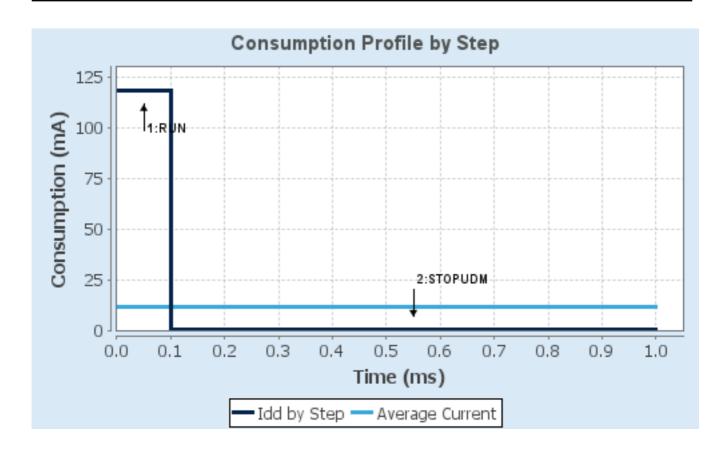
	1		
Step	Step1	Step2	
Mode	RUN	STOP UDM (Under Drive)	
Vdd	3.3	3.3	
Voltage Source	Battery	Battery	
Range	Scale1-High	No Scale	
Fetch Type	ICTM FLASH-SingleBank REGON	n/a	
CPU Frequency	Frequency 216 MHz 0 Hz		
Clock Configuration			
Clock Source Frequency 4 MHz		0 Hz	
Peripherals			
Additional Cons.	0 mA	0 mA	
Average Current	118 mA	130 μΑ	
Duration	0.1 ms	0.9 ms	
DMIPS	462.0	0.0	
Ta Max	89.42	104.98	
Category	In DS Table	In DS Table	

### 6.5. Results

Sequence Time	1 ms	Average Current	11.92 mA
Battery Life	2 days, 4 hours	Average DMIPS	462.24005
			DMIPS

### 6.6. Chart

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# 7. Peripherals and Middlewares Configuration

### **7.1. CORTEX\_M7**

#### 7.1.1. Parameter Settings:

#### **Cortex Interface Settings:**

Flash Interface AXI Interface
ART ACCLERATOR Disabled
Instruction Prefetch Disabled
CPU ICache Disabled
CPU DCache Disabled

#### **Cortex Memory Protection Unit Control Settings:**

MPU Control Mode MPU NOT USED

#### 7.2. RCC

#### 7.2.1. Parameter Settings:

#### **System Parameters:**

VDD voltage (V) 3.3

Flash Latency(WS) 0 WS (1 CPU cycle)

**RCC Parameters:** 

HSI Calibration Value 16

TIM Prescaler Selection Disabled
HSE Startup Timout Value (ms) 100
LSE Startup Timout Value (ms) 5000

**Power Parameters:** 

Power Over Drive Disabled

Power Regulator Voltage Scale Power Regulator Voltage Scale 3

#### 7.3. SYS

**Timebase Source: TIM1** 

7.4. FREERTOS

Interface: CMSIS\_V1

7.4.1. Config parameters:

API:

FreeRTOS API CMSIS v1

Versions:

FreeRTOS version 10.0.1 CMSIS-RTOS version 1.02

Kernel settings:

USE\_PREEMPTION Enabled

CPU\_CLOCK\_HZ SystemCoreClock

1000 TICK\_RATE\_HZ MAX\_PRIORITIES 7 MINIMAL\_STACK\_SIZE 128 MAX\_TASK\_NAME\_LEN 16 USE\_16\_BIT\_TICKS Disabled IDLE\_SHOULD\_YIELD Enabled Enabled USE\_MUTEXES USE\_RECURSIVE\_MUTEXES Disabled USE\_COUNTING\_SEMAPHORES Disabled QUEUE\_REGISTRY\_SIZE 8 USE\_APPLICATION\_TASK\_TAG Disabled ENABLE\_BACKWARD\_COMPATIBILITY Enabled USE\_PORT\_OPTIMISED\_TASK\_SELECTION Enabled USE\_TICKLESS\_IDLE Disabled Enabled USE\_TASK\_NOTIFICATIONS RECORD\_STACK\_HIGH\_ADDRESS Disabled

Memory management settings:

Memory Allocation Dynamic / Static

TOTAL\_HEAP\_SIZE 15360

Memory Management scheme heap\_4

**Hook function related definitions:** 

USE\_IDLE\_HOOK Disabled

USE\_TICK\_HOOK Disabled

USE\_MALLOC\_FAILED\_HOOK Disabled

USE\_DAEMON\_TASK\_STARTUP\_HOOK Disabled

CHECK\_FOR\_STACK\_OVERFLOW Disabled

Run time and task stats gathering related definitions:

GENERATE\_RUN\_TIME\_STATS Disabled
USE\_TRACE\_FACILITY Disabled
USE\_STATS\_FORMATTING\_FUNCTIONS Disabled

Co-routine related definitions:

USE\_CO\_ROUTINES Disabled MAX\_CO\_ROUTINE\_PRIORITIES 2

Software timer definitions:

USE\_TIMERS Disabled

#### Interrupt nesting behaviour configuration:

LIBRARY\_LOWEST\_INTERRUPT\_PRIORITY 15
LIBRARY\_MAX\_SYSCALL\_INTERRUPT\_PRIORITY 5

#### 7.4.2. Include parameters:

#### Include definitions:

vTaskPrioritySet Enabled uxTaskPriorityGet Enabled Enabled vTaskDelete Disabled vTaskCleanUpResources Enabled vTaskSuspend Disabled vTaskDelayUntil Enabled vTaskDelay Enabled xTaskGetSchedulerState Enabled xTaskResumeFromISR xQueueGetMutexHolder Disabled xSemaphoreGetMutexHolder Disabled Disabled pcTaskGetTaskName uxTaskGetStackHighWaterMark Disabled Disabled xTaskGetCurrentTaskHandle Disabled eTaskGetState xEventGroupSetBitFromISR Disabled Disabled xTimerPendFunctionCall Disabled xTaskAbortDelay xTaskGetHandle Disabled

#### \* User modified value

# 8. System Configuration

# 8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
GPIO	PC0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	EBlue
	PC3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	ERed

## 8.2. DMA configuration

nothing configured in DMA service

## 8.3. NVIC configuration

# 8.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority		
Non maskable interrupt	true	0	0		
Hard fault interrupt	true	0	0		
Memory management fault	true	0	0		
Pre-fetch fault, memory access fault	true	0	0		
Undefined instruction or illegal state	true	0	0		
System service call via SWI instruction	true	0	0		
Debug monitor	true	0	0		
Pendable request for system service	true	15	0		
System tick timer	true	15	0		
TIM1 update interrupt and TIM10 global interrupt	true	0	0		
PVD interrupt through EXTI line 16	unused				
Flash global interrupt	unused				
RCC global interrupt	unused				
FPU global interrupt	unused				

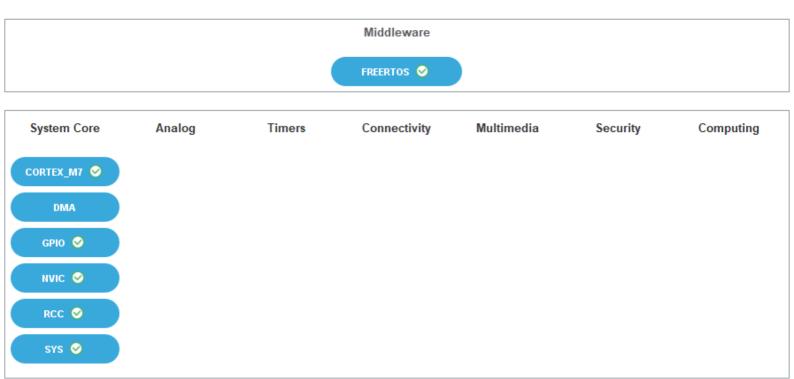
### 8.3.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	false	false
Debug monitor	false	true	false
Pendable request for system service	false	false	false
System tick timer	false	false	true
TIM1 update interrupt and TIM10 global interrupt	false	true	true

#### \* User modified value

# 9. System Views

- 9.1. Category view
- 9.1.1. Current



## 10. Docs & Resources

Type Link

Datasheet http://www.st.com/resource/en/datasheet/DM00273119.pdf

Reference http://www.st.com/resource/en/reference\_manual/DM00224583.pdf

manual

Programming http://www.st.com/resource/en/programming manual/DM00237416.pdf

manual

Errata sheet http://www.st.com/resource/en/errata\_sheet/DM00257543.pdf

Application note http://www.st.com/resource/en/application\_note/CD00167594.pdf

Application note http://www.st.com/resource/en/application\_note/CD00211314.pdf

Application note http://www.st.com/resource/en/application\_note/CD00259245.pdf

Application note http://www.st.com/resource/en/application\_note/CD00264321.pdf

Application note http://www.st.com/resource/en/application\_note/CD00264342.pdf

Application note http://www.st.com/resource/en/application\_note/CD00264379.pdf

Application note http://www.st.com/resource/en/application\_note/DM00042534.pdf

Application note http://www.st.com/resource/en/application\_note/DM00046011.pdf

Application note http://www.st.com/resource/en/application\_note/DM00072315.pdf

Application note http://www.st.com/resource/en/application\_note/DM00073742.pdf

Application note http://www.st.com/resource/en/application\_note/DM00073853.pdf

Application note http://www.st.com/resource/en/application\_note/DM00080497.pdf

Application note http://www.st.com/resource/en/application\_note/DM00081379.pdf

Application note http://www.st.com/resource/en/application\_note/DM00129215.pdf

Application note http://www.st.com/resource/en/application\_note/DM00160482.pdf

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