ALTIOBUF IP Core User Guide

Updated for Intel® Quartus® Prime Design Suite: **19.1**


Online Version


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UG-01024

ID: **683471**

Version: **2020.01.13**

Contents

ALTIOBUF IP Core User Guide

The ALTIOBUF implements either an I/O input buffer (ALTIOBUF_IN), I/O output buffer (ALTIOBUF_OUT), or I/O bidirectional buffer (ALTIOBUF_BIDIR). You can configure the IP core through the IP Catalog and parameter editor in the Intel® Quartus® Prime software.

This user guide assumes that you are familiar with IP cores and how to configure them.

Related Information

- Introduction to Intel FPGA IP Cores
  Provides general information about all Intel FPGA IP cores, including parameterizing, generating, upgrading, and simulating IP cores.
- Creating Version-Independent IP and Qsys Simulation Scripts
  Create simulation scripts that do not require manual updates for software or IP version upgrades.
- Project Management Best Practices
  Guidelines for efficient management and portability of your project and IP files.
- ALTIOBUF IP Core User Guide Archives on page 22
  Provides a list of user guides for previous versions of the ALTIOBUF IP core.

Device Family Support

Table 1. Intel Device Family Support

Device Family	Support Level
Stratix® V	Final
Stratix IV	Final
Arria® V	Final
Arria II	Final
Intel Cyclone® 10 LP	Final
Cyclone V	Final
Cyclone IV	Final

The following terms define device support levels for Intel FPGA IP cores:

- Advance support—the IP core is available for simulation and compilation for this device family. Timing models include initial engineering estimates of delays based on early post-layout information. The timing models are subject to change as silicon testing improves the correlation between the actual silicon and the timing models. You can use this IP core for system architecture and resource utilization studies, simulation, pinout, system latency assessments, basic timing assessments (pipeline budgeting), and I/O transfer strategy (data-path width, burst depth, I/O standards tradeoffs).
- Preliminary support—the IP core is verified with preliminary timing models for this device family. The IP core meets all functional requirements, but might still be undergoing timing analysis for the device family. It can be used in production designs with caution.
- Final support—the IP core is verified with final timing models for this device family. The IP core meets all functional and timing requirements for the device family and can be used in production designs.

ALTIOBUF Features

The ALTIOBUF IP core provides the following features:

- Capable of bus-hold circuitry
- Can enable differential mode
- Can specify open-drain output
- Can specify output enable port (`oe`)
- Can enable dynamic termination control ports for I/O bidirectional buffers
- Can enable series and parallel termination control ports for I/O output buffers and I/O bidirectional buffers
- Can enable dynamic delay chains for I/O buffers

I/O Buffer and Dynamic Delay Integration

Intel recommends that you use the ALTIOBUF IP core to utilize the I/O buffers for any purpose that includes:

- LVDS interfaces—using the ALTLVDS IP core, enabling dynamic delay through Intel Quartus Prime Setting File (`.qsf`) statements
- DDR interfaces—using the ALTDDIO_IN, ALTDDIO_OUT, ALTDDIO_BIDIR, ALTDQ, ALTDQS, and ALTDQ_DQS IP cores
- Dynamic on-chip termination (OCT) control—using the ALTOCT IP core

ALTIOBUF Common Application

The I/O buffers have standard capabilities such as bus-hold circuitry, differential mode, open-drain output, and output enable port.

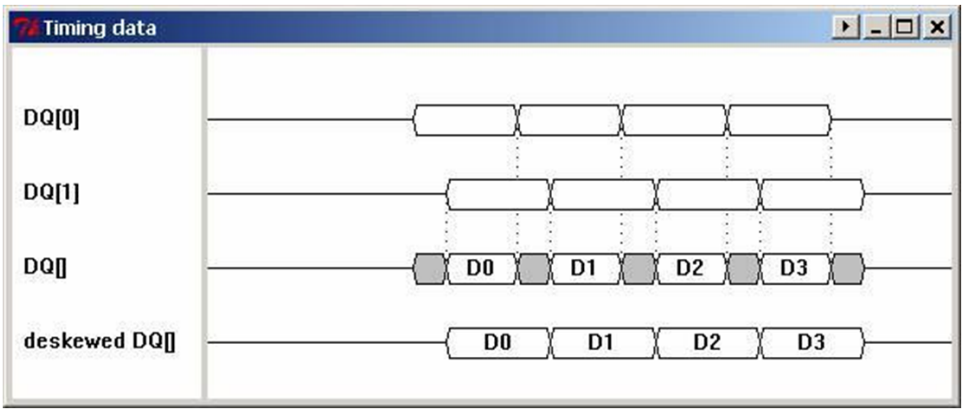
One of the key applications for this IP core is to have more direct termination control of the buffers. By enabling series and parallel termination control ports for the I/O output buffers and I/O bidirectional buffers, you can connect these ports to the ALTOCT IP core to enable dynamic calibration for on-chip termination.

The additional dynamic termination control ports allow control when series termination or parallel termination are enabled for bidirectional buffers. Parallel termination needs to only be enabled when the bidirectional I/O is receiving input. Otherwise, it needs to be disabled so that the output performance and power dissipation is optimal.

Another key application for this IP core is for dynamic delay chain in the I/O buffer. Dynamic I/O delay allows implementing automatic deskew, especially for memory interfaces, such as DDR3, which is handled by the memory interface intellectual property (IP). You need to dynamically deskew and not calculate manually because much of the skew can come from the I/O buffers of either the FPGA or the other device the FPGA is interfacing with (for example, memory). Even if the trace lengths are matched, there can still be electrical skew in the system. Also, this skew changes and can change from device to device. Having the ability to deskew from the fabric allows you to remove uncertainties that would have to be considered in the timing budget. This allows you to gain more timing margin, which allows higher frequencies.

Figure 1. Example Illustrating Deskew

This figure shows an example of deskew.



For example, if the input (or output) bus signals are `DQ[0]` and `DQ[1]`, board trace skew, transmitter device skew, or even FPGA package skew could cause signals that were initially aligned to become misaligned. The third waveform shows the window available to the receiver for capturing the data. If `DQ[0]` was delayed a bit to match `DQ[1]`, a wider window would become available to the receiver.

Note: The deskew delay chains are not meant to find the middle of a data valid window, but just to deskew the incoming (or outgoing) data to widen the overall window for a bus of inputs (or outputs). To do this, you only need to align just one edge (for example, the left edge) of the data valid window of all the pins.

To find the left and right edges of the data valid window, you need to do coarser adjustments (one possible method is to use the new phase adjustment functionality of the PLL (ALTPLL IP core). The range of the deskew delay chains is only designed to compensate for a reasonable amount of board and package/layout skew.

Related Information

ALTOCT IP Core User Guide
Provides information about connecting the ALTIOBUF ports to ALTOCT IP core.

ALTIOBUF Parameters

This table lists the options ALTIOBUF IP core parameters.

Table 2. ALTIOBUF IP Core Parameters: General Tab

Parameter	Description
Currently selected device family:	Specify the device family you want to use.
How do you want to configure this module?	Specify whether it is an input buffer, output buffer, or bidirectional buffer.
What is the number of buffers to be instantiated?	Specify the number of buffers to be used. This defines the size of the buffer.
Use bus hold circuitry	If enabled, the bus-hold circuitry can weakly hold the signal on an I/O pin at its last-driven state. Available in input buffer, output buffer, or bidirectional buffer.
Use differential mode	If enabled, `datain/datain_b` is used for input buffers, both `dataout/dataout_b` are used for output buffers, and both `dataio/dataio_b` are used for bidirectional buffers.
Use open drain output	If enabled, the open drain output enables the device to provide system-level control signals (for example, interrupt and write-enable signals) that can be asserted by multiple devices in your system. This option is only available for output buffers and bidirectional buffers.
Use output enable port(s)	If enabled, there is a port used to control when the output is enabled. This option is only available for output buffers and bidirectional buffers.
Use dynamic termination control(s)	If enabled, this port receives the command to select either `Rs` code (when input value = low) or `Rt` code (when input value = high) from the core. Only enable `Rt` when the bi-directional I/O is receiving input. Otherwise, it needs to be disabled so that the output performance and power dissipation is optimal. This option is available only for input and bidirectional buffers. An error is issued if parallel termination (`Rt`) is on and dynamic termination control is not connected on a bidir pin. An error is issued if parallel termination (`Rt`) is off and dynamic termination control is connected on an input or bidirectional pin. Note that two I/Os in the same dynamic termination control group needs to have the same dynamic termination control signal. If the I/Os have separate dynamic termination control signals, the Intel Quartus Prime software produces a fitting error. A dynamic termination control group is a group of pins that share the same physical dynamic termination control signal on the chip. This option is not available in Cyclone III, Cyclone IV, and Intel Cyclone 10 LP devices.
Use series and parallel termination controls	If enabled, this allows the series and parallel termination control ports to be used. These ports can then be connected to termination logic blocks to receive the Rs or Rt code from the termination logic blocks. This option is only available for output buffers and bidirectional buffers. The series and parallel termination control ports are 14-bit wide for series or parallel termination.

continued...

Parameter	Description
	For Cyclone III, Cyclone IV, Intel Cyclone 10 LP, and Cyclone V devices, this option is available for output buffers and bidirectional buffers, but not for input buffers. Only series termination is available. The series termination control ports are 16-bit wide. The width of these ports increases depending on the amount of buffers instantiated.
Use left shift series termination control	If enabled, you can use the left shift series termination control to get the calibrated OCT R_s with half of the impedance value of the external reference resistors connected to RUP and RDN pins. This option is useful in applications which required both 25-Ω and 50-Ω calibrated OCT R_s at the same V_{ccio}. For more information, refer to I/O features chapter of the respective device handbooks.

Table 3. ALTIOBUF Parameters: Dynamic Delay Chains Tab

Parameter	Description
Enable input buffer dynamic delay chain	If enabled, the input or bidirectional buffer incorporates the user-driven dynamic delay chain in the IP core; that is, the `IO_CONFIG` and the input delay cell. Additional input ports are enabled: `io_config_clk`, `io_config_clkena`, `io_config_update`, and `io_config_datain`. This option is not available for Cyclone III, Cyclone IV, and Intel Cyclone 10 LP devices.
Enable output buffer dynamic delay chain 1	If enabled, the output or bidirectional buffer incorporates the user-driven dynamic delay chain in the IP core; that is, the `IO_CONFIG` and the first output delay cell. Additional input ports are enabled: `io_config_clk`, `io_config_clkena`, `io_config_update`, and `io_config_datain`. This option is not available for Cyclone III, Cyclone IV, and Intel Cyclone 10 LP devices.
Enable output buffer dynamic delay chain 2	If enabled, the output buffer or bidirectional buffer incorporates a user-driven dynamic delay chain in the IP core; that is, the `IO_CONFIG` and the second output delay cell. Additional input ports are enabled: `io_config_clk`, `io_config_clkena`, `io_config_update`, and `io_config_datain`. This option is not available for Cyclone III, Cyclone IV, and Intel Cyclone 10 LP devices.
Create a 'clkena' port	If enabled, there is a port used to control when the configuration clock is enabled. This option is not available for Cyclone III, Cyclone IV, and Intel Cyclone 10 LP devices.

Using the Port and Parameter Definitions

Instead of using the parameter editor GUI, you can instantiate the IP core directly in your Verilog HDL, VHDL, or AHDL code by calling the IP core and setting its parameters as you would any other module, component, or subdesign.

Related Information

ALTIOBUF References on page 13

ALTIOBUF Functional Description

ALTIOBUF Input, Output, and OE Paths

The three path types used with the I/O buffer in the delay chain architecture are input path, output path, and oe path.

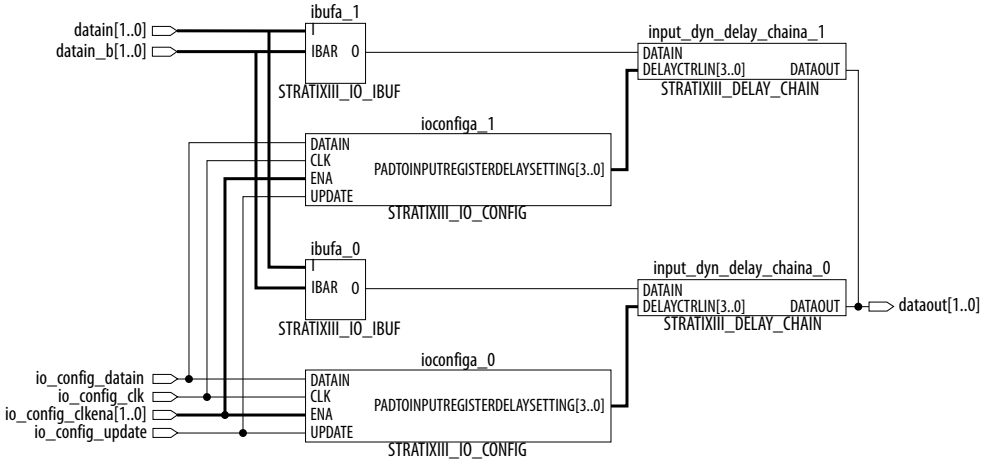
Dynamic delay chains are integrated in the input path for input and bidirectional buffers. Dynamic delay chains are integrated in the output and oe paths for output and bidirectional buffers. This section describes the dynamic delay chain-related components only.

All paths share a similar configuration in which the delay cells are getting their delay control signal from the IO_CONFIG component. For the input path, the IO_CONFIG's PADTOINPUTREGISTERDELAYSETTING output port drives the DELAY_CHAIN's (input delay cell) DELAYCTRLIN input port. For the output and oe path, use the IO_CONFIG's OUTPUTDELAYSETTING 1 and 2 output ports to drive the DELAYCTRLIN port of the first and second output delay cells, respectively.

The number of delay chains needed is NUMBER_OF_CHANNELS. Each instance of the I/O buffer includes a delay chain. Assume NUMBER_OF_CHANNELS is equal to ×. There must be × instances of input delay chain for × input buffer, and 2× instances of the first output delay chain and 2× instances of the second output delay chain output buffer because it uses the output and oe paths. The bidirectional buffer combines all instances of the delay chains mentioned above.

Figure 2. Sample ALTIOBUF (Input Buffer Mode) Architecture when NUMBER_OF_CHANNELS = 2

This figure shows the internal architecture of the ALTIOBUF IP core (input buffer mode) when NUMBER_OF_CHANNELS is equal to 2 and the dynamic delay chain feature is enabled.



ALTIOBUF Input Buffer

The input buffer IP core uses the input path of the dynamic delay chain.

The `datain` and `datain_b` input ports of the ALTIOBUF IP core (input buffer mode) connect to the `i` and `ibar` ports (if differential mode is enabled) of the input buffer, respectively. In the input path, the value of the input buffer's `dataout` port is passed into the input delay chain. The `dataout` port of the ALTIOBUF IP core (input buffer mode) is the output of the `dataout` delay chain.

You must add a register external to the IP core, either a regular DFFE or a DDIO and connect its input to the IP core's `dataout` port.

Figure 3. Internal Architecture of ALTIOBUF (Input Buffer Mode)

This figure shows the internal architecture of the input buffer in the ALTIOBUF IP core.

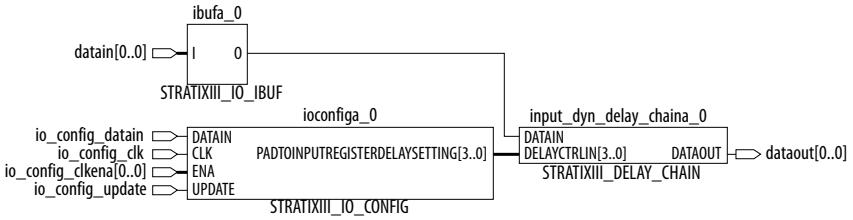
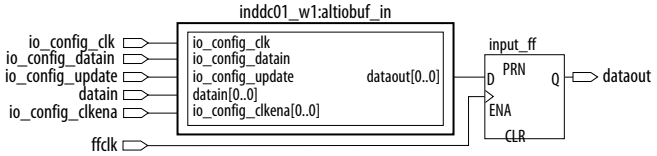


Figure 4. ALTIOBUF (Input Buffer Mode) Connected to the External Flipflop

This figure shows how to connect the external register to the IP core.



Differential Mode Pin Naming Convention

Use the following pin naming convention for differential mode:

```
<pin_name>[1..0]
```

Where:

- `<pin_name>[0]` is connected to the `datain` port
- `<pin_name>[1]` is connected to the `datain_b` port.

Note: You must apply a differential I/O standard to both pins.

ALTIOBUF Output Buffer

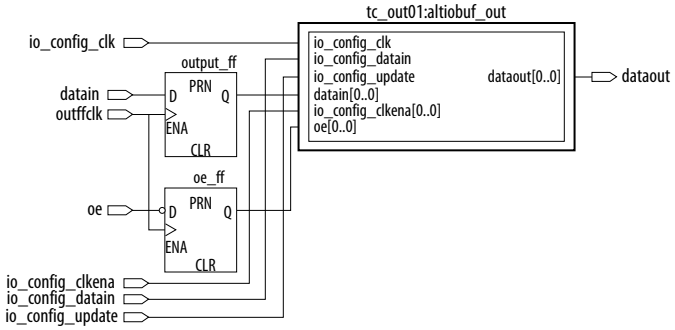
The ALTIOBUF IP core (output buffer mode) uses the output and oe path of the dynamic delay chain, where both share the same IO_CONFIG settings.

Contrary to the input path in the output and oe paths, you can add two optional registers, which are external to the IP core. One is for the output path and the other is for the oe path.

Instead of connecting the input data to the `datain` port of the ALTIOBUF IP core (output buffer mode), it is connected to the input of the registers that are external to the IP core. The output of the register is then driven to the `datain` port of the first output delay chain port. In a similar way, the inverted input oe is connected to the oe register that is external to the IP core, which drives the `datain` port of the first oe delay chain port.

Figure 5. ALTIOBUF (Output Buffer Mode) Connected with the External Flipflops

This figure shows how to connect the output and oe registers to the ALTIOBUF IP core.

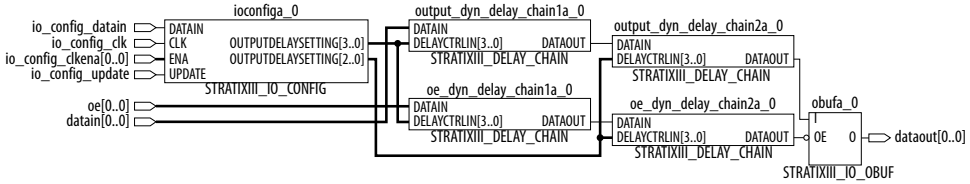


Each of the output and oe delay chains are built from two cascaded output delay chains. The first output delay chain's `dataout` is connected to the second output delay chain's datain. Depending on the parameter chosen (`use_out_dynamic_delay_chain1` or `use_out_dynamic_delay_chain2`), one or both of the output delay chains can be dynamic. In this IP core, you can set the delay only for the dynamic delay chains.

The second output delay chain's `dataout` is connected to the output buffer's i input port for the output path and to the output buffer's oe port for the oe path. Note that the output path and the oe path have their own cascaded delay chains.

Figure 6. Internal Architecture of ALTIOBUF (Output Buffer Mode)

This figure shows the internal architecture of the ALTIOBUF IP core.

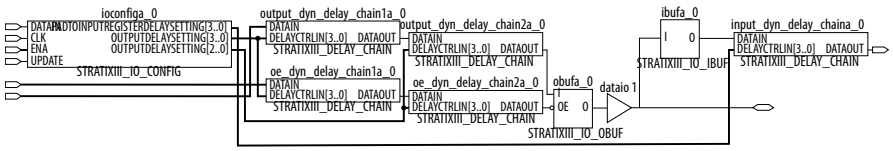


ALTIOBUF Bidirectional Buffer

The bidirectional buffer essentially combines the input buffer and the output buffer, incorporating the input path, output path, and oe path.

By combining the input and output buffers, the output path and oe path are placed before the buffer and the input path is placed after the buffer.

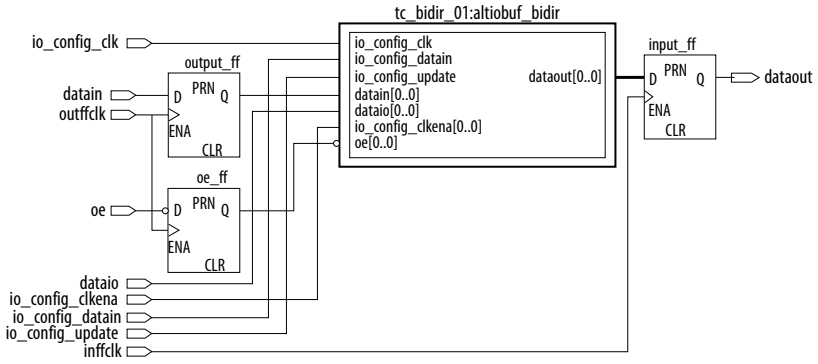
Figure 7. Internal Architecture of ALTIOBUF (Bidirectional Buffer Mode)



By following these specifications, only the input path needs a register external to the IP core. The output and oe registers that are added externally to the IP core are optional.

Figure 8. ALTIOBUF (Bidirectional Buffer Mode) Connected with External Flipflops

This figure shows an example of the ALTIOBUF IP core (bidirectional buffer mode) when output, oe, and input path registers are used that are external to the IP core.



The external register placement is similar to the input/output buffers, where the output and oe registers drive the datain and oe ports of the ALTIOBUF IP core (bidirectional buffer mode) and the dataout port drives the input register.

Note:

- The dynamic termination control path also contains output delay chain 1 and output delay chain 2, which are not accessible through the ALTIOBUF IP core (bidirectional buffer mode). When both the oe and dynamic termination control are used, the two signals (oe and dynamic termination control) can be out of synchronization.
- It is not recommended to switch these two signals simultaneously.

Dynamic Delay Chain Valid Values

For information about the delay chain valid values, refer to the Programmable IOE Delay section of the respective device handbook or data sheet.

Assignments Necessary For Dynamic Delay Chain Usage

If you utilize the dynamic delay chain for the I/O buffer IP core, a `MEMORY_INTERFACE_DATA_PIN_GROUP` assignment to the I/O buffer block is necessary to enable it to go through fitting.

This is because the IP core utilizes the `IO_CONFIG` and `DELAY_CHAIN` blocks that are associated with the use of DDR interfaces. Therefore, the Intel Quartus Prime Fitter requires the assignment to determine the placement of the blocks with the respective `IO_xBUF` block.

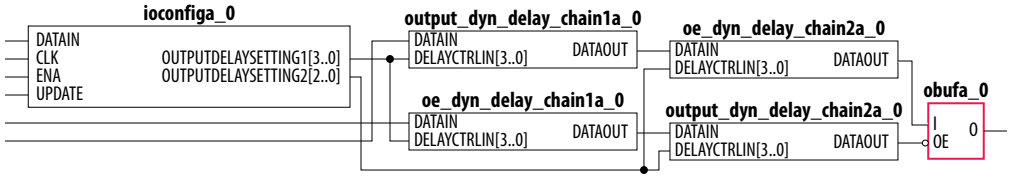
The format of the MEMORY_INTERFACE_DATA_PIN assignments generally appears as the following:

```
MEMORY_INTERFACE_DATA_PIN_GROUP {4|9|18|36} -from iobuf[0] -to iobuf[0]
MEMORY_INTERFACE_DATA_PIN_GROUP {4|9|18|36} -from iobuf[0] -to iobuf[1]
MEMORY_INTERFACE_DATA_PIN_GROUP {4|9|18|36} -from iobuf[0] -to iobuf[2]
….
MEMORY_INTERFACE_DATA_PIN_GROUP {4|9|18|36} -from iobuf[0] -to iobuf[n]
```

`iobuf` is the name of the buffer, either a `stratixiii_io_obuf` (for the output buffer) or `stratixiii_io_ibuf` (for the input buffer). For the bidirectional buffer, either one is acceptable.

Figure 9. Output Buffer

This figure shows an example of an output buffer.



To allow this particular design to be fit, add the following line in the Intel Quartus Prime Setting File (.qsf):

```
set_instance_assignment -name MEMORY_INTERFACE_DATA_PIN_GROUP 4 -from "u2|
test_output_iobuffer_iobuf_out_kk21:test_output_iobuffer_iobuf_out_kk21_componen
t|obufa_0" -to "u2|
test_output_iobuffer_iobuf_out_kk21:test_output_iobuffer_iobuf_out_kk21_componen
t|obufa_0"
```

You can also use the Assignment Editor to set the column fields as shown in the following table:

Table 4. Assigning the MEMORY_INTERFACE_DATA_PIN_GROUP Assignment

Column	Setting
From	u2| test_output_iobuffer_iobuf_out_kk21:test_output_iobuffer_iobuf_out_kk21_component|obufa_0
To	u2| test_output_iobuffer_iobuf_out_kk21:test_output_iobuffer_iobuf_out_kk21_component|obufa_0
Assignment Name	MEMORY_INTERFACE_DATA_PIN_GROUP
Value	4
Enable	Yes

Then, set the **Value** field as shown in the following table:

Table 5. MEMORY_INTERFACE_DATA_PIN_GROUP Value

Number of Channels	MEMORY_INTERFACE_DATA_PIN_GROUP Value
1–6	4
7–12	9
13–24	18
25–48	36

The design example associated with this user guide has this assignment.

Related Information

ALTDQ_DQS2 IP Core User Guide
Provides the I/O configuration block bit sequence for Arria V, Cyclone V, and Stratix V devices

ALTIOBUF References

Provides the signals, parameters, Verilog HDL prototype, and VHDL component declaration for ALTIOBUF IP core.

Related Information

Using the Port and Parameter Definitions on page 7

ALTIOBUF Signals and Parameters: As Input Buffer

Table 6. ALTIOBUF (As Input Buffer) Input Ports

This table lists the input ports for the ALTIOBUF IP core (as input buffer).

Name	Required	Description
datain[]	Yes	The input buffer normal data input port. Input port [NUMBER_OF_CHANNELS - 1..0] wide. The input signal to the I/O output buffer element. For differential signals, this port acquires the positive signal input.
datain_b[]	No	The negative signal input of a differential signal to the I/O input buffer element. Input port [NUMBER_OF_CHANNELS - 1..0] wide. When connected, the datain_b port is always fed by a pad/port atom. This port is used only if the USE_DIFFERENTIAL_MODE parameter value is TRUE.
io_config_datain	No	Input port that feeds the datain port of IO_CONFIG for user-driven dynamic delay chain. Input port used to feed input data to the serial load shift register. The value is a 1-bit wire shared among all I/O instances. This port is available only if the USE_IN_DYNAMIC_DELAY_CHAIN parameter value is TRUE.
io_config_clk	No	Input clock port that feeds the IO_CONFIG for user-driven dynamic delay chain. Input port used as the clock signal of shift register block. The maximum frequency for this clock is 30 MHz. The value is a 1-bit wire shared among all I/O instances. This port is available only if the USE_IN_DYNAMIC_DELAY_CHAIN parameter value is TRUE.
io_config_clkena[]	No	Input clock-enable that feeds the ena port of IO_CONFIG for user-driven dynamic delay chain. Input port [NUMBER_OF_CHANNELS - 1..0] wide. Input port used as the clock enable signal of the shift register block. This port is available only if the USE_IN_DYNAMIC_DELAY_CHAIN parameter value is TRUE.
io_config_update	No	Input port that feeds the IO_CONFIG update port for user-driven dynamic delay chain. When asserted, the serial load shift register bits feed the parallel load register. The value is a 1-bit wire shared among all I/O instances. This port is available only if the USE_IN_DYNAMIC_DELAY_CHAIN parameter value is TRUE.
dynamicterminationcontrol[]	No	Input signal for bidirectional I/Os. Input port [NUMBER_OF_CHANNELS - 1..0] wide. When specified, this port selects from the core either Rs code, when the input value is LOW; or Rt code, when the input value is HIGH. Enable Rt only when the bidirectional I/O is receiving input. When the bidirectional I/O is not receiving input, disable this port for optimal output performance and power dissipation.

continued...

Name	Required	Description		
		Value	Rs Code	Rt Code
		0	1	0
		1	0	1

Table 7. ALTIOBUF (As Input Buffer) Output Ports

This table shows the output ports for the ALTIOBUF IP core (as input buffer).

Name	Required	Description
dataout[]	Yes	Input buffer output port. Input port [NUMBER_OF_CHANNELS - 1..0] wide. The I/O input buffer element output.

Table 8. ALTIOBUF (As Input Buffer) Parameters

This table lists the parameters for the ALTIOBUF IP core (as input buffer).

Name	Required	Type	Description
ENABLE_BUS_HOLD	No	String	Specifies whether the bus hold circuitry is enabled. Values are TRUE and FALSE. When set to TRUE, bus hold circuitry is enabled and the previous value, instead of high impedance, is assigned to the output port when there is no valid input. If omitted, the default is FALSE. Currently, ENABLE_BUS_HOLD and USE_DIFFERENTIAL_MODE cannot be used simultaneously.
USE_DIFFERENTIAL_MODE	No	String	Specifies whether the input buffer is differential. Values are TRUE and FALSE. When set to TRUE, the output is the difference between the datain and datain_b ports. If omitted, the default is FALSE. Currently, ENABLE_BUS_HOLD and USE_DIFFERENTIAL_MODE cannot be used simultaneously.
USE_IN_DYNAMIC_DELAY_CHAIN	No	String	Specifies whether the input buffer incorporates the user-driven dynamic delay chain in the IP core, specifically, IO_CONFIG and an input delay cell. Values are TRUE and FALSE. If omitted, the default is FALSE.
NUMBER_OF_CHANNELS	Yes	Integer	Specifies the number of I/O buffers that must be instantiated. Value must be greater than or equal to 1. A value of 1 indicates that the buffer is a 1-bit port and accommodates wires; a value greater than 1 indicates that the port can be connected to a bus of width NUMBER_OF_CHANNELS.
USE_DYNAMIC_TERMINATION_CONTROL	No	String	Specifies dynamic termination control. Values are True and False. If omitted, the default is False.

ALTIOBUF Signals and Parameters: As Output Buffer

Table 9. ALTIOBUF (As Output Buffer) Input Ports

This table lists the input ports for the ALTIOBUF IP core (as output buffer).

Name	Required	Description
datain[]	Yes	The output buffer input port. Input port [NUMBER_OF_CHANNELS - 1..0] wide. For differential signals, this port supplies the positive signal input. Inputs are fed to the I/O output buffer element.
io_config_datain	No	Input port that feeds the datain port of IO_CONFIG for user-driven dynamic delay chain. Input port used to feed input data to the serial load shift register. The value is a 1-bit wire shared among all I/O instances. This port is available when the USE_OUT_DYNAMIC_DELAY_CHAIN1 or USE_OUT_DYNAMIC_DELAY_CHAIN2 parameter value is TRUE.
io_config_clk	No	Input clock port that feeds the IO_CONFIG for user-driven dynamic delay chain. Note that the maximum frequency for this clock is 30 MHz. Input port used as the clock signal of shift register block. The value is a 1-bit wire shared among all I/O instances. This port is available when the USE_OUT_DYNAMIC_DELAY_CHAIN1 or USE_OUT_DYNAMIC_DELAY_CHAIN2 parameter value is TRUE.
io_config_clkena[]	No	Input clock-enable that feeds the ena port of IO_CONFIG for user-driven dynamic delay chain. Input port [NUMBER_OF_CHANNELS - 1..0] wide. Input port used as the clock signal of shift register block. This port is available when the USE_OUT_DYNAMIC_DELAY_CHAIN1 or USE_OUT_DYNAMIC_DELAY_CHAIN2 parameter value is TRUE.
io_config_update	No	Input port that feeds the IO_CONFIG update port for user-driven dynamic delay chain. When asserted, the serial load shift register bits feed the parallel load register. The value is a 1-bit wire shared among all I/O instances. This port is available when the USE_OUT_DYNAMIC_DELAY_CHAIN1 or USE_OUT_DYNAMIC_DELAY_CHAIN2 parameter value is TRUE.
oe[]	No	The output-enable source to the tri-state buffer. Input port [NUMBER_OF_CHANNELS - 1..0] wide. When the oe port is asserted, dataout and dataout_b are enabled. When oe is deasserted, both dataout and dataout_b are disabled. This port is used only when the USE_OE parameter value is TRUE. If omitted, the default is V_{CC}.
seriesterminationcontrol[]	No	Receives the current state of the pull up and pull down Rs control buses from a termination logic block. Input port [WIDTH_STC * NUMBER_OF_CHANNELS - 1..0] wide.

continued...

Name	Required	Description
		Port is available only when the USE_TERMINATION_CONTROL parameter value is TRUE.
seriesterminationcontrol_b	No	Receives the current state of the pull up and pull down Rs control buses from a termination logic block. Input port [WIDTH_STC * NUMBER_OF_CHANNELS - 1..0] wide. Port is available only when the USE_DIFFERENTIAL_MODE parameter value is TRUE.
parallelterminationcontrol[]	No	Receives the current state of the pull up and pull down Rt control buses from a termination logic block. Input port [WIDTH_PTC * NUMBER_OF_CHANNELS - 1..0] wide. The port is available for Stratix III device families only. Supported in Stratix series only. Port is available only when the USE_TERMINATION_CONTROL parameter value is TRUE.
parallelterminationcontrol_b	No	Receives the current state of the pull up and pull down Rt control buses from a termination logic block. Input port [WIDTH_PTC * NUMBER_OF_CHANNELS - 1..0] wide. Port is available only when the USE_DIFFERENTIAL_MODE parameter value is TRUE. The port is available for Stratix III device families only. Supported in Stratix series only. Port is available only when the USE_DIFFERENTIAL_MODE parameter value is TRUE.

Table 10. ALTIOBUF (As Output Buffer) Output Ports

This table lists the output ports for the ALTIOBUF IP core (as output buffer).

Name	Required	Description
dataout[]	Yes	Output buffer output port. Output port [NUMBER_OF_CHANNELS - 1..0] wide. The I/O output buffer element output.
dataout_b[]	No	Differential output buffer-negative output. Output port [NUMBER_OF_CHANNELS - 1..0] wide. The I/O output buffer negative output. Port is available only when the USE_DIFFERENTIAL_MODE parameter value is TRUE.

Table 11. ALTIOBUF (As Output Buffer) Parameter

This table lists the parameters for the ALTIOBUF IP core (as output buffer).

Name	Required	Type	Description
ENABLE_BUS_HOLD	No	String	Specifies whether the bus hold circuitry is enabled. Values are TRUE and FALSE. When set to TRUE, bus hold circuitry is enabled, and the previous value, instead of high impedance, is assigned to the output port when there is no valid input. If omitted, the default is FALSE.

continued...

Name	Required	Type	Description
			Currently, ENABLE_BUS_HOLD and USE_DIFFERENTIAL_MODE cannot be used simultaneously.
USE_DIFFERENTIAL_MODE	No	String	Specifies whether the output buffer mode is differential. Values are TRUE and FALSE. When set to TRUE, both the dataout and dataout_b ports are used. If omitted, the default is FALSE. Currently, ENABLE_BUS_HOLD and USE_DIFFERENTIAL_MODE cannot be used simultaneously.
OPEN_DRAIN_OUTPUT	No	String	Open drain mode. Values are TRUE and FALSE. If omitted, the default is FALSE. *Note:* Currently, OPEN_DRAIN_OUTPUT and USE_DIFFERENTIAL_MODE cannot be used simultaneously.
USE_TERMINATION_CONTROL	No	String	Specifies series termination control and parallel termination control. Values are TRUE and FALSE. If omitted, the default is FALSE. When this parameter is used for Arria II GX devices and the Cyclone series, only series termination control is available. Stratix series support both.
USE_OUT_DYNAMIC_DELAY_CHAIN1	No	String	Specifies whether the output buffer incorporates a user-driven dynamic delay chain in the IP core, specifically, IO_CONFIG and the first output delay cell. Additional input ports are io_config_clk, io_config_clkena, io_config_update, and io_config_datain. Values are TRUE and FALSE. If omitted, the default is FALSE.
USE_OUT_DYNAMIC_DELAY_CHAIN2	No	String	Specifies whether the output buffer incorporates a user-driven dynamic delay chain in the IP core, specifically, IO_CONFIG and the second output delay cell. Additional input ports are io_config_clk, io_config_clkena, io_config_update, and io_config_datain. Values are TRUE and FALSE. If omitted, the default is FALSE.
NUMBER_OF_CHANNELS	Yes	Integer	Specifies the number of I/O buffers that must be instantiated. Value must be greater than or equal to 1. A value of 1 indicates that the buffer is a 1-bit port and accommodates wires. A value greater than 1 indicates that the port can be connected to a bus of width NUMBER_OF_CHANNELS.
WIDTH_STC	No	Integer	Specifies the width setting for the series termination control bus.
WIDTH_PTC	No	Integer	Specifies the width setting for the parallel termination control bus.

continued...

Name	Required	Type	Description
USE_OE	No	String	Specifies whether the oe port is used.
LEFT_SHIFT_SERIES_TERMINATION_CONTROL	No	String	Values are True and False. If omitted, the default is False. Available for all supported devices except Cyclone series device family.
PSEUDO_DIFFERENTIAL_MODE	No	String	Specifies the pseudo differential mode. Values are True and False. If omitted, the default is False. Available only when the USE_DIFFERENTIAL_MODE parameter value is TRUE.

ALTIOBUF Signals and Parameters: As Bidirectional Buffer

Table 12. ALTIOBUF (As Bidirectional Buffer) Input Ports

This table lists the input ports for the ALTIOBUF IP core (as bidirectional buffer).

Name	Required	Description
datain[]	Yes	The input buffer input port. Input port [NUMBER_OF_CHANNELS - 1..0] wide. The input signal to the I/O output buffer element.
io_config_datain	No	Input port that feeds the datain port of IO_CONFIG for user-driven dynamic delay chain. Input port used to feed input data to the serial load shift register. The value is a 1-bit wire shared among all I/O instances. This port is available only if the USE_IN_DYNAMIC_DELAY_CHAIN, USE_OUT_DYNAMIC_DELAY_CHAIN1, or USE_OUT_DYNAMIC_DELAY_CHAIN2 parameter value is TRUE.
io_config_clk	No	Input clock port that feeds the IO_CONFIG for user-driven dynamic delay chain. The maximum frequency for this clock is 30 MHz. Input port used as the clock signal of shift register block. The value is a 1-bit wire shared among all I/O instances. This port is available only if the USE_IN_DYNAMIC_DELAY_CHAIN, USE_OUT_DYNAMIC_DELAY_CHAIN1, or USE_OUT_DYNAMIC_DELAY_CHAIN2 parameter value is TRUE.
io_config_clkena[]	No	Input clock-enable that feeds the ena port of IO_CONFIG for user-driven dynamic delay chain. Input port [NUMBER_OF_CHANNELS - 1..0] wide. Input port used as the clock signal of the shift register block. This port is available only if the USE_IN_DYNAMIC_DELAY_CHAIN, USE_OUT_DYNAMIC_DELAY_CHAIN1, or USE_OUT_DYNAMIC_DELAY_CHAIN2 parameter value is TRUE.
io_config_update	No	Input port that feeds the IO_CONFIG update port for user-driven dynamic delay chain. When asserted, the serial load shift register bits feed the parallel load register. The value is a 1-bit wire shared among all I/O instances.

continued...

Name	Required	Description
		This port is available only if the USE_IN_DYNAMIC_DELAY_CHAIN, USE_OUT_DYNAMIC_DELAY_CHAIN1, or USE_OUT_DYNAMIC_DELAY_CHAIN2 parameter value is TRUE.
oe[]	Yes	The output-enable source to the tri-state buffer. Input port [NUMBER_OF_CHANNELS - 1..0] wide. If omitted, the default is V_{CC}.
oe_b	No	The output-enable source to the tri-state buffer. Input port [NUMBER_OF_CHANNELS - 1..0] wide. If omitted, the default is V_{CC}. Port is available only when the USE_DIFFERENTIAL_MODE parameter value is TRUE.
dynamicterminationcontrol[]	No	Input signal for bidirectional I/Os. Input port [NUMBER_OF_CHANNELS - 1..0] wide. When specified, this port selects from the core either Rs code, when the input value is LOW; or Rt code, when the input value is HIGH. Enable Rt only when the bidirectional I/O is receiving input. When the bidirectional I/O is not receiving input, disable this port for optimal output performance and power dissipation.
dynamicterminationcontrol_b	No	Input signal for bidirectional I/Os. Input port [NUMBER_OF_CHANNELS - 1..0] wide. When specified, this port selects from the core either Rs code, when the input value is LOW; or Rt code, when the input value is HIGH. Enable Rt only when the bidirectional I/O is receiving input. When the bidirectional I/O is not receiving input, disable this port for optimal output performance and power dissipation. Port is available only when the USE_DIFFERENTIAL_MODE parameter value is TRUE.
seriesterminationcontrol[]	No	Receives the current state of the pull up and pull down Rs control buses from a termination logic block. [WIDTH_STC * NUMBER_OF_CHANNELS - 1..0] wide. Port is applicable only when the USE_TERMINATION_CONTROL parameter value is TRUE.

Value	Rs Code	Rt Code
0	1	0
1	0	1

Value	Rs Code	Rt Code
0	1	0
1	0	1

continued...

Name	Required	Description
seriesterminationcontrol_b	No	Receives the current state of the pull up and pull down Rs control buses from a termination logic block. [WIDTH_STC * NUMBER_OF_CHANNELS - 1..0] wide. Port is applicable only when the USE_TERMINATION_CONTROL parameter value is TRUE.
parallelterminationcontrol[]	No	Receives the current state of the pull up and pull down Rt control buses from a termination logic block. Input port [((WIDTH_PTC * NUMBER_OF_CHANNELS) - 1)..0] wide. Port is applicable only when the USE_TERMINATION_CONTROL parameter value is TRUE.
parallelterminationcontrol_b	No	Receives the current state of the pull up and pull down Rt control buses from a termination logic block. Input port [((WIDTH_PTC * NUMBER_OF_CHANNELS) - 1)..0] wide. Port is applicable only when the USE_TERMINATION_CONTROL parameter value is TRUE.

Table 13. ALTIOBUF (As Bidirectional Buffer) Output Ports

This table lists the output ports for ALTIOBUF IP core (as bidirectional buffer)

Name	Required	Description
dataout[]	Yes	Buffer output port. Output port [NUMBER_OF_CHANNELS - 1..0] wide. The I/O output buffer element output.

Table 14. ALTIOBUF (As Bidirectional Buffer) Bidirectional Ports

This table lists the bidirectional ports for ALTIOBUF IP core (as bidirectional buffer)

Name	Required	Description
dataio[]	Yes	Bidirectional port that directly feeds a bidirectional pin in the top-level design. Bidirectional port [(NUMBER_OF_CHANNELS - 1)..0] wide.
dataio_b[]	No	Bidirectional DDR port that directly feeds a bidirectional pin in the top-level design. Bidirectional port [(NUMBER_OF_CHANNELS - 1)..0] wide. The negative signal input/output to/from the I/O buffer. This port is used only if the use_differential_mode_parameter is set to TRUE.

Table 15. ALTIOBUF (As Bidirectional Buffer) Parameter

This table lists the parameters for ALTIOBUF IP core (as bidirectional buffer)

Name	Required	Type	Description
ENABLE_BUS_HOLD	No	String	Specifies whether the bus hold circuitry is enabled. Values are TRUE and FALSE. When set to TRUE, bus hold circuitry is enabled, and the previous value, instead of high impedance, is assigned to the output port when there is no valid input. If omitted, the default is FALSE. Currently, ENABLE_BUS_HOLD and USE_DIFFERENTIAL_MODE cannot be used simultaneously.
USE_ DIFFERENTIAL_MODE	No	String	Specifies whether the bidirectional buffer is differential. Values are TRUE and FALSE. When set to TRUE, the output is the difference between the dataio and dataio_b ports. If omitted, the default is FALSE.

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Name	Required	Type	Description
			Currently, ENABLE_BUS_HOLD and USE_DIFFERENTIAL_MODE cannot be used simultaneously.
OPEN_DRAIN_OUTPUT	No	String	Open drain mode. Values are TRUE and FALSE. If omitted, the default is FALSE. OPEN_DRAIN_OUTPUT and USE_DIFFERENTIAL_MODE cannot be used simultaneously.
USE_TERMINATION_CONTROL	No	String	Specifies series termination control and parallel termination control. Values are TRUE and FALSE. If omitted, the default is FALSE. When this parameter is used for Arria II GX devices and Cyclone series, only series termination control is available. Stratix series supports both.
USE_DYNAMIC_TERMINATION_CONTROL	No	String	Specifies dynamic termination control. Values are TRUE and FALSE. If omitted, the default is FALSE. An error is issued if parallel termination (Rt) is on and dynamic termination control is not connected on a bidir pin. An error is issued if Rt is off and dynamic termination control is connected on an input or bidirectional pin.
USE_IN_DYNAMIC_DELAY_CHAIN	No	String	Specifies whether the input buffer incorporates the user-driven dynamic delay chain in the IP core, specifically, IO_CONFIG and an input delay cell. Additional input ports are io_config_clk, io_config_clkena, io_config_update, and io_config_datain. Values are TRUE and FALSE. If omitted, the default is FALSE.
USE_OUT_DYNAMIC_DELAY_CHAIN1	No	String	Specifies whether the output buffer incorporates a user-driven dynamic delay chain in the IP core, specifically, IO_CONFIG and the first output delay cell. Additional input ports are io_config_clk, io_config_clkena, io_config_update, and io_config_datain. Values are TRUE and FALSE. If omitted, the default is FALSE.
USE_OUT_DYNAMIC_DELAY_CHAIN2	No	String	Specifies whether the output buffer incorporates a user-driven dynamic delay chain in the IP core, specifically, IO_CONFIG and the second output delay cell. Additional input ports are io_config_clk, io_config_clkena, io_config_update, and io_config_datain. Values are TRUE and FALSE. If omitted, the default is FALSE.
NUMBER_OF_CHANNELS	Yes	Integer	Specifies the number of I/O buffers that must be instantiated. Value must be greater than or equal to 1. A value of 1 indicates that the buffer is a 1-bit port and accommodates wires. A value greater than 1 indicates that the port can be connected to a bus of width NUMBER_OF_CHANNELS.
WIDTH_STC	No	Integer	Specifies the width setting for the series termination control bus.
WIDTH_PTC	No	Integer	Specifies the width setting for the parallel termination control bus.

Verilog HDL Prototype

You can locate the Verilog HDL prototype in the Verilog Design File (`.v`) `altera_mf.v` in the `<Intel Quartus Prime installation directory>\eda\sim_lib` directory.

VHDL Component Declaration

You can locate VHDL component declaration in the VHDL Design File (`.vhd`) `altera_mf_components.vhd` in the `<Intel Quartus Prime installation directory>\libraries\vhdl\altera_mf` directory.

VHDL LIBRARY-USE Declaration

The VHDL LIBRARY-USE declaration is not required if you use the VHDL Component Declaration.

```
LIBRARY altera_mf;
USE altera_mf.altera_mf_components.all;
```

ALTIOBUF IP Core User Guide Archives

If an IP core version is not listed, the user guide for the previous IP core version applies.

IP Core Version	User Guide
17.0	I/O Buffer (ALTIOBUF) IP Core User Guide
14.1	I/O Buffer (ALTIOBUF) IP Core User Guide

Document Revision History for the ALTIOBUF IP Core User Guide

Document Version	Intel Quartus Prime Version	Changes
2020.01.13	19.1	Updated the topic about I/O buffer and dynamic delay integration to clarify that for LVDS interfaces using the ALTLVDS IP core, you enable the dynamic delay in the `.qsf` file.
2019.11.18	19.1	• Added table listing the device family support for the ALTIOBUF IP core. • Changed document title to *ALTIOBUF IP Core User Guide*. • Names and text rebranded to Intel.

Date	Version	Changes
June 2017	2017.06.19	• Added support for Intel Cyclone 10 LP devices. • Renamed "Quartus II" to "Quartus Prime". • Removed topics about the installing and licensing IP cores, IP catalog and parameter editor, customizing and generating IP cores, and upgrading IP cores. These topics are available and updated in *Introduction to Intel FPGA IP Cores*.
December 2014	2014.12.15	Template update.

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Date	Version	Changes
2014.06.30	4.0	• Replaced MegaWizard Plug-In Manager information with IP Catalog. • Added standard information about upgrading IP cores. • Added standard installation and licensing information. • Removed outdated device support level information. IP core device support is now available in IP Catalog and parameter editor. • Removed all references to obsolete SOPC Builder tool.
June 2013	3.2	• Added "Differential Mode Pin Naming Convention" • Updated the "Assignments Necessary For Dynamic Delay Chain Usage" to include a link to the ALTDQ_DQS2 Megafunction User Guide.
June 2013	3.1	Updated Table 2–1 on page 2–1 and Table 2–2 on page 2–2 to update the device family support.
February 2012	3.0	• Updated device support • Added references to device handbook for delay chain values
November 2010	2.1	• Updated to new template • Updated ports and parameters • Added prototypes and component declarations
December 2008	2.0	• Added sentence to I/O Buffer and Dynamic Delay Integration • Added two last paragraph to Common Applications • Added extra note to Table 3–5 • Remove figures
November 2007	1.0	Initial Release.