AER Hardware and cabling

This document describes the cabling and protocol for the AER boards.

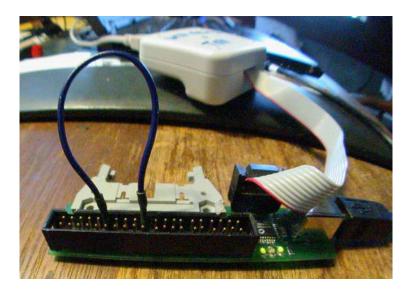
The hardware is receives and sends word-parallel point to point or multisender AER, using active low request and acknowledge signals.

There is a USB device connector and two functionally equivalent AER connectors: a CAVIAR standard 40 pin 100mil double row header and a Rome 20 pin connector. The pin assignments on the CAVIAR connector are specified in the CAVIAR document "Consortiumstandards.pdf" in the repository folder CAVIAR/wp7 and are repeated here for reference:

	Header (on PCB, front view)																		
Reserved	Reserved	Reserved	Reserved	Reserved	/ACK	Reserved	Reserved	Reserved	/REQ	GND	AE[0]	AE[1]	AE[2]	AE[3]	AE[4]	AE[5]	AE[6]	AE[7]	Reserved
390	370	350	330	310	290	270	250	230	210	190	170	150	130	110	90	⁷ O	50	30	10
400	38℃	36⊖	340	320	300	280	260	240	220		180	160	140	120	100	80	60	40	20
GND	Reserved	Reserved	Reserved	Reserved	GND	Reserved	GND	GND	GND	key pin pin missing	AE[15]	AE[14]	AE[13]	AE[12]	AE[11]	AE[10]	AE[9]	AE[8]	GND

Figure 1: IDC 40 plugs for ATA/133 based AER bus standard

Note that on the SimpleMonitor/SimpleSequencer board based on the SiLabsC8051F320 chip, the cutout is opposite pin 1, which can be identified by its square solder pad. A patch from !Req to !Ack is shown below. The SimpleMonitor/Sequencer board is being debugged and programmed with the SiLabs USB Debug Adapator. Pin 1 of the IDE header is at the upper left.



The other connector on the board is a 20 pin SCX Rome PCI-AER connector on it. That cabling follows

