AER Hardware and cabling

This document describes the cabling and protocol for the AER boards.

The hardware is receives and sends word-parallel point to point or multisender AER, using active low request and acknowledge signals.

There is a USB device connector and two functionally equivalent AER connectors: a CAVIAR standard 40 pin 100mil double row header and a Rome 20 pin connector. The pin assignments on the CAVIAR connector are specified in the CAVIAR document "Consortiumstandards.pdf" in the repository folder CAVIAR/wp7 and are repeated here for reference:

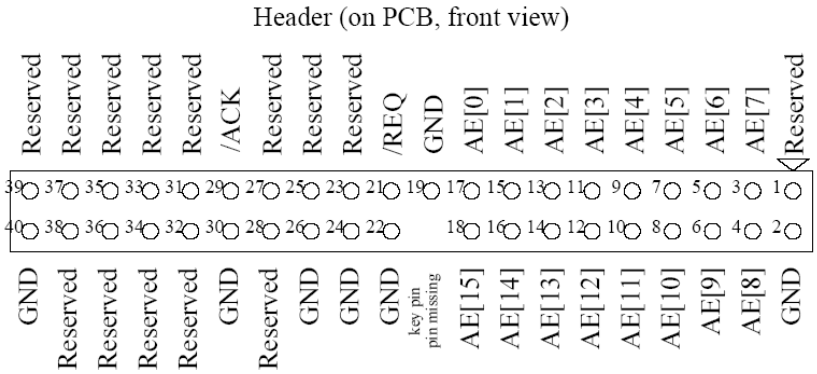
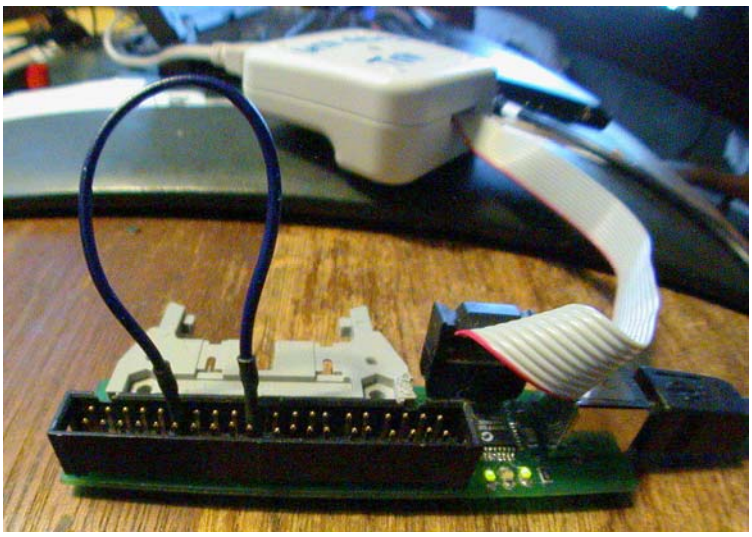


Figure 1: IDC 40 plugs for ATA/133 based AER bus standard

Note that on the SimpleMonitor/SimpleSequencer board based on the SiLabsC8051F320 chip, the cutout is opposite pin 1, which can be identified by its square solder pad. A patch from !Req to !Ack is shown below. The SimpleMonitor/Sequencer board is being debugged and programmed with the SiLabs USB Debug Adapator. Pin 1 of the IDE header is at the upper left.



The other connector on the board is a 20 pin SCX Rome PCI-AER connector on it. That cabling follows