

Sistemi Operativi I

Corso di Laurea in Informatica
2022-2023



SAPIENZA
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Contiguous Memory Allocation

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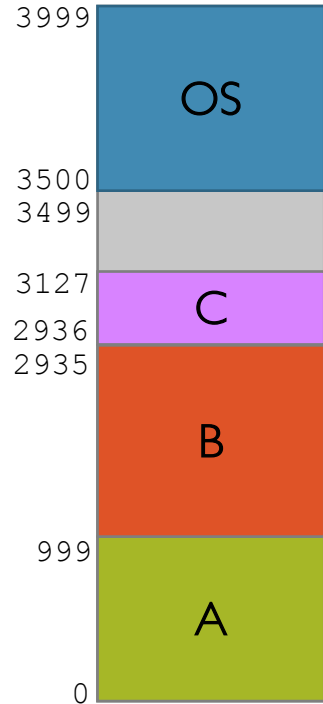
- So far, we have assumed each process is allocated into a contiguous space of physical memory
- One simple method is to divide upfront all available memory dedicated to user processes into **equally-sized** segments/partitions
 - Assign each process to a segment
 - Implicitly restricts the grade of multiprogramming (i.e., the number of simultaneous processes) and their size
 - No longer used!

Contiguous Memory Allocation

An alternative approach is for the OS to keep track of **free** (unused) memory segments, as processes enter the system, grow, and terminate

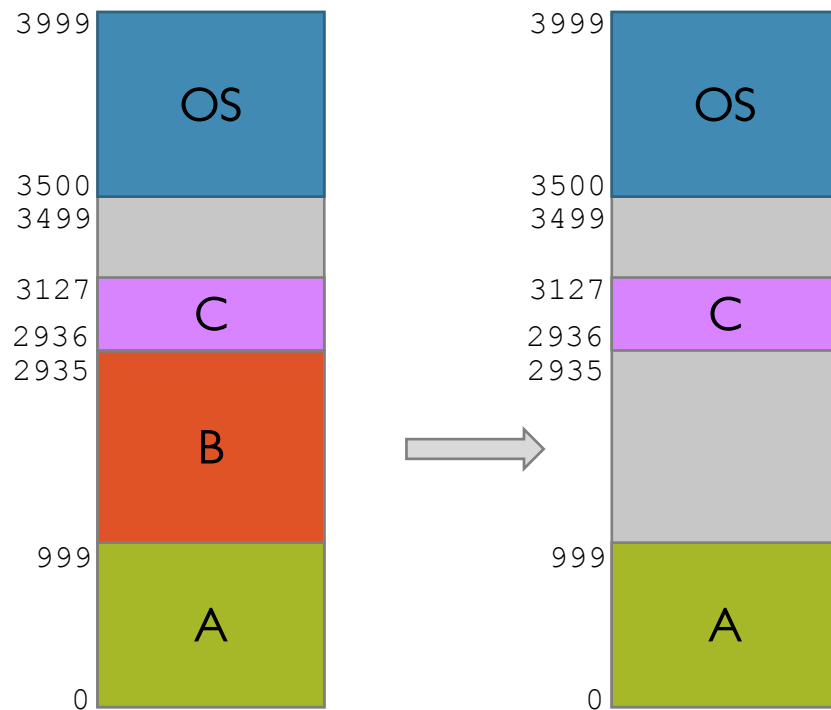
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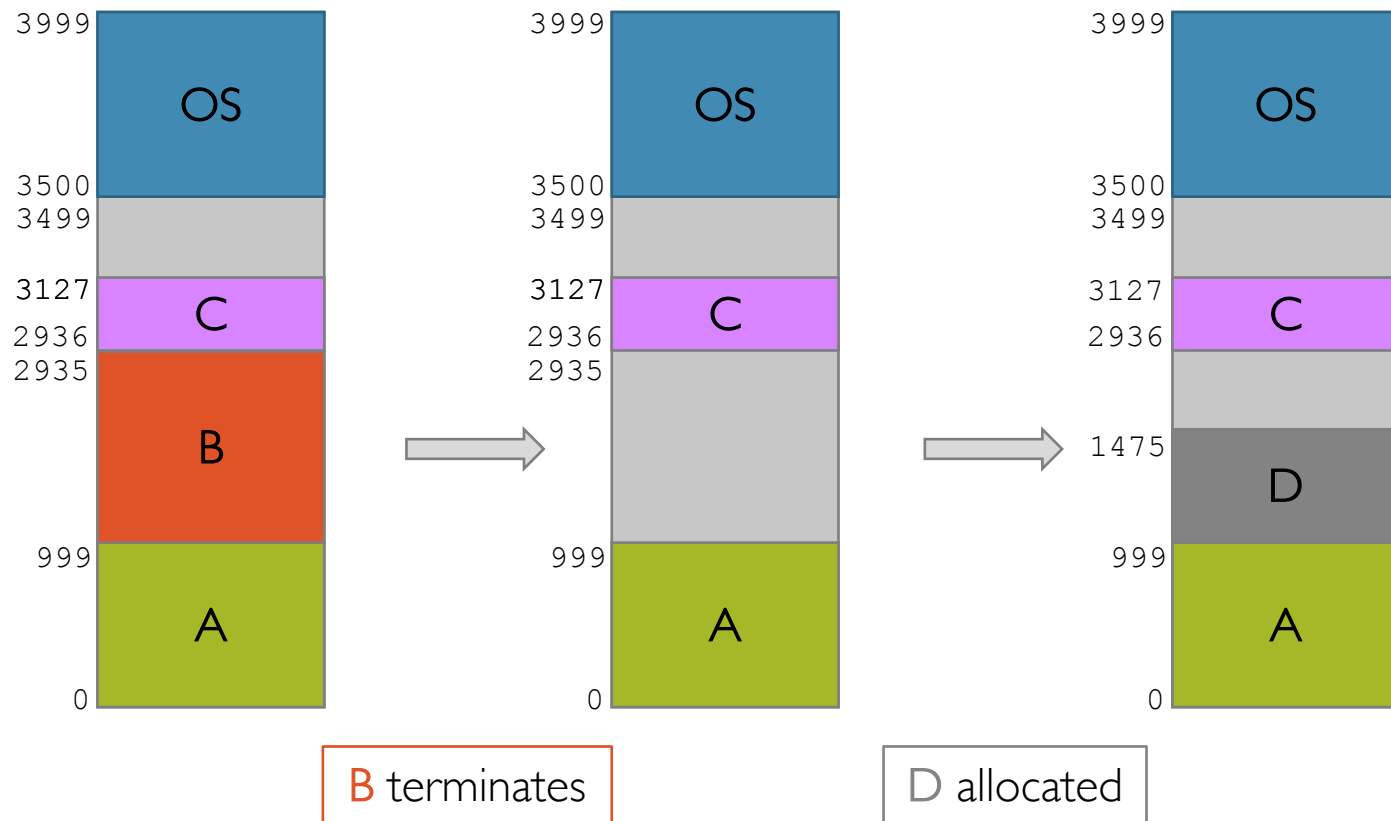
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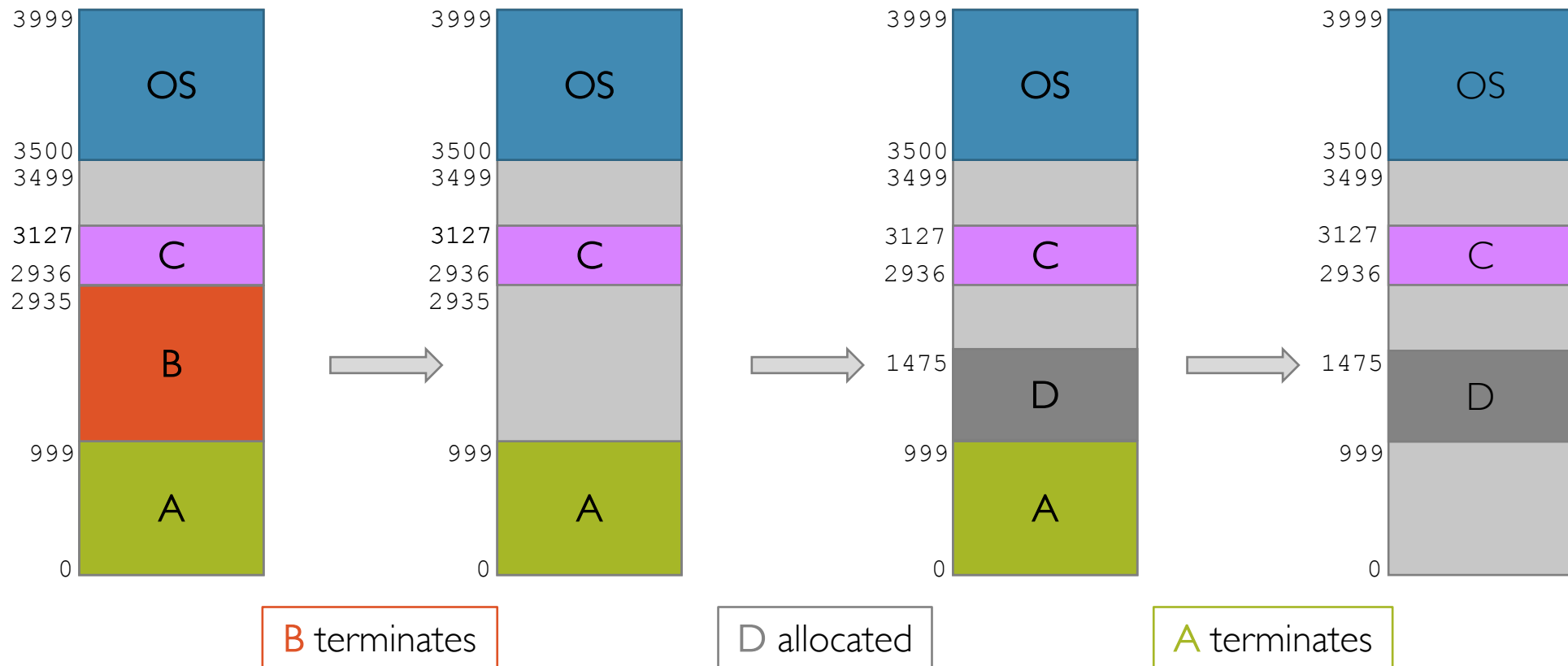
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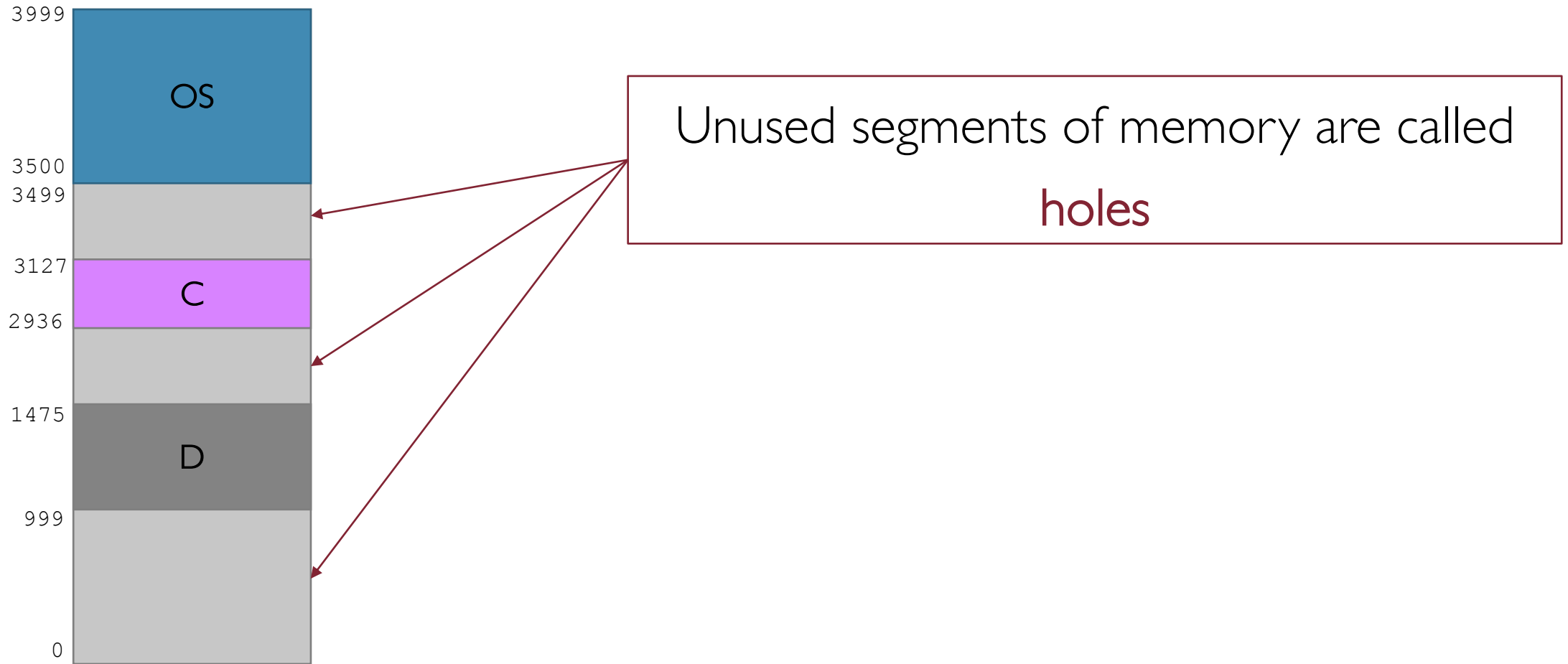


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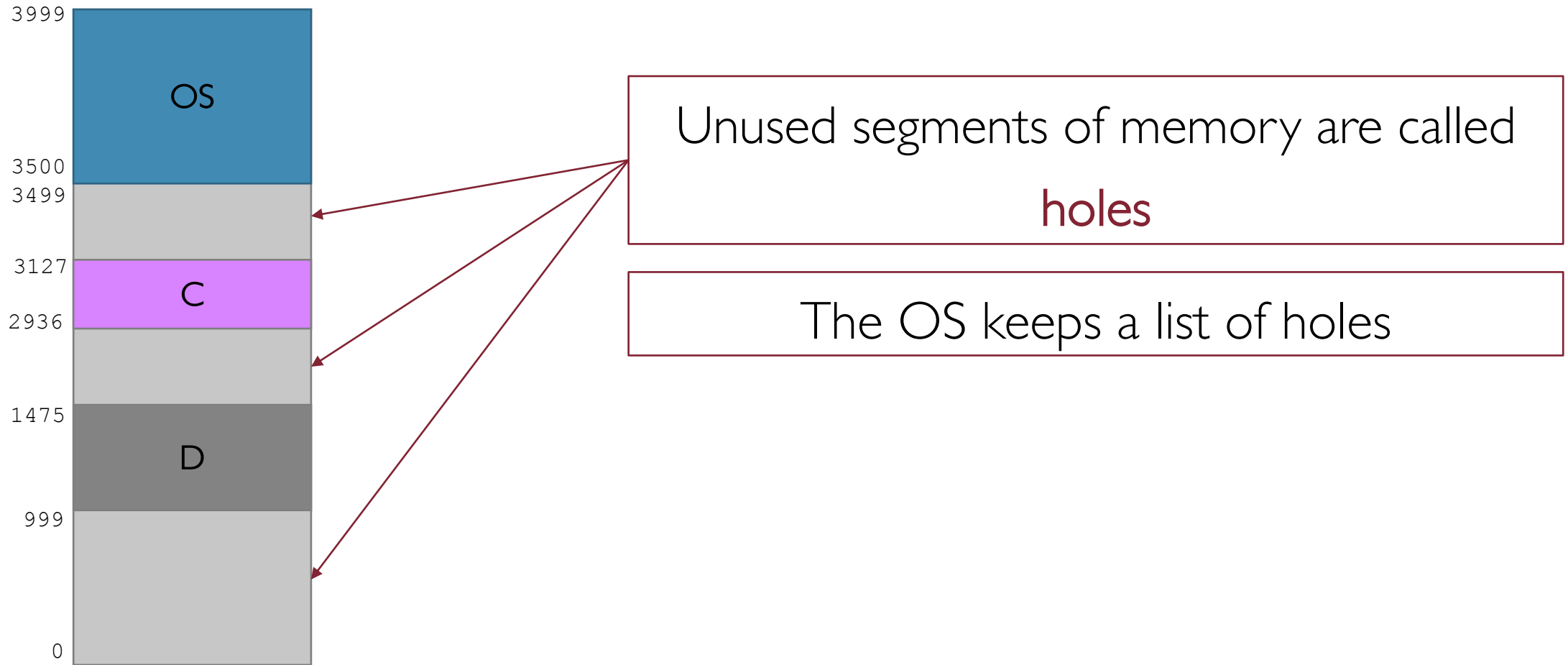
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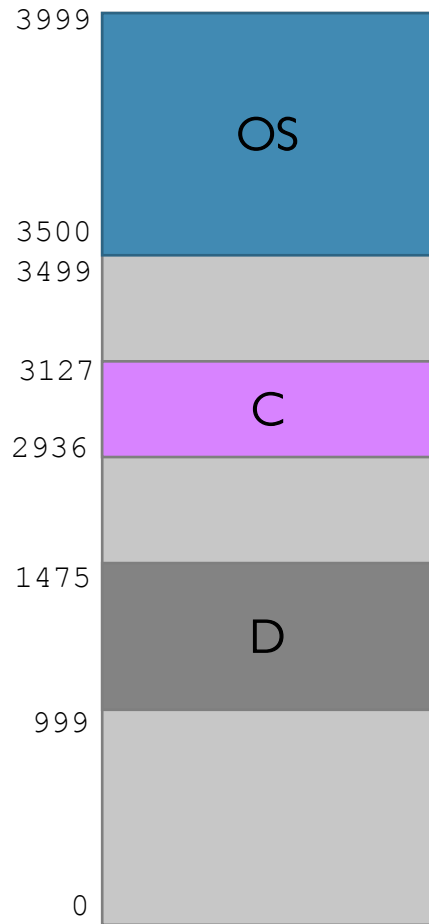
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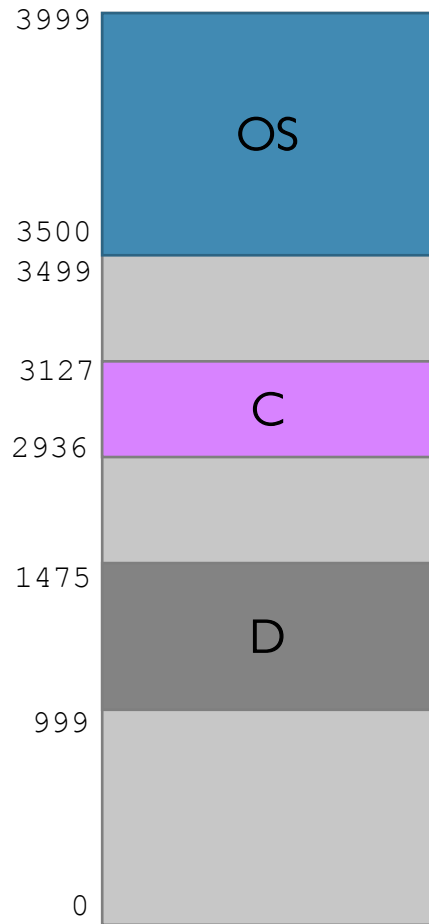


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How?

Memory Allocation Policies: First-Fit

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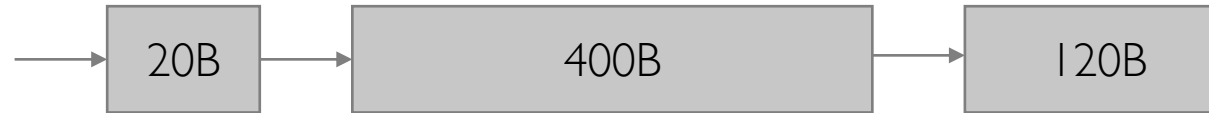
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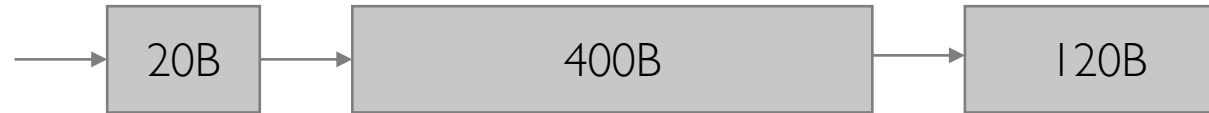
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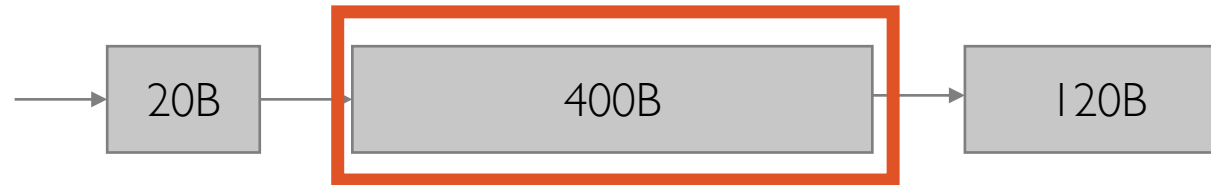
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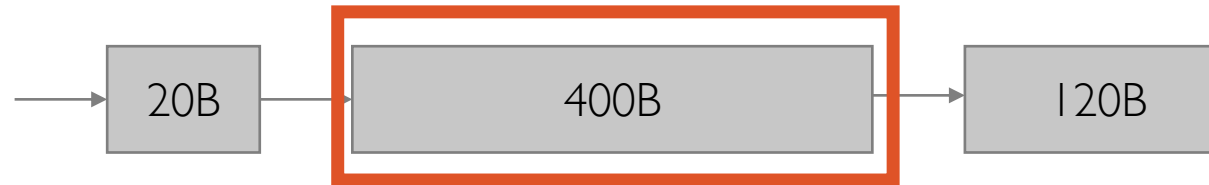
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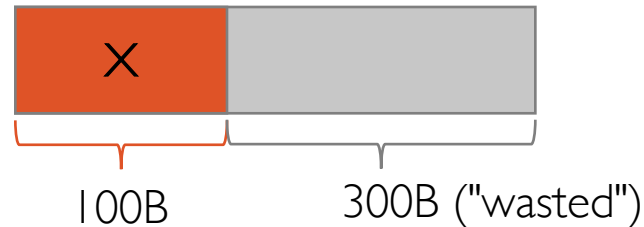
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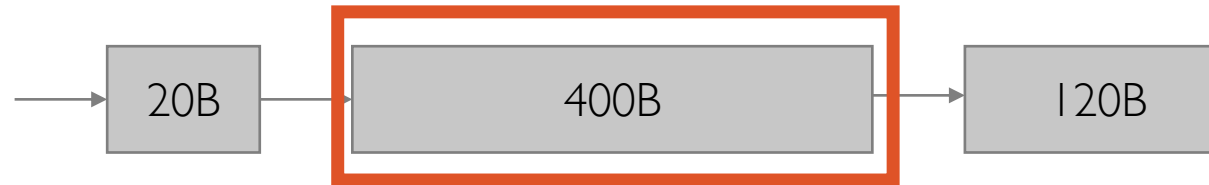


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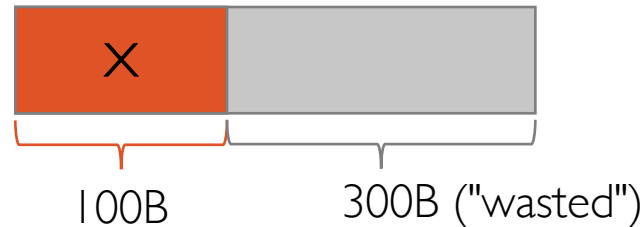


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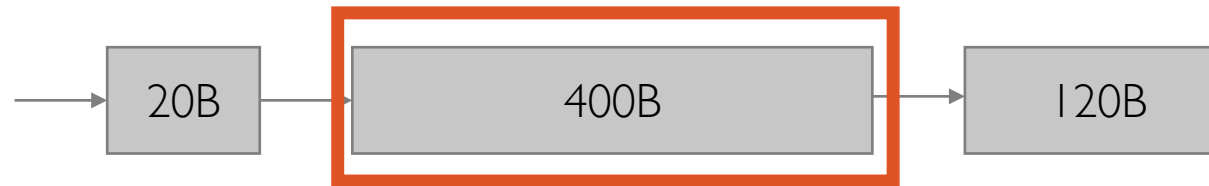
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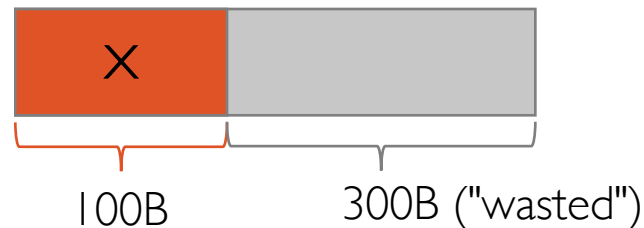
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We will not be able to satisfy this request even if theoretically we could

Memory Allocation Policies: Best-Fit

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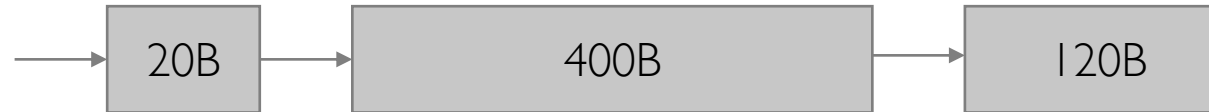
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Binary Search Tree (BST)

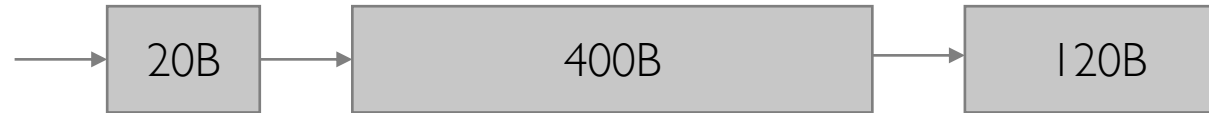
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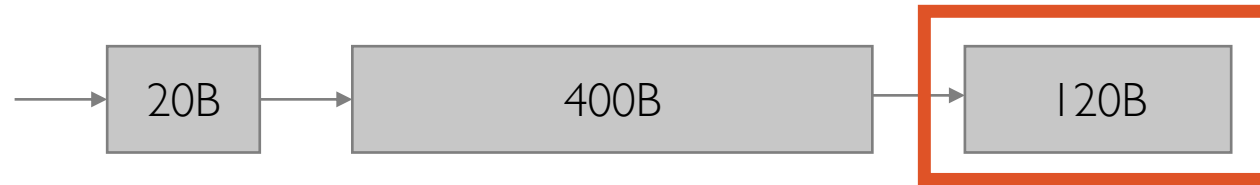
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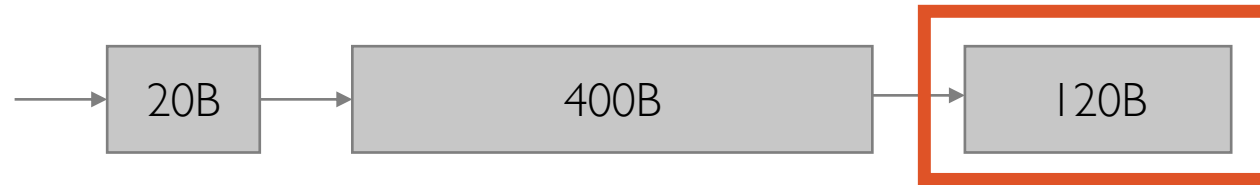
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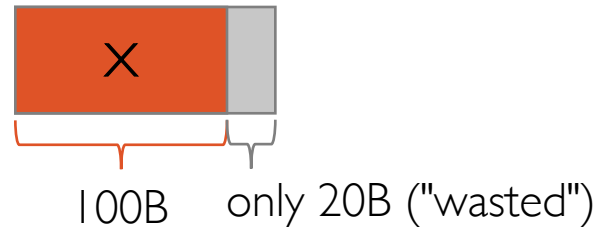
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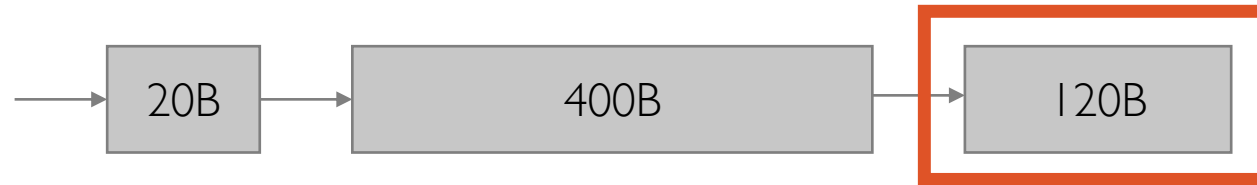


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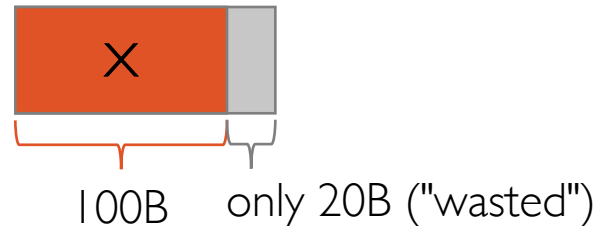


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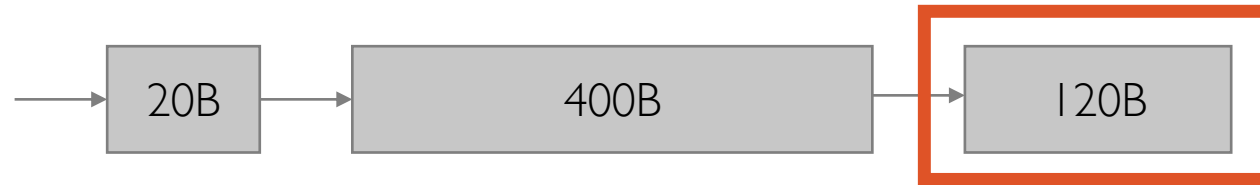
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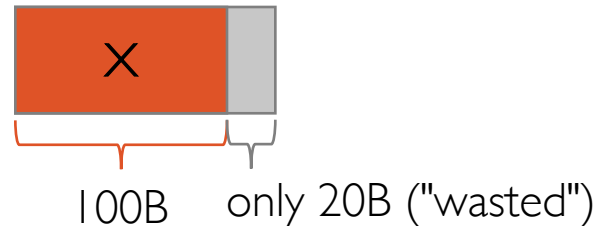
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We can now assign it the second available hole segment (400B)

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- First-Fit is also generally faster than Best-Fit

Fragmentation

Problem

Individual holes may be too small to serve a process request
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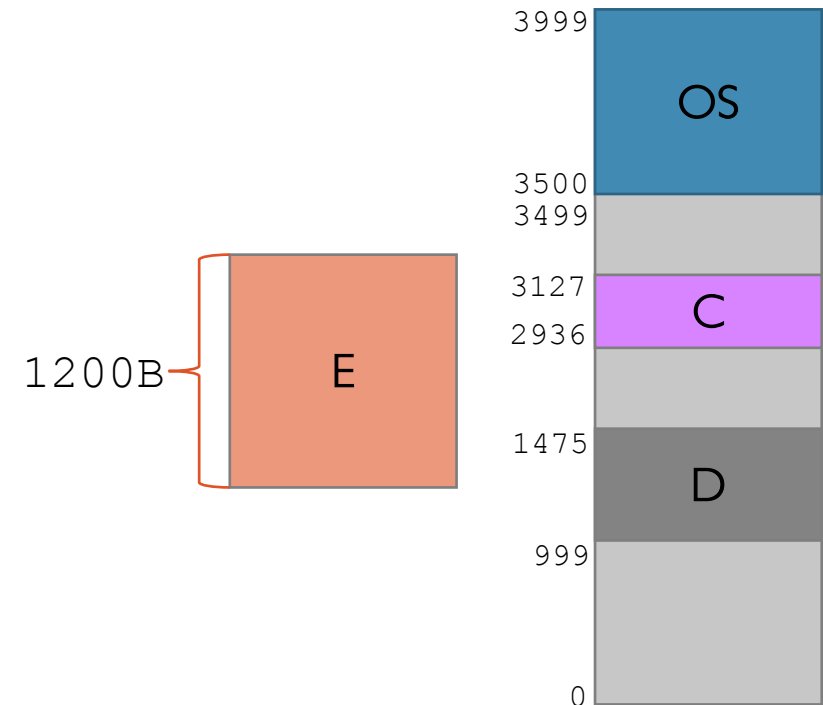
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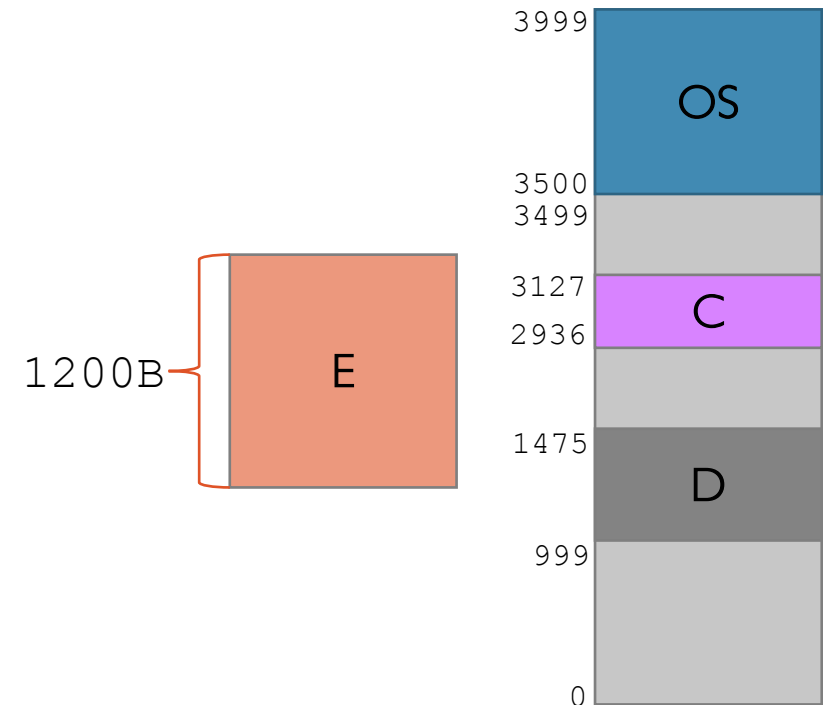


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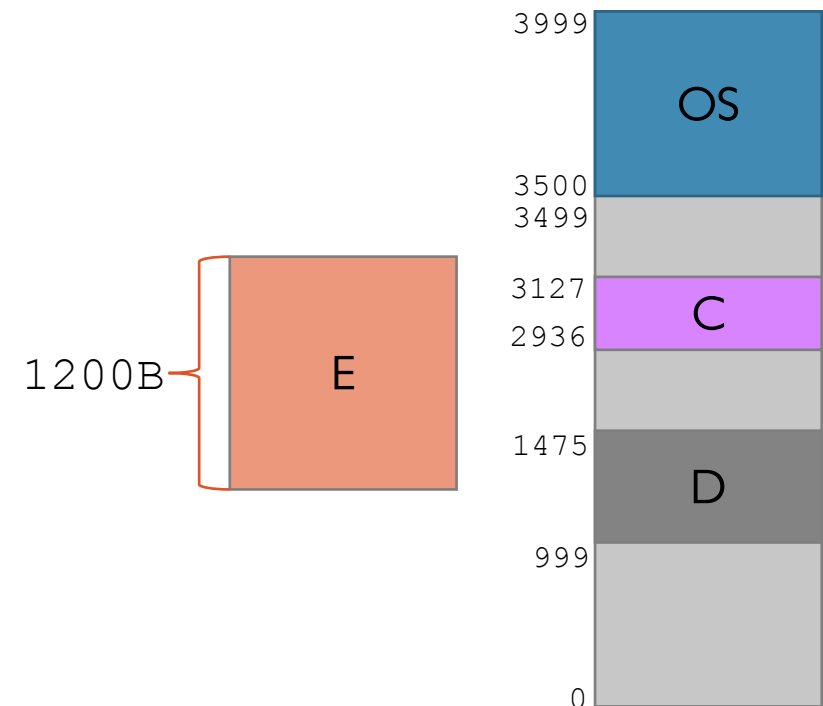
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Goal:

Allocation policy that minimizes wasted space!



Internal Fragmentation

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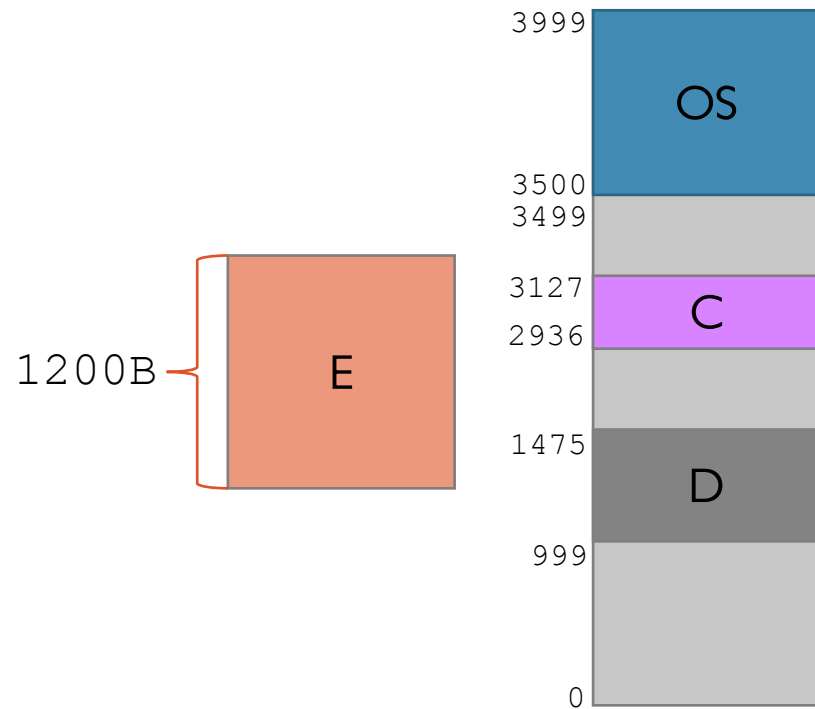
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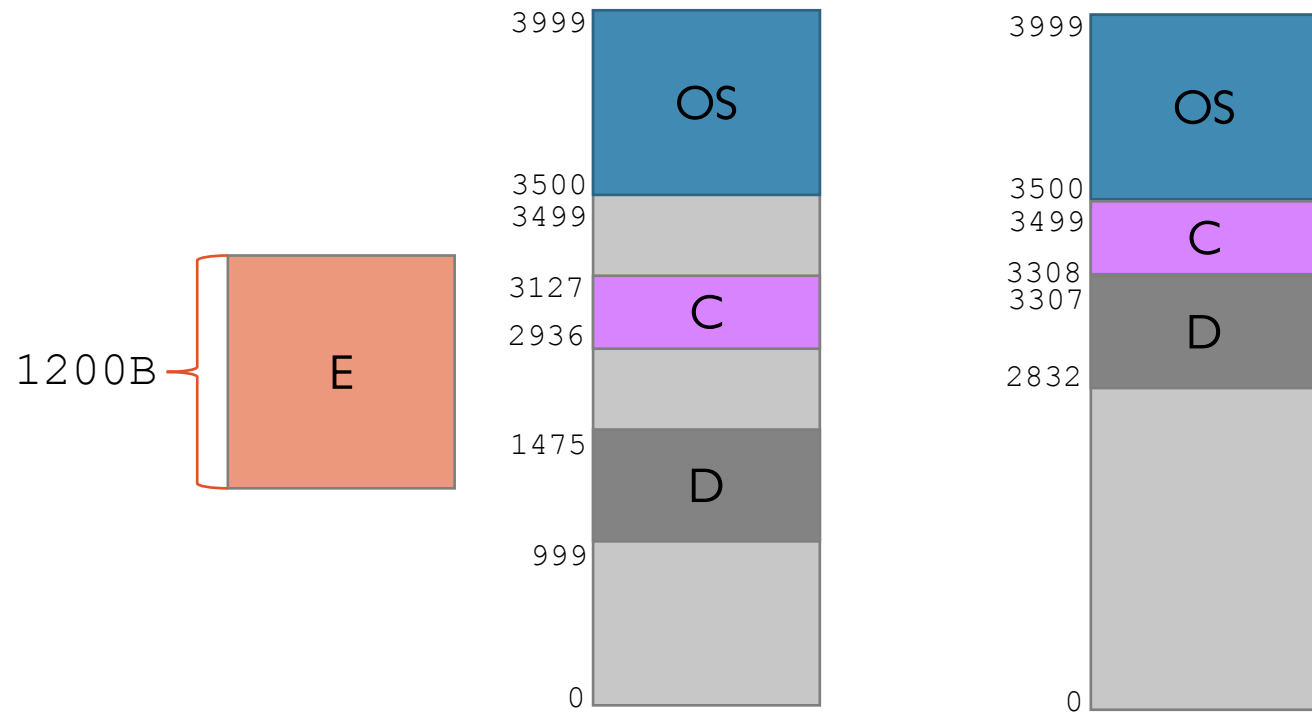
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- It may be much more efficient to allocate the process the whole block (and waste 2B) rather than keep track of a tiny 2B hole

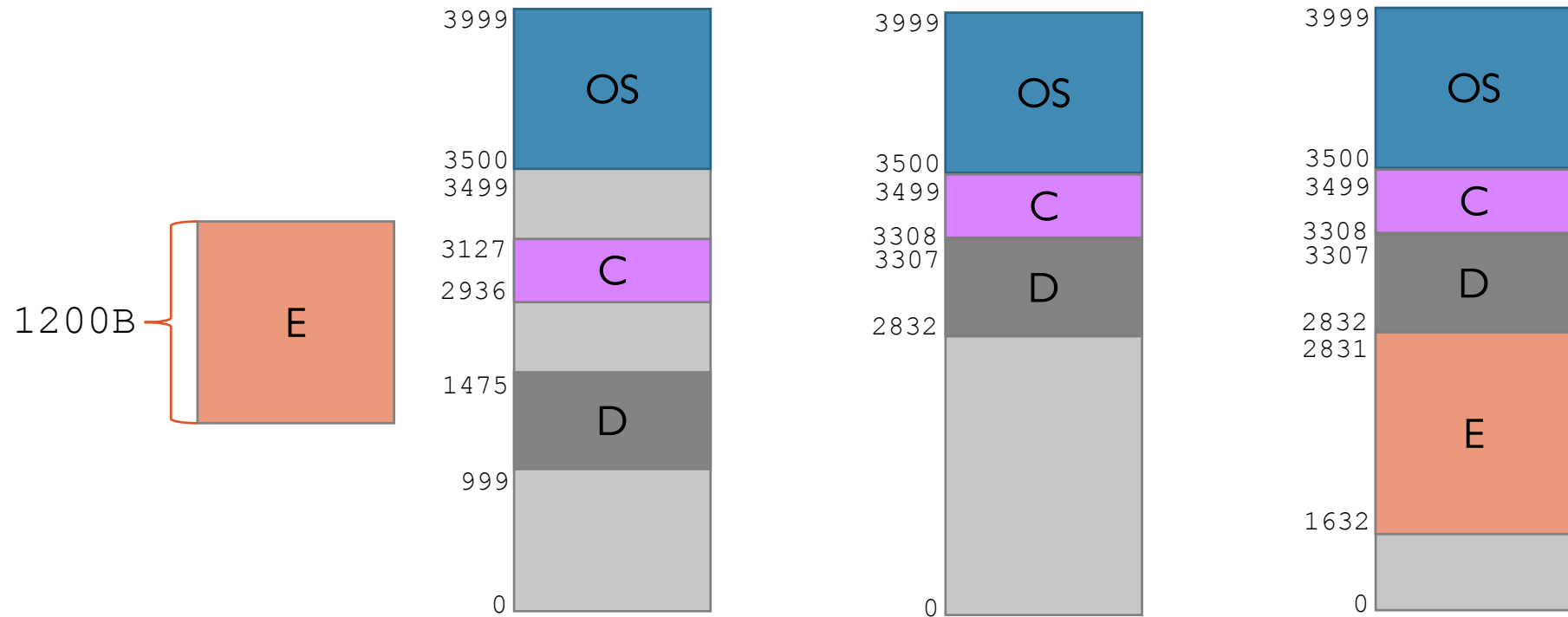
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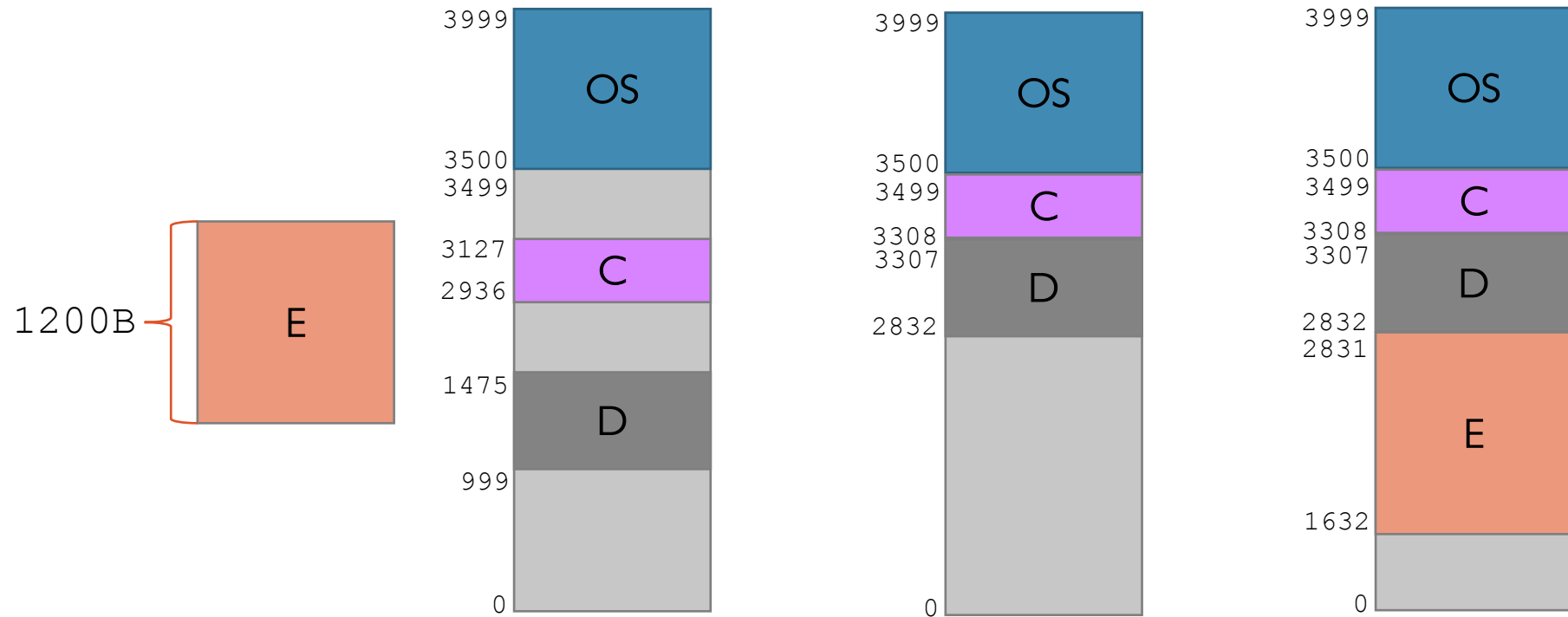
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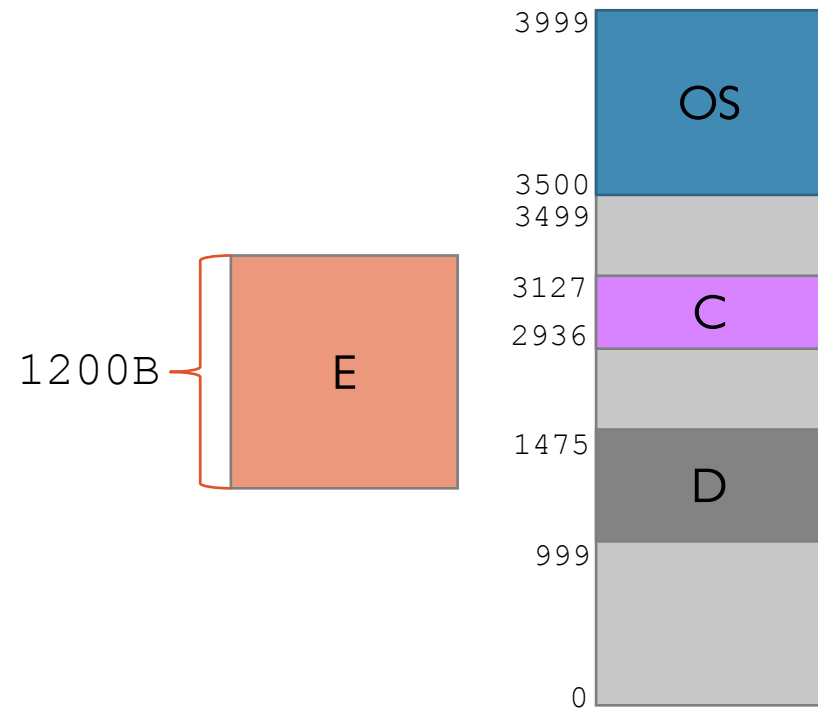


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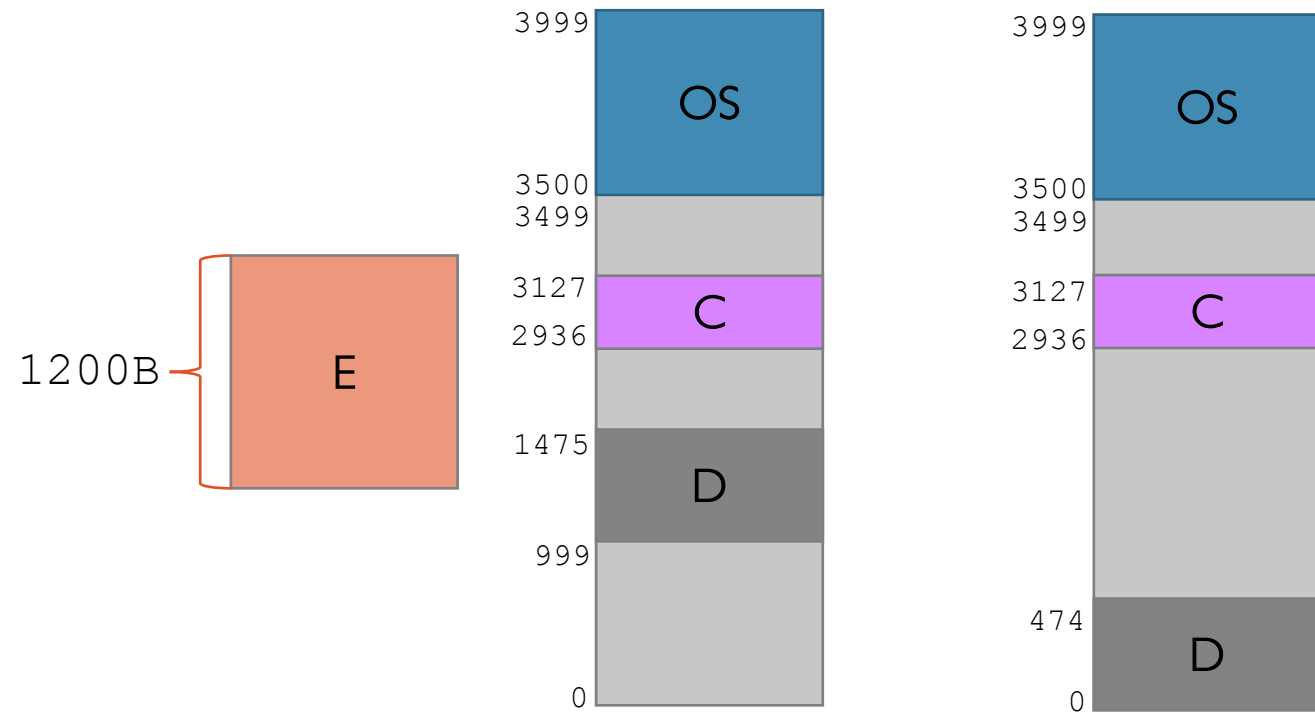


Only one hole is left but two processes need to be moved (C and D)

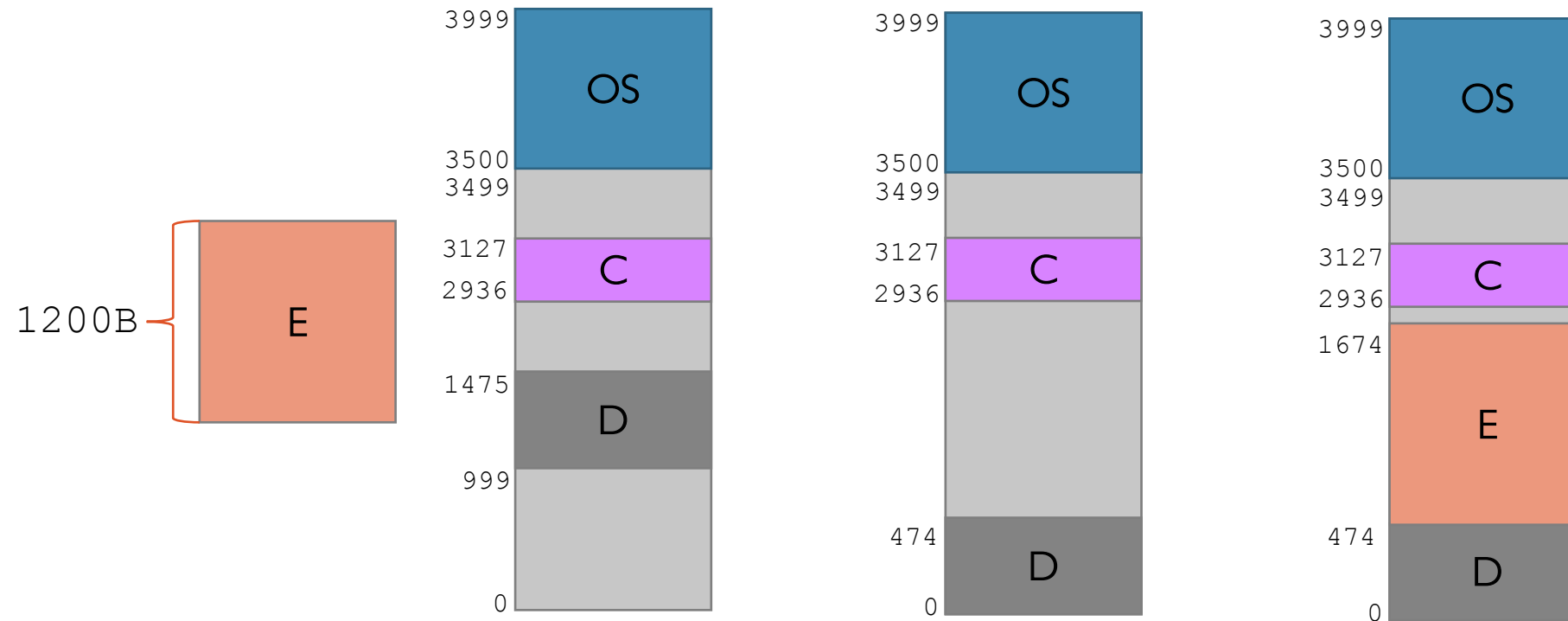
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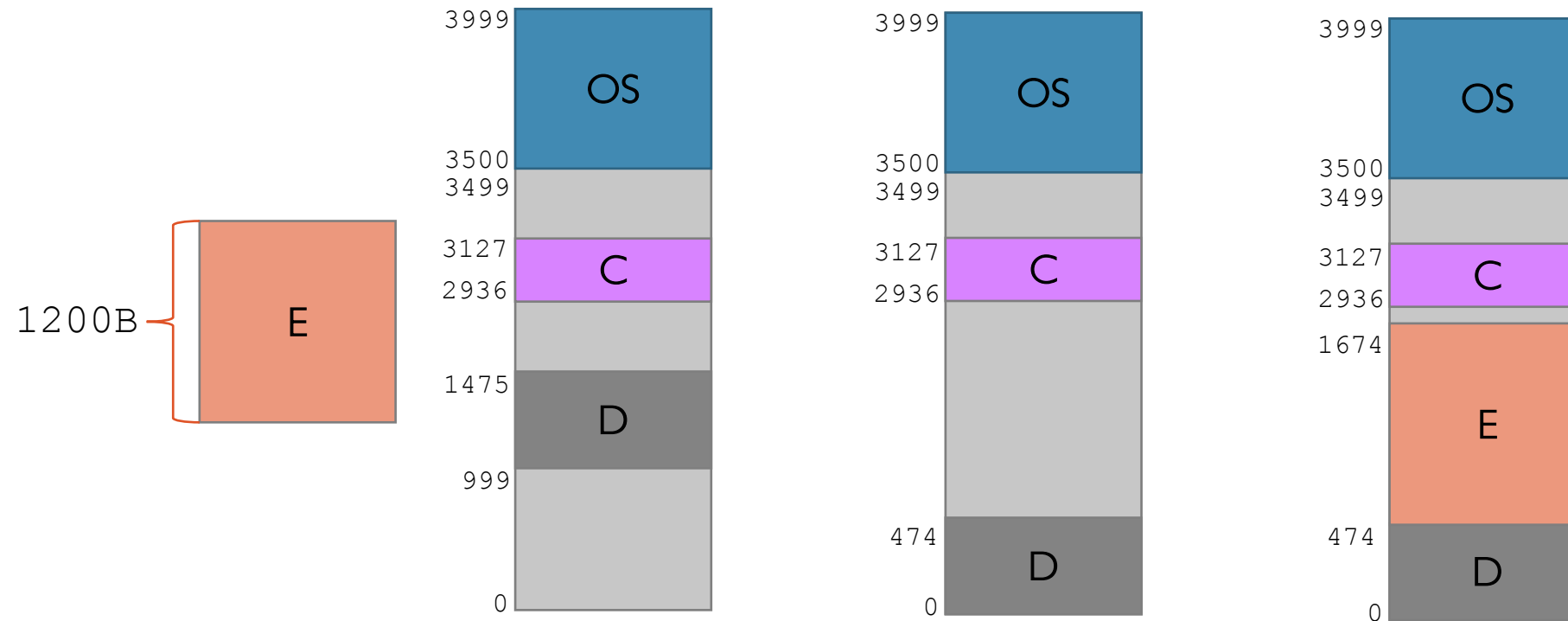
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Still some holes left but only one process is moved (D) rather than two

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- That process can be "swapped out" from memory to disk to make room for other processes

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- Using swapping, fragmentation can be tackled easily
 - Just run compaction before swapping-in a process

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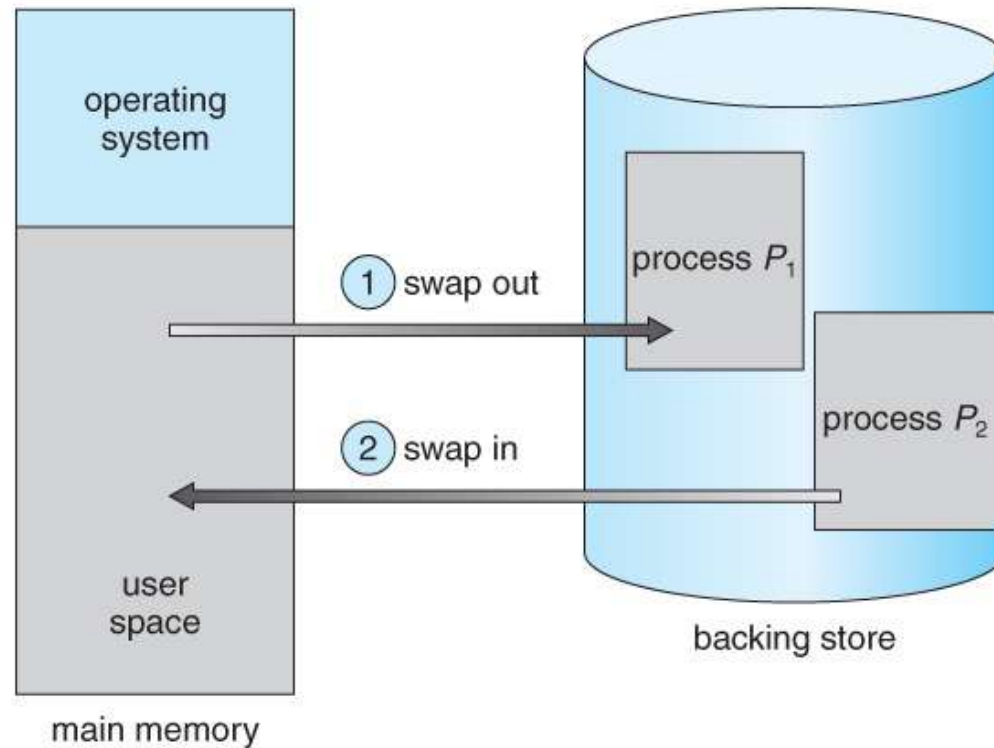
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- Time slice is usually way smaller than that!

Swapping



Most modern OSs no longer use swapping, because it is too slow and there are faster alternatives available (e.g., **paging**)

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- Process entirely loaded
 - Swapping helps but it may be too inefficient

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90/10 Rule

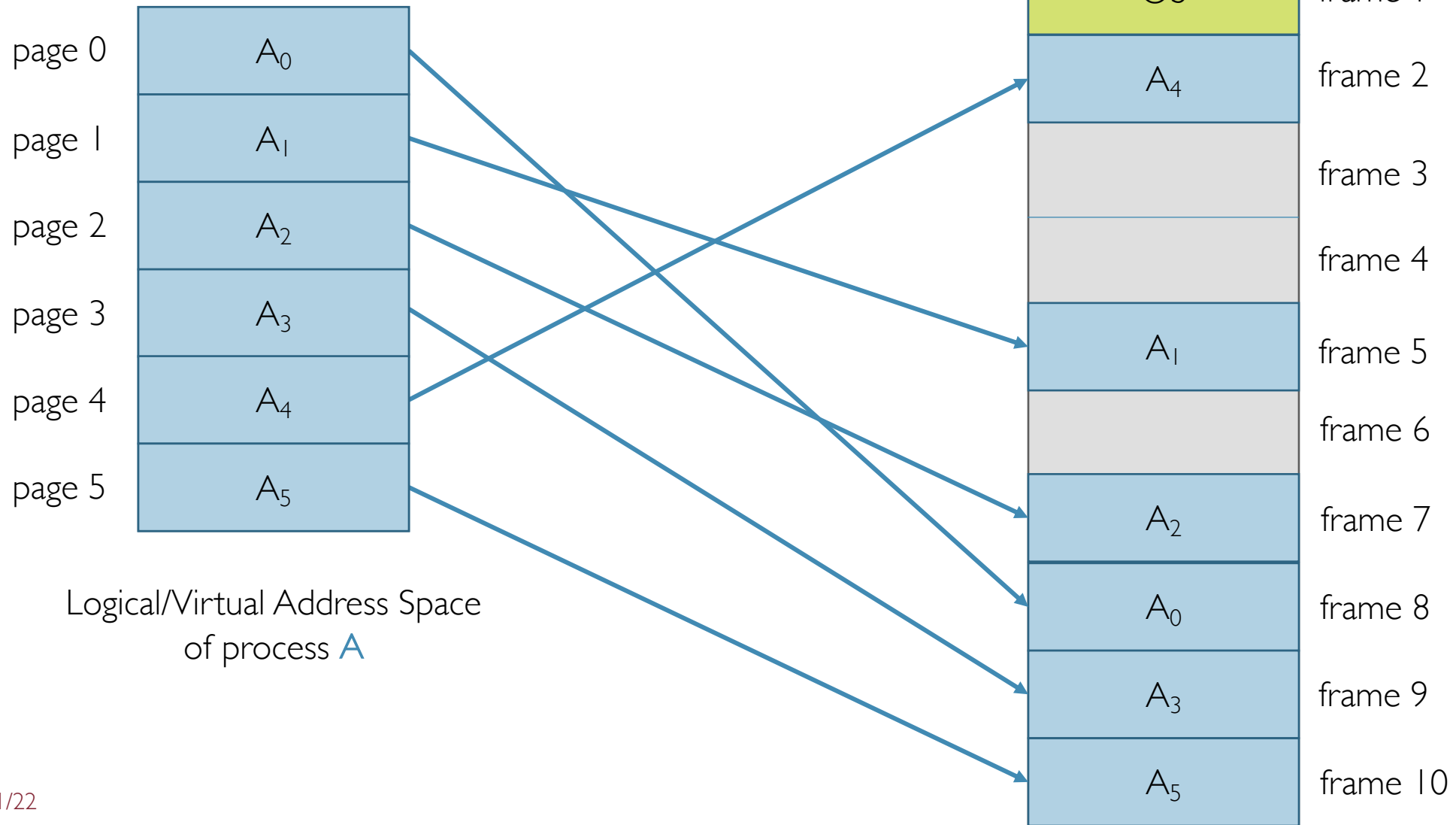
Processes spend **90%** of their time accessing only **10%** of their allocated memory space

Paging: The Big Picture

page 0	A_0
page 1	A_1
page 2	A_2
page 3	A_3
page 4	A_4
page 5	A_5

Logical/Virtual Address Space
of process A

Paging: The Big Picture



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 - Remember, memory addresses are referenced all the time
- OS needs dedicated support for doing it → Page Table

Page Table: Mapping Pages to Frames

0	A_0
1	A_1
2	A_2
3	A_3
4	A_4
5	A_5

OS	0
OS	1
A_4	2
	3
	4
A_1	5
	6
A_2	7
A_0	8
A_3	9
A_5	10

Page Table: Mapping Pages to Frames

Lookup table to efficiently retrieve what frame a page is stored in

0	A_0
1	A_1
2	A_2
3	A_3
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5	A_5

Page	Frame
0	8
1	5
2	7
3	9
4	2
5	10

OS	0
OS	1
A_4	2
	3
	4
A_1	5
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A_2	7
A_0	8
A_3	9
A_5	10

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0	A ₀	Page	Frame	OS	0
1	A ₁	0	8	OS	1
2	A ₂	1	5	A ₄	2
3	A ₃	2	7		3
4	A ₄	3	9		4
5	A ₅	4	2	A ₁	5
		5	10		6
				A ₂	7
				A ₀	8
				A ₃	9
				A ₅	10

So far, we have simply assumed **all** pages of a process is mapped to physical frames, but we will see this is not always the case

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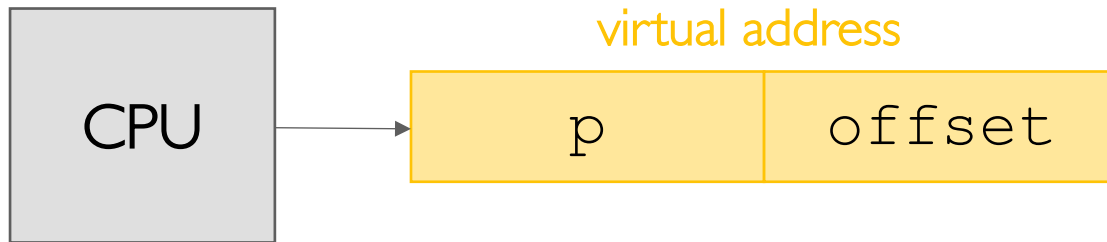
Page Table: Virtual to Physical Address

- Processes use virtual (logical) addresses to refer to memory (not page number!)
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Page Table: Virtual to Physical Address

virtual address consists of 2 parts:

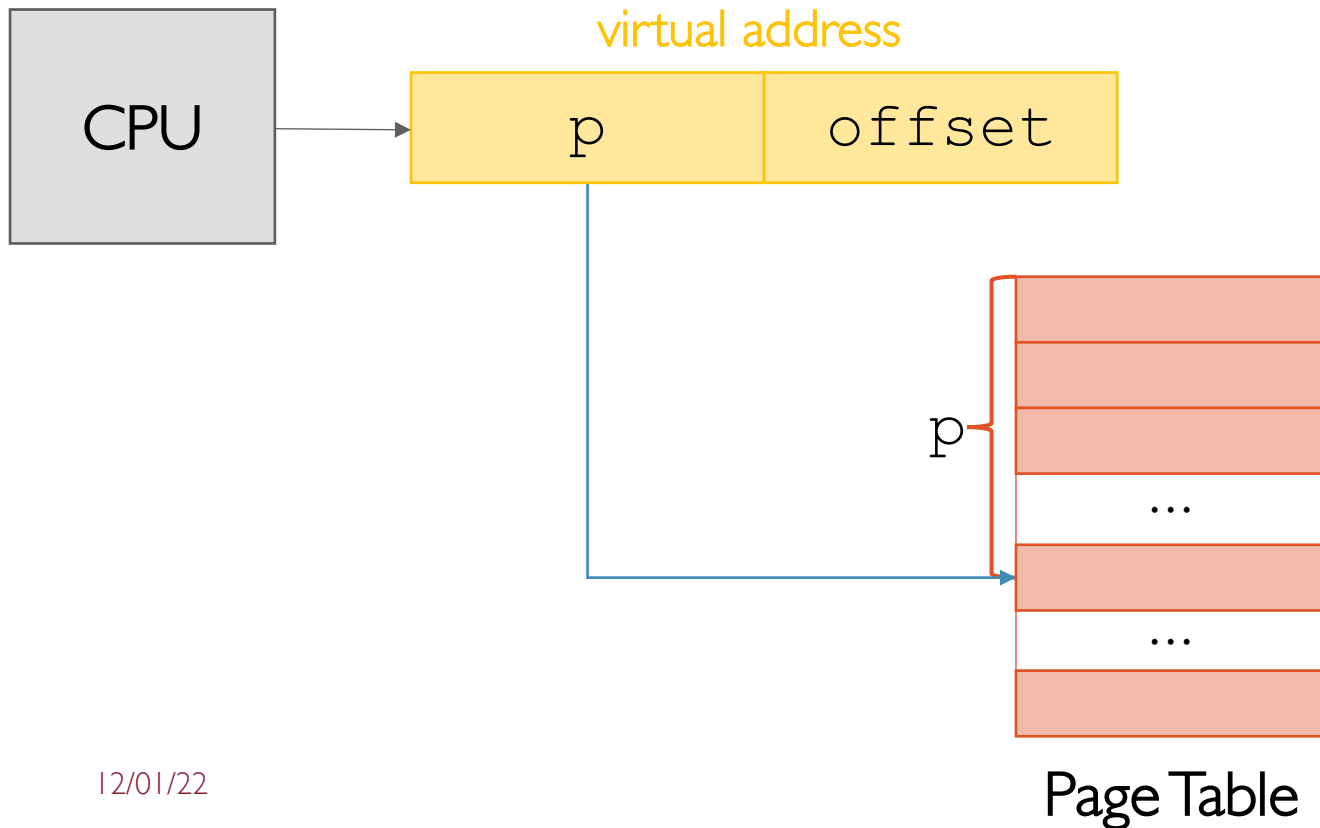
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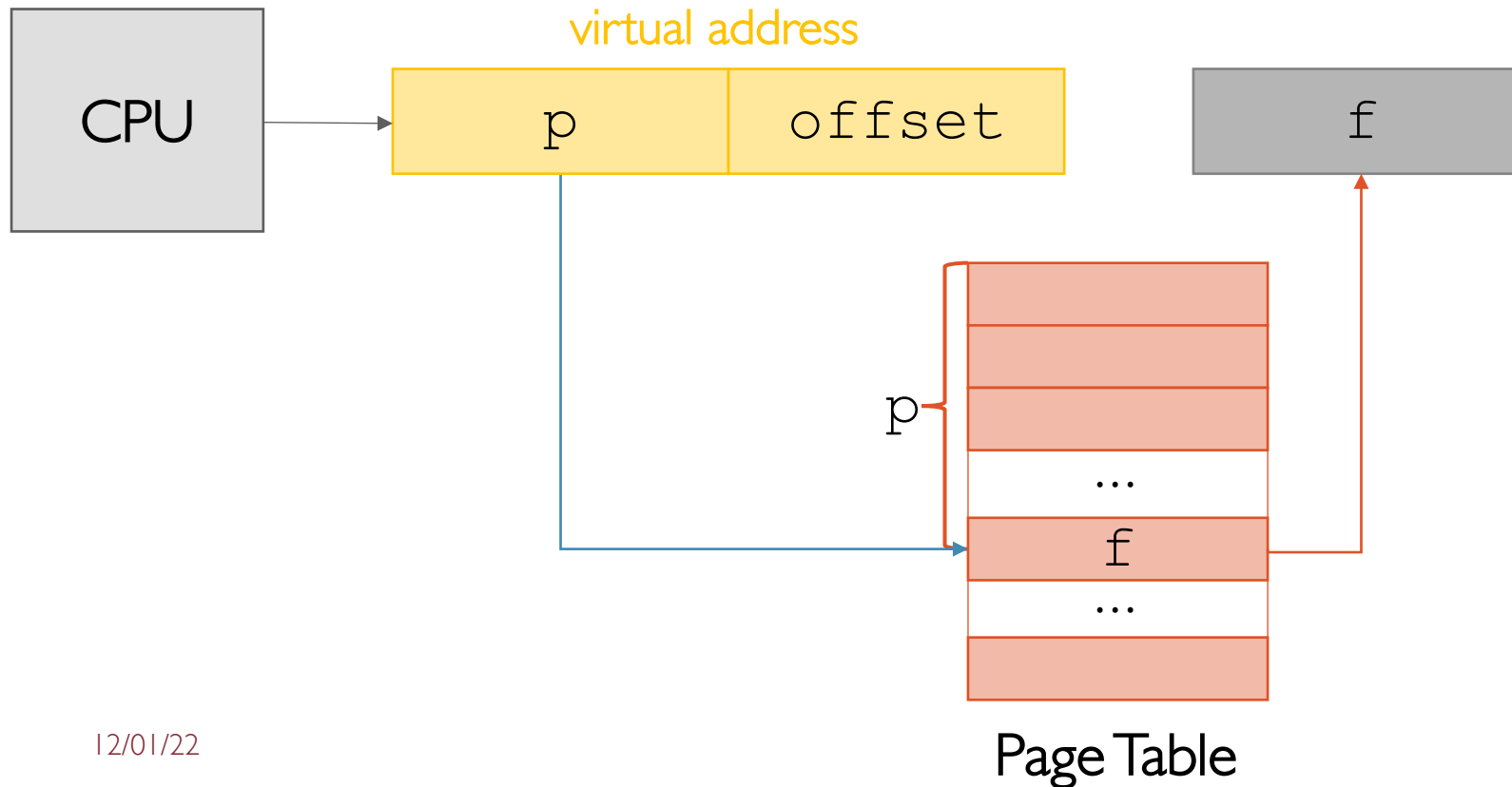
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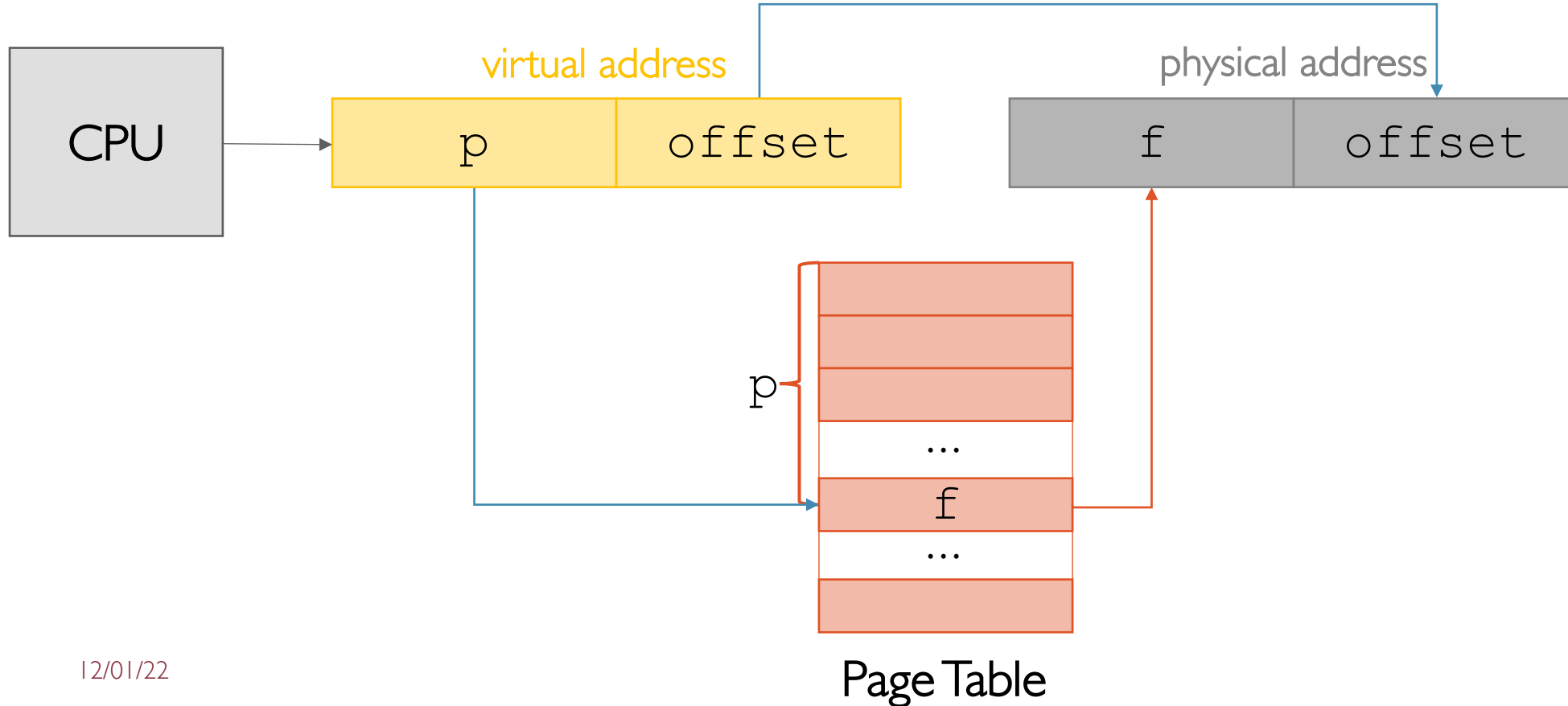
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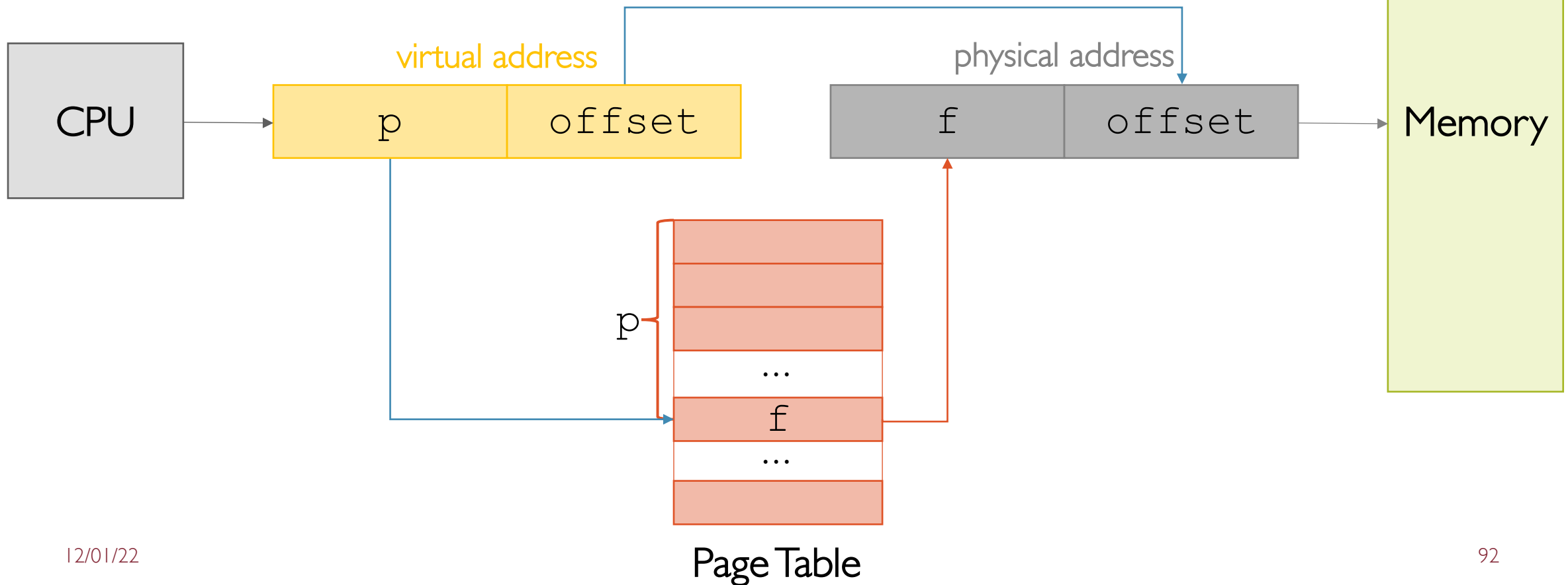
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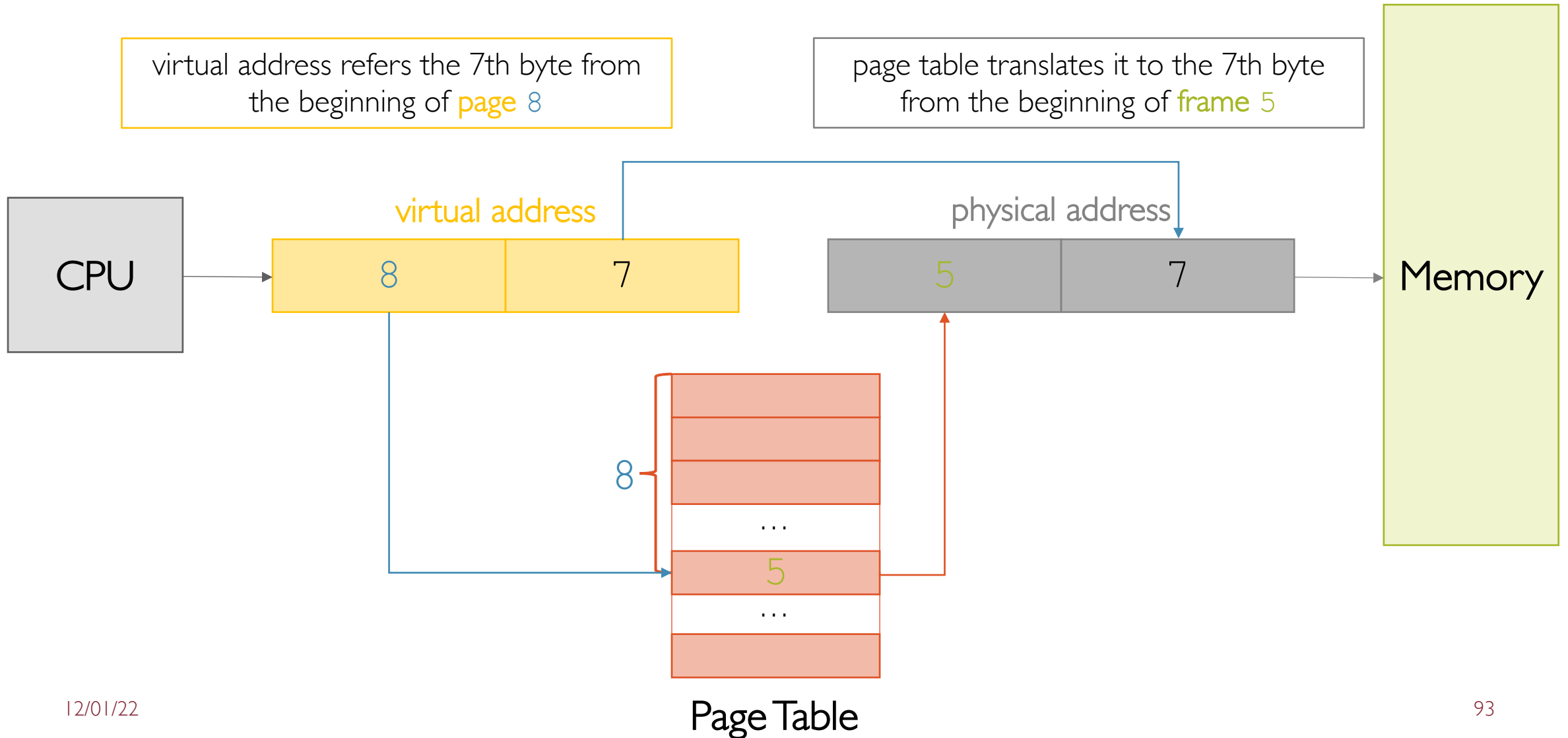
- p: page number where the address resides
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physical address also consists of 2 parts:

- f: physical frame number
- offset: as above



Page Table: Example of Address Translation



Paging as Dynamic Relocation

- Paging is a form of dynamic relocation
- Each virtual address is bound by the page table to a physical address
- Page table can be seen just as a set of base (relocation) registers, one for each frame
- Mapping is invisible to the user process: the OS maintains the page table and translation happens in hardware
- Protection is provided similarly to dynamic relocation (limit register)

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Paging: Steps

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1. Get the page number (**p**) and the **offset** where the virtual address **x** resides
2. Use **p** to index into the page table to retrieve the frame number **f**
3. Combine **f** with **offset** to obtain the physical address **y**

Paging: Get **p** and **offset** from **x**

Suppose we have **50B** of physical memory available for user processes

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Address translation requires a **div** and a **mod** operation

Paging: Implementation Details

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Why?

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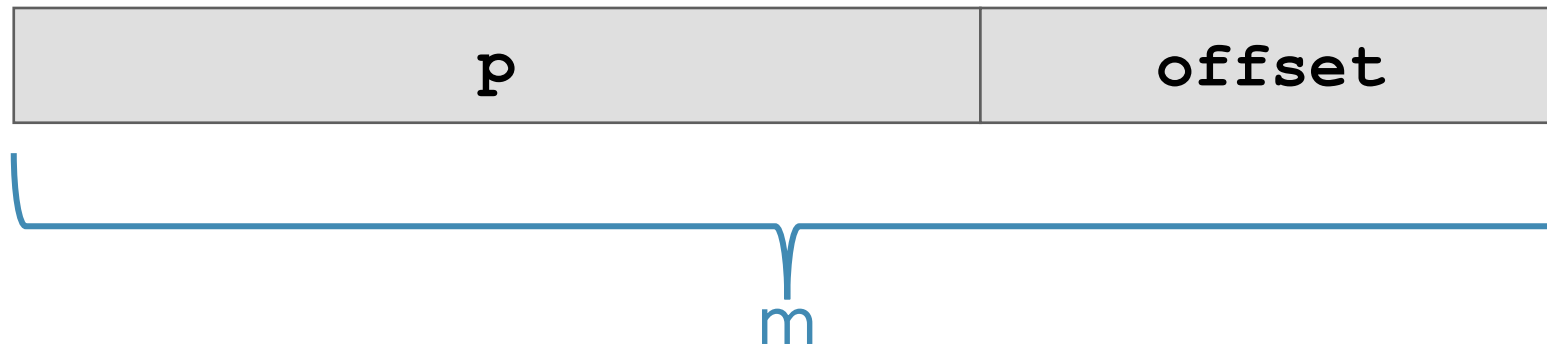
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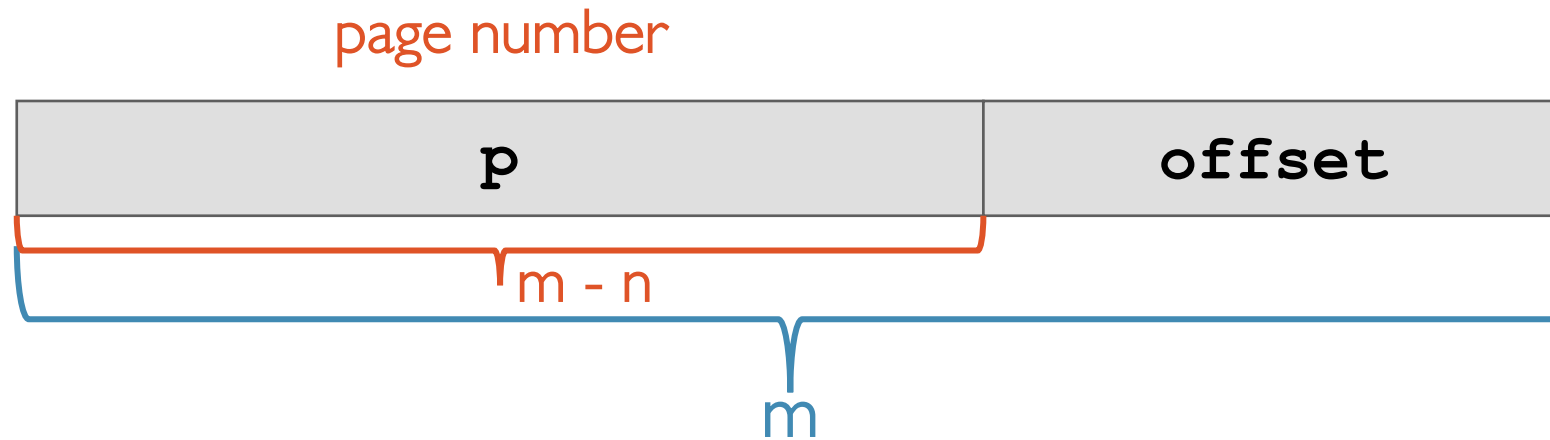
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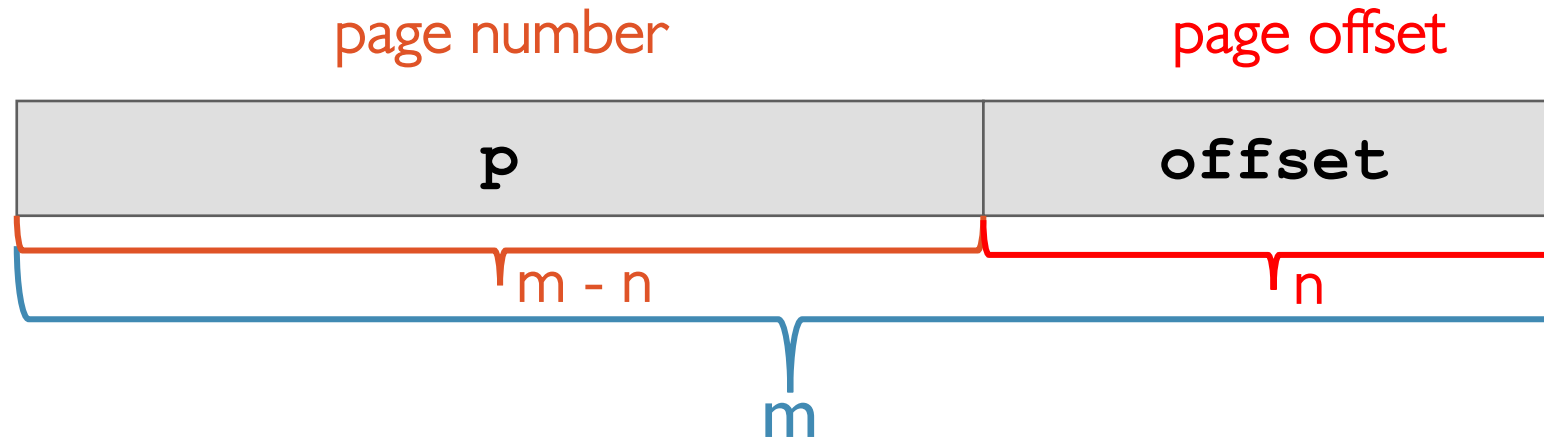
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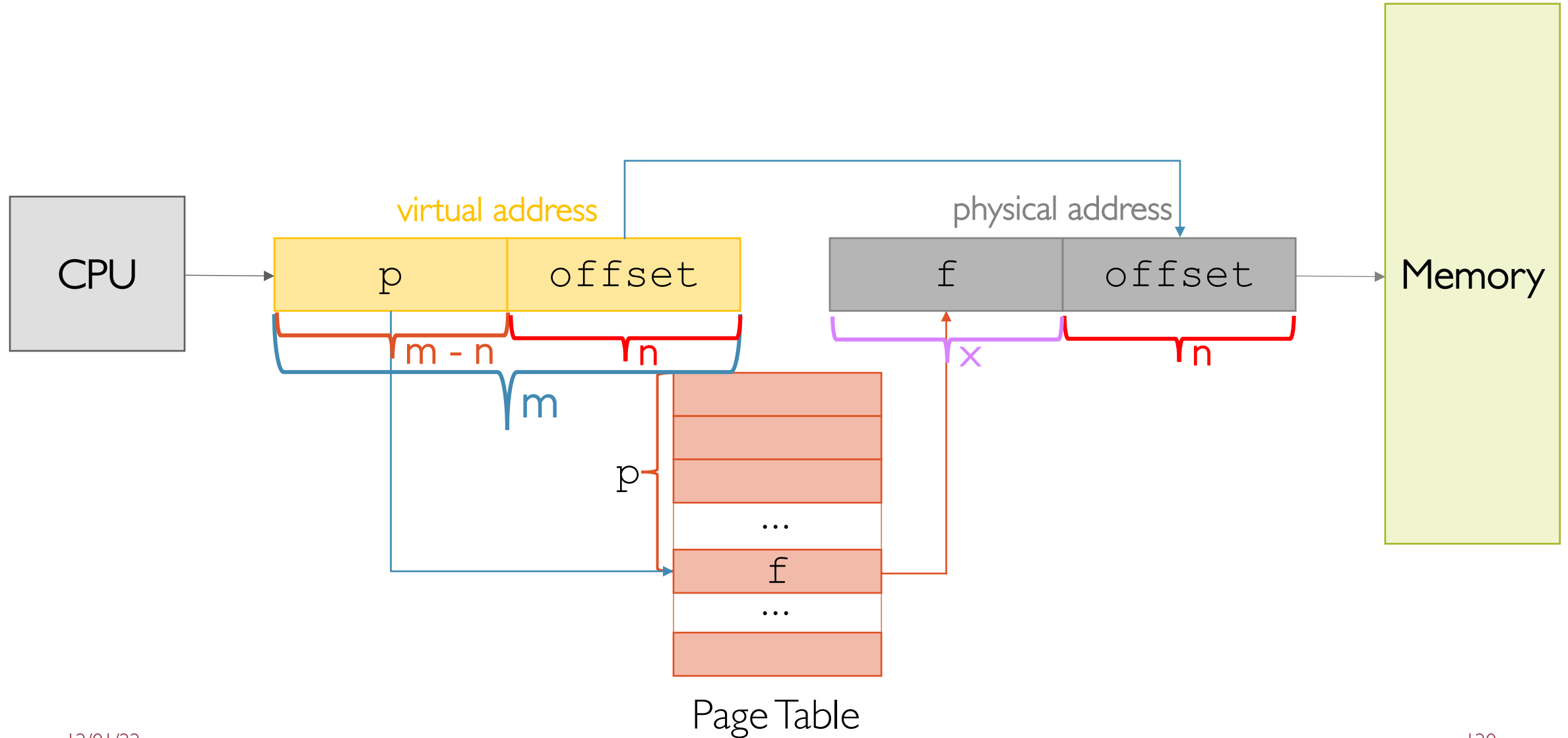
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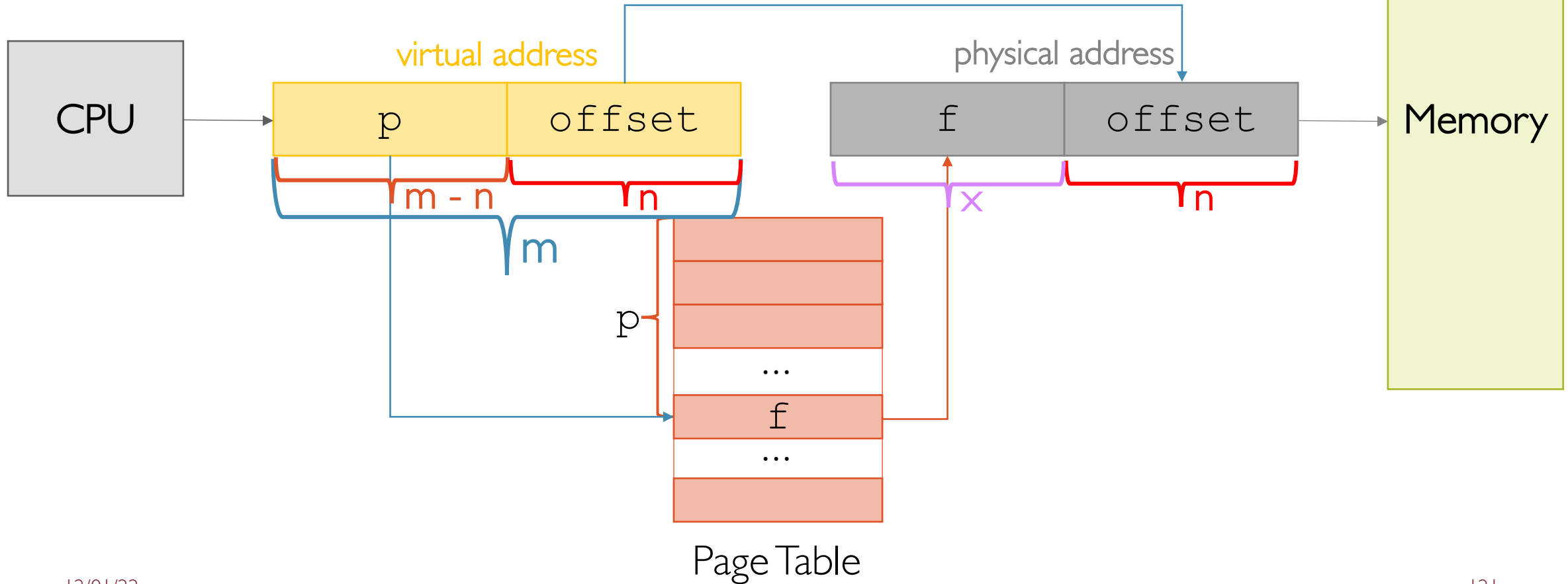
Paging: Practical Details



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NOTE

$m-n$ doesn't necessarily have to be equal to x



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- Typical values of page/frame sizes is $n = 12$ bits
 - That means each page/frame is $2^{12} = 4\text{KiB}$
- Assuming $m = 32$ bits, there are $2^{m-n} = 2^{20} = \sim 1\text{M}$ pages/frames
 - That means page table has 2^{20} entries (i.e., one for each page/frame)

Paging: Practical Example

Suppose we have a virtual memory and a physical memory, both of size $M = 1024\text{B}$ (1 KiB)

Q1

How many bits are needed for a virtual/physical address (assuming single-byte addressing)

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R1

10 bits to address $M = 1024$ bytes (both for virtual and physical address)

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Q2

How big is the page table? (i.e., how many pages/entries does it have to index?)

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R2

$$T = M / S = 1024 \text{ memory bytes} / 16 \text{ bytes per page} = 64 \text{ pages}$$

Paging: Practical Example

Q3

What is `p` and `offset` (i.e., how many bits for `p` and `offset`?)

Paging: Practical Example

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What is p and `offset` (i.e., how many bits for p and `offset`?)

R3

Our logical address is made of $m = 10$ bits

$n = 4$ bits are used to represent the `offset`, as each page/frame is $S = 16$ bytes

$m - n = 6$ bits are used to represent page number p , as there are $T = 64$ pages

Paging: Practical Example

Q4

Translate the virtual address $x = 42$, assuming the following page table

page	frame
0	12
1	5
2	37
3	0
...	..
63	29

Paging: Practical Example

Q4

Translate the virtual address $x = 42$, assuming the following page table

page	frame
0	12
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2	37
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R4

$$p = x \text{ div } S = 42 \text{ div } 16 = 2$$

Paging: Practical Example

Q4

Translate the virtual address $x = 42$, assuming the following page table

page	frame
0	12
1	5
2	37
3	0
...	..
63	29

R4

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Q4

Translate the virtual address $x = 42$, assuming the following page table

page	frame
0	12
1	5
2	37
3	0
...	..
63	29

R4

$p = x \text{ div } S = 42 \text{ div } 16 = 2$
 $\text{offset} = x \text{ mod } S = 42 \text{ mod } 16 = 10$
10th byte from the beginning of frame 37

Paging: Practical Example 2

Suppose we still have a virtual memory and a physical memory, both of size $M = 1024B$

Q1

So far, we have assumed that computers work on single-byte (i.e, 8-bit architecture)
Modern computers however operate natively on multiple of bytes (i.e., **words**) rather than single-byte. Typical values of word length is: 16, 32 or 64 bits.

If we assume 32-bit architecture (i.e., word = 32 bits = 4 bytes), virtual addresses refer to words instead of bytes

How many bits are therefore needed to address the number of words available on M?

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How many bits are therefore needed to address the number of words available on M?

R1

8 bits to address $M = 1024/4 = 256$ 4-byte **words** (both for virtual and physical address)

Paging: Practical Example 2

Now, assume we still use paging with page/frame size $S = 16B$

Q2

How big is the page table? (i.e., how many pages/entries does it have to index?)

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Q2

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R2

$$T = M / S = 1024 \text{ memory bytes} / 16 \text{ bytes per page} = 64 \text{ pages}$$

Paging: Practical Example 2

Q3

What is `p` and `offset` (i.e., how many bits for `p` and `offset`?)

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Q3

What is p and `offset` (i.e., how many bits for p and `offset`?)

R3

Our logical address is now made of $m = 8$ bits

$n = 2$ bits are used to represent the `offset`, as each page/frame is:

$S = 16$ bytes = $4 * 4$ -byte words

$m - n = 6$ bits are used to represent page number p , as there are still $T = 64$ pages

Paging: Practical Example 2

Q4

Translate the virtual address $x = 7$, assuming the following page table

page	frame
0	12
1	5
2	37
3	0
...	..
63	29

Paging: Practical Example 2

Q4

Translate the virtual address $x = 7$, assuming the following page table

page	frame
0	12
1	5
2	37
3	0
...	..
63	29

Remember: now virtual address refers to a 4-byte word!

Paging: Practical Example 2

Q4

Translate the virtual address $x = 7$, assuming the following page table

page	frame
0	12
1	5
2	37
3	0
...	..
63	29

$S = 16 \text{ bytes} = 4 * 4\text{-byte words}$
Must be expressed in terms of
number of words

R4

$$p = x \text{ div } S = 7 \text{ div } 4 = 1$$

Paging: Practical Example 2

Q4

Translate the virtual address $x = 7$, assuming the following page table

page	frame
0	12
1	5
2	37
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R4

$$p = x \text{ div } S = 7 \text{ div } 4 = 1$$

$$\text{offset} = x \text{ mod } S = 7 \text{ mod } 4 = 3$$

3rd word from the beginning of frame 5

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- Trade-off solution: **Translation Look-aside Buffer (TLB)**

Appendix: Registers and Main Memory

- All memory accesses are equivalent: the memory hardware doesn't know what a particular part of memory is being used for
- CPU can only access its registers and main memory (any access to other devices, e.g., hard drive, requires data to be moved into main memory first)
- Access to registers is very fast, generally one clock cycle
- Access to main memory is comparatively slow, and may take several clock cycles to complete

Appendix: Cache Memory

- Bridge the gap between fast registers and slower main memory
- **Cache Memory:** on-chip (thereby, fast!) intermediary memory built into most modern CPUs
- Several chunks of memory transferred from main memory to the cache
- Access individual memory locations one at a time from the cache rather than from memory directly

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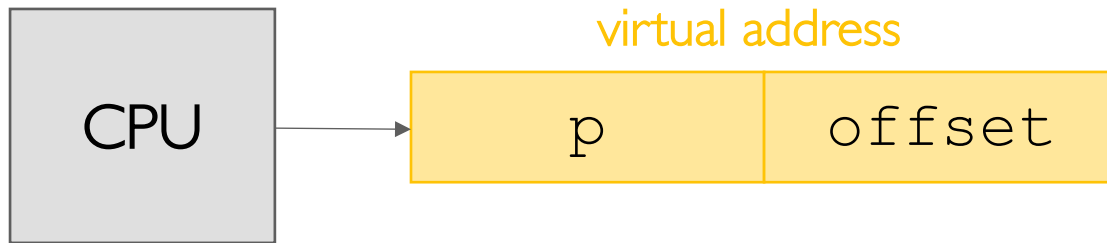
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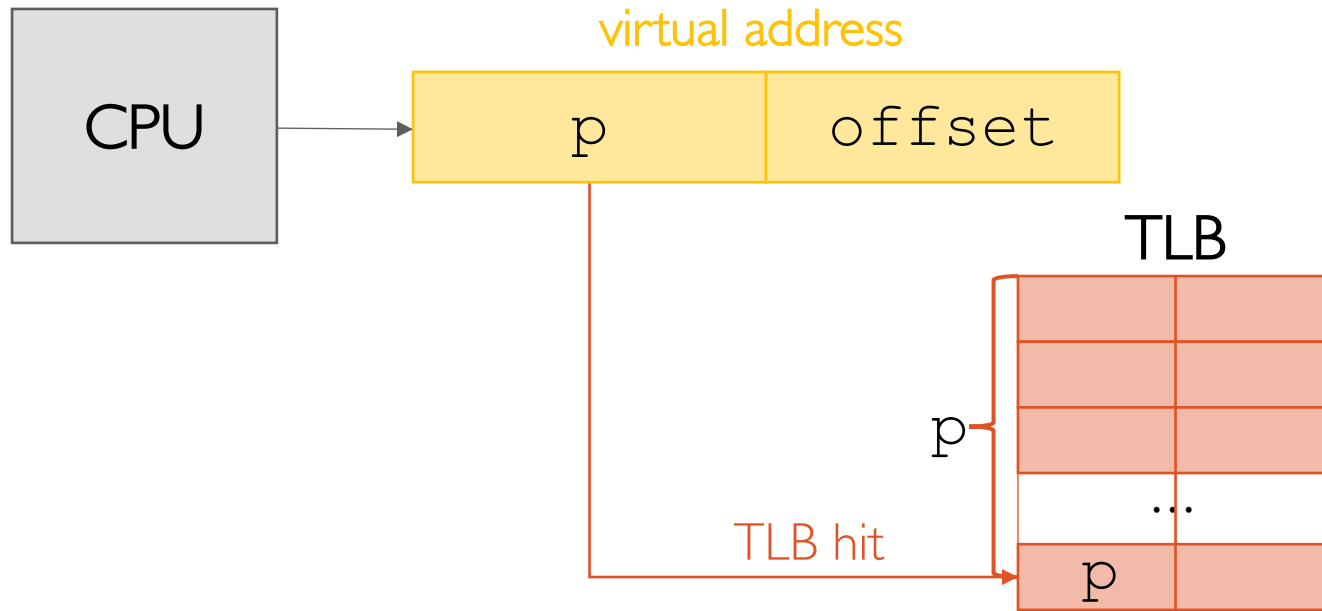
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- Typical TLB sizes range from 8 to 2048 entries

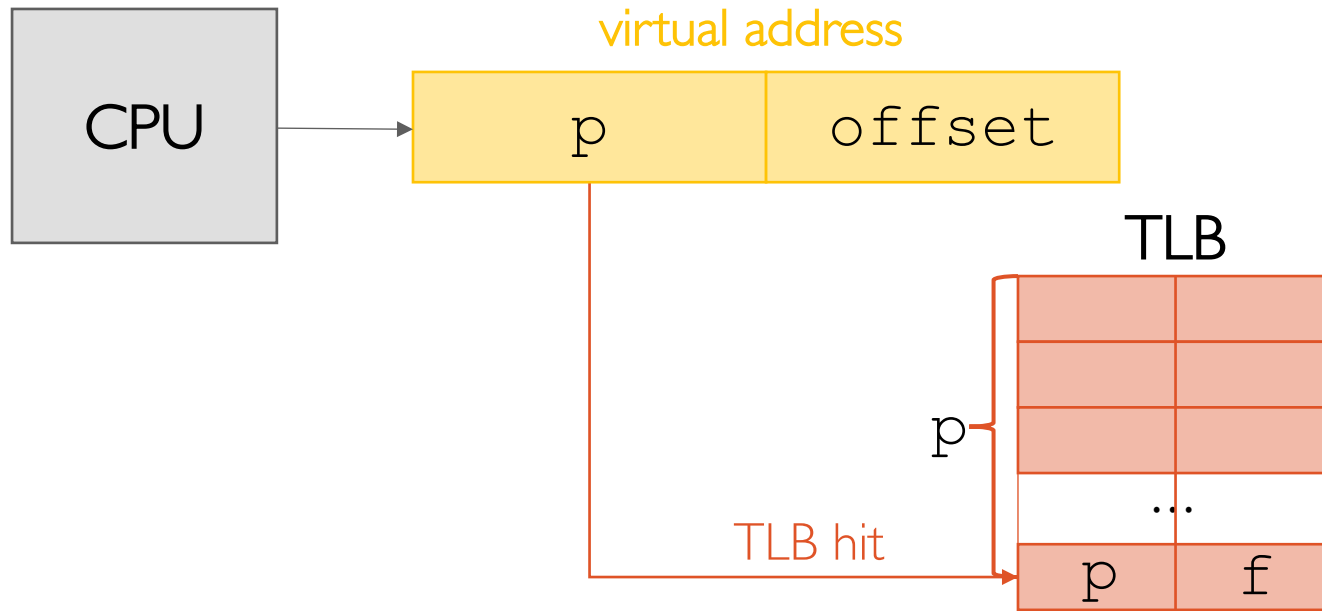
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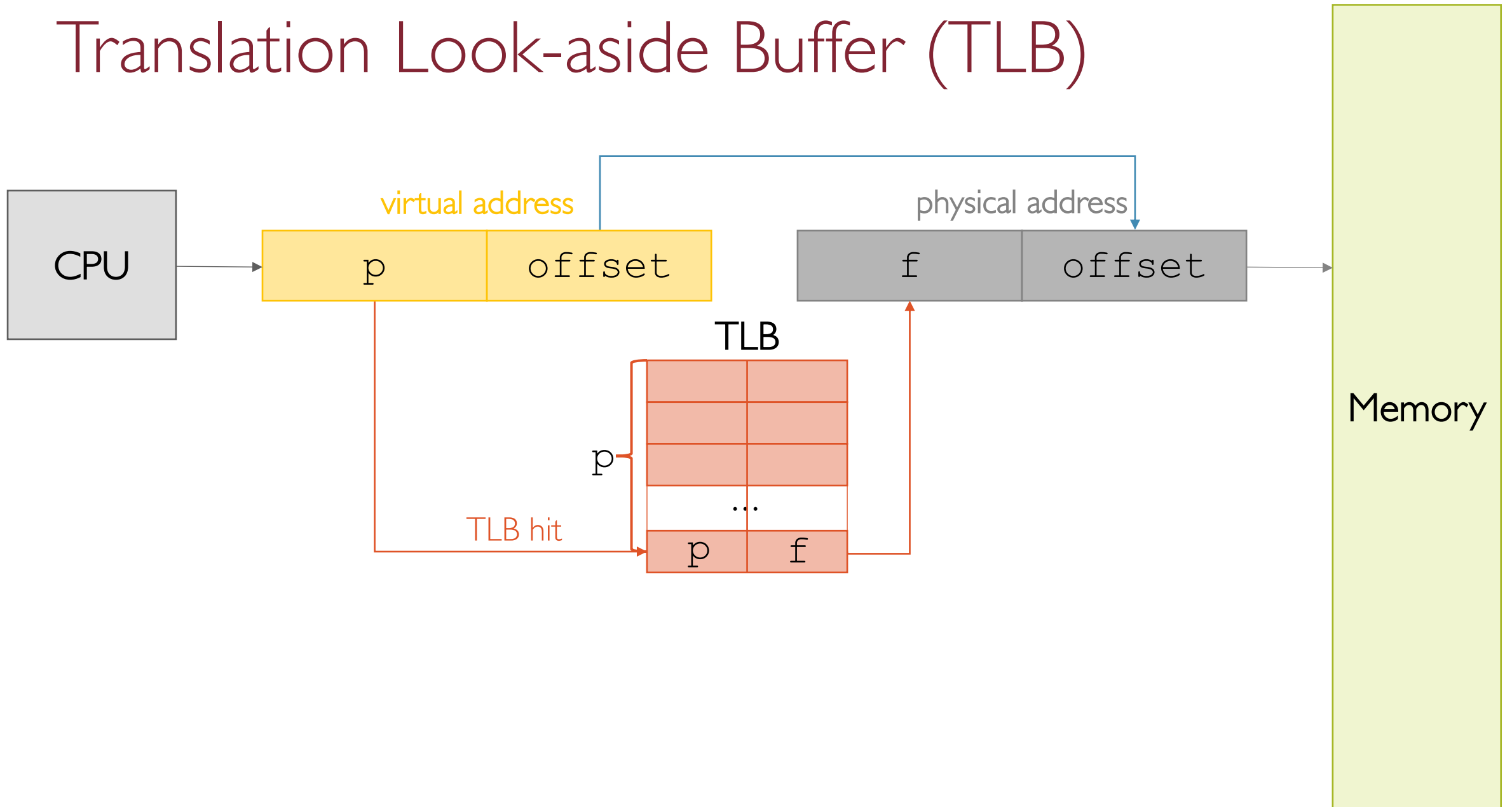
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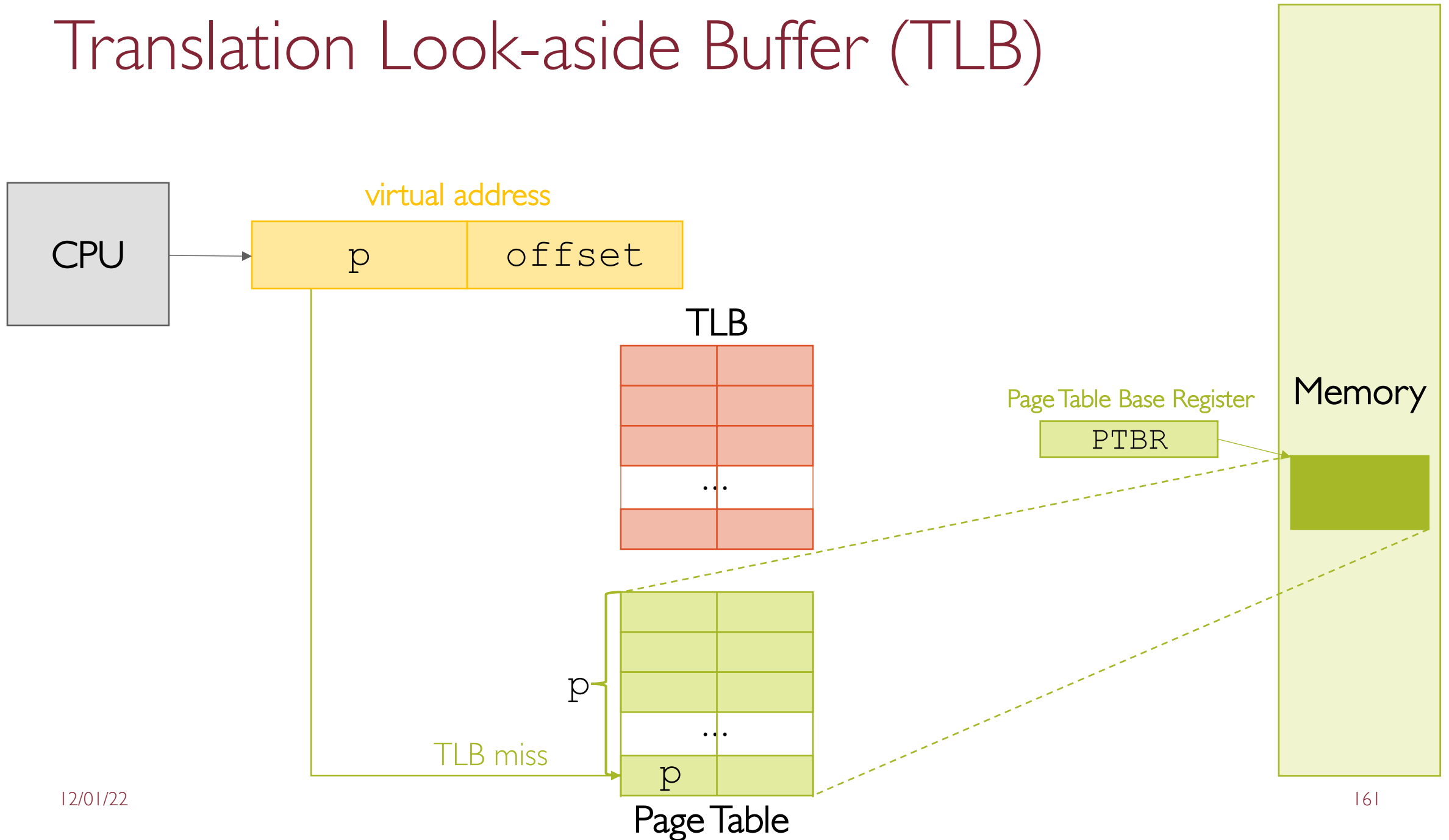
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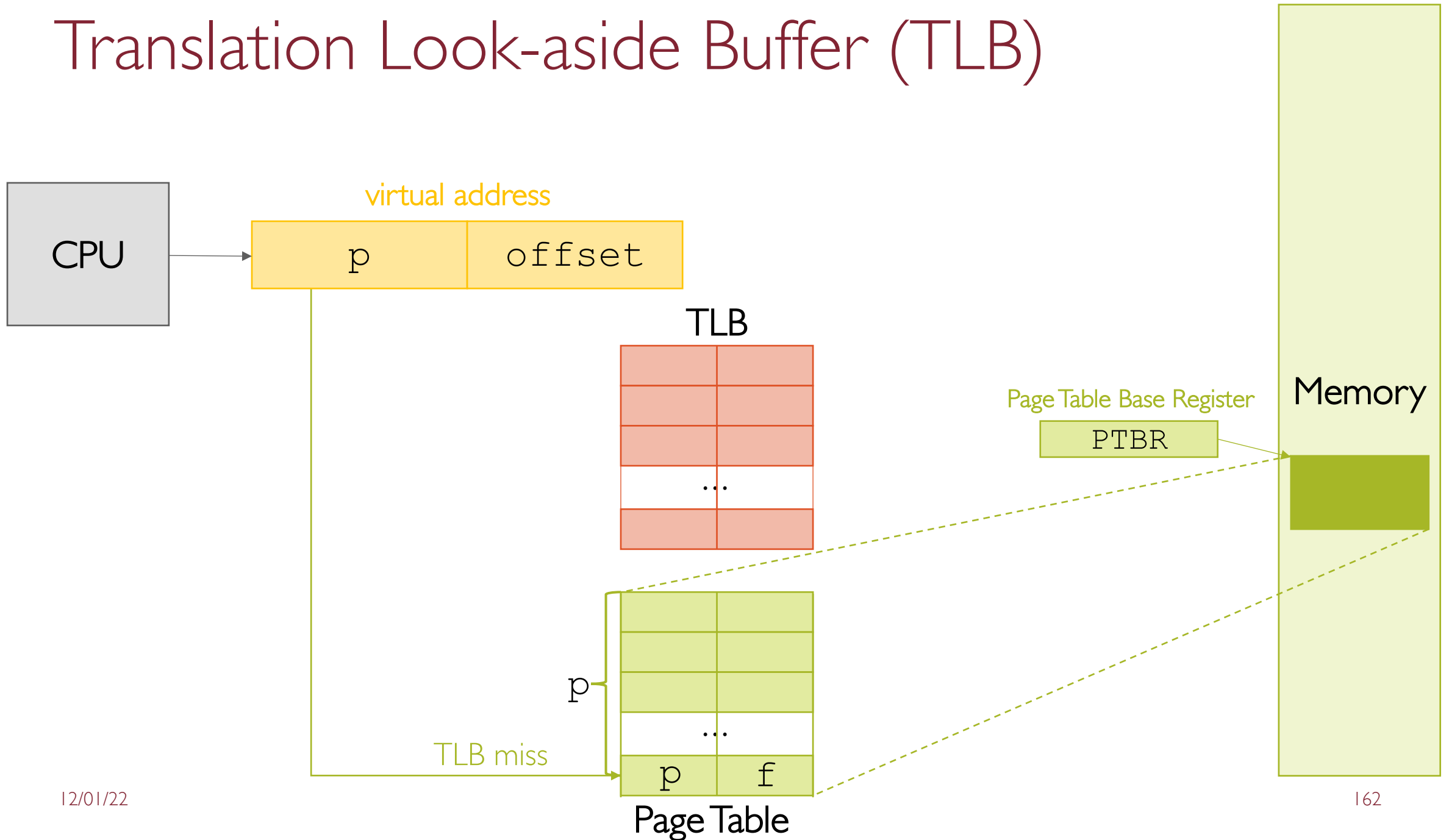
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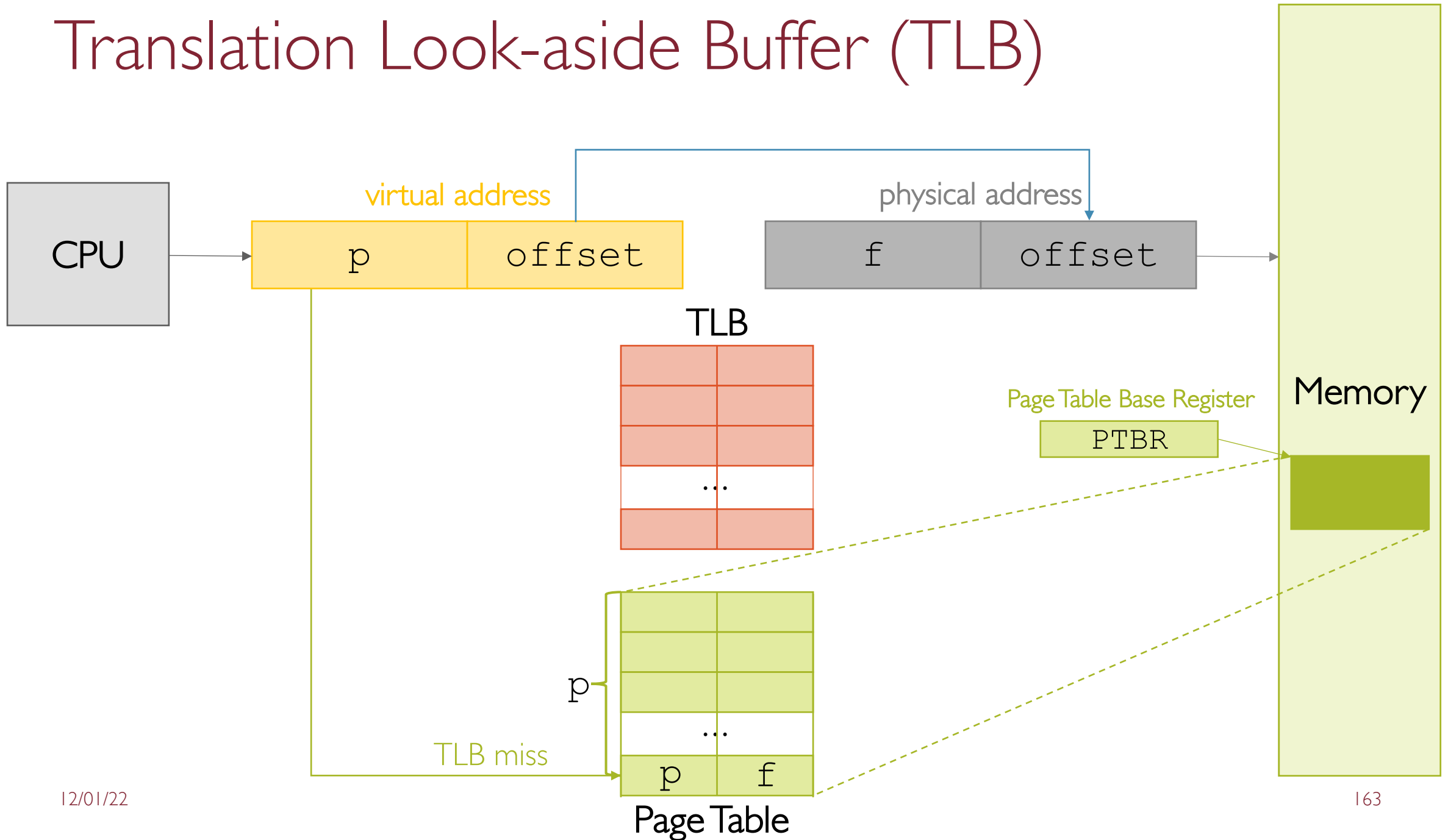
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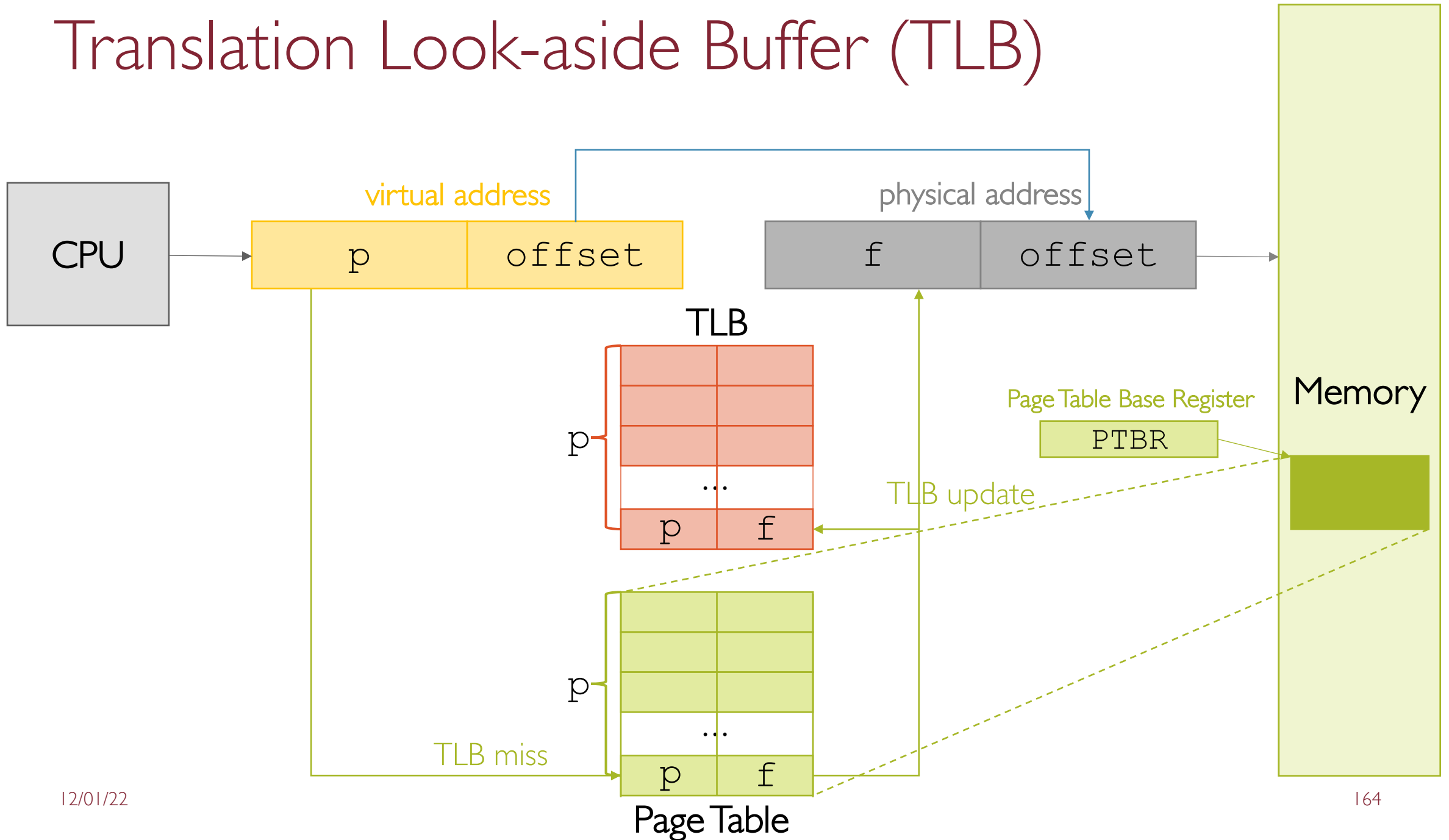
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 - **basic:** at each context switch the content of the TLB is fully flushed and cleaned (cold-start → the first accesses will generate all TLB misses)
 - **advanced:** TLB entries dumped and restored within the PCB or adding a so-called process context ID (PCID) to each entry (the CPU will use a TLB entry iff the PCID of that entry corresponds to the ID of the running process)

Memory Access Cost

t_{MA} = physical memory access time

t_{TLB} = lookup time on the TLB cache

(NOTE: $t_{TLB} \ll t_{MA}$)

p = probability of TLB cache hit (i.e., *hit ratio*)

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$$T_{MA} = p * \underbrace{(t_{MA} + t_{TLB})}_{\text{TLB hit}} + (1-p) * \underbrace{(2 * t_{MA} + t_{TLB})}_{\text{TLB miss}}$$

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p = probability of TLB cache hit (i.e., *hit ratio*)

T_{MA} = total time required to *actually* get to physical memory each time a virtual address is referenced

without TLB

(i.e., Page Table full in memory)

$$T_{MA} = 2 * t_{MA}$$

with TLB

$$T_{MA} = p * \underbrace{(t_{MA} + t_{TLB})}_{\text{TLB hit}} + (1-p) * \underbrace{(2 * t_{MA} + t_{TLB})}_{\text{TLB miss}}$$

The larger the TLB the higher the probability p of hit ratio, thereby decreasing the average memory access cost

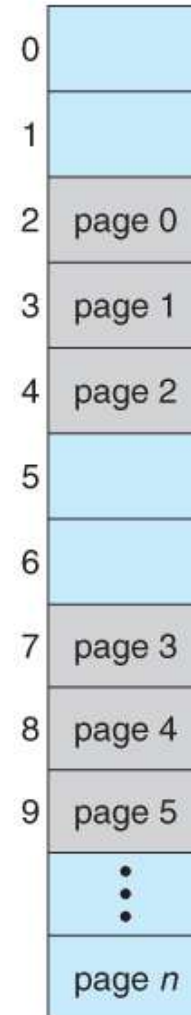
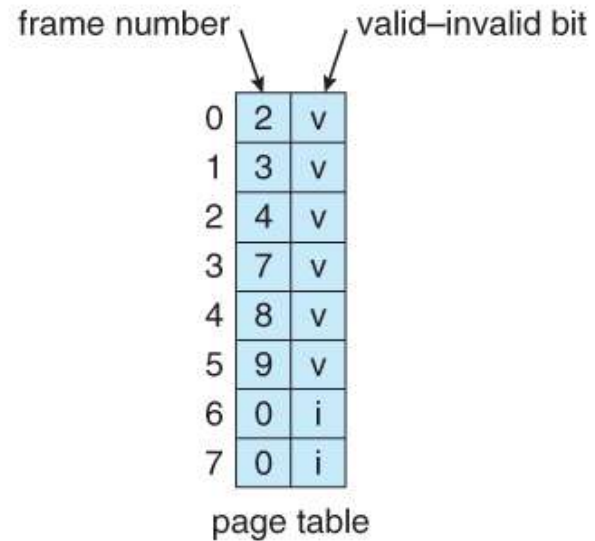
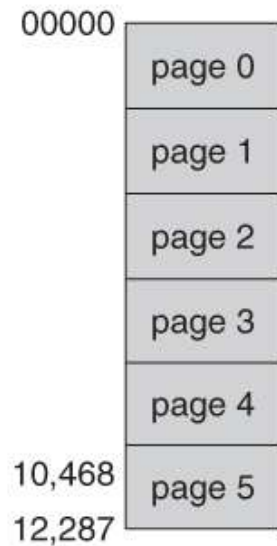
Additional Protection

- The page table can also help to protect processes from accessing memory they shouldn't, or their own memory in correct ways
- A bit or bits can be added to the page table to classify a page as read-write, read-only, read-write-execute, or combination of those
- Each memory reference can be checked to ensure it is accessing the memory in the appropriate mode
- Valid/invalid bits can be added to "mask off" entries in the page table that are not in use by the current process

Additional Protection

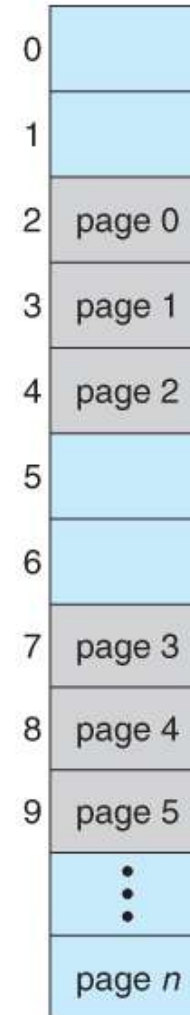
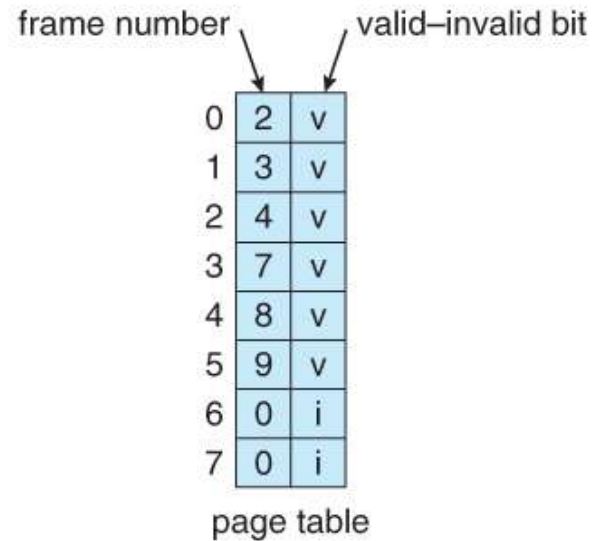
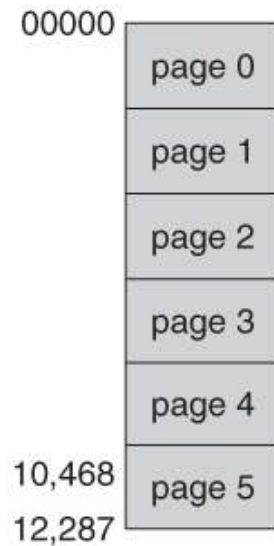
- valid/invalid bits cannot block all illegal memory accesses, due to the internal fragmentation
- Many processes do not use all of the page table entries available, particularly in modern systems with very large potential page tables
- Some systems use a page-table length register (PTLR) to specify the length of the page table

Additional Protection



valid/invalid bits can be used to flush TLB entries upon context switch if basic setup is used

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any entry whose invalid bit is set will be discarded (and updated)

Initializing Memory when Starting a Process

1. Process requests for k pages

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5. As process runs, OS loads TLB missed entries possibly replacing existing entries if TLB is full

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 - Possibly a copy of the TLB entries
- On a context switch:
 - Copy the PTBR value to the PCB
 - Copy the TLB to the PCB (optional)
 - Flush the TLB (if TLB is not saved to/restored from the PCB)
 - Restore the PTBR (i.e., with the value of the new running process)
 - Restore the TLB (if it was previously saved)

Sharing Pages

- Paging systems can make it very easy to share blocks of memory, since memory doesn't have to be contiguous anymore

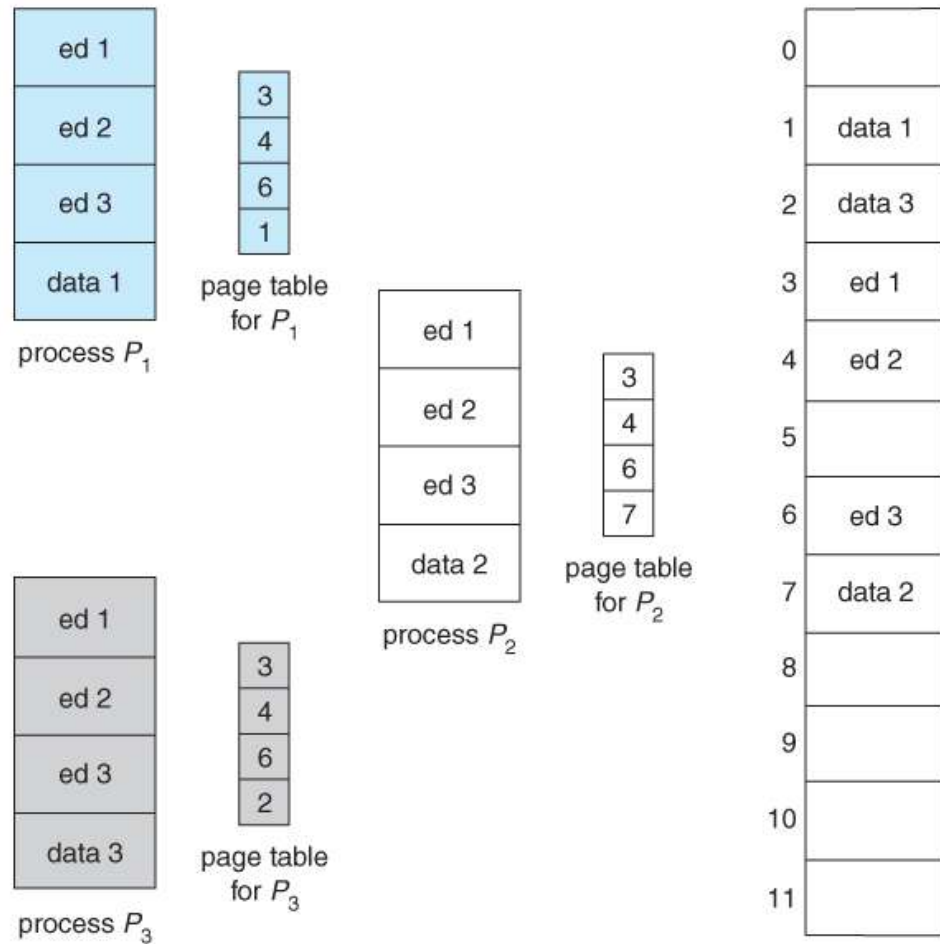
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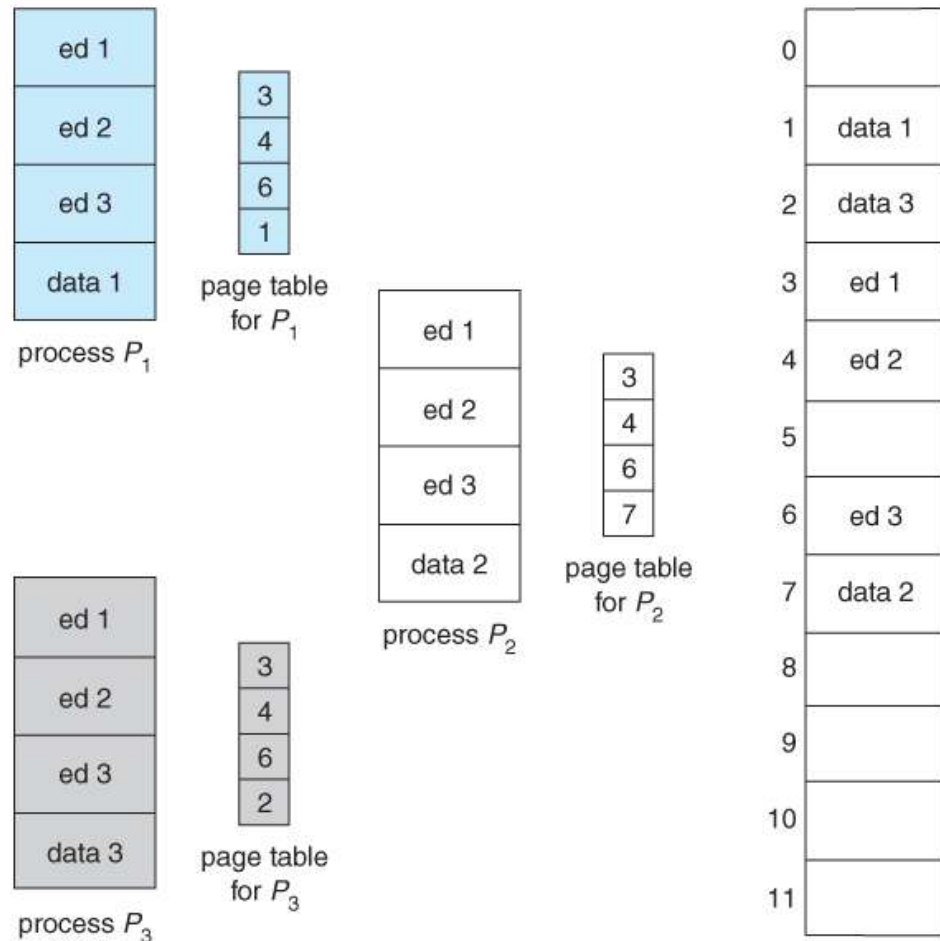
- Paging systems can make it very easy to share blocks of memory, since memory doesn't have to be contiguous anymore
- This can be done by simply duplicating page entries of different processes to the same page frames (both for code and data)
- Only if code is **reentrant**:
 - it does not write to or change the code (i.e., it is non self-modifying)
 - the code can be shared by multiple processes, as long as each has their own copy of the data and registers, including the instruction register

Sharing Pages: Example



3 user processes are using the editor program ed

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Only a **single copy** of the code of ed is actually loaded in main memory

Paging: Summary

- A big improvement over **relocation**
 - Eliminates the problem of external fragmentation and therefore the need for compaction
 - Allows code sharing among processes, reducing memory footprint
 - Enables processes to run when they are partially loaded

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- A big improvement over **relocation**
 - Eliminates the problem of external fragmentation and therefore the need for compaction
 - Allows code sharing among processes, reducing memory footprint
 - Enables processes to run when they are partially loaded
- However, paging comes with its costs:
 - Virtual/Physical address translation may be time consuming
 - Hardware support like TLB cache is needed to make it efficient enough
 - OS has to be inevitably more complex