ENEL491 – Solar Fabrication Lab Report

Andreas Ming, [redacted], ami162@uclive.ac.nz

Abstract

A fabricated single-junction solar cell based on a p-type wafer shows an average efficiency of 7.3% and 65% fill factor. A pn-junction at a depth of $434nm$ is formed through a phosphorus spin-on-dopant, which is then diffused in a constant source diffusion process. Rectangular windows are formed through a $450nm$ thick silicon oxide layer etched with a HF-acid. The top and bottom contacts are made out of aluminium, deposited through an electron beam evaporator. A positive photoresist is then used to etch grid fingers of different sizes into the top layer. A Light and Dark IV characterization of the solar cells is performed. This revealed a moderate correlation between the ratio of the concealed and the exposed area of the top contacts fingers and the solar cell parameters. For further improvement of the solar cell performance surface texturing, as well as the incorporation of passivation layers in either a PERL or HIT structure are suggested.

Table of Contents

Introduction

With an increasing population, the overall energy demand is assumed to increase. To address this and further achieve zero fossil fuel use by 2050, renewable energy production must increase 6-fold if the demand is held constant, or 8-fold if the demand increases by 50% from the 2020 energy demand level [1]. Solar alone has a potential of 6500TW, however only 0.008TW are currently utilized [2]. Furthermore, solar energy has the potential of low carbon emission, no fossil fuel requirement, long term solar resources, and less payback time [3].

The first solar cell in 1941 with 1% conversion efficiency, as well as the state-of-the-art solar cell with 25% conversion efficiency, are both made out of crystalline and multicrystalline silicon [4]. Today this efficiency can be achieved using industrially-sized silicon wafers, which in parallel increases production volume and lowers the price. In comparison to other photoactive materials, silicon has the advantage of being an absorbent material that is stable, non-toxic, abundant, and well understood. Furthermore, the energy band gap of $1.12eV$ in silicon corresponds to the light absorption cut-off wavelength of roughly $1160nm$. This cut-off wavelength is matched to the solar spectrum and very close to the optimum value for solar-to-electric energy conversion. [5]

Accounting for more than 95% of the global market, homojunction crystalline silicon cells, with high-temperature diffused junctions, are the most widely used photovoltaic system [6]. This report describes the fabrication process of such a silicon solar cell under lab conditions and critically evaluates the performance.

Fabrication Processes

This chapter describes the fabrication process of a single junction silicon solar cell.

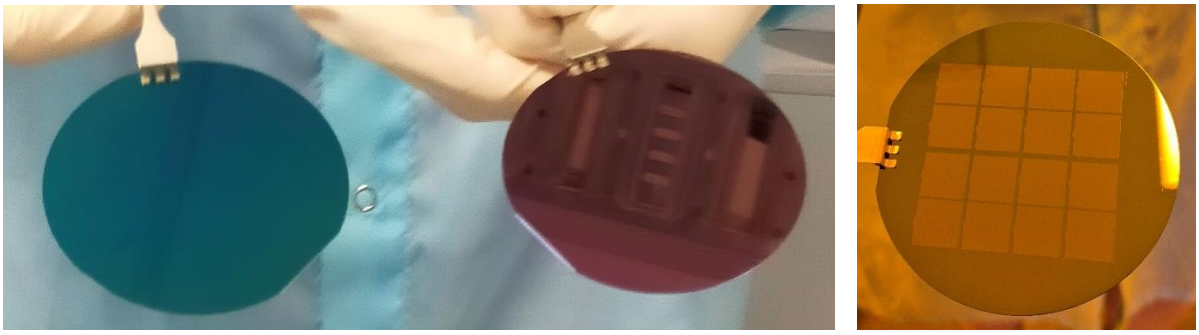
Oxide Growth and Windowing

The solar cell is fabricated on a <100> oriented 3" p-type wafer of 380µm thickness and a boron background concentration of $6 * 10^{15} cm^{-3}$. Piranha solution of a 5:1 (H_2SO_4:H_2O_2) concentration is used to remove any natural and organic residue. To insulate each solar cell from each other a oxide layer is grown through a long 3.5h wet thermal oxidation process at a 1000°C. This produces a oxide layer of theoretical thickness of (see appendix "Thermal Oxide Growth" for parabolic rate constant B)

$$X_0 = (Bt)^{1/2} = \left(0.315\frac{\mu m^2}{h} * 3.5h\right)^{1/2} = 1.05\mu m.$$

Instead of boiling water, 95°C warm water is used to limit harmful condensation within the lab equipment. This results in a dryer oxidation and thus a true oxide layer thickness of 450nm, as can be confirmed through the colour change in Figure 1b. Additionally, a dry oxidation annihilation for 10min at 1000°C, is performed before and after the wet oxidation to improve the oxide quality at the top and bottom oxide surfaces.

To form the cell openings in the silicon oxide, positive photoresist is spun, soft baked for 2min at 95°C, and exposed with $365nm$ UV light through a mask in optical lithography for 8s. After a development bath and a rinse in deionized water, the exposed silicon oxide is etched away with buffered hydrofluoric (HF) acid, thus exposing the untreated p-type silicon beneath (see Figure 1c).



a) b) c)

Figure 1: Wafers before (a) and after (b) oxidation, the thickness of the oxide can be deduced from the colour change [7]. (c) shows the wafer with the etched cell openings.

Doping

To lower the sheet resistance on the back of the wafer, a p+ region is formed through additional doping with boron atoms [8]. After placing the waver on a spin coater, the liquid dopant is poured on the wafer (Figure 2a) and evenly distributed through the centrifugal force. Soft baked on a hotplate for 10min at 200°C is done to stabilize the spin-coated dopant. The boron is then diffused at 1000°C for 30min into the p-type wafer, forming a $300\mu m$ deep heavier doped p+ region. To counteract thermal warping of the wafers, they must be inserted and extracted slowly in and out of the diffusion oven (Figure 2b). This allows them to adjust evenly to the high temperatures. Furthermore, the wafers are placed on a quartz tray which is capable of withstanding the high temperatures, with a melting point of 2000°C. After the cool down, the wafers are HF cleaned to remove the remaining spin-on dopant.

The same steps are repeated on the top side with Filmtronics spin-on dopant P509 serving as a phosphorus n-type dopant. This forms the pn-junction needed to separate the photo-generated carriers (electron-holes pairs). The pn-junction is located $434nm$ beneath the surface (see appendix “Depth pn-Junction”).

a) b)

Figure 2: Spin on dopant deposition on wafer (a) and insertion of the wafers on a quartz tray into diffusion oven for constant source diffusion (b).

Contacts

To form the contacts, aluminium is deposited on the top side (Figure 3a). This is done in a Temescal FC-1800 electron beam evaporator, in which electrons produced by a hot filament are accelerated to an energy of $9keV$ and then deflected onto a crucible containing aluminium metal. The high energy electron beam vaporizes a small spot of aluminium and the aluminium

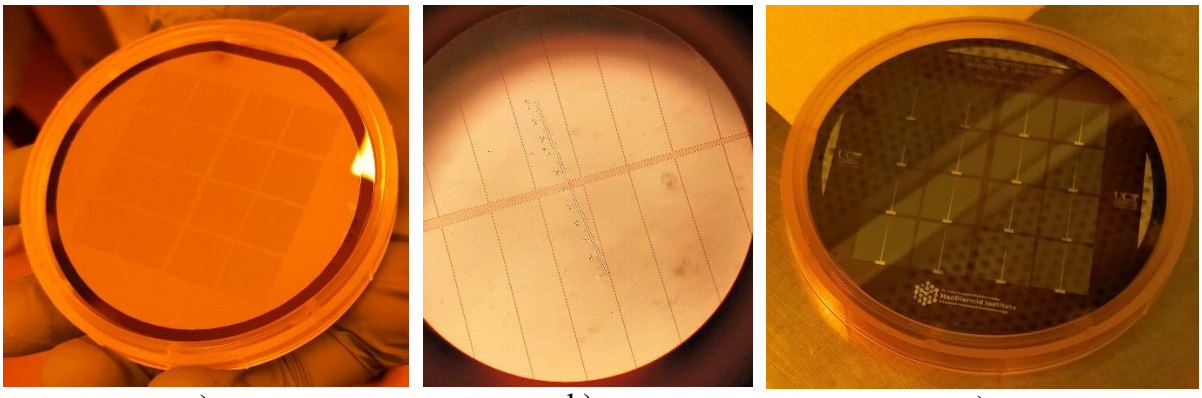
vapor then deposits on the wafers. This occurs inside a vacuum chamber at a pressure of less than $10^{-5}mbar$. With a deposition rate of $0.8\frac{nm}{s}$ it takes approximately 6min to deposit the target thickness of $300nm$ of aluminium.

Photoresist AZ 1518 is then deposited on the wafer which is placed on the spin coater. Spinning the wafer at 3000rpm for 60s leaves behind approximately $1.5\mu m - 1.7\mu m$ photoresist. To stabilize the photoresist, the wafer is soft baked for 2min at 95°C on a hotplate. To pattern the top aluminium collection grids the wafer is masked through UV photo lithography. The wafer is placed on the Karl Suss MA-6 mask aligner which has a microscope to view the alignment markers present on the mask and the already etched wafer. Once the mask (See Figure 10 in Appendix "Aluminium Top Contact Pattern") is correctly aligned, the photoresist is exposed with $365nm$ UV light for 8s at a UV intensity of approximately $5\frac{mW}{cm^2}$.

After exposure, the photoresist is developed for approximately 60s in AMZIF326 developer. As positive resist is used, the grid pattern is left behind (Figure 3b). To remove any traces of the developer solution, the wafer is rinsed off thoroughly with deionized water, and dried with nitrogen gas. The remaining photoresist can be checked under an optical microscope (see Figure 3b) before being hard baked in a hotplate for 10min at 100°C. If the quality of the photoresist is insufficient, it must be cleaned off with acetone and the spin-on, exposure, and developer steps have to be repeated.

The aluminium not covered by the hard baked photoresist is etched away by an aluminium etching solution of 80% phosphoric acid, 10% water, 5% glacial acetic acid, and 5% nitric acid. With appropriate personal safety equipment in place, the wafer is placed in the 37°C warm etching solution for 2-3min. After etching, the wafer has to be thoroughly cleaned in two deionized water baths, running water, and blow dried with nitrogen gas to stop the etching process.

Through a standard solvent clean the remaining hard baked photoresist is stripped of the wafer. Acetone, methanol, and isopropanol are used one after the other to remove residue. The wafer is then blow dried with nitrogen gas. Finally, to form the back contact of the solar cell, aluminium is deposited in the same way as the aluminium on the front, through electron beam evaporation.



a) b) c)

Figure 3: The aluminium coated wafer (a), the left behind grid pattern after photoresist developing (b) and the finished cells after etching and photoresist removal (c)

Solar Cell Performance

To determine the solar cell performance, we measure the Dark and Light current-voltage (IV) characteristics. The results are discussed in the chapter "Critical Evaluation". Because the pn-junction within the solar cell, which also acts as a diode in dark conditions, a diode IV test can be performed. For this a voltage sweep from $-1.2V$ to $1.2V$ in $40mV$ increments is performed, and the respective current measured. With the forward and reverse bias current, we can calculate the rectifying ratio which lies between $11.8 * 10^3$ and $67.0 * 10^3$ for the three tested cells (see appendix "Rectifying Ratio"). The exponential increase of the diode current above $0.4V$ in Figure 4 shows the avalanche effect expected of a pn-junction, and therefore confirms a diode functionality. The linear slope above $0.6V$ in Figure 4 suggests that the ohmic components dominate the IV characteristic of the solar cell.

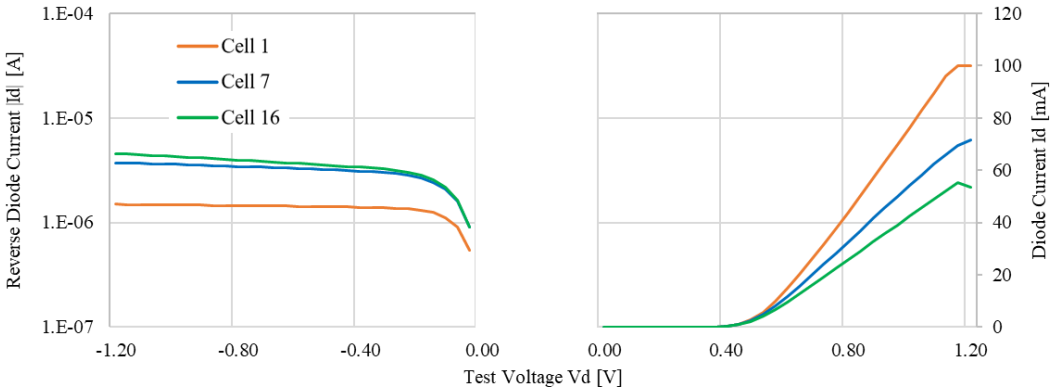


Figure 4: Dark IV bias current characteristics of Cells 1, 7 and 16

To determine the solar cell merits under direct sun exposure, a ABET Technologies Sun 3000 solar simulator is used. This simulates an AM1.5 solar spectrum with a total irradiance of $100\frac{mW}{cm^2}$. As the active area of each solar cell is approximately $1cm^2$ the incident power on each cell is around $100mW$. After contacting a cell individually with a micro manipulator, the wafer is exposed, and a voltage sweep from $-1.2V$ to $1.2V$ in $40mV$ increments is performed. The resulting current curve is the sum $I = I_{light} - I_{diode}$, where I_{diode} describes the diode current acquired through the Dark IV test in Figure 4. Rearranging this equation to I_{light}, reveals the IV-curve of the solar cell. Multiplying cell current and voltage $P = V * I_{light}$ shows the power (PV) characteristics of the solar cells, as seen in Figure 5.

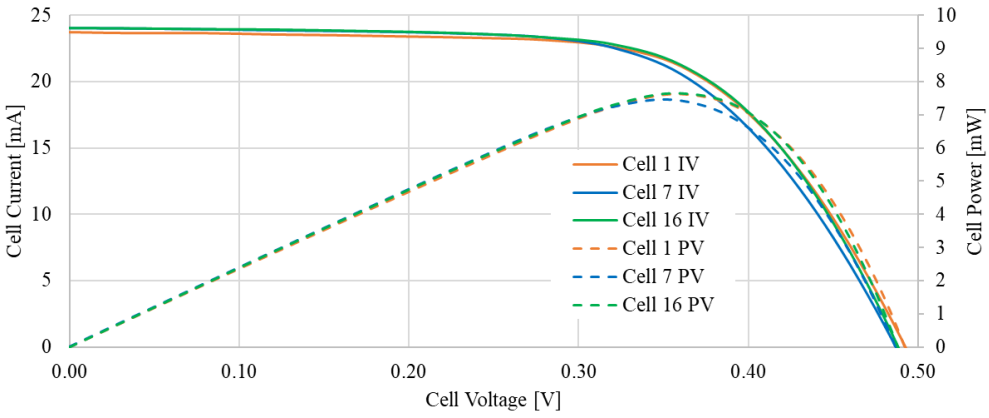


Figure 5: IV and PV characteristic of the measured cells

Furthermore, the retrieved data (see appendix "Light IV Results") shows an average efficiency of 7.29% with a std deviation of 0.29%, and an average fill factor of 64.8% with a std deviation of 0.82% over all measured cells. The open circuit voltage, and the short circuit current are within 3% over all measured cells at average $484mV$ and $23.2mA$ respectively. The shunt resistance shows the highest variance of all parameters, ranging from 602Ω up to $6.41k\Omega$. Series resistance lies within 5% on 3.90Ω average.

Finally, an optical assessment of the solar cells is performed to verify the quality of the fabrication process. The FILMETRICS Profilm3D Optical Profilometer is used to measure the aluminium film thickness, and an optical microscope is used to examine the cells for defects. The aluminium film thickness lies between $256nm$ and $287nm$ on the measured cells.

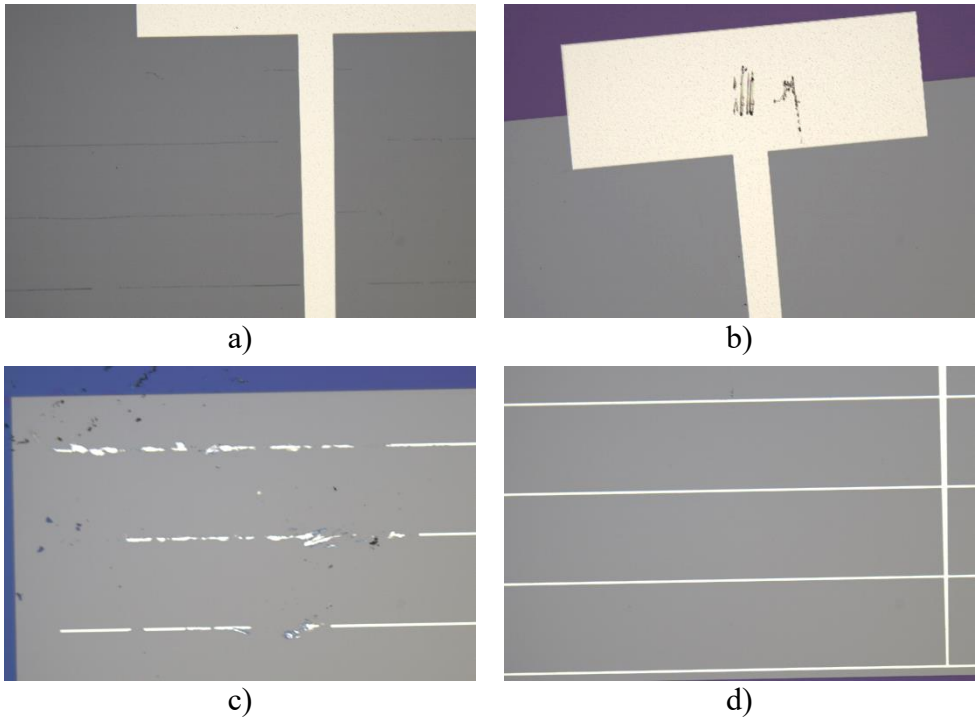


Figure 6: Images taken on a optical microscope. Defected aluminium grids on cell 1 (a) and 16 (c), scratch marks after Dark IV testing on cell 7 (b), intact grid pattern on cell 16 (d).

Critical Evaluation

Putting the physical differences between the cells and their measured performance in correlation shows that the efficiency (0.73), fill factor (0.67), open circuit voltage (0.73), and the maximum power (0.73) are strongly correlated. Whereas the short circuit current (0.46), shunt resistance (0.44), and series resistance (-0.58) are only moderately correlated (see Table 6 in appendix "Light IV Results"). Due to manufacturing errors (see Figure 6a) there are cells with partially broken or completely absent grid fingers (see Figure 9 in appendix "Solar Cells on Wafer"). This changes the ratio, and therefore the correlation of the incomplete cells. With the corrected ratio of cell 5 and 7 from 5.5 to 0 showed very little effect on the correlations with the values lying in between 10%. This is due to a very small sample size, and because the damaged cells have the smallest concealed area already.

To evaluate the quality of the pn-junction, the Dark and Light IV test results are used. The IV characteristic of the Light test shows all samples are very similar to each other, showing consistent curvatures and similar open circuit voltages (see Figure 11 in appendix "Light IV

Results"). These observations suggest a high degree of uniformity in the pn-junction, and indicates a homogeneous n-diffusion throughout the surface material.

The manufacturing errors introducing the damaged and missing grid fingers can be traced back to a too long development time of the photoresist, masking the grid fingers for aluminium etching. As the developer also attacks the UV exposed and hardened photoresist, although at a much lower rate, the structures of the finest $5\mu m$ grid fingers were damaged in the process. This can be examined under the microscope immediately following development in Figure 7.

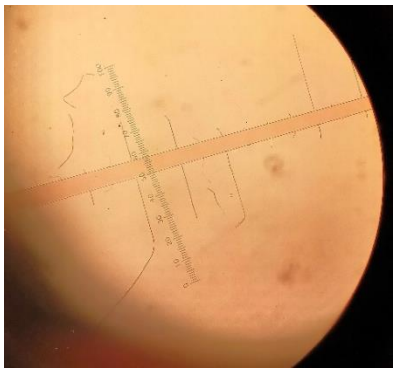


Figure 7: Damaged photoresist structure after development.

Rectangular grid fingers are the predominant top contact grid fingers used in the industry. The form factor and aspect ratios can vary greatly to counterweight shadowing losses and low contact resistances [9]. The grid fingers on the presented solar cells varied in width and spacing from cell to cell (see Figure 10 in appendix "Aluminium Top Contact Pattern"). It has been found, that the cells with a concealed to exposed ratio of 0.04 and 0.05 result the best efficiency of 7.6%. These two cells consist of 23 and 56 bars with $20\mu m$ and $10\mu m$ width and a $500\mu m$ and $200\mu m$ spacing respectively. It must be noted that not all aspect ratios present on the wafer are measured. To eliminate shadowing losses completely, interdigitated-back-contact (IBC) cells with no present shadowing have been produced and show the capability of very high short circuit currents [5].

Another effective way to improve the solar cell efficiency is to texture the silicon surface of the cells to enhance the absorption of incident light. Texture can reduce reflectivity of a raw silicon wafer from more than 45% to less than 10% [10]. Such a texture can be achieved through chemical etching at low cost [11]. Additionally, a passivation layer on the top and bottom surface can be introduced to minimise recombination losses and reflectance. A passivation layer is typically introduced through a SiO_2 growth and Al annealing forming a passivated emitter rear locally diffused (PERL) cell (see Figure 8a) [4]. The back oxide layer furthermore enhances the reflectiveness of the backside aluminium layer. The back contacts are formed through small holes in the oxide, where the metal contact region is heavily doped to further suppress recombination loss and enhance sheet resistance. [5], [12]

Another use of passivation layers is the heterojunction with intrinsic thin layer (HIT) solar cell (see Figure 8b). A very thin layer ($\sim 5nm$) of hydrogen amorphous silicon is inserted underneath the electron- and hole-selective layers, resulting in a nearly recombination-free surface. To form these, $10nm$ of silicon are deposited onto the passivation layer and doped with boron and phosphorus for p-type and n-type respectively. Full area contacts are formed through a transparent indium tin oxide layer. Such HIT solar cells yield efficiencies of up to 24.7% and open-circuit voltages of 750mV. [5]

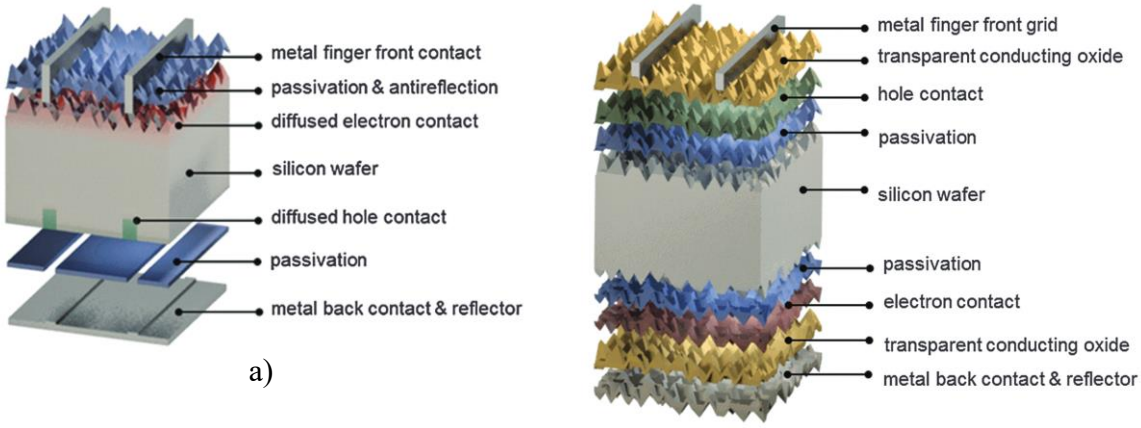


Figure 8: Schematic representation of the components of a PERL (a) and a HIT (b) single junction solar cell. [5]

Modern single junction solar cell, as described so far, are approaching the theoretical limits of 29% efficiency, due to the fixed band gap of a single junction [13], [14]. The proposed solution to this is the use of multi-junction solar cells, where multiple junctions with different bandgaps are formed – which result in higher efficiencies at wavelengths more distant to the optimal $1100nm$ of a pure silicon pn-junction. Current multi-junction solar cells are mostly gallium based and show high efficiencies of up to 35%. Due to high production cost and low availability, this technology is not yet suited for terrestrial applications. [15]

Conclusion

The solar cell described, has been successfully fabricated on a silicon wafer. Phosphorous spin-on dopant formed a pn-junction within the silicon oxide window openings through a constant source diffusion. The uniformity of the pn-junction is confirmed by a Light and Dark IV measurement. The top and bottom contacts are made out of aluminium and show a grid pattern of varying size on the top. Due to a too long development of the photoresist for the grid fingers, the thinnest $5\mu m$ grid fingers are damaged or absent on the final solar cells. This however only led to a slight change in the measured parameters.

Overall, the solar cells have been found to have an average efficiency of 7.29% and an average fill factor of 64.8%. The open circuit voltage and the short circuit current average $484mV$ and $23.2mA$ respectively. The shunt resistance shows the highest variance of all parameters, ranging from 602Ω up to $6.41k\Omega$. Series resistance, in contrast, lies within 5% on 3.90Ω average. A moderate correlation has been found between the parameters and the concealed to exposed area ratio of each solar cell.

For higher efficiencies, structuring of the surface, and the incorporation of passivation layers are proposed. Either in a simple PERL configuration with passivation layers on the top and bottom of the solar cell, or through a more complex HIT process, where the passivation layers lie underneath the electron- and hole-selective layers. A bigger leap in efficiency would be the change from a single-junction cell to a multi-junction configuration. With this, parts of the suns spectrum further apart from the ideal silicon wavelength can be converted more efficiently.

References

[1] J. L. Holechek, H. M. E. Geli, M. N. Sawalhah, and R. Valdez, "A Global Assessment: Can Renewable Energy Replace Fossil Fuels by 2050?," *Sustainability*, vol. 14, no. 8, Art. no. 8, Jan. 2022, doi: 10.3390/su14084792.

[2] U.S. Energy Information Administration (EIA), "International Energy Outlook 2023." Accessed: Apr. 02, 2024. [Online]. Available: https://www.eia.gov/outlooks/ieo/index.php

[3] M. M. Aman *et al.*, "A review of Safety, Health and Environmental (SHE) issues of solar energy system," *Renew. Sustain. Energy Rev.*, vol. 41, pp. 1190–1204, Jan. 2015, doi: 10.1016/j.rser.2014.08.086.

[4] M. A. Green, "The path to 25% silicon solar cell efficiency: History of silicon cell evolution," *Prog. Photovolt. Res. Appl.*, vol. 17, no. 3, pp. 183–189, 2009, doi: 10.1002/pip.892.

[5] C. Battaglia, A. Cuevas, and S. De Wolf, "High-efficiency crystalline silicon solar cells: status and perspectives," *Energy Environ. Sci.*, vol. 9, no. 5, pp. 1552–1576, 2016, doi: 10.1039/C5EE03380B.

[6] J. Zhou *et al.*, "Recent advancements in poly-Si/SiOx passivating contacts for high-efficiency silicon solar cells: technology review and perspectives," *J. Mater. Chem. A*, vol. 10, no. 38, pp. 20147–20173, Oct. 2022, doi: 10.1039/D2TA04730F.

[7] HTE Labs, "SiO2 color chart for thermally grown silicon dioxide, HTE Labs, sputter deposition services, thin film vacuum deposition,wafer foundry, bipolar process development, contract R&D, bipolar wafer foundry services, thin film vacuum deposition services." Accessed: Apr. 18, 2024. [Online]. Available: http://www.htelabs.com/appnotes/sio2_color_chart_thermal_silicon_dioxide.htm

[8] W. Yang *et al.*, "Performance of p^+ layer formed by B diffusion using boron paper," *Mater. Res. Express*, vol. 5, no. 3, p. 035902, Mar. 2018, doi: 10.1088/2053-1591/aab070.

[9] J. S. Ward, A. Duda, D. J. Friedman, J. Geisz, W. McMahon, and M. Young, "High aspect ratio electrodeposited Ni/Au contacts for GaAs-based III–V concentrator solar cells," *Prog. Photovolt. Res. Appl.*, vol. 23, no. 5, pp. 646–653, 2015, doi: 10.1002/pip.2490.

[10] X. Dai *et al.*, "The influence of surface structure on diffusion and passivation in multicrystalline silicon solar cells textured by metal assisted chemical etching (MACE) method," *Sol. Energy Mater. Sol. Cells*, vol. 186, pp. 42–49, Nov. 2018, doi: 10.1016/j.solmat.2018.06.011.

[11] D. Zhang *et al.*, "Fabrication of inverted pyramid structure for high-efficiency silicon solar cells using metal assisted chemical etching method with CuSO4 etchant," *Sol. Energy Mater. Sol. Cells*, vol. 230, p. 111200, Sep. 2021, doi: 10.1016/j.solmat.2021.111200.

[12] J. Zhao, A. Wang, P. Altermatt, and M. Green, "Twenty-four percent efficient silicon solar cells with double layer antireflection coatings and reduced resistance loss," *Appl. Phys. Lett.*, vol. 66, pp. 3636–3638, Jun. 1995, doi: 10.1063/1.114124.

[13] X. Y. Chin *et al.*, "Interface passivation for 31.25%-efficient perovskite/silicon tandem solar cells," *Science*, vol. 381, no. 6653, pp. 59–63, Jul. 2023, doi: 10.1126/science.adg0091.

[14] S. Schafer and R. Brendel, "Accurate Calculation of the Absorptance Enhances Efficiency Limit of Crystalline Silicon Solar Cells With Lambertian Light Trapping," *IEEE J. Photovolt.*, vol. 8, no. 4, pp. 1156–1158, Jul. 2018, doi: 10.1109/JPHOTOV.2018.2824024.

[15] S. Sundaram, D. Benson, and T. K. Mallick, "Chapter 3 - Potential Environmental Impacts From Solar Energy Technologies," in *Solar Photovoltaic Technology Production*, S. Sundaram, D. Benson, and T. K. Mallick, Eds., Academic Press, 2016, pp. 23–45. doi: 10.1016/B978-0-12-802953-4.00003-2.

[16] A. Muhammad Afzal *et al.*, “Tunneling-based rectification and photoresponsivity in black phosphorus/hexagonal boron nitride/rhenium diselenide van der Waals heterojunction diode,” *Nanoscale*, vol. 12, no. 5, pp. 3455–3468, 2020, doi: 10.1039/C9NR07971H.
[17] C. Ulbrich, D. C. Jordan, S. R. Kurtz, A. Gerber, and U. Rau, “Direct analysis of the current density vs. voltage curves of a CdTe module during outdoor exposure,” *Sol. Energy*, vol. 113, pp. 88–100, Mar. 2015, doi: 10.1016/j.solener.2014.12.004.
[18] T. Nguyen-Duc, H. Nguyen-Duc, T. Le-Viet, and H. Takano, “Single-Diode Models of PV Modules: A Comparison of Conventional Approaches and Proposal of a Novel Model,” *Energies*, vol. 13, no. 6, Art. no. 6, Jan. 2020, doi: 10.3390/en13061296.
[19] Y. Li *et al.*, “Evaluation of methods to extract parameters from current–voltage characteristics of solar cells,” *Sol. Energy*, vol. 90, pp. 51–57, Apr. 2013, doi: 10.1016/j.solener.2012.12.005.
[20] “Profilometer and 3D Optical Profiler - Filmetrics.” Accessed: Apr. 04, 2024. [Online]. Available: https://www.filmetrics.com/profilometers/profilm3d

Appendix

Nomenclature

Table 1: Nomenclature

k	Boltzmann's constant	$1.38 * 10^{-23}\frac{J}{K} = 8.617 * 10^{-5}\frac{eV}{K}$
$T[K]$	Absolute temperature	$T\ [°C] + 273\frac{K}{°C}$
SiO_2	Silicon oxide	
Al	Aluminium	

Thermal Oxide Growth

From the table provided in the lecture slides we get the parameters

$$D_0 = 386\frac{\mu m^2}{h};\ E_A = 0.78eV$$

for the Arrhenius function. With these we get the parabolic rate constant

$$B = D_0 \exp\left(-\frac{E_A}{kT}\right) = 386\frac{\mu m^2}{h} \exp\left(-\frac{0.78eV}{8.617 * 10^{-5}\frac{eV}{K} * 1273K}\right) = 0.315\frac{\mu m^2}{h}$$

for wet oxidation on <100> silicon at 1000°C.

Depth pn-Junction

The constant source diffusion of the n-type phosphorus ($D_0 = 10.5\frac{cm^2}{s}$, $E_A = 3.69eV$, $N_0 = 9 * 10^{20}cm^{-3}$) dopant into the p-type wafer with background concentration of $N_B = 6 * 10^{15}cm^{-3}$ and a diffusion coefficient

$$D = D_0 \exp\left(-\frac{E_A}{kT}\right) = 10.5\frac{cm^2}{s} \exp\left(-\frac{3.69eV}{8.617 * 10^{-5}\frac{eV}{K} * 1273K}\right) = 25.8 * 10^{-15}\frac{cm^2}{s}$$

leads to a pn-junction depth of

$$X_j = 2\sqrt{Dt} * erfc^{-1}\left(\frac{N_B}{N_0}\right) = 2\sqrt{25.8 * 10^{-15}\frac{cm^2}{s} * 1800s} * erfc^{-1}\left(\frac{6 * 10^{15}cm^{-3}}{9 * 10^{20}cm^{-3}}\right)$$

$$= 43.4 * 10^{-6}cm = 434nm.$$

Solar Cells on Wafer

16 cells are fabricated onto one wafer, for identification throughout the production and measurement the cells are numbered as shown in Figure 9. Furthermore, the colour indicates present (Green), absent (Red) or damaged (Orange) grid fingers.

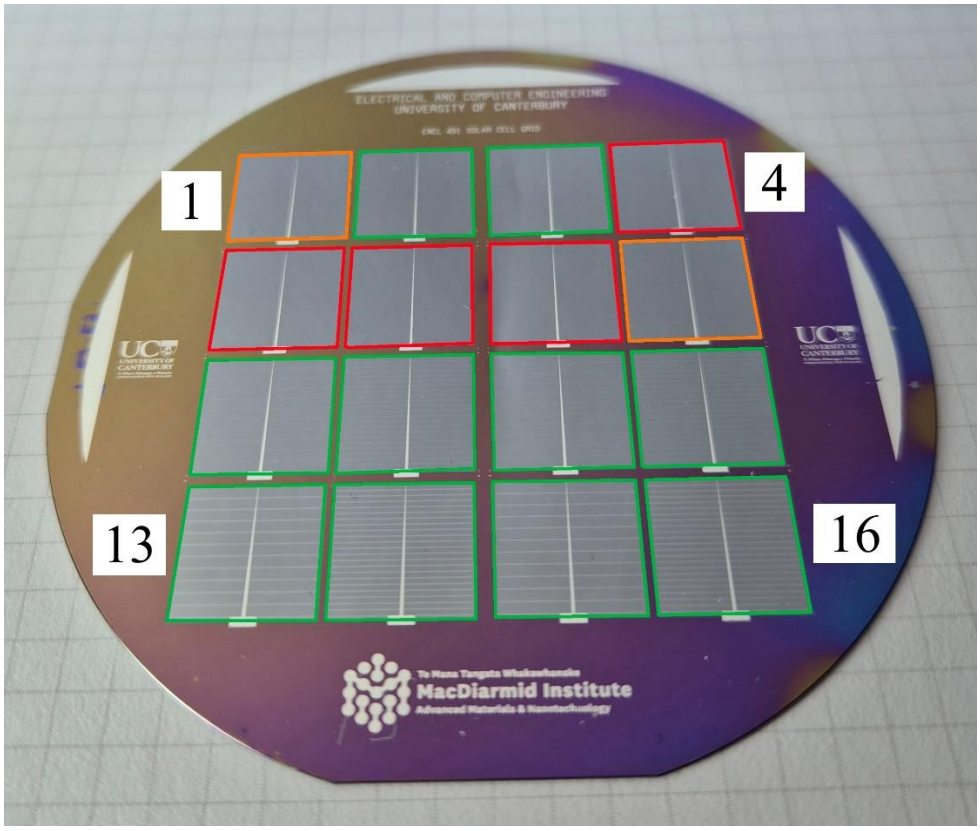


Figure 9: Cell annotation and state of each solar cell on the wafer

Aluminium Top Contact Pattern

The Pattern of the aluminium top contacts follow the following mask.

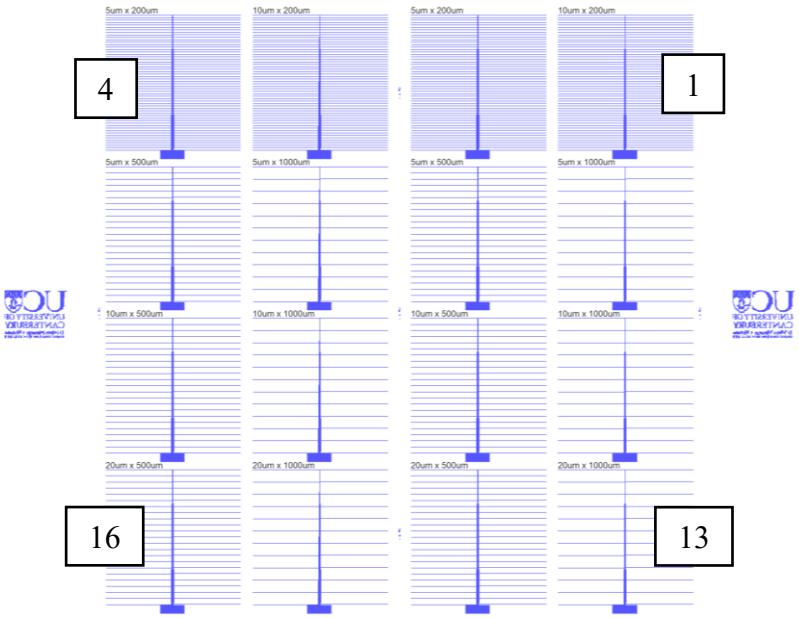


Figure 10: Cell annotation on the aluminium contact grid mask (pay attention to mirroring)

With the data from the mask, we can work out the concealed and exposed areas of the measured solar cells. Furthermore the ratio $A_{concealed}/A_{exposed}$ can be calculated for further analysis.

Table 2: By aluminium exposed and concealed area and the corresponding ratio per cell.

Cell		1	2	5	7	9	13	15	16
$A_{concealed}$	[cm^2]	0.056	0.028	0.006	0.006	0.012	0.024	0.024	0.046
$A_{exposed}$	[cm^2]	1.10	1.10	1.10	1.10	1.10	1.10	1.10	1.10
Ratio	*10^{-3}	50.9	25.5	5.5	5.5	10.9	21.8	21.8	41.8

Figure 9 shows that not all cells consist of grid fingers, specifically the $5\mu m$ wide grid fingers are absent. Therefore the values in Table 2 need to be adjusted to the totally exposed cells 5 and 7.

Table 3: The concealed to exposed ratio with the corrected concealed area for cell 5 and 7

Cell		1	2	5	7	9	13	15	16
$A_{concealed}$	[cm^2]	0.056	0.028	0	0	0.012	0.024	0.024	0.046
$A_{exposed}$	[cm^2]	1.10	1.10	1.10	1.10	1.10	1.10	1.10	1.10
Ratio	*10^{-3}	50.9	25.5	0.0	0.0	10.9	21.8	21.8	41.8

Rectifying Ratio

The rectifying ratio is ratio between the forward bias current I_f and the reverse bias current I_r [16]

$$Rectifying\ ratio = \frac{I_f}{I_r}.$$

For the three Dark IV tested cells we get the rectifying ratios described in Table 4.

Table 4: Rectifying ratio of measured cells, determined through a Dark IV measurement

	Cell 1	Cell 7	Cell 16
Rectifying ratio	$67.0 * 10^3$	$19.2 * 10^3$	$11.8 * 10^3$

Light IV Results

The Light IV measurement is conducted with a ABET Technologies Sun 3000 solar simulator, operating at 1.5AM and reveal the solar cell characteristics listed in Table 5. We obtain information about efficiency (EFF), Fill-Factor (FF), Open-Circuit-Voltage (V_{oc}), Short-Circuit-Voltage (I_{sc}) and the differential resistances R_{sc} and R_{oc}, i.e., the reciprocal slopes of the IV curves at short circuit and open circuit [17], [18]. Under the simplest assumption of reasonably good solar cell properties, one can say, that these reciprocal slopes describe the shunt resistance R_{sh} and series resistance R_s of a solar cell [19]. Maximum power can be calculated through $P_{max} = FF * V_{oc} * J_{sc}$.

Table 5: Light IV measurement results of measured cells

Cell		1	2	5	7	9	13	15	16	avg	std dev.
EFF	%	7.62	7.34	6.80	7.42	7.04	7.02	7.42	7.65	7.29	0.29
FF	%	65.3	65.1	63.6	63.4	64.8	65.9	65.2	65.3	64.8	0.82
V_{oc}	mV	492	483	478	486	481	480	487	487	484	4.16
I_{sc}	mA	23.7	23.3	22.3	24.1	22.6	22.2	23.4	24.0	23.2	0.70
$R_{sc} \approx R_{sh}$	Ω	929	5708	857	871	602	1042	946	6408	2170	2254
$R_{oc} \approx R_s$	Ω	3.95	3.77	4.20	4.06	3.97	3.78	3.79	3.66	3.90	0.17
P_{max}	mW	7.62	7.34	6.79	7.42	7.04	7.02	7.41	7.65	7.29	0.29

Measuring the current over a applied voltage from $-1.2V$ to $1.2V$ reveals the IV characteristics (see Figure 11) of the solar cell under light. The current is the sum $I = I_{light} - I_{diode}$, where I_{diode} revers to the IV-curve acquired in the dark IV test.

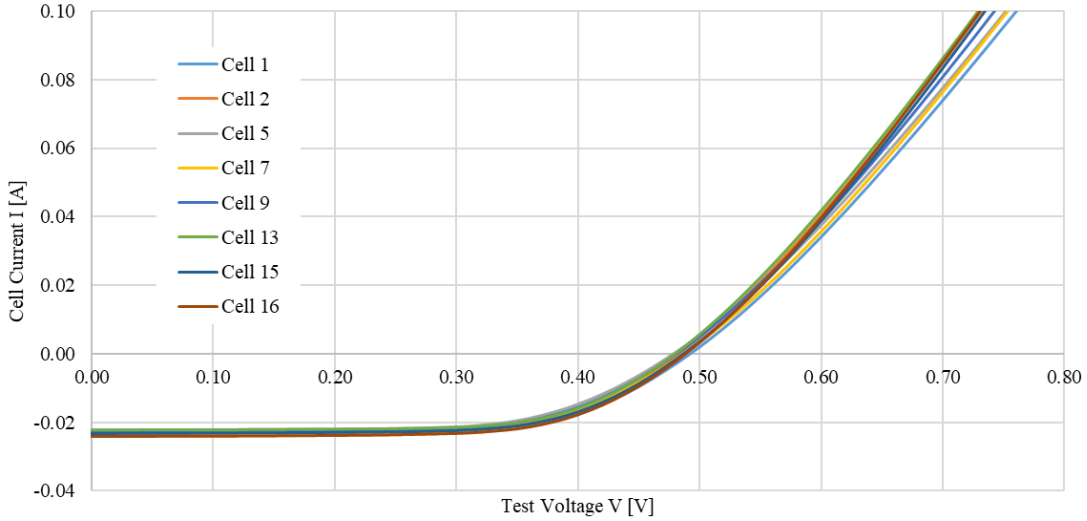


Figure 11: Light IV characteristics of measured cells

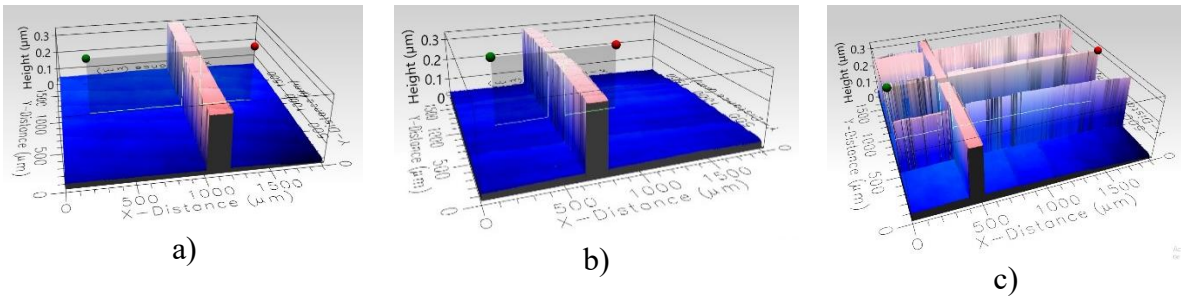
To set the determined values into relation with the deliberately introduced physical differences, we look at the correlation between the parameters and the grid area ratio calculated in Table 2 appendix “Aluminium Top Contact Pattern”.

Table 6: Correlation between the parameters of the cells and their concealed to exposed area ratio. The correlation is given for the target (Table 2) and actual (Table 3) ratio as well as how much the correlation changed.

	Correlation to area ratio Target ratio	Correlation to area ratio Actual ratio	Change of correlation [%]
EFF	0.728	0.708	2.73
FF	0.673	0.738	-9.61
V_{oc}	0.727	0.696	4.33
I_{sc}	0.455	0.413	9.37
$R_{sc} \approx R_{sh}$	0.436	0.441	-1.00
$R_{oc} \approx R_s$	-0.583	-0.638	-9.31
P_{max}	0.727	0.708	2.67

Aluminium Film thickness measurement

FILMETRICS Profilm3D Optical Profilometer is used to measure the aluminium film thickness on each cell. The 3D structure of a sample is acquired contactless through white light interferometry (WLI) and phase shifting interferometry, which provides a resolution down to $1nm$ [20].



a) b) c)

Figure 12: Bus bar height of (a) cell 1 (267nm), (b) cell 2 (287nm) and (c) cell 16 (255nm)