Andre Chang

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Summary

Areas of interest are: hardware accelerators, compilers and deep learning.

Education

Ph.D. - Purdue University West Lafayette, IN, US 09/2019
Electrical and Computer Engineering: DNN Hardware Accelerators and compilers (3.88/4.0)

Master of Science - Purdue University West Lafayette, IN, US 05/2016
Electrical and Computer Engineering: RNN Hardware Accelerators (3.8/4.0)

Bachelor - Universidade Tecnológica Federal do Paraná (UTFPR), Brazil 07/2014
Electronic Engineering (0.87/1)

Exchange Studies - Franklin W. Olin College of Engineering, MA, US 01 – 12/2012
Electrical and Computer Engineering (3.77/4.0)

Experience

Deep Learning Compiler Engineer Micron WA, US 09/2019 - now
- Lead compiler team to deliver software product
- Implementing tools to map DNNs to custom accelerators

Co-Founder and Lead Compiler Engineer FWDNXT IN, US 09/2017 - 05/2019
- Implemented tools to run DNN on custom hardware accelerator
- Implementing compiler optimizations for custom DNN accelerators

Research Assistant e-Lab Purdue University IN, US 09/2014 – 08/2017
- Wrote compiler to generate custom instructions for custom DNN accelerators
- Wrote library to accelerate deep learning on mobile phones using openGL
- Designed a low power hardware accelerator for recurrent neural networks using FPGA

Research Intern Sonoscan IL, US 05 – 08/2015
- Developed Bluetooth LE interface for transducer tagging
- Implemented firmware for the transceiver, Android App to communicate with mobile phones and program to communicate with PC
- Designed the Bluetooth LE circuit board using nrf51822 chip

Technical Assistant Sapiens Eletrônica ltda PR, Brazil 06/2013 – 08/2014
- Programmed industrial controller for automatic length sensing for cutting cardboard

Research Assistant UTFPR PR, Brazil 08/2013 – 07/2014
- Designed and implemented hardware for ultrasound signal processing to generate real time B-mode medical images, using FPGA
- Designed a prototype that acquires ultrasound signals for wood characterization

Research Assistant Franklin W. Olin engineering college, MA, US 05 – 08/2012
- Created simulation models of Wireless-Power-Transfer systems for optimization purposes

Patent applications

Hardware Accelerator for Convolutional Neural Networks and Method of Operation Thereof US Patent App. 15/990,365.
Evolutionary Imitation Learning: a mechanism to continuously optimize neural networks from non-optimal data samples 2020-1980.00/US.
ANN-Powered Compiler for Deep Learning Accelerators 2020-0144.00/US.
Deep Neural Networks Compiler for a Trace-Based Accelerator U.S. Provisional Patent App No. 62/754,148.
Inference Engine Circuit Architecture U.S. Provisional Patent App No. 62/739,184.

Publications and Conferences

A.X.M. Chang, P. Khopkar, B. Romanous, A. Chaurasia, E. Culurciello, et.al. "*Reinforcement Learning Approach for Mapping Applications to Dataflow-Based Coarse-Grained Reconfigurable Array.*" Arxiv 2022.

A.X.M. Chang, A. Zaidy, M. Vitez, L. Burzawa E. Culurciello. "*Deep neural networks compiler for a trace-based accelerator.*" JSA 2020.

A.X.M. Chang, A. Zaidy, L. Burzawa E. Culurciello. "*WIP: Deep Neural Networks compiler for a trace-based accelerator.*" LCTES 2018.

A.X.M. Chang, A. Zaidy, E. Culurciello. "*Efficient compiler code generation for Deep Learning Snowflake co-processor.*" EMC2 Workshop 2018 co-located with ASPLOS 2018.

A.X.M. Chang, A. Zaidy, E. Culurciello. "*Compiling Convolutional Neural Networks for FPGA Accelerator.*" OpenSuCO Workshop 2017 co-located with Super Computing 2017.

A.X.M. Chang, A. Zaidy, V. Gokhale, E. Culurciello. "*Compiling Deep Learning Models for Custom Hardware Accelerators.*" arXiv preprint https://arxiv.org/pdf/1708.00117.pdf (2017).

A.X.M. Chang, A. Zaidy, V. Gokhale, E. Culurciello. "*Generating instructions for deep learning custom hardware.*" Poster presentation at Computational Science and Engineering Student Conference - CSESC 2017.

A.X.M. Chang, E. Culurciello. "*Hardware Accelerators for Recurrent Neural Networks on FPGA.*" In press - ISCAS May 27 2017.

V. Gokhale, A. Zaidy, **A.X.M. Chang**, E. Culurciello. "*Snowflake: an Efficient Hardware Accelerator for Convolutional Neural Networks.*" In press - ISCAS May 27 2017.

A. Zaidy, **A.X.M. Chang**, V. Gokhale, E. Culurciello. "*Snowflake: A Hardware Accelerator for Convolutional Neural Networks.*" Poster presentation at Workshop: Hardware and Algorithms for Learning On-a-chip (HALO) - ICCAD November 10 2016.

A.X.M. Chang, B. Martini, E. Culurciello. "*Recurrent Neural Networks Hardware Implementation on FPGA.*" arXiv preprint arXiv:1511.05552 (2015).

A.X.M. Chang, A.A. Assef, J.M. Maia and F.K. Schneider. "*Control system based on FPGA/DSP for acquisition, conditioning and processing of ultrasound signals*", in XXIV Brazilian Congress on Bio-medical Engineering Brazil, 2014, 193.

A.X.M. Chang, F.K. Schneider and J.M. Maia. "*System for acquisition and processing of ultrasound signal for wood characterization*", in XVIII SICITE2013 Brazil, 2013, 0075.

Conference Reviews

- EMC2 2019
- MICPRO 2018
- ICLR 2017
- ICLR 2021

Awards/Certificates

Toastmasters International - Competent Communicator	05/2016
Eta Kappa Nu chapter beta - IEEE honor society — Alumni	05/2016
Award IIE Student of the Month	06/2015
Scholarship Brazil Science without Boarders - Masters	08/2014
Scholarship Brazil Science without Boarders - Undergraduate Exchange Study	01/2012
Tutorial education program of Education Ministry of Brazil	10/2011
Certificate CAE Cambridge English: Advanced	08/2011

Courses

- Convolutional Neural Networks by deeplearning.ai on Coursera. 05/2018
- Sequence Models by deeplearning.ai on Coursera. 04/2018
- Neural Networks and Deep Learning by deeplearning.ai on Coursera. 03/2018
- Advanced Computer Systems (Purdue)
- Artificial Intelligence (Purdue)
- Digital Systems Design Automation (Purdue)
- MOS VLSI Design (Purdue)

Skills

Coding: C, C++, Python, Verilog, Pytorch, React, JScript, Flutter, ONNX, Torchscript
Languages: English Fluent and Portuguese Fluent