NDC architecture contains a Coarse Grain Reconfigurable Array (CGRA) Streaming Engine (SE). It is a custom hardw
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reinforcement learning, data-flow mapping, coarse grain reconfigurable array
Introduction As Dennard scaling ends, big-data applications such as real-time image processing, graph analytics, and d
The tiles in the CGRA are interconnected with both a synchronous fabric (SF) and an asynchronous fabric (AF) as sho
Mapping the instructions from the computation graph of a program onto the compute elements of the SE while adherin
In this work we propose a Deep Reinforcement Learning (RL) method to explore and find optimal mappings in an unsu
This line of research is inspired by recent work that used RL for chip placement. Our problem requirement of mapping
Method In the computation graph to be mapped, each node represents an instruction that needs to be placed onto a SI
Reinforcement learning tackles optimization problems by using the REINFORCE algorithm. It trains actor and critic n
In our neural network architecture, a graph neural network (GNN) is used to create embeddings from the computation
Related work
The RL mapper tool lowers SE usability barrier. The user doesn't need to be SE architecture expert, saving training co
In [**?**], a RL method for chip placement is presented. A graph neural network to create embedding from a netlist graph
In our case, the input is a combination of computation graph, SE device state and node to be placed. Instead of only fe
Another difference from [**?**] is that our strategy is to place one computation node at a time, instead of generating a whc
Results
The implemented RL approach was able to successfully map the computation graphs for vector addition and multiply-a
This method also presents an advantage compared to baselines random search and evolutionary search (ES) methods w
Conclusion
Our RL mapper improves and increments the capabilities of the toolset used to program the SE device. It can search fo
Optimizing training methods to obtain mappings for problems like IFFT which have a bigger search space than currently us
Increasing sample efficiency of learning methods and improving the simulation environment for the SE by adding more cons
Integration of RL mapper into the SE toolset
To Robert, for the bagels and explaining CMYK and color spaces.
Research Methods
Part One
Lorem ipsum dolor sit amet, consectetur adipiscing elit. Morbi malesuada, quam in pulvinar varius, metus nunc fermen
Part Two
Etiam commodo feugiat nisl pulvinar pellentesque. Etiam auctor sodales ligula, non varius nibh pulvinar semper. Susp
Online Resources
Nam id fermentum dui. Suspendisse sagittis tortor a nulla mollis, in pulvinar ex pretium. Sed interdum orci quis metus
Nam interdum magna at lectus dignissim, ac dignissim lorem rhoncus. Maecenas eu arcu ac neque placerat aliquam. N