Low Complexity UWB Radios for Precise Wireless Sensor Network Synchronization

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***Abstract*—Wireless sensor networks are becoming widely diffused because of the flexibility and scalability they offer. However, distributed measurements are significant only if the readout is coupled to time information. For this reason, network-wide time synchronization is the main concern. The objective of this paper is to exploit a very simple hardware implementation of an IR-UWB radio for realizing an accurate synchronization system for wireless sensors. The proposed solution relies on commercial-off-the-shelf discrete electronic components (rather than on specialized transceivers). It is designed for providing accurate timestamping of the packet time of arrival (TOA) to an adder-based tunable clock, which tracks the network time reference. The comprehensive set of experimental results based on prototypes, shows a TOA detection error with a standard deviation well below 1 ns. On the other hand, in the FPGA-based prototype, the synchronization performance reaches an overall synchronization error of few nanoseconds. Finally, in order to highlight the tradeoff between timestamping accuracy, clock stability, and synchronization performance, some additional simulations have been carried out: a synchronization error in the order of 1 ns is possible, if good local oscillator sources are available in the nodes and if the adjustable clock has a sufficient resolution.**

***Index Terms*—Distributed systems, synchronization, UWB systems, wireless sensor network (WSN).**

I. Introduction

IT IS WELL KNOWN that accurate time dissemination is a crucial issue in distributed measurement and control systems. The advent of smart devices capable of extracting meaningful information from raw data [1] and the use of dedicated networks to interconnect them [2], [7] require that the communication medium transports both time and measurement information. Many results have been published that propose various approaches to tackle this problem. However, the use of the IEEE1588 standard is nowadays universally accepted as the reference solution [3]. Simulated, analytical, and experimental results show the achievable accuracy using IEEE1588 and illustrate how influencing quantities degrade performance [4], [5].

Recently, wireless sensor networks (WSNs) became feasible at reasonable prices, also due to availability of powerful but low-cost device derived from the consumer market [6], [7]. They are gaining popularity because of their performance, that is comparable with that of many wired solutions, and also because of their extreme scalability and enhanced flexibility [8]. For such distributed applications, time awareness is a very important issue—not only to coordinate coherent data acquisition by several nodes deployed in the same area [9], but also to coordinate protocol activities (e.g., wakeups or transmissions), to save energy and communication bandwidth [10]. In particular, the adoption of impulse-radio-based ultra-wideband technology (IR-UWB) has been suggested to fulfil these requirements, due to its potential low complexity and low cost [11]. In addition, UWB noise-like signal properties simplify coexistence with other systems and ensure resistance to severe multipath and jamming. Finally, IR-UWB solution has very good time-domain resolution thus allowing for precise location and time synchronization.

Real-world devices measure time using local clocks driven by low-cost quartz oscillators. Unfortunately, even if the accuracy of such oscillators is in the range of only a few ppm, inevitable phase noise and drifts (e.g., due to aging or thermal effects) cause local time readings to quickly diverge. In order to spread and maintain a common notion of time across the whole network, time synchronization procedures must therefore be adopted [12]. While solutions for wired networks have existed for many years, approaches tailored to the needs of WSNs are relatively new [13]. Among them, the Reference Broadcast Synchronization (RBS) [14], the Timing-Sync Protocol for Sensor Networks (TPSN) [15] and the Flooding Time Synchronization Protocol (FTSP) [16] are the most prominent ones. An analysis of their performance is given in [17].

As a matter of fact, synchronization protocols do not provide synchronization *per se*. They only establish rules about how

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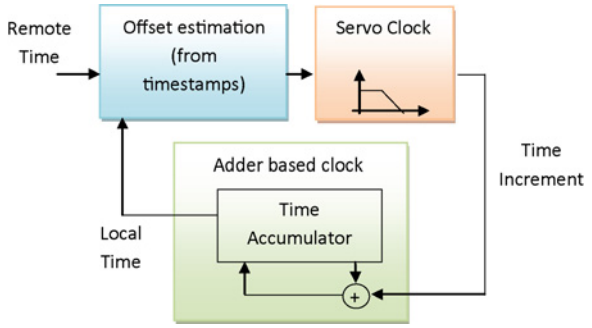

Fig. 1. Correcting the local clock in order to follow the reference using an adder-based clock.

time information must be exchanged among the nodes in the network. Since WSNs are typically packet-based, there is no continuous, global signal available that can be used to derive timing information. Synchronization is therefore performed on a per-packet basis, exploiting timestamps. These timestamps represent individual snapshots of the nodes' local time and are subsequently used to calculate, in a decentralized way, a more accurate time estimate for each node. The quality of the timestamping procedure is therefore crucial. The more accurate it is, the more accurate the resulting synchronization will be.

Drawing accurate timestamps is not straightforward, particularly in wireless networks. The aim of this paper is to present a real-world prototype for synchronization using IR-UWB technology, and a testbed to verify its performance. Section II presents a brief resume of time synchronization, with emphasis on wireless network issues. In Section III, the design and implementation of low-complexity UWB nodes are described. Section IV discusses the use of the UWB radio for accurate timestamping. In Section V, the experimental setup and results are described. Finally, some conclusions are drawn.

II. Network Synchronization

Since the advent of distributed systems, clock synchronization issues arise from inevitable clock drifts that are difficult to model and correct [18]. Inherent errors stem from the message delay through the network. For this reason well-known synchronization protocols, like the Network Time Protocol (NTP) or the IEEE1588, define means to estimate the delays. These delay measurements are typically round-trip measurements where the egress and ingress times (timestamps) of messages are recorded for calculating the residence time (i.e., the time a message is stored on a node before being forwarded) and the actual transmission delays. Once the time difference between clocks is estimated, the unsynchronized clock can be adjusted to reflect the time reference scale.

An ordinary digital clock is based on a counter, fed by an oscillator running at the nominal clock frequency f_0. In order to be adjusted for compensating the estimated offset and drift, the oscillator tick sequence must be altered, using suitable hardware-based mechanisms. One possible solution is to use a voltage controlled oscillator (VCO) [19]; another possibility is to remove or insert pulses of an oscillator running at a multiple of the nominal frequency, but this is usually considered an inefficient strategy requiring a huge system bandwidth [20]. Most practical solutions use an adder-based clock (ABC), as in [21] and [45]. This replaces traditional counters with: a time accumulator register containing the local time, a time increment register, and a large high-speed adder. At every update period, (also called G_t, time granularity) the content of the increment register, as obtained from a servo-clock-based control loop, is added to the time accumulator register, producing a new value of the local time. Changing the content of the time increment register leads to a modification of the local clock slope. If G_c (clock granularity) is the resolution in the increments, we usually have $G_c << G_t$, allowing easy adjustment of the ABC clock drift. A graphical description of this adjusting strategy is given in Fig. 1.

A. Synchronization Accuracy

As described in [22], the synchronization accuracy ε can be expressed as

$$\varepsilon = C_1 \cdot e + C_2 \cdot G_c + C_3 \cdot G_t + C_4 \cdot P \cdot d \qquad (1)$$

where C_i, $\mathrm{i} = 1.4$ are (small) integer constants depending on the adopted synchronization algorithm, e is the error in the timestamp estimation, G_c and G_t are the clock and time granularity, respectively, and $P \cdot d$ is the clock drift cumulated in the resynchronization period (computed as the length of the resynchronization interval P times the oscillator drift d). In practical realizations, the G_t and G_c terms depend on how the local adjustable clock is implemented. For instance, when an ABC is considered, the clock granularity is determined by the accumulator register width, i.e., the local time resolution, while the time granularity coincides with the period of the oscillator driving the ABC update.

The timestamps are always affected by jitter originating from various sources, such as fluctuations in the signal propagation time, variations in the signal processing times, or different execution times of the software stacks. As previously seen, this jitter impairs the achievable synchronization accuracy and should be kept as low as possible. Generally, the further down in the communication protocol stack one can draw the timestamps, the smaller the jitter is.

In wired networks, software-only implementations exploiting advanced statistical methods can yield accuracies in the $10\,\mu$s range [23]. If one implements the timestamping in hardware on the medium access level, accuracies spanning from the tens of nanoseconds [24] to the sub-ns range [25] can be achieved.

B. Synchronization in the Wireless Domain

One general advantage wireless channels have over wired ones is that they are inherently symmetric, while cables (especially for full duplex Ethernet) may be asymmetric, which leads to an offset in the synchronization that may not be recovered [26]. However, additional challenges must be met. Especially for WSNs, their peculiar characteristics strongly affect requirements in time synchronization protocols: scalability, low cost, and low power consumption are compulsory.

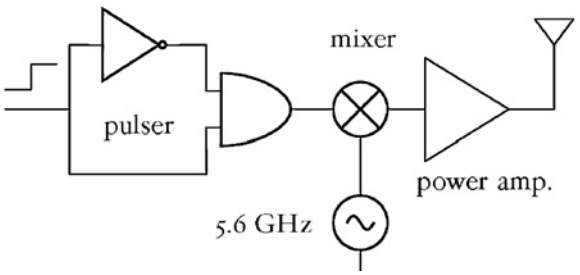

Fig. 2. AHCMOS-based pulse generator block diagram.

Nevertheless, the basic operation principles for synchronization are the same as in the wired case. Again, the more accurate the timestamping procedure is, the more accurate the time synchronization becomes. In particular, packets include a preamble for timing acquisition (i.e., a sort of well-known training sequence) and a subsequent payload separated by a frame delimiter. Both preamble and delimiter are good candidates as the timestamping point [21]. For instance, if wireless local area network (WLAN) technology is considered, a purely software-based timestamping may achieve sub-μs accuracy [27]. If more effort is spent and the timing information is extracted from the raw signal, performance can be improved, like in the wired case.

One principal problem in obtaining precise timestamping in WSNs signals is limited bandwidth. Signal slopes are typically very smoothed, which also limits the performance of correlation filters used for detecting, for instance, the preamble. UWB has an advantage in this respect, because of its wider signal bandwidth. As an application example, a wireless extension of the LXI protocol based on UWB radios was proposed for remote instrument triggering, since the possibility of hardware triggering that is used in many wired busses [28] is not available for wireless connections. However, it must be recalled that only few commercial devices based on low cost IR-UWB radios are available and, despite their localization capabilities are widely remarked, their time synchronization accuracy is usually poorly documented.

C. Synchronization and Localization Issues

Localization and geo-referencing has gained more and more importance over the last years due to the wide diffusion of large distributed systems. There are several commercial real time localization systems (RTLS) available, such as the products by UbiSense and Ekahau [29] that have been proposed for applications like asset management or patients monitoring. Since the aim of the timestamping procedure is an accurate determination of the time-of-arrival (TOA) of an incoming wireless signal, a very close relationship exists with the problems associated to localization [30]. In the past, these two problems have been investigated separately: synchronization mainly from the protocol design point of view and localization mainly from the signal processing point of view. Nevertheless, TOA measurements in a wireless infrastructure can also be used for localization purposes [31], [49] and have been shown to be superior to methods based on received signal strength [32]. Because of its flexibility and the favourable properties, including precise TOA estimates and good immunity against dense multipath scenarios, the IR-UWB technology is also a suitable candidate [33]. In particular, the use of low-complexity and cost effective IR-UWB transceivers is intriguing for WSNs, since it allows the development of a node possessing communication, synchronization, and ranging capabilities. For example, the IEEE802.15.4a [34] amendment to IEEE802.15.4 physical layer specifies the IR-UWB modulation for localization purposes; some (few) commercial products based on this technology are also available today [35]. However, this standard only takes into account issues of round trip time estimation and does not provide an effective timestamping mechanism or an explicit support for time synchronization protocols; for instance, the ranging counter wraps every 70 ms, which is a too short period for reliable synchronization. Furthermore, it is explicitly stated that the practical implementation of the counter is beyond the scope of the standard.

III. Cost Effective UWB Nodes

UWB technology dates back to the early 1960s within the field of time-domain electromagnetics. Only in the recent past, with the advent of monolithic microwave integrated circuits (MMICs), its use for communication purposes has been eased and suggested.

The transceiver used in our experiments is entirely designed and realized using commercial off-the-shelf-components. The proposed architecture exploits a 5.6 GHz homodyne approach. In particular, since long UWB pulses repetition periods (PRP) are tolerable in WSN scenarios where small data packets are exchanged, non-coherent peak detection is applicable and allows simplifying the receiver design. On the other hand, the transmitter implements a logic pulser. The transceiver is fully described in [36] for positioning applications. Here, only the main building blocks are briefly detailed to ease readability and to discuss their contribution to inaccuracies when time synchronization and non localization is the main processing goal.

A. Pulser

The transmitter is based on a UWB pulse generator and an up-converting mixer using a 5.6 GHz sinewave carrier. The pulse generator is realized by exploiting the race condition inherent in the two logic port networks shown in Fig. 2. The AND gate generates a short glitch, whose duration mostly depends on the inverter propagation delay, while its transition time is determined by the rise time of the gate. For more details, refer to [37]. Despite the variability due to discrete component implementation, the choice of advanced high speed complementary metal-oxide (AHCMOS) logic gates has allowed the realization of several pulsers capable of providing a pulse bandwidth in the order of 1 GHz, with a rise time lasting few hundreds of picoseconds, as experimentally quantified. Obviously, an integrated solution could lead to even better results because of reduced parasitic effects and a more accurate control of technology processes.

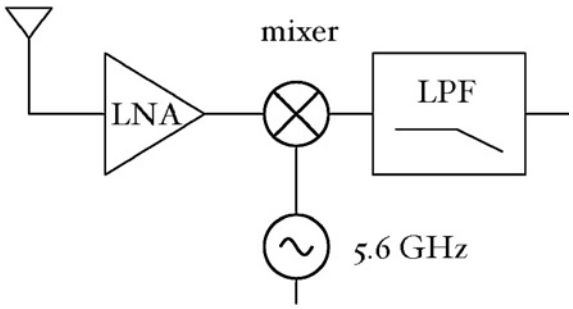

Fig. 3. Down-mixing stage block diagram.

From a theoretical point of view, pulse-based UWB transmission does not strictly require an additional carrier to be transmitted over the air, so that it can also be considered as being a baseband approach. Nevertheless, pulses are usually modulated onto a carrier and run through some conditioning stages, in order to be compliant with spectrum emission limits and to reduce the physical dimensions of the antennas. In the proposed approach, a local oscillator shifts the pulse spectrum around the 5.6 GHz region. Finally, a power amplifier completes the transmitting section.

B. Detector

The receiver architecture consists in a down-mixing stage, shown in Fig. 3, and in a baseband stage.

In the former, a low-noise amplifier drives the mixer used to down-convert the signal into the baseband. A 5.6-GHz sinewave is provided by the local oscillator. A low-pass filter preserves meaningful information discarding interferers and wideband noise. The subsequent baseband block (not shown in Fig. 3; for more details refer to [36]) includes a baseband amplifier followed by a commercial peak detector, and by a fast comparator. An intermediate low-noise amplifier ensures a good signal-to-noise ratio (SNR) over the whole spectrum range of interest.

C. Threshold Setting

Performance of the detector greatly depends on the choice of the comparator threshold in the output stage. In particular, this threshold should be dynamically modified according to the SNR which may vary due to external interferences and/or variable distance between the transmitter and the receiver. From the hardware point of view, this is not a real problem; the remaining logic block of the transceiver used to demodulate the signal can also be used to generate this threshold. However, in this paper the focus is on synchronization capability, and the threshold has been fixed to an optimal value according to the experimental scenario described in Section V. Thus, the effect of threshold variations on timestamping accuracy can be ignored. Alternatively, a saturation approach can be applied, as suggested in [38] where a detector similar to the one adopted in the present work is used.

In addition, it must be stressed that the main characteristic of the proposed architecture is low complexity and low cost. In the literature, several algorithms have been proposed to dynamically adapt the threshold. Just to mention one of them, consider [39] in which the well-known constant false alarm rate, originally developed for radar applications, is exploited. However, the implementation and the improvement of such techniques is out of the scope of this paper and would increase the complexity of the receiver logic and thus the overall cost with relatively small benefits.

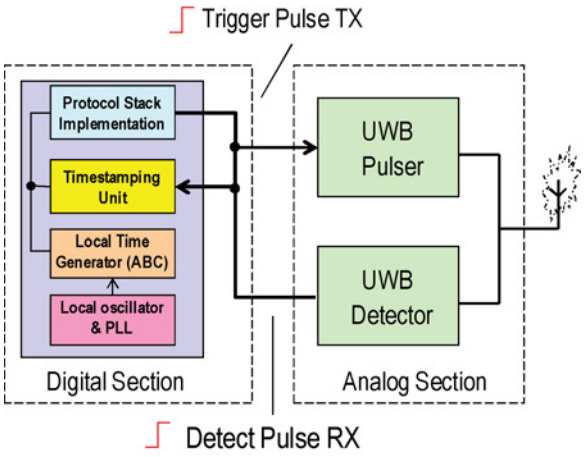

Fig. 4. Block diagram of the proposed transceiver.

D. Actual Wireless Node

The previous sections describe the detector and the pulser, which are the analog part of the transceiver. In [40], the authors follow a hybrid approach, jointly using these analog blocks with a traditional WSN transceiver. However, if a real transceiver must be implemented, some forms of digital logic must follow/precede these blocks to (de)code the user data stream, to collect timestamps, and to implement the adjustable clock (e.g., an ABC). A simplified block diagram is shown in Fig. 4. In order to limit the node complexity, a simple solution based on the use of a microcontroller (μC) can be realized for protocol stack implementation, e.g., including the modulation scheme detailed in the next section and other upper layers. Timestamping and software adjustable clock could be implemented exploiting the embedded time processing unit (TPU) of the same μC, but usually performance is inadequate. A more accurate external time to digital converter (TDC) may be adopted, based on digital delay line, which can be a commercial device (e.g., consider the GP2 [40] from Acam) or implemented in a FPGA. In addition, it must be noticed that well-known interpolating techniques based on fine and coarse time interval measurements [41] can be used to estimate the incoming packet TOA with a resolution in the ps range and an accuracy mainly limited by the stability of the local clock.

Obviously, this is the most critical hardware section from the time synchronization perspective, as clearly shown in (1).

IV. UWB TIMESTAMPING

In this section, a brief description of the adopted modulation scheme is provided and the timestamping estimation procedure is described. As stated before, the IR-UWB is probably the

simplest solution to implement an UWB transceiver. Usually, IR-UWB is associated with time hopping (TH) coding for multiple medium accesses, as described in [42]. Generally speaking, this technique assigns a fixed length time-slot (i.e., the aforementioned pulse repetition period) to each bit of the user data stream; in the actual transmission different network nodes add a different offset in the pulse position within the time-slot. Regarding user data transmission, the easiest modulation is the On-Off Keying (OOK). A general description of the baseband signal $S\ (t,\ i)$ of an individual transmitter i at time t is given by

$$S(t,i) = \sum_j A_P \cdot p(t - jT_{PRP} - T_{TH}(t,i)) \quad t \in \Re, \quad i \in [0, N-1],\ N: \text{number of nodes} \tag{2}$$

where $p\ (\cdot)$ is the UWB pulse function, T_{PRP} is the pulse repetition period, $T_{TH}(\cdot) < T_{\text{PRP}}$ is the time offset introduced by the node according to the assigned $TH\ (t,\ i)$ coding, and $A_P \in [0,\ 1]$ represents the pulse amplitude. The signal (2) can easily be generated by a time-slot clock generator, a delay generator, and a simple logic controller, e.g., using a μC as described in Section III. Obviously, from the synchronization point of view, performance is mainly dictated by the accuracy of the reference clock source.

A widespread approach to solve the synchronization issue is to start the transmission with a well-known preamble, which is part of the data packet header. This implies that the expected inter-arrival time ΔT of consecutive pulses in the preamble is fixed and known and can be used to discard timestamps excessively affected by noise. In particular, building on what is suggested in [43], the proposed timestamping algorithm starts with the detection of the first threshold crossing at the receiver side, which is supposed to be the beginning of a new data packet. If the packet is detected starting from the ith bit in the preamble sequence (i.e., the timeout for the expected arrival time of previous i -1 bits has expired), the corresponding bit timestamp $T\ (i)$ is computed according to

$$T(i) = T_i - (i-1) \cdot \Delta T \quad i \in [1, P-1],\ P:\ \text{number of bits in the preamble} \tag{3}$$

where T_i is the estimated TOA of the ith bit. The timestamp estimation is considered correct if more than half of the preamble bits are correctly received, i.e., their arrival time is within the guard time window. Such an observation window is a tradeoff between the desired accuracy and the SNR at the receiver side. Starting from this set of TOAs (one for each pulse transmitted in the preamble), the actual packet timestamp T can be finally obtained by a simple averaging procedure. In such a way jitter effects can easily be mitigated. It must be also noted that the transmitter can purposely add some jitter to control the statistical properties of the jitter at the receiver side (e.g., as it usually occurs with non-subtractive dithering applied to AD converters [44]).

In addition, it must be highlighted that the availability of several ΔT computed within the same preamble sequence allows to simultaneously estimate the local clock drift Δf_{CK}. In particular, single clock drift estimates between the receiver and the transmitter result from the ratio between the measured inter-arrival time between the last correctly detected bit timestamp and the initial one and the expected interval imposed by the transmitter. In order to reduce the variability, the local clock drift estimation Δf_{CK} is actually obtained as the average of these ratio values over several incoming data packets. This drift compensation has a very good behavior since the short-term time drift is approximately linear.

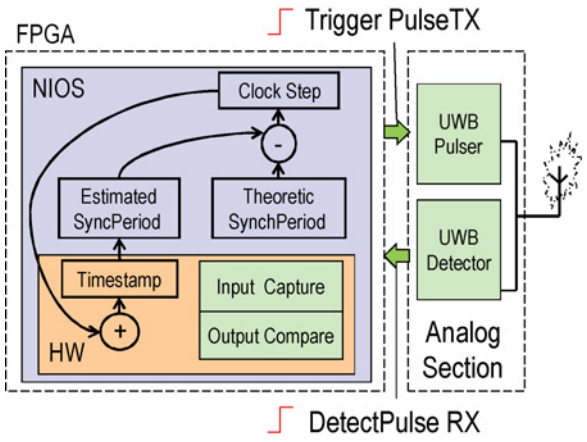

Fig. 5. Actual implementation of the UWB transceiver.

V. Experimental Results

According to (1), synchronization accuracy is affected by timestamping accuracy and resolution, by local clock adjusting capability and by resynchronization interval duration. In this paper, we start focusing on the TOA estimation mechanism, which is the basis for accurate timestamping, and then the synchronization performance is studied.

The aim of the experiments described in this section is to verify that a very simple hardware implementation, based on discrete electronic components (and not on devices engineered for mass production) allows accurate signaling of packet TOA. The proposed transceiver (Fig. 4) has been implemented in a practical prototype using off-the-shelf-components. The analog section has been realized using discrete components to satisfy low-cost, low-complexity constraints. The PCB hosting active components has a conventional copper coating (thickness 35 μm) and a FR4 substrate and has been realized using an in-house PCB prototyping machine. Finally, the IR-UWB analog section has been interfaced to a digital section based on FPGA.

The rest of the section is organized as follows; first a preliminary description of the prototype and experimental test bench is resumed; then the capability of the prototype to behave as a transceiver with enhanced TOA-detection is tested and finally the prototype synchronization accuracy is discussed.

A. Prototype Description and Experimental Test Bench

The generic architecture described in Fig. 4 has been modified as depicted in Fig. 5. An FPGA (Stratix II EP2S60F672C3 from Altera) is used to implement the TPU and the ABC; it also hosts the softcore processor (NIOS II) running the

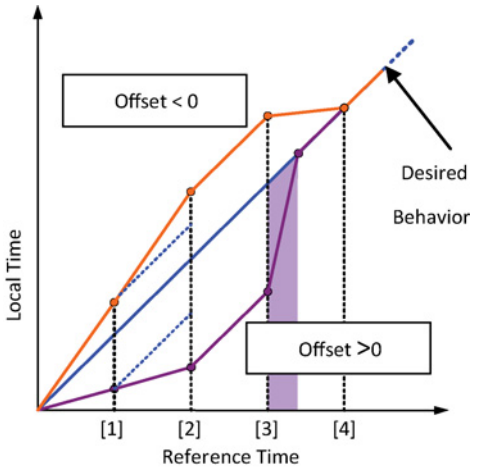

Fig. 6. Example of step update and offset compensation of the ABC clock.

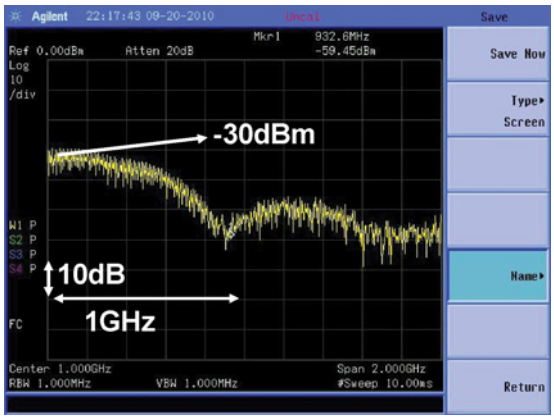

Fig. 7. Spectrum of the pulser output.

synchronization algorithm and the communication protocol stack. The step correction and offset compensation mechanisms are shown in Fig. 6. The vertical dotted line represents periodic synchronization events. In particular, the clock rate is corrected in the interval between the events 2 and 3, while the compensation of the offset starts after the event 3, the so called amortization phase [45], in which the step is modified in order to quickly correct the offset. The FPGA runs at 100 MHz, and the time granularity (G_t) is 10 ns.

The analog section uses the detector LTC5536 by linear technology. According to data reported in [46], the LTC5536's RF detector is optimized as a positive peak detector, thus it responds to a rising signal at the RF input more rapidly than to a falling signal. In particular, the minimum propagation delay is about 20 ns for rising edges and 50 ns for falling edges. Clearly, these delays determine the fastest allowable PRP, i.e., the maximum raw bit rate of the proposed system.

The signal spectrum at the output of the pulser (at the mixer input, Fig. 2) has been measured with an Agilent N9320B spectrum analyser and is shown in Fig. 7. When the signal is analyzed in the time domain, it features a rise time of less than 1 ns.

In order to demonstrate the prototype effectiveness, some UWB experiments were carried out in our laboratory with the experimental setup of Fig. 8. The signal at the output of the transmitter mixer is shown in Fig. 9, as obtained by acquiring several consecutive pulses by means of the equivalent–time sampling oscilloscope Wavexpert 100H by Lecroy. Due to acquisition method, the signal envelope is more interesting than fine details in this figure; the received pulse has a similar shape but also includes replicas due to multipath induced effects [47].

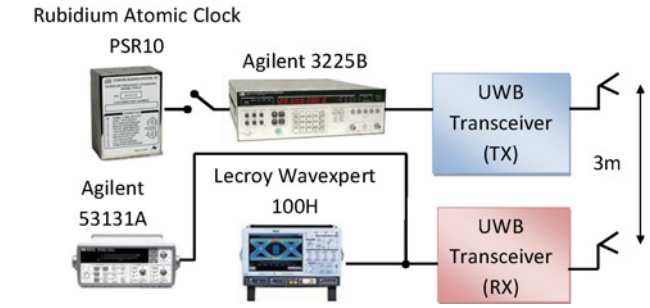

Fig. 8. Experimental setup to evaluate the UWB systems.

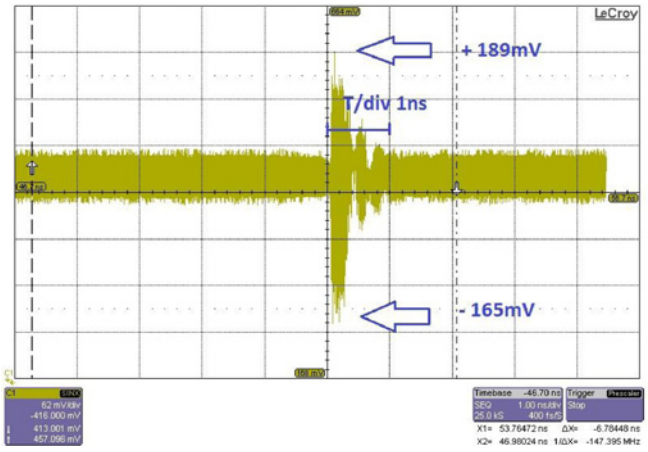

Fig. 9. Transmitted UWB pulse (captured using an equivalent time oscilloscope with 20 GHz analog bandwidth, 20 dB attenuation and 10 MS/s sampling rate).

B. Using the IR-UWB Radio for Data Communication

The same test setup shown in Fig. 8 has been adopted to verify the ability of the transceiver to handle the transmission and reception of a generic user data stream. Two nodes separated by 3 m (in order to ensure good SNR) exchange a pre-programmed data sequence modulated according the TH-OOK scheme, and the received sequence is compared with the transmitted one. In Fig. 10, the receiver comparator output derived from the transmission of the user data byte 0xD3 by two different nodes is shown as acquired by the oscilloscope. The time slot duration is $T_{\mathrm{PRP}} = 3\ \mu$s and the time hopping delay is $T_{\mathrm{TH},1} = 0$ s for the transmitting node and $T_{\mathrm{TH},2} = 100$ ns for the second one, respectively (the output is held at the high level by the detector itself). This experiment has confirmed the capability of the proposed system to finely regulate transmission instants to implement TH access strategy.

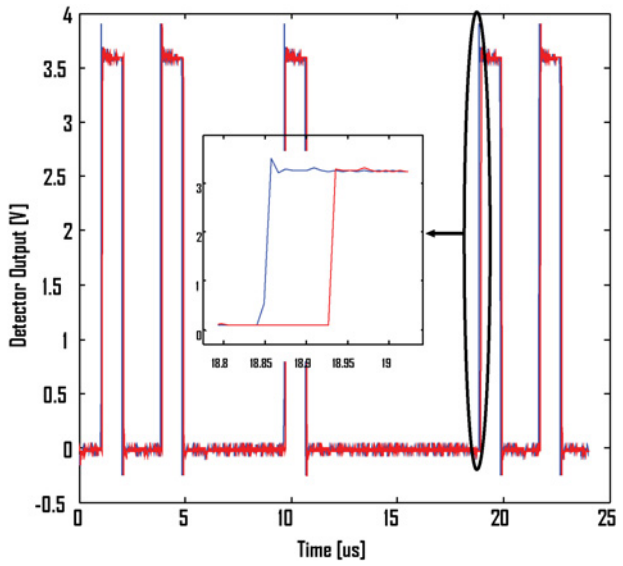

Fig. 10. Reception of a user data byte (0xD3); the signal acquisition is performed at the output of the comparator embedded in the detector; blue line is a node having $T_{TH} = 0$ s, red line is a node having $T_{TH} = 100$ ns.

C. Detection of Time of Arrivals

To analyze the performance of the TOA detector, a regular pattern of 1000 consecutive UWB pulses is sent by the transmitter with a $T_{PRP} = 3.3$ μs. A very stable frequency reference is provided by a Stanford Research PRS10 rubidium atomic clock with a 10 MHz output signal and a short-term stability of $5 \cdot 10^{-12}$. Thus, the overall observation time is 3.3 ms, and the experiment allows verifying the performance and repeatability of the proposed timestamping system. The output of two different nodes, which simultaneously receive the same pulse stream, was collected by using a digital counter (Agilent 53131A) and compared. The differences in T_{PRP} measurement results, as provided by the counter, represent an error whose distribution is shown in Fig. 11. An average error of 326.73 ps and a standard deviation of 15 fs resulted from the first node, while the second one showed an average error of 326.77 ps and a standard deviation of 16 fs. The average error takes into account the effect of delays introduced by the signal conditioning stages, while the standard deviation (comparable in the two nodes) provides an estimate of the clock stability, i.e., the actual lower bound for synchronization accuracy in the proposed solution. For the sake of completeness, it must be highlighted that these results are in good agreement with those obtained using UWB radios developed in the PULSER II European project [48], where a more complicated and expensive approach was used.

In order to better verify the short term stability of the detector output, a longer acquisition has been performed over an overall observation time of more than 20 s, reducing the repetition rate to $T_{PRP} = 1$ ms. The signal has been treated as a clock and the Allan variance has been roughly estimated, as shown in Fig. 12, confirming the very good performance, especially if compared with the stability characteristic of the PSR10 atomic clock reported in [25], [49].

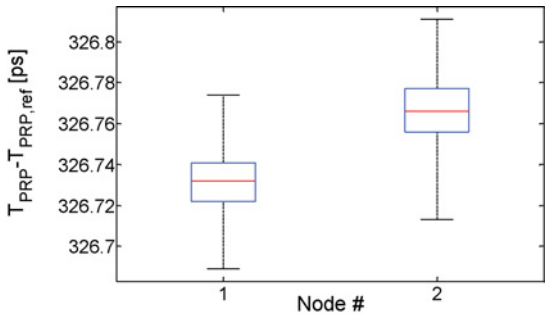

Fig. 11. Box-plot of the detector output for node 1 and node 2.

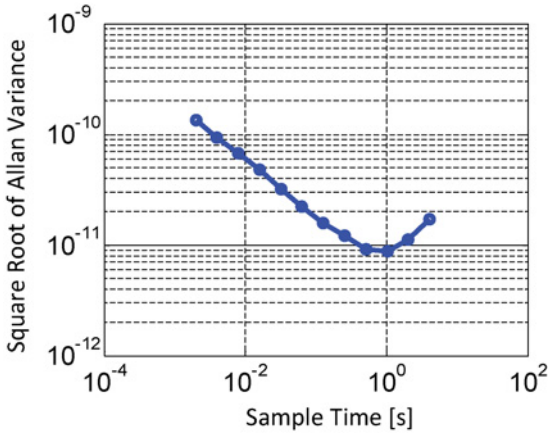

Fig. 12. Stability of the pulse detector output.

D. Evaluation of Prototype Synchronization Accuracy

An experiment has been carried out to verify the synchronization performance; two different boards have been used in order to verify the repeatability. The experimental setup is shown in Fig. 13; the 10 MHz reference signal of the Agilent 53131A counter is fed to the Agilent 33120A function generator, which, in turn, creates the 1-PPS input clock signal for the prototype. The counter is used for the measurements of the 1-PPS output of the prototype, so that a ratiometric approach is adopted and the instrument jitter can be neglected. Offset errors, evaluated using the counter in the Start-Stop mode, are shown in Fig. 14. Since, with respect to the reference, the error could be positive or negative, a digital delay line ($\Delta = 100$ μs) has been implemented in the FPGA and added to the 1-PPS output signal and numerically subtracted. The maximum offset deviation of both boards is well below 100 ns over 4000 measurement samples (i.e., 2 hours). In particular the average error is 15.39 ns (with a standard deviation of 9.29 ns) for Board 1 and 8.53 ns (with a standard deviation of 6.73 ns) for Board 2. The worse behavior of the first board with respect to the second one, is probably due to different local oscillator crystals.

Results show that despite the very precise detection of the TOA, the time synchronization error remains in the ns range. Clearly, the bottleneck in the prototype synchronization system is represented by the resolution of the timestamping mechanism and of the ABC tunable clock, which frustrates the high performance of the UWB-based TOA estimation (described in Section V-C).

TABLE I
STANDARD DEVIATION OF THE SYNCHRONIZATION ERROR IN THE SIMULATED EXPERIMENT

STD of the synchronization error	$\sigma_\theta = 10^{-7}$s $\sigma_\gamma = 10^{-8}$	$\sigma_\theta = 10^{-7}$s $\sigma_\gamma = 10^{-9}$	$\sigma_\theta = 10^{-9}$s $\sigma_\gamma = 10^{-9}$
$\sigma_{TS} = 2 \cdot 10^{-14}$s	103.3 ns	103.3 ns	1.0 ns
$\sigma_{TS} = 2 \cdot 10^{-11}$s	103.3 ns	103.3 ns	1.0 ns
$\sigma_{TS} = 2 \cdot 10^{-8}$s	108.6 ns	108.6 ns	31.3 ns
$\sigma_{TS} = 2 \cdot 10^{-7}$s	330.2 ns	330.2 ns	312.2 ns

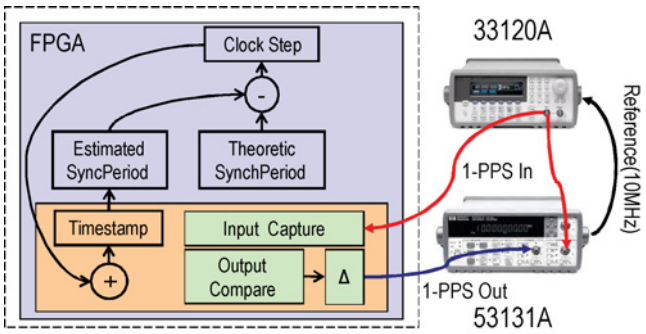

Fig. 13. Experimental setup for tunable clock characterization.

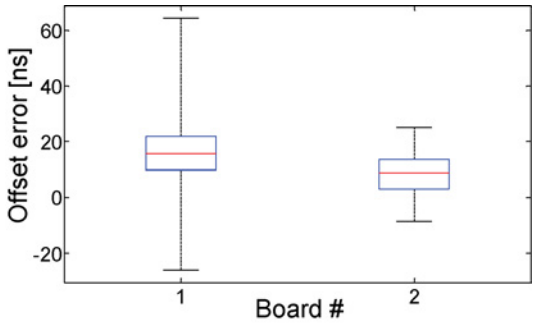

Fig. 14. Offset error of the realized synchronizing block.

E. Estimation of the Best Achievable Synchronization Accuracy

In order to study the best achievable synchronization performance, a final simulated experiment has been performed. The goal is to show the synchronization capability in a well-defined scenario, taking advantage of both *a-priori* knowledge and of the possibility to control influencing quantities. In particular, using the simulation data, it has been possible to evaluate easily the effect of different values of timestamping accuracy and clock stability. The simulated Simulink-based model, shown in Fig. 15, exploits a proportional-integral (PI) servo clock as in the PTPd solution [50], and implements a tunable clock with an ideal resolution (i.e., only limited by the MATLAB arithmetic).

The local clock behavior is described by means of the well-known state-variable model [51], based on the offset θ and the skew γ. Uncorrelated white Gaussian noise has been added to θ, γ and also to the timestamp; all of these influencing quantities have zero mean and standard deviation σ_θ, σ_γ, and σ_{TS}, respectively. Several trials have been carried out changing these parameters: the results are reported in Table I, assuming a synchronization interval of 1 s and an overall observation time of 30 min (the initial transient is eliminated). Results confirm

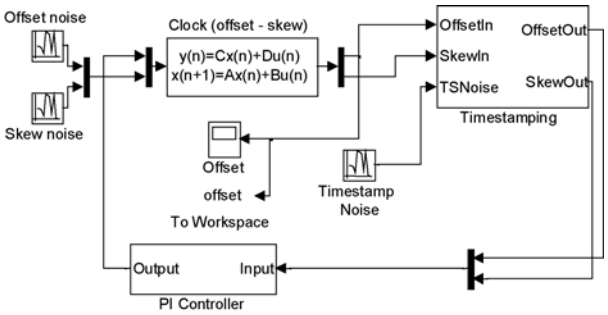

Fig. 15. Model of the synchronizing block.

the effectiveness of the proposed approach and allow estimating system complexity for a desired time synchronization error. As expected, increasing the timestamping accuracy allows decreasing the standard deviation of the synchronization error, until saturation is reached, depending on the intrinsic performance of the unregulated clock. This behavior was expected, since, even with an accurate timestamping mechanisms, such as the one described in this paper, a slave clock cannot be synchronized better than its intrinsic stability [51].

VI. CONCLUSION

Time synchronization is a big issue in all distributed measurement systems; both communication protocols and measurement ordering require all nodes to share a common sense of time. Referring to wired communications, many solutions were proposed in the past, able to push accuracy down to the sub-ns range. On the contrary, despite the increasing interest in WSNs due to their flexibility and scalability, very precise synchronization mechanisms for these systems are still missing. The main problem is the determination of the time-of-arrival of the line-of-sight signals, suffering from non-idealities of the transmission medium (e.g., multipath). The aim of the work discussed in this paper was to propose and characterize an accurate wireless time synchronization system despite the exploited low-cost methodologies. In particular, UWB-IR techniques were used to detect the TOA of incoming wireless messages. Well known results available in the literature confirm the ability of similar systems to minimize the channel non-idealities, but usually require expensive setup. We have been able to obtain very good short term performance (stability of about 10^{-11} with an observation interval of 1 s) in the message detection using commercial off-the-shelf components; several measurement campaigns have shown that the actual system bottleneck is represented by the timestamping block and tunable clock implementation. In particular, a simple ABC clock allows obtaining overall synchronization accuracy in the

ns range. Further developments will improve timestamping and clock granularity while preserving low system complexity. However, simulation results presented in the paper showed that the actual limiting factor is the clock stability. Hence, to further improve the synchronization accuracy, better clocks will be ultimately needed.

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