High Precision Wireless Synchronization Receiver for M-Sequence UWB Radio Systems

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***Abstract*—This work deals with M-sequence UWB Radio architectures for high-precision indoor localization and low data rate radio transmission. So far, UWB M-sequence devices were only used in Radar mode which applies wired synchronization between transmitter and receiver. Radio systems have different architecture since receiver and transmitter are spatially separated from each other. This paper focuses on the phase and frequency synchronization between the clock of the transmitter and receiver. The proposed architecture deals with 10 gigachips per second achieving a high frequency bandwidth ranging from DC upto 5 GHz or consequently from 5 GHz to 15 GHz depending on the device structure. It is very costly and power demanding to process such signals in the digital domain to perform the synchronization. Thus, a low power and low cost technique is introduced using analog blocks for the synchronization achieving a maximum time error of 5 ps between the received and reference M-Sequence waveforms.**

***Index Terms*—M-Sequence, noise modulated signals, SiGe HBT, ultra wide band (UWB), wireless synchronization.**

I. Introduction

Ultra Wide Band (UWB) radar and localization systems are becoming more reliable and extensively present in several applications nowadays as they are suitable for a multitude of indoor and outdoor scenarios. Various methods exist to synthesize a proper transmitted signal covering the wide frequency range. A famous applied method is the impulse response technique. A train of short pulses in the nanosecond range are generated which spread in the spectrum. To spread enough energy over the UWB frequency range, high peak powers for the short pulses are used. This method requires highly linear transceivers otherwise they will saturate. The UWB M-sequence principle [1] is a radar principle which promotes monolithic integration of system components since high-voltage peaks, as in classical impulse systems, are avoided. Furthermore, the properties of the transmitted waveform signal enable a measurement system of very high time accuracy due to the used system architecture in connection with correlation processing [2]. So far, this measurement system is solely used in radar applications with wired synchronization between transmitter and receiver. In several applications as precise indoor localization or vital sign detection for ambient assisted living (AAL) purposes [3], the transmitter and the receiver are separated from each other. Thus, a wired synchronization will either hinder the device handling or it will even prevent its use. A practical example can be illustrated in rescue missions after an earthquake, UWB radar may be applied to detect survived people buried by rubble. This requires the distribution of several antennas over the rubble hill which will cause some practical problems for the rescue crew if the antennas must be mutually wired.

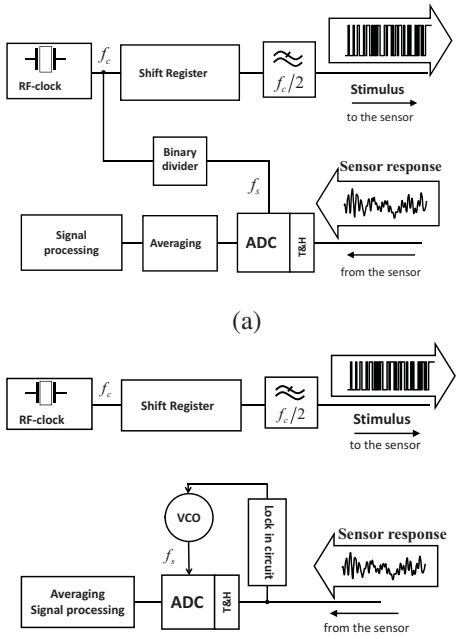

Fig. 1. Basic structure of an UWB M-sequence using wired synchronization (a) and wireless synchronization (b).

In order to open up also such applications for the M-sequence principle, a wireless synchronization is needed which would also enable the combination of sensing tasks with low data rate transmissions. First ideas of analog wireless synchronization of an UWB M-sequence device are introduced in [4] on the system level. This paper will discuss some new aspects of system layout and practical implementation.

A. The M-Sequence Principle

The classical M-sequence principle is depicted in Fig. 1.a. In this paper, we only refer to the baseband approach. Extensions

for arbitrary frequency bands can be found in [5]. A stable single tone RF-clock generator controls rigidly the whole system. It is one reason for the high timing performance of the device. The high speed digital shift register generates the ultra wide band pseudo noise code which is typically an M-sequence, but it can generate another codes as in [6]. This transmitted signal serves as stimulus of the device under test. The scattered response signal is captured by a sub-sampling approach by capturing the data at the rate 2^{-m} of the chip frequency, m is the order of the binary divider, in order to reduce the speed requirements onto the receiver electronics. The sampling clock is gained from a binary divider which is pushed by the same clock generator as the shift register. The captured signal is synchronously averaged and subjected a correlation processing. The reference signal for the correlation represents the known code of the shift register which is digitally stored in the receiver. The coherence between the stored reference and the digitized response signal is guaranteed by the binary divider. If we want separate the transmitter from the receiver, we have to cut the connection between the RF-clock and the ADC clock (Fig. 1.b) without losing the coherence between reference and response signal. In order to achieve high noise suppression, the coherence between both signals has to be maintained over a comparatively long time. This is hardly to be done by two free running oscillators. Hence we need locking mechanism, which pulls the sampling rate to the correct value independently from temporal variations of the RF-clock or Doppler effects due to moving transmitter or receiver.

B. The UWB M-Sequence synchronization

The synchronization process has to be very precise to have correct data acquisition for accurate sensing. Moreover, the transmitted signals suffer from many reflections and multipath fading which makes synchronizing to the received signal more complicated. Synchronization is accomplished using either digital or analog blocks. The digital synchronization is done by different architectures like Rake receivers, Delay-Locked Loop (DLL) or Tau-Dither Loop (TDL). The disadvantage of using such methods is the extra effort done to sample the received analog signal. Sampling wide bandwidth signals increases power consumption and costs to build an analog to digital converter. Thus, doing the synchronization in the analog domain is more efficient and consumes less power.

A new architecture similar to the DLL that combines both coarse and fine synchronization in one block is discussed. This architecture is presented as a solution for accurate wireless synchronization and introducing a solution for multipath fading. The architecture is implemented using analog correlators, delay elements, shift registers and Voltage Controlled Oscillator(VCO). The proposed architecture takes the advantage of the unique property of the M-sequence. The auto-correlation of the M-sequence is an impulse response with a certain amplitude. Thus, correlating the received signal with the reference M-sequence locally generated in the receiver, an impulse signal is produced which can be detected by a simple comparator.

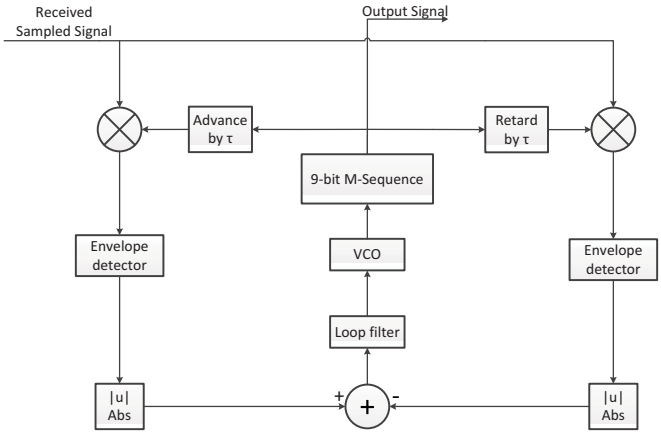

Fig. 2. The normal DLL architecture.

II. Concept of the Proposed architecture and implementation

The work presented here is investigated on a 9-bit M-sequence generator presented in [7] derived with a 5 GHz clock producing 10 GS/s. Before going into the details of the proposed modified DLL, a brief explanation of the normal synchronization procedure is described. The synchronization process is performed on two phases. The first phase is called the acquisition phase, during which the received signal is sampled and correlated with a locally generated M-sequence. The cross correlation is applied on one period of the M-sequence and the output is compared to a certain threshold. According to [8], the following equation shows the time required for initial synchronization:

$$T_{initsync} = \frac{T_u}{T_c/2} T_d = 2NT_u \tag{1}$$

where T_u is the initial timing uncertainty, T_c is one chip duration, T_d is the total time of one M-sequence period and N is the number of bits in one sequence. If the output is less than the threshold voltage, the reference M-sequence is shifted by half a chip or less and the correlation process is repeated until initial acquisition is obtained. The second phase is the tracking phase which is used for fine synchronization and tracking the received signal begins. This phase is implemented using the DLL shown in Fig. 2. After achieving the initial synchronization, the received signal is multiplied again by two signals from the reference M-sequence. The delay between these two signals is $2\tau \leq T_c$. The two products are envelope detected then subtracted from each other giving an error signal. The error signal is applied to the loop filter that drives the VCO. If the two signals are synchronized ideally, both multiplied signals will have the same output waveform. In case that synchronization is not precise, one of the multipliers output will have higher signal values than the other leading to an error signal that controls the VCO towards synchronization. The drawback of this architecture is the difficult constraints facing the designer to build an ADC to sample the received signal. The bandwidth of the incoming signal is

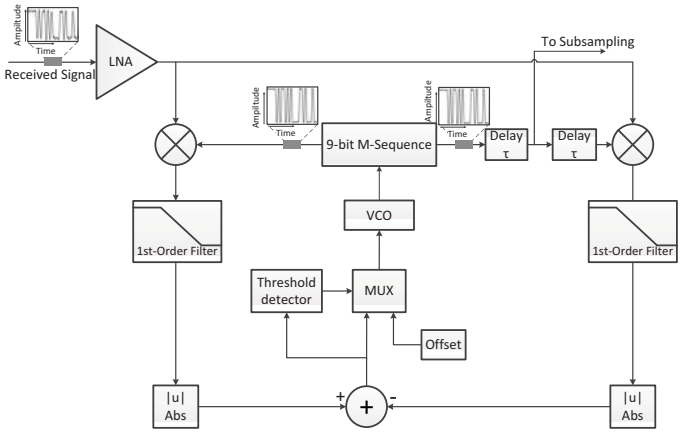

Fig. 3. The proposed DLL architecture.

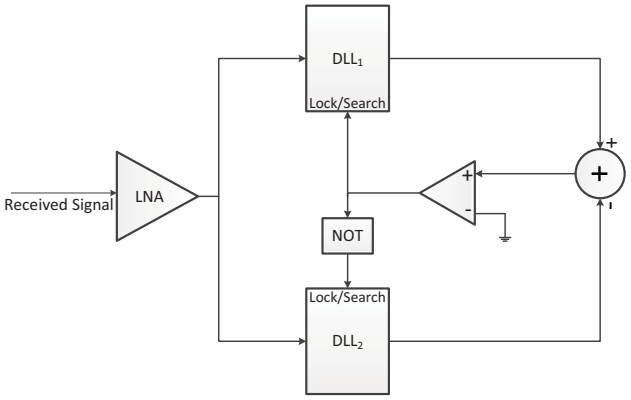

Fig. 4. The solution introduced for multipath fading.

with 5 GHz bandwidth which means an ADC of minimum 10 GS/s is required for correct data acquisition. Such ADC's consume high power as shown in [9] and [10], their power consumption exceeds 2 W which is four times the estimated power consumption of the proposed architecture.

The analog implementation of the synchronization system is implemented as shown in Fig. 3. The signal is received by a Low Noise Amplifier (LNA) to decrease the noise figure of the whole circuit. The signal is then multiplied by two versions of the reference M-sequence as shown previously. The cross correlation function can be applied using a multiplier followed by an integrator in the form of a first order low pass filter. The VCO runs freely with an offset frequency slightly faster than the normal frequency of the incoming signal. The initial synchronization is indicated when the difference between the two signals is exceeding a certain threshold. Accordingly, the circuit starts working in the second phase for fine tuning and tracking.

To have more illustration of the above circuit, we assume that the VCO is continuously running in the search mode and we ignore the threshold detector at the moment. The output of the subtraction between the two branches will have pulse shape signal over time as shown in Fig. 5. The positive peak in the pulse signal indicates that the non delayed path is synchronized with the received signal, while the negative peak indicates that the synchronization is with the delayed path. Thus, the

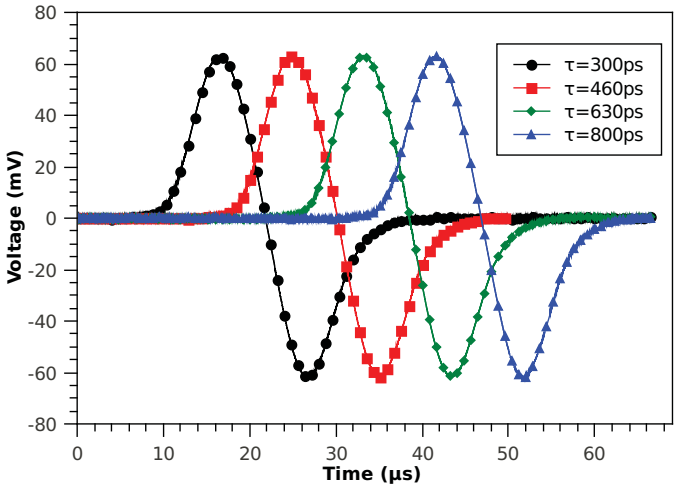

Fig. 5. The pulse shape for different input delays.

pulse shape is a notification of the coarse synchronization which should be identified by the threshold detector. The pulse amplitude is directly proportional to τ value and inversely proportional to the offset frequency of the VCO. The time estimated for the initial synchronization for the M-sequence is shown in the following equation:

$$T_{initsync,analog} = \frac{T_u}{T_c}\frac{1}{\triangle f} \tag{2}$$

where $\triangle f$ is the offset frequency added to the center frequency of the VCO.

Fig. 4 illustrates the detection of the strongest path apart from the paths that are suffering from several reflections. The architecture is based on using additional DLL circuit such that DLL_1 is locking to a certain path, while DLL_2 is in the search mode for a stronger path. Each circuit correlates its own reference signal with the received path and then are fed to a comparator which decides to lock on the stronger path.

The frequency offset of the VCO should be few hundreds of KHz so that the waveform of the reference M-sequence signal preserves its shape for high synchronization process. To assure the accurate synchronization, the analog blocks before the low pass filter should have broad band frequency response upto 10 GHz and with a maximum group delay variations of 10 ps according to (3).

$$\triangle \tau_g \leq \frac{T_c}{10} = 10ps \tag{3}$$

where $\triangle \tau_g$ is the group delay of the analog blocks. The multiplier used is a four quadrant Gilbert cell multiplier shown in Fig. 6. The delay elements and the VCO are described in Verilog-A code for simplicity. The low pass filter is done using an ideal op-amp of frequency unity gain 10 GHz with feedback resistor and capacitor to have a cut off frequency of 80 KHz. The transistors are biased to have the maximum available transconductance for good frequency response. The reference M-sequence is fed into V_1 with the suitable input power and the received signal is fed into V_2. The output voltage of the

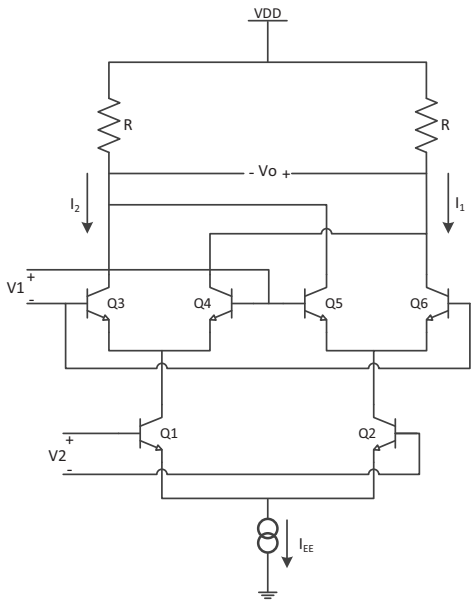

Fig. 6. The Gilbert cell used as a multiplier.

multiplier assuming small signal approximation is shown as follows:

$$V_o = (I_2 - I_1)R = I_{EE}R \cdot V_1 V_2 \tag{4}$$

where I_{EE} is the tail current and V_1 and V_2 should be less than the thermal voltage which is around 25 mV. In case of higher voltage amplitudes, a $\tanh^{-}1$ circuit is used at the input to compensate the non-linearity of the gilbert cell.

III. System Simulation and Results

The multiplier is designed in the SGB25V technology of IHP using $0.25\,\mu m$ HBT transistors with a peak f_T value of 50 GHz. The impedance matching is not considered here because the multiplier is an internal stage. The multiplier is biased with a current of 5 mA from a 3.3 V supply resulting in a power consumption of only 16.5 mW. The simulation of the multiplier is performed in Cadence IC6.1.5 by applying at the inputs the simulated waveform from the designed 9-bit M-sequence in [7]. Fig. 7 shows the transient simulation of multiplying two M-sequence waveforms using the Gilbert cell and an ideal multiplier. The output multiplication shows the correct expected waveform with a voltage gain about 9.5 dB compared to the ideal output waveform. The output voltage waveform of the multiplexer in Fig. 8. During the first $2\,\mu s$, the multiplexer is showing the offset voltage output which means that the VCO is in the search mode with a frequency offset. After $2\,\mu s$, the threshold detector indicates the presence of coarse synchronization, the multiplexer is switched to the error signal. These damping oscillations are indication of fine synchronization and tracking. The output waveform of the received and the reference M-sequence signals are shown in Fig. 9 after synchronization. A 1-bit signal is plotted to have a closer look on the error which has a maximum of 5 ps.

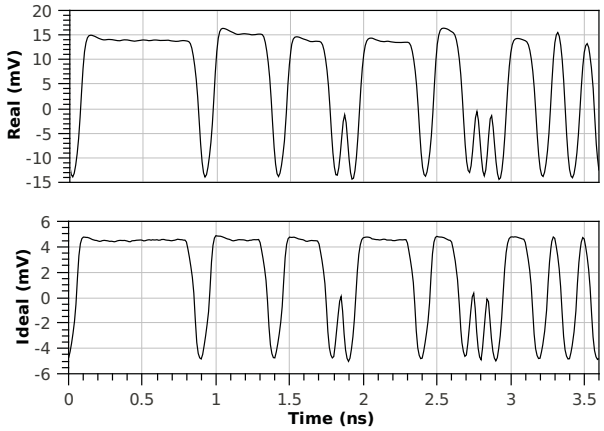

Fig. 7. The multiplication of the M-sequence using Gilbert cell and ideal multiplier.

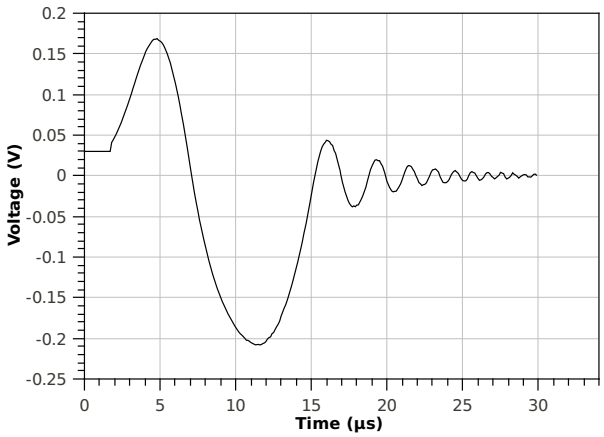

Fig. 8. The error signal coming out from the multiplexer.

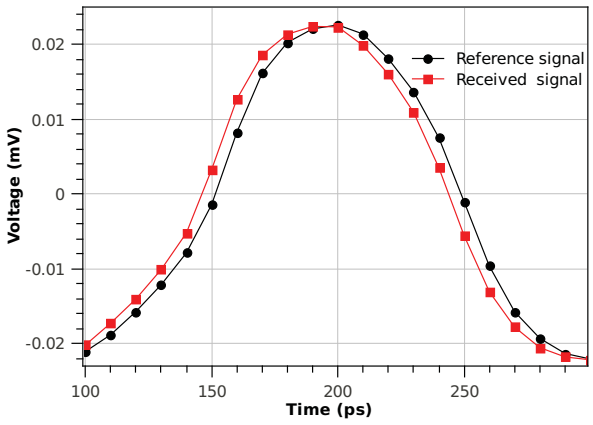

Fig. 9. The two M-sequence waveforms after fine synchronization with error of 5 ps.

IV. Conclusion

In this paper, a practical implementation of wireless synchronization for M-sequence UWB systems is discussed. This implementation gives the opportunity for M-sequence to have wider field of applications since the transmitter and the receiver are separated from each other and not restricted to complicated wiring. The system is implemented in the analog domain to save costs and power consumed by data converter. A Gilbert cell is used as a multiplier which proves to function with high accuracy output voltage waveform. The power consumption of the multiplier is 16.5 mW with a supply voltage of 3.3 V. A solution for multipath fading is also introduced here by using an additional synchronization circuit. The locking process is illustrated and time error between the two synchronized M-sequence signals is shown to be not more than 5 ps. As a further step, the complete system is implemented in transistor level using IHP technology.

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