

Apéndice C

Registros de control del 68HC11

\$1000	BIT 7	-	-	-	-	-	-	BIT 0	PORTA	Puerto A
\$1001									Reserv.	
\$1002	STAF	STAI	CWOM	HNDS	OIN	PLS	EGA	INVB	PIOC	Control Puertos
\$1003	BIT 7	-	-	-	-	-	-	BIT 0	PORTC	Puerto C
\$1004	BIT 7	-	-	-	-	-	-	BIT 0	PORTB	Puerto B
\$1005	BIT 7	-	-	-	-	-	-	BIT 0	PORTCL	Latch Puerto C
\$1006									Reserv.	
\$1007	BIT 7	-	-	-	-	-	-	BIT 0	DDRC	Modo E/S Puerto C
\$1008			BIT 5	-	-	-	-	BIT 0	PORTD	Puerto D
\$1009			BIT 5	-	-	-	-	BIT 0	DDRD	Modo E/S Puerto D
\$100A	BIT 7	-	-	-	-	-	-	BIT 0	PORTE	Puerto E
\$100B	FOC1	FOC2	FOC3	FOC4	FOC5				CFORC	Forzar comparaciones
\$100C	OC1M7	OC1M6	OC1M5	OC1M4	OC1M3				OC1M	OC1: Control
\$100D	OC1D7	OC1D6	OC1D5	OC1D4	OC1D3				OC1D	OC1: datos
\$100E	BIT 15	-	-	-	-	-	-	BIT 8	TCNT	Registro contador
\$100F	BIT 7	-	-	-	-	-	-	BIT 0		
\$1010	BIT 15	-	-	-	-	-	-	BIT 8	TIC1	Captura entrada 1
\$1011	BIT 7	-	-	-	-	-	-	BIT 0		
\$1012	BIT 15	-	-	-	-	-	-	BIT 8	TIC2	Captura entrada 2
\$1013	BIT 7	-	-	-	-	-	-	BIT 0		
\$1014	BIT 15	-	-	-	-	-	-	BIT 8	TIC3	Captura entrada 3
\$1015	BIT 7	-	-	-	-	-	-	BIT 0		
\$1016	BIT 15	-	-	-	-	-	-	BIT 8	TOC1	Comparador 1
\$1017	BIT 7	-	-	-	-	-	-	BIT 0		
\$1018	BIT 15	-	-	-	-	-	-	BIT 8	TOC2	Comparador 2
\$1019	BIT 7	-	-	-	-	-	-	BIT 0		
\$101A	BIT 15	-	-	-	-	-	-	BIT 8	TOC3	Comparador 3
\$101B	BIT 7	-	-	-	-	-	-	BIT 0		

\$101C	BIT 15	-	-	-	-	-	-	BIT 8	TOC4	Comparador 4
\$101D	BIT 7	-	-	-	-	-	-	BIT 0		
\$101E	BIT 15	-	-	-	-	-	-	BIT 8	TOC5	Comparador 5
\$101F	BIT 7	-	-	-	-	-	-	BIT 0		
\$1020	OM2	OL2	OM3	OL3	OM4	OL4	OM5	OL5	TCTL1	Control 1 tempor.
\$1021			EDG1B	EDG1A	EDG2B	EDG2A	EDG3B	EDG3A	TCTL2	Control 2 tempor.
\$1022	OC1I	OC2I	OC3I	OC4I	OC5I	IC1I	IC2I	IC3I	TMSK1	Másc. 1 interr. temp.
\$1023	OC1F	OC2F	OC3F	OC4F	OC5F	IC1F	IC2F	IC3F	TFLG1	Flags 1 interr. temp.
\$1024	TOI	RTII	PAOVI	PAII			PR1	PR0	TMSK2	Másc. 2 interr. temp.
\$1025	TOF	RTIF	PAOVF	PAIF					TFLG2	Flags 2 interr. temp.
\$1026	DDRA7	PAEN	PAMOD	PEDGE			RTR1	RTR0	PACTL	Control contador pulsos
\$1027	BIT 7	-	-	-	-	-	-	BIT 0	PACNT	Contador de pulsos
\$1028	SPIE	SPE	DWOM	MSTR	CPOL	CPHA	SPR1	SPR0	SPCR	Control del SPI
\$1029	SPIF	WCOL		MODF					SPSR	Estado del SPI
\$102A	BIT 7	-	-	-	-	-	-	BIT 0	SPDR	Datos del SPI
\$102B	TCLR		SCP1	SCP0	RCKB	SCR2	SCR1	SCR0	BAUD	Baudios del SCI
\$102C	R8	T8		M	WAKE				SCCR1	Control 1 del SCI
\$102D	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK	SCCR2	Control 2 del SCI
\$102E	TDRE	TC	RDRF	IDLE	OR	NF	FE		SCSR	Estado del SCI
\$102F	BIT 7	-	-	-	-	-	-	BIT 0	SCDR	Datos del SCI ← <u>Buffer</u>
\$1030	CCF		SCAN	MULT	CD	CC	CB	CA	ADCTL	Control/Estado CAD
\$1031	BIT 7	-	-	-	-	-	-	BIT 0	ADR1	Resultado CAD 1
\$1032	BIT 7	-	-	-	-	-	-	BIT 0	ADR2	Resultado CAD 2
\$1033	BIT 7	-	-	-	-	-	-	BIT 0	ADR3	Resultado CAD 3
\$1034	BIT 7	-	-	-	-	-	-	BIT 0	ADR4	Resultado CAD 4
\$1035 hasta \$1038									Reserv.	
\$1039	ADPU	CSEL	IRQE	DLY	CME		CR1	CR0	OPTION	Config. sistema
\$103A	BIT 7	-	-	-	-	-	-	BIT 0	COPRST	Control del COP
\$103B	ODD	EVEN		BYTE	ROW	ERASE	EELAT	EEPGM	PPROG	Control de EEPROM
\$103C	RBOOT	SMOD	MDA	IRV	PSEL3	PSEL2	PSEL1	PSEL0	HPRIO	Prioridad interrup.
\$103D	RAM3	RAM2	RAM1	RAM0	REG3	REG2	REG1	REG0	INIT	Direccion. RAM y E/S
\$103E	TILOP		OCCR	CBYP	DISR	FCME	FCOP	TCON	TEST1	Test de fábrica
\$103F	-	-	-	-	NOSEC	NOCOP	ROMON	EEON	CONFIG	Habilita COP, ROM,...