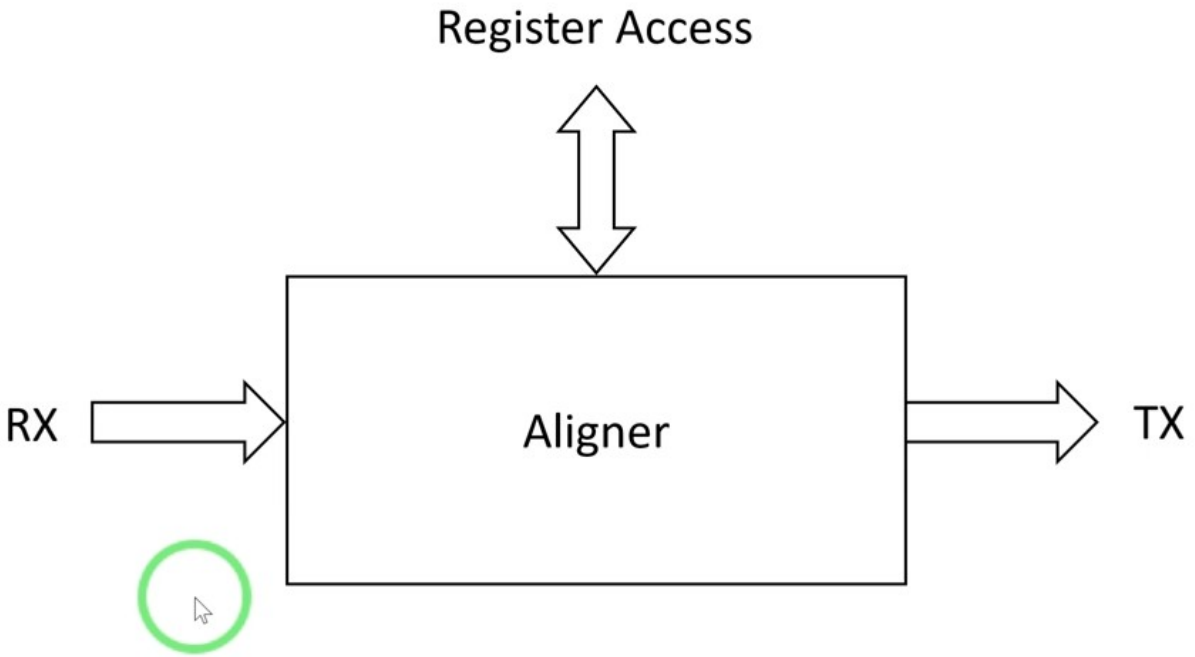
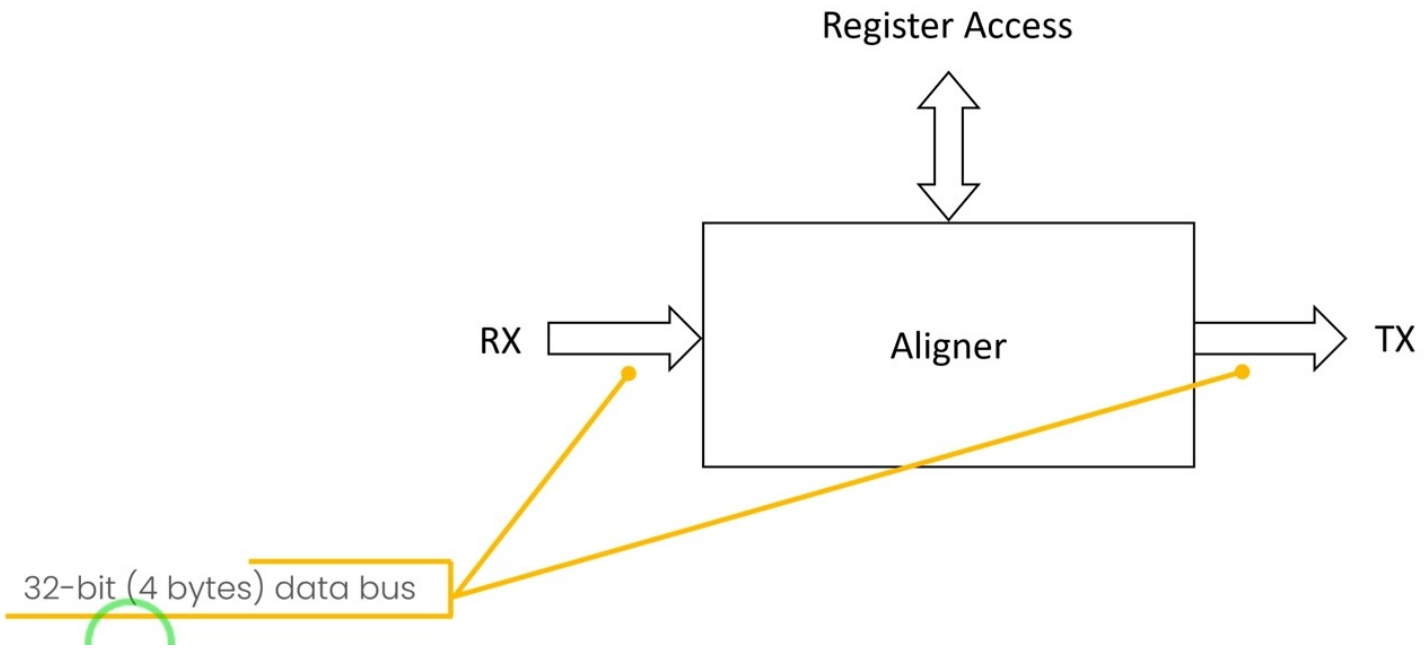
Proyecto 1

Device Under Test (DUT)

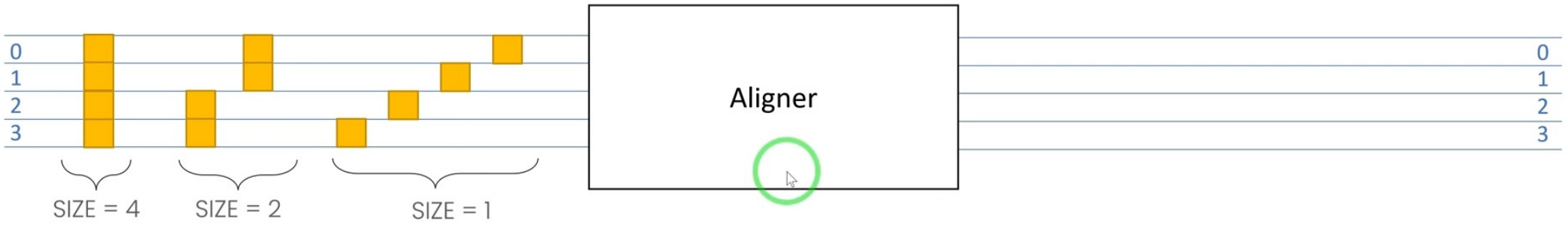
Alignment



Alignment



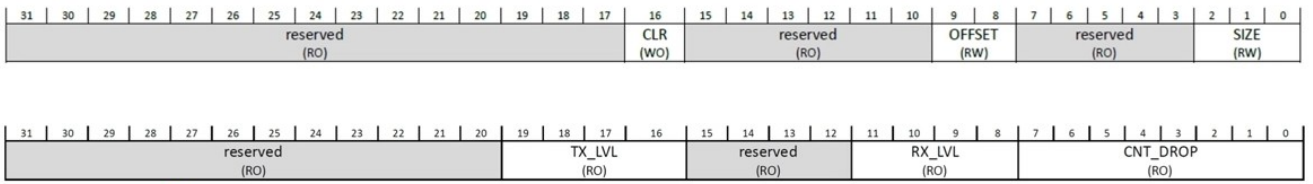
Alignment



Control Register

((ALGN_DATA_WIDTH / 8) + offset) % size != 0

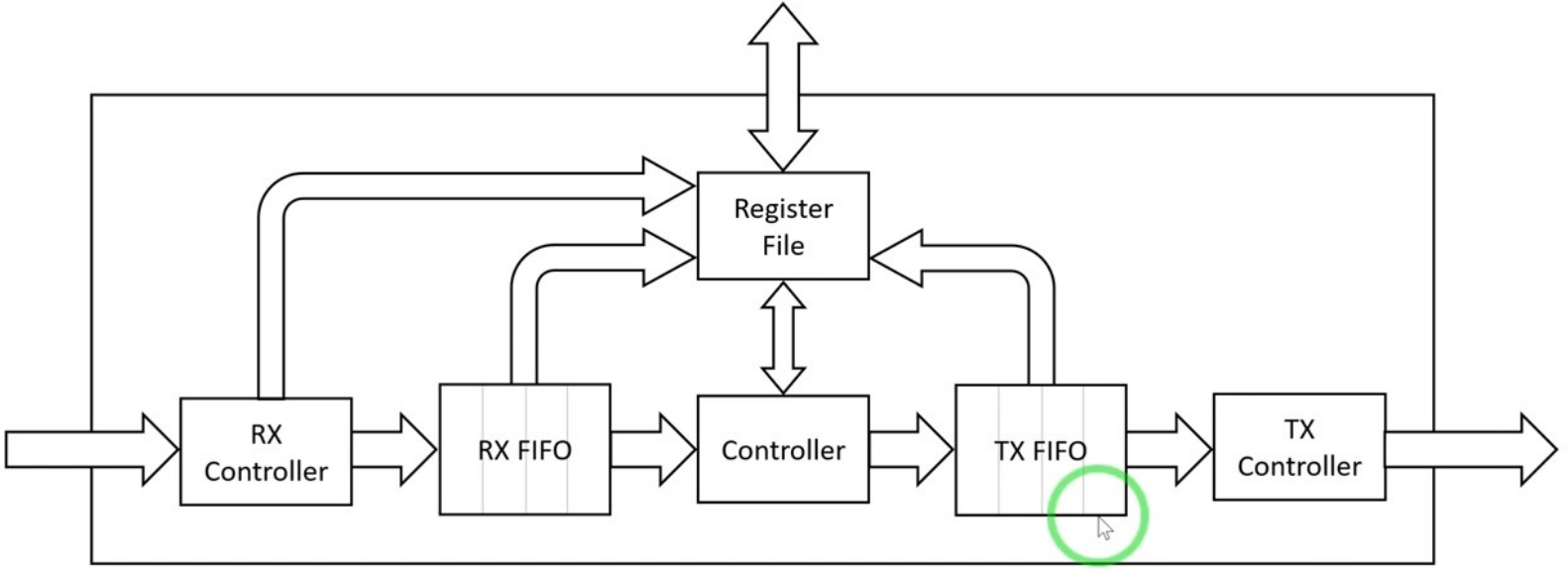
Drop Counter



Status Register

RX And TX FIFO Levels

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
reserved (RO)												TX_LVL (RO)				reserved (RO)				RX_LVL (RO)				CNT_DROP (RO)							



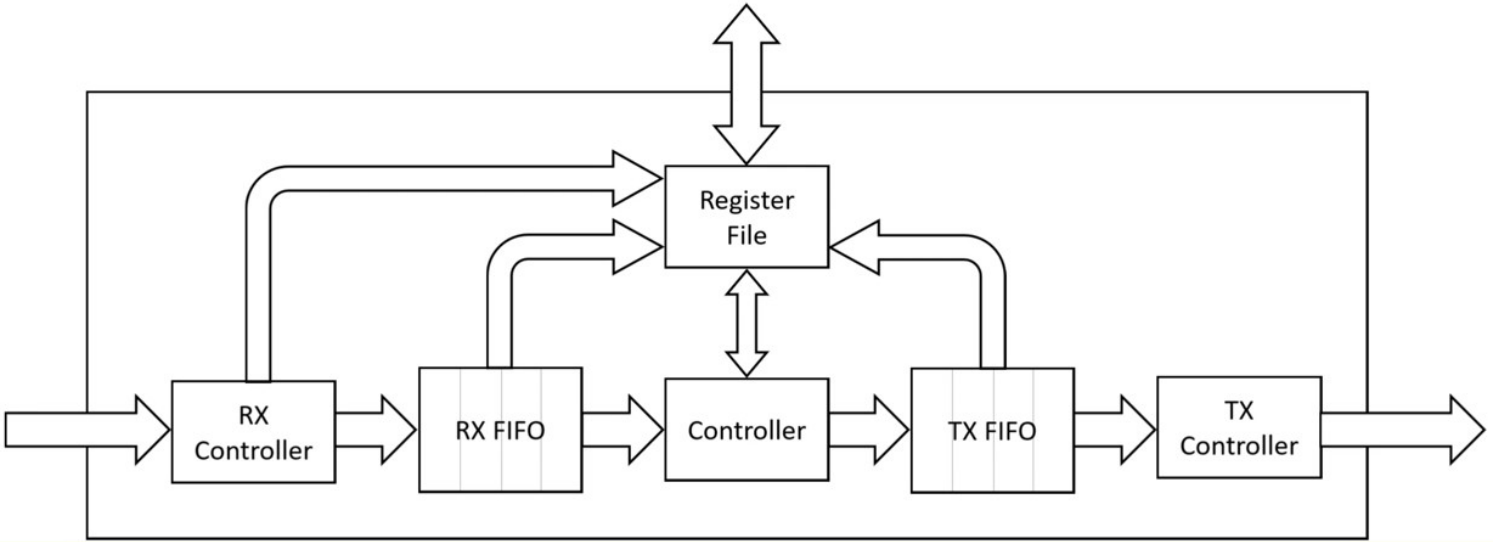
Interrupt Requests

Interrupt Requests Enable Register

31–5	4	3	2	1	0
reserved (RO)	MAX_DROP (RW)	TX_FIFO_FULL (RW)	TX_FIFO_EMPTY (RW)	RX_FIFO_FULL (RW)	RX_FIFO_EMPTY (RW)

Interrupt Requests Register

31–5	4	3	2	1	0
reserved (RO)	MAX_DROP (W1C)	TX_FIFO_FULL (W1C)	TX_FIFO_EMPTY (W1C)	RX_FIFO_FULL (W1C)	RX_FIFO_EMPTY (W1C)



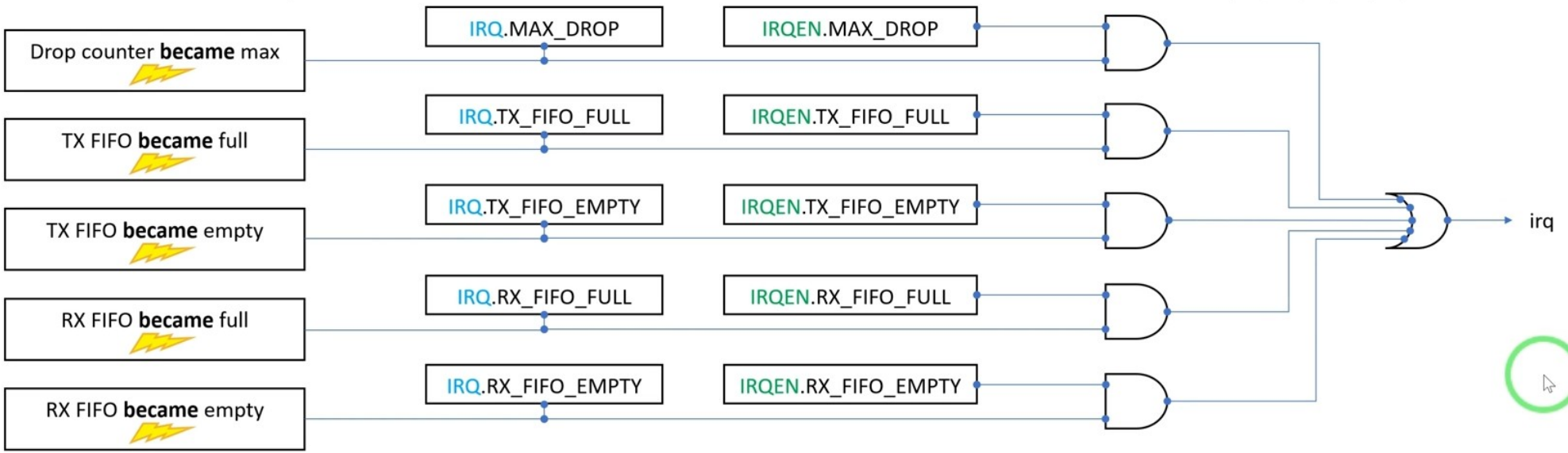
Interrupt Requests

Interrupt Requests Enable Register

31 … 5	4	3	2	1	0
reserved (RO)	MAX_DROP (RW)	TX_FIFO_FULL (RW)	TX_FIFO_EMPTY (RW)	RX_FIFO_FULL (RW)	RX_FIFO_EMPTY (RW)

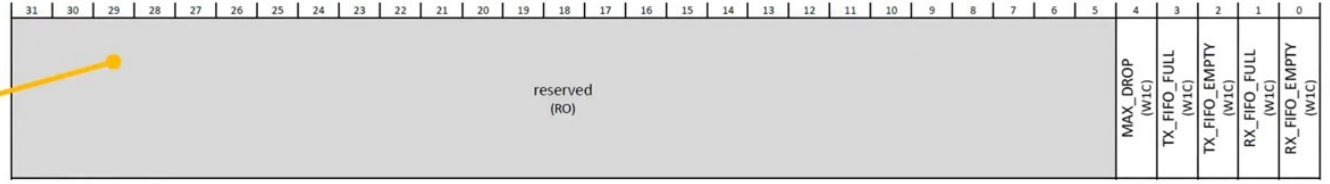
Interrupt Requests Register

31 … 5	4	3	2	1	0
reserved (RO)	MAX_DROP (W1C)	TX_FIFO_FULL (W1C)	TX_FIFO_EMPTY (W1C)	RX_FIFO_FULL (W1C)	RX_FIFO_EMPTY (W1C)



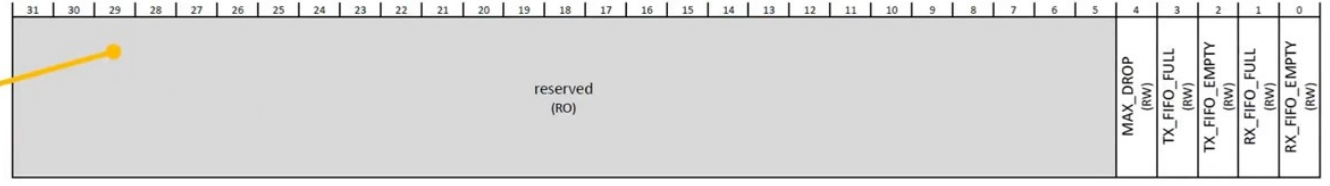
Register Access – APB Interface

Interrupt Requests Register



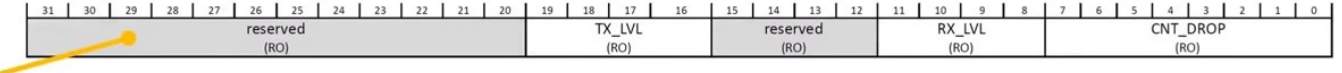
IRQ

Interrupt Requests Enable Register



IRQEN

Status Register

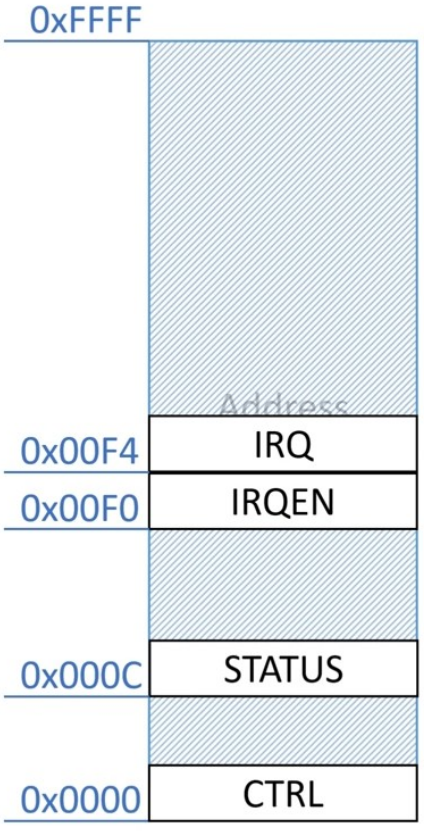


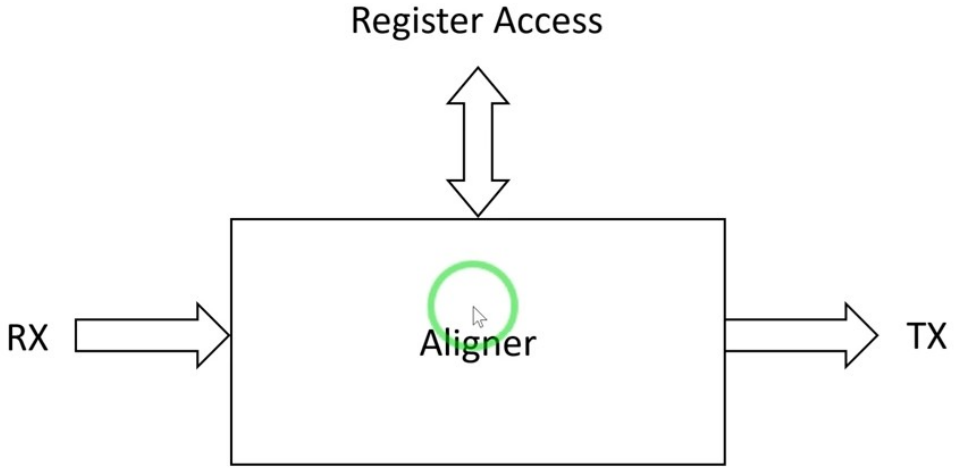
STATUS

Control Register

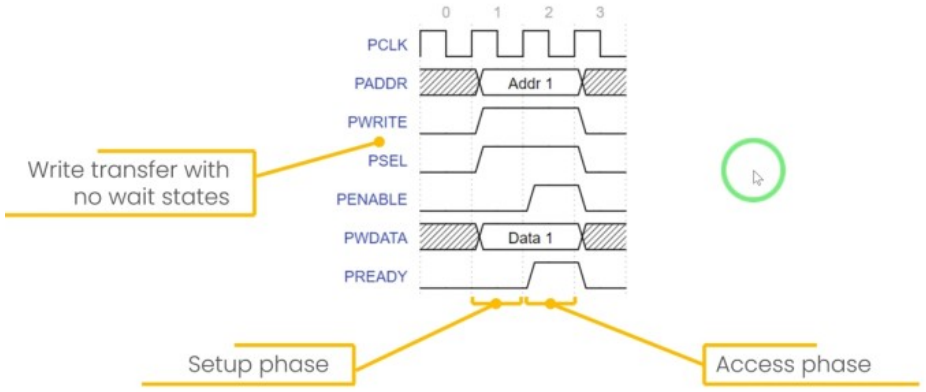
CTRL

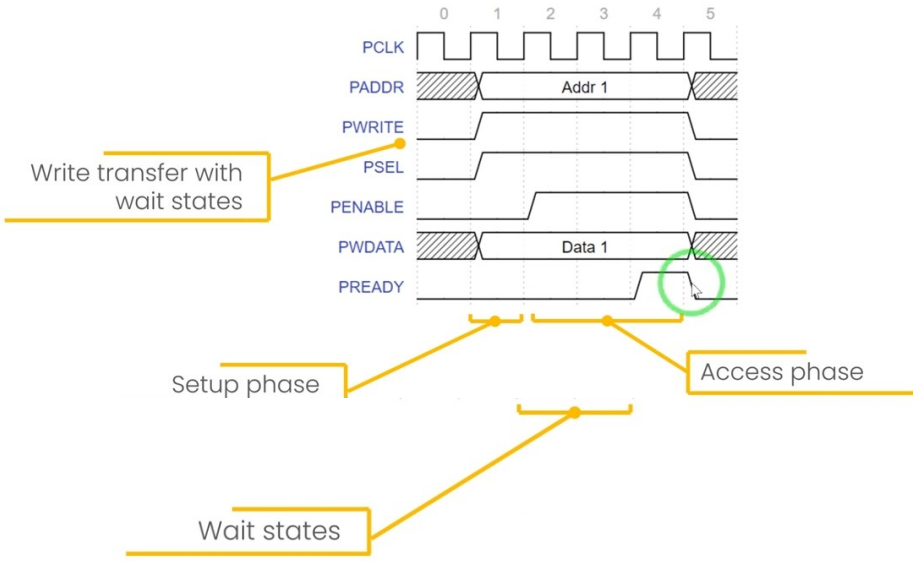
Register Access – APB Interface





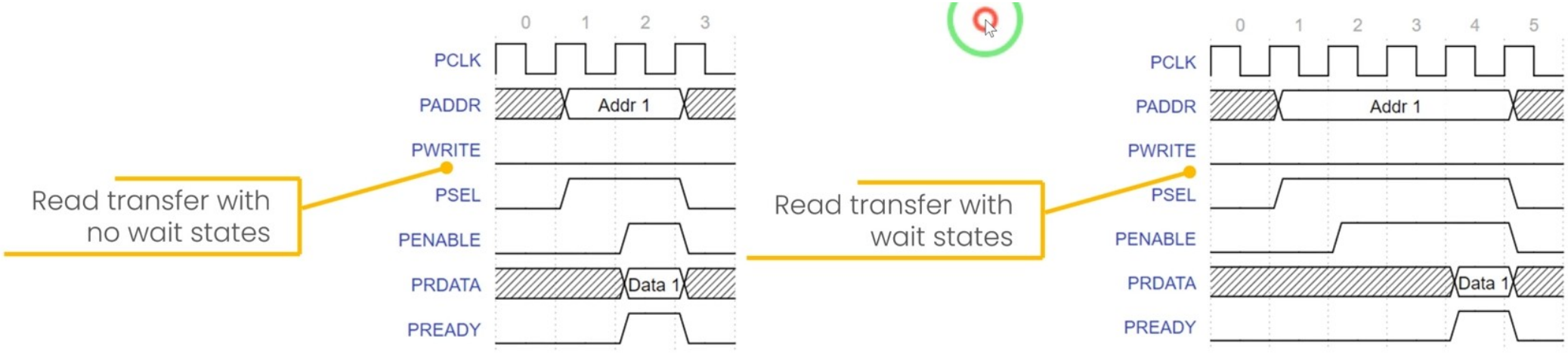
Register Access – APB Interface





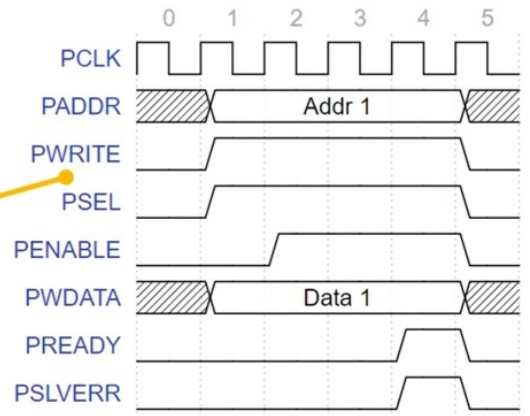
Write access to the registers

Read access to the registers

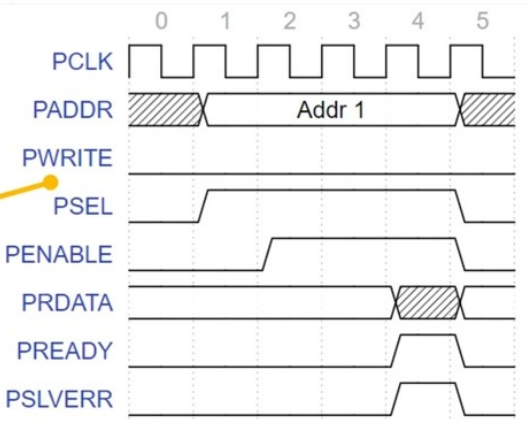


Register Access – APB Interface

Write transfer with error response



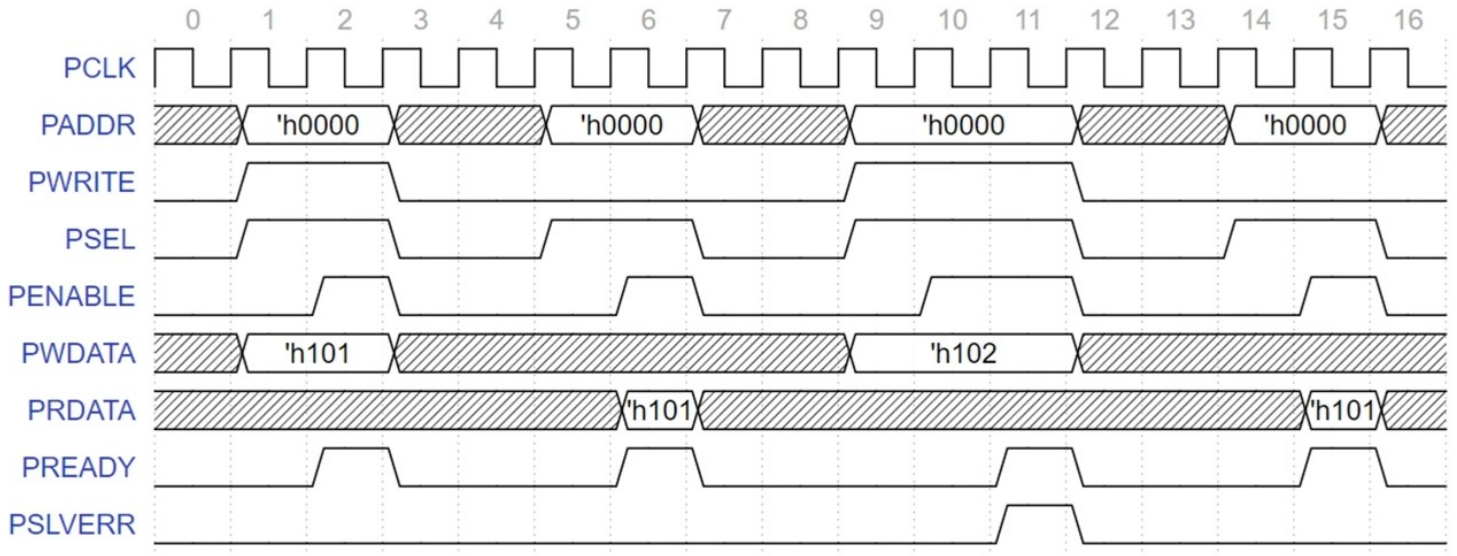
Read transfer with error response

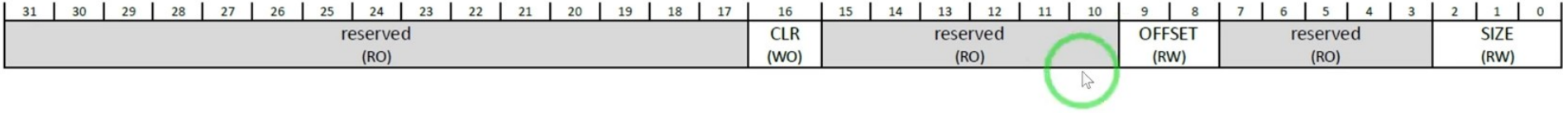


Error scenarios:

- Access to an unmapped location
- Write access to STATUS register
- Write access to CTRL with an illegal combination of new values for CTRL.OFFSET and CTRL.SIZE

Register Access – APB Interface





MD Interface