SuperAudioBoard Design Guide

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1. Introduction

The SuperAudioBoard is a high quality audio breakout board that was originally designed for the Teensy 3.x series of ARM microcontroller boards. The design, however, only requires a controller that can provide an I2S audio interface, an I2C control interface, and a single reset line. This means that the design is also compatible with the Raspberry Pi, and any other controller capable of driving those interfaces.

The initial reason for designing the SuperAudioBoard was to provide high quality audio input and output for the Teensy 3.x. Paul, who designed the Teensy, had introduced an audio adapter board that uses a CD quality audio codec (the Freescale SGTL5000). Many of the Teensy forum contributors started asking about higher sample rates and bit depths. In the discussion that followed, Paul mentioned some minimal requirements that he had in mind for a higher quality solution, but that he did not have the time to work on such a design.

I thought that such a design would be a good way to work on my analog design skills, so I eventually decided to take on the challenge of designing an audio board for the Teensy that could achieve very high performance.

2. Design Overview

In this design, the first step was to decide on an audio codec. For the highest performance, a solution could have been designed using separate ADC and DAC ICs, but a single chip codec that provides bothe the ADC and DAC in a single package reduces both overall cost, component count, and design complexity.

There are a lot of high performance codecs with various levels of functionality available. Even the SGTL5000 has a lot of DSP functionality built in. The CS4272 was chosen for the following reasons:

1. High performance
    a. The CS4272 has very high performance specifications:
        i. -100dB THD+N
        ii. 114 Dynamic Range
        iii. Sample rates to 200kHz
2. Simplicity
    a. Many of the higher performance codecs also include a lot of DSP and other functionality, which can make the design process more difficult and tends to make them more expensive

3. Solderability
    a. The design needed to be hand solderable so that I (and anyone else who wanted to) could hand load a board for one-off needs or for prototypes.
    b. Almost all of the other codecs that had similar performance came in packages that are very difficult to hand solder, such as QFN (Quad-Flat-No-lead).
    c. Although the CS4272 has very tight pin pitch (0.65mm), I find these types of packages much easier to hand solder than QFNs, and other small packages.

Once the codec was chosen, it defined the requirements for the rest of the system. The CS4272 needs differential input and output buffers for the audio IO's. It needs a low noise +5V supply as well as a digital supply (+3.3V was used for compatibility with the Teensy 3.x).

One part of the system level design that is not driven by the codec is the use of digital isolator ICs to isolate the codec from the controller. Paul mentioned in one of his forum posts that he would like to see this isolation in any high quality audio boards so that the quality won't be compromised by ground loops. Although this addition does add some cost, it should eliminate the most likely cause of signal degradation in an audio system.

In some situations, the isolation isn't really required. For example, if the controller (the Teensy, Raspberry Pi, etc) is powered by a battery and not connected at all to the wall supply, then there will be no ground loops through the controller, and the isolation is not required. In that case, the user of the board may want to use the same battery power supply for both the audio board and the controller. If that is the use case, the user can bypass the isolation by adding a few 0 Ohm jumpers.

3. Detailed Design Walkthrough

1. Power Supply

There are a number of design goals that I had in mind when putting together the power supply:

1. First and foremost, the analog supply for the codec and audio IO buffers needs to be very, very clean to prevent adding excessive noise to the audio lines.
2. The design should be capable of using a wide range of inputs
    a. Batteries
    b. USB power
    c. Teensy Vin
3. Current requirements for the supply voltages:

Supply	SI8662	SI8602	CS4272	4x THS4521	Total
+5V analog	0	0	53mA	20mA	73mA
+3.3V digital	10mA	5mA	28mA	0	43mA

a. The current requirements are pretty modest, so fairly low current devices can be used.

The requirement for a low noise analog power supply pretty much requires that the regulators that generate the final supply voltages are linear, low dropout regulators, not switching regulators. This means that these regulators must be fed with a voltage that is at least a 300-500mV greater than their output voltage. I chose an intermediate voltage of 5.7V to give the 5V regulator 700mV of dropout for some design margin, and the dropout on the 3.3V regulator (2.4V) isn't so much that it burns an excessive amount of power (700mV * 100mA = 70mW for the 5V regulator, and 2.4V*50mA = 120mW for the 3.3V regulator).

I chose the Linear Tech LT1962 linear regulators for both final voltage regulators because it has very low output noise (20uVRMS), comes in +3.3V and +5V fixed output versions, requires minimal external components, and is pretty inexpensive.

The next step was to find a switching regulator to generate the 5.7V intermediate voltage. The LTC3534 stood out because it has applications information for 4xAA battery and USB input voltages, which is exactly the kind of inputs that I was looking for. This part is a pretty cool; it can do buck, boost, and buck-boost operation to cope with input voltages above, close to, and below the output voltage. It's switching frequency is pretty high (1MHz) so it can use a fairly small surface mount inductor. And, because the Super Audio Board application is so similar to the applications mentioned in the LTC3534 datasheet, I was able to directly use the example application schematic with a single resistor change to generate 5.7V instead of 5.0V.

The most important part of the switching regulator design is the inductor selection. Unfortunately, the inductor used in the example application schematic has a very difficult to solder design. The recommended Coilcraft inductor only has pads on the bottom of the package and no accessible metal on the side of the part to heat with a soldering iron. The LTC3534 demo board from Linear actually uses a different inductor that has metal strips on either side, the TOKO A916CY-3R3M. I couldn't find that inductor at any of the parts distributors that I normally use (ie, digikey and mouser), so I tried to find a similar inductor from Coilcraft. The MSS1038 series fit the bill, and met all the recommended specifications in the LTC3534 datasheet (saturation current, DC resistance, self-resonant frequency, etc). Another benefit of this series of inductors is that it is shielded, so the changing currents in the inductor won't radiate as much as they would with an unshielded inductor.

Unfortunately, at the high switching frequencies used by the LTC3534, pretty much any trace will start to radiate, so care is required to minimize the length of any traces carrying high frequency energy. Surface mount ferrite beads were added as close as possible to the input and output of the switching regulator to attenuate high frequency components, and some major filtering needed to be done to

ensure that none of the switching noise made it into the sensitive analog areas of the design.

The filter needs to be between the switching regulator and the final, linear regulators for two reasons: first, this minimizes the overall length of the traces carrying any significant switching noise, and second, the linear regulators don't have good input ripple rejection above 100kHz. The switching regulator runs at 1MHz, so the filter will need to have high rejection for this frequency and its harmonics.

The two supplies should also be pretty well isolated from one another so that any digital switching noise on the +3.3V supply doesn't make it to the sensitive analog side of the board through the +5V supply. In order to achieve the isolation, the intermediate supply is split right after the ferrite bead on the switching supply output, then each side goes through one inductor before the two LDOs (Illustration 3.1).

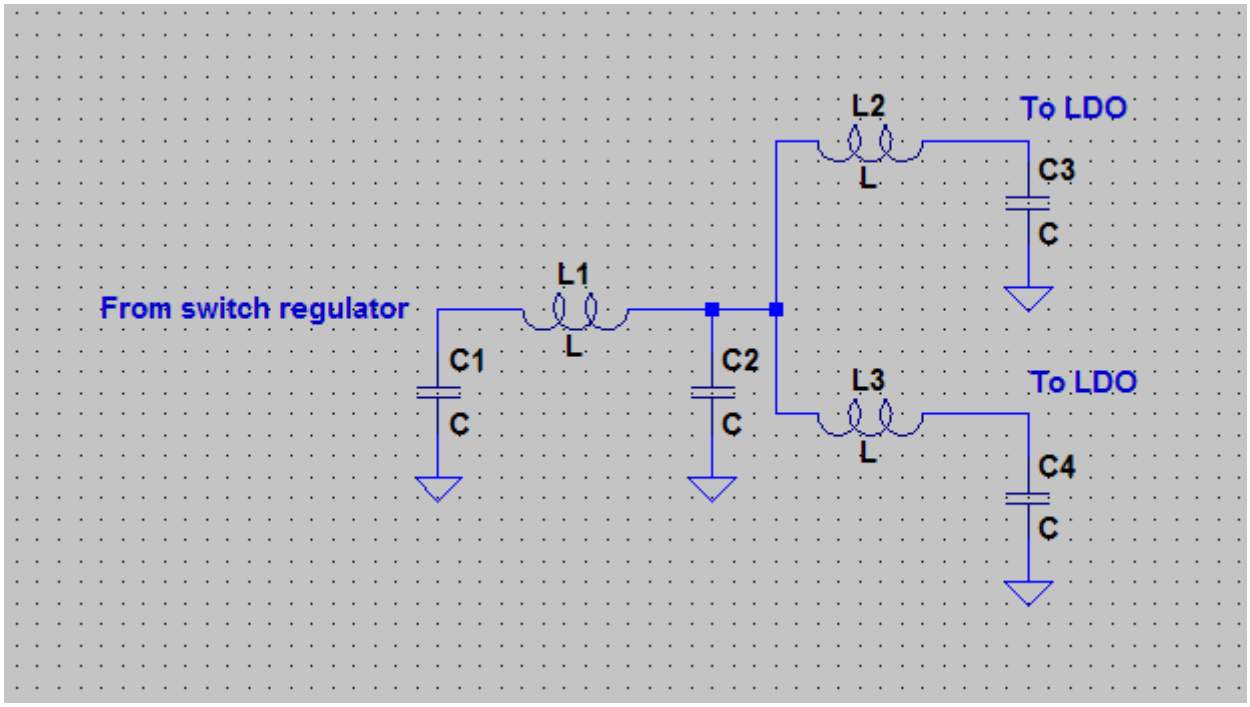

Illustration 3.1: 1st power supply filter topology

In this topology, most of the components are already fixed: C1 is the switching regulator output capacitor, L1 is the ferrite bead on the output of the switching regulator, and for simplicity L2 and L3 have been chosen to be the same inductor as used in the switching regulator. This only leaves choices for capacitors C2-4. C3 and C4 also double as the input capacitors for the LDOs, so they must be >1uF to meet the LDO requirements.

I spent a lot of time looking into different capacitor choices. In the end, I decided to use a 10uF X7R capacitor in a 1210 package. The choice was mostly dictated by the need for at least 10uF of capacitance at the LDO outputs. Simulations revealed that a pair of 10uF capacitors had better inductance characteristics than a single larger capacitor, or a 10uF capacitor paired with a ~1uF

capacitor in a slightly smaller package.

With C2, C3, and C4 replaced with 2 10uF capacitors each, the filter has very good rejection between 200kHz and 1GHz (Illustration 3.2). The peaking frequency response indicates that there will likely be some overshoot and ringing if the filter is driven by a voltage step. Simulations confirmed that there is a significant overshoot, but, luckily, the LTC3534 has a built in soft start function that controls the output voltage ramp on startup. The application schematic in the LTC3534 datasheet uses the soft start feature so that the output voltage ramp takes 1-2ms. With this slow of a voltage ramp, there is almost no overshoot whatsoever (Illustration 3.3).

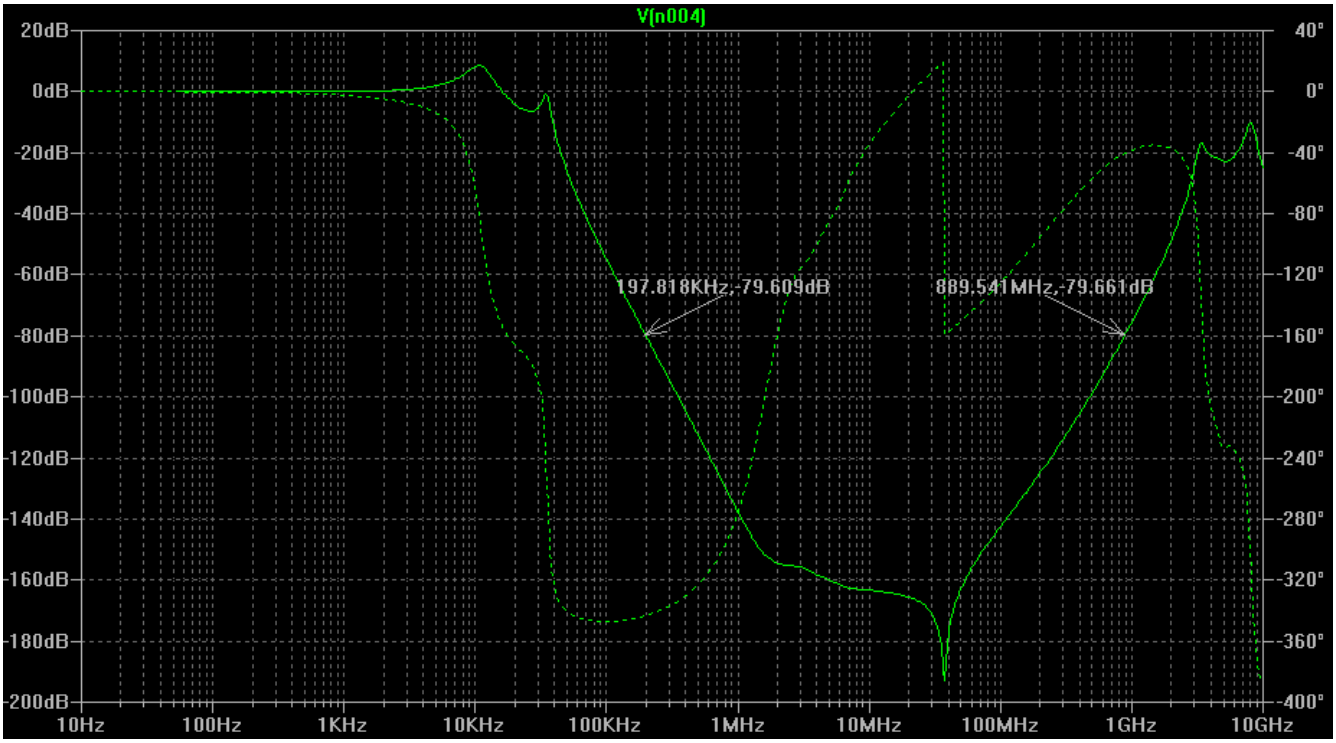

Illustration 3.2: Ripple rejection of 1st power supply filter

Illustration 3.3: Filter overshoot with a step input and a 1-2 ms ramp

The linear regulators are setup in a normal configuration. 2 10uF capacitors are used as both the input and output capacitors, and there is a 0.01uF bypass capacitor included for noise rejection.

All the devices that use the +5V analog supply have a ferrite bead in series with their supply pins to further filter out any supply noise. The final decoupling uses a single 10uF capacitor in parallel with a 0.1uF capacitor. Although prevailing logic indicates that a full decade series should be used (ie, 10uF, 1uF, and 0.1uF), simulations using real device models and some board parasitics revealed that the addition of a 1uF capacitor did not improve noise rejection or reduce the power supply impedance as delivered to the final IC.

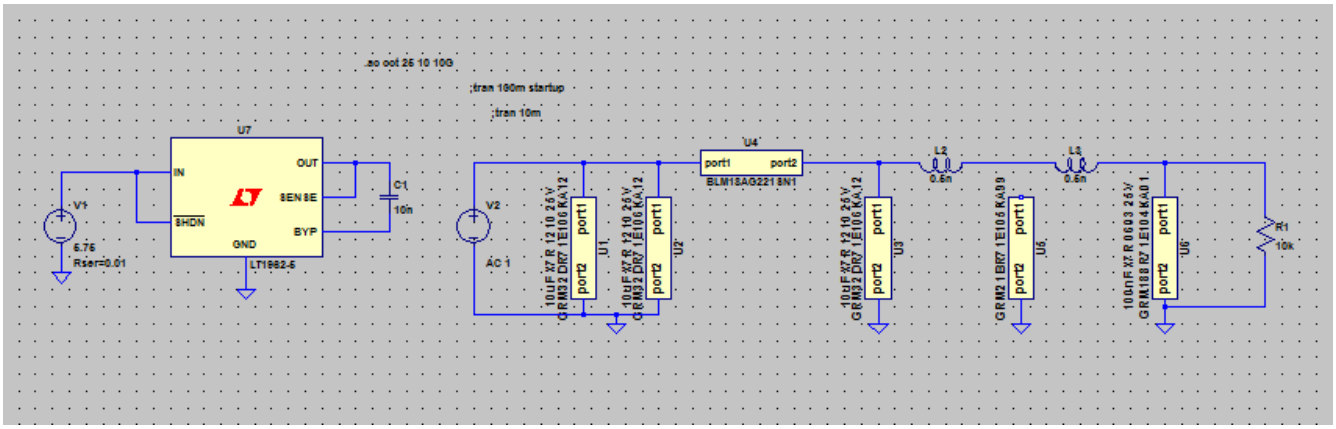

Illustration 3.4: Individual decoupling network

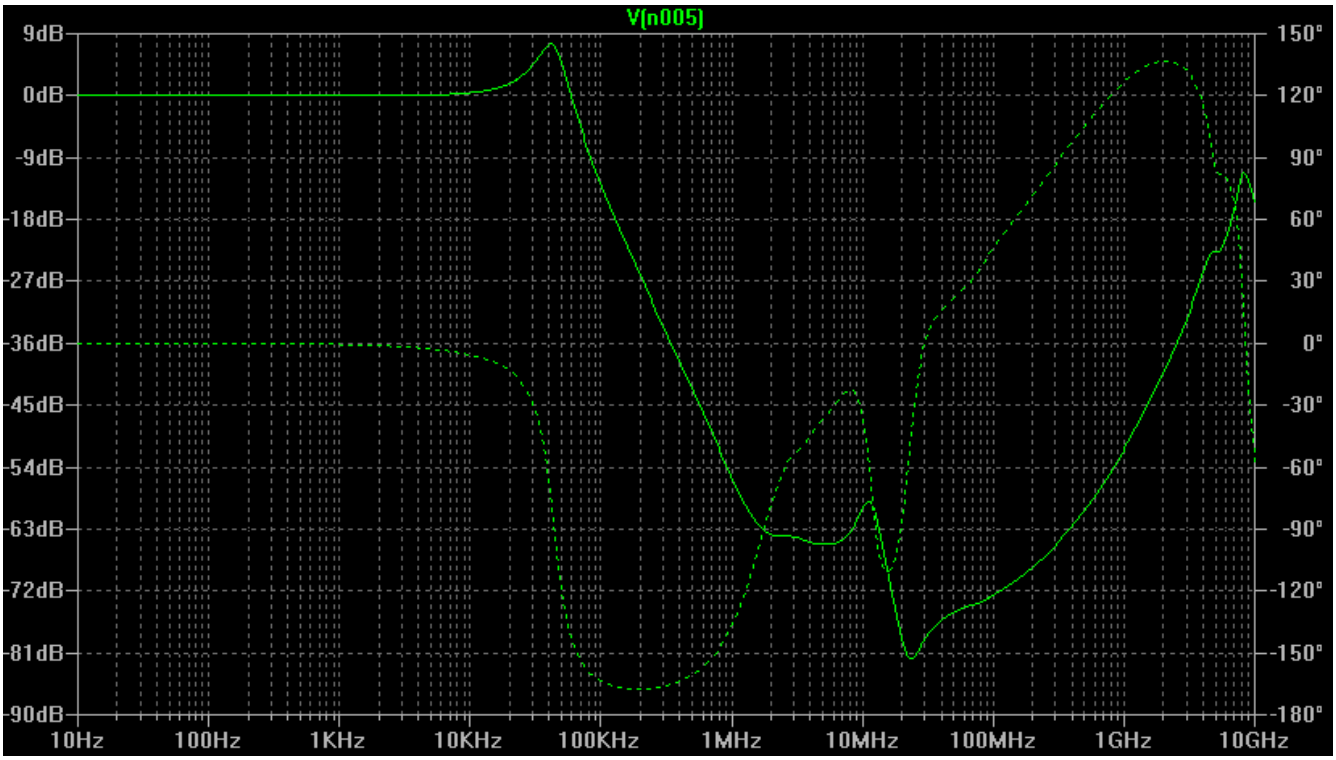

Illustration 3.5: Ripple rejection of final power supply decoupling network.

The design of the final decoupling network is a balance between achievable filtering and component count versus the keeping the impedance of the supply low to the IC pin. Ideally, the power connection should have very low impedance at all frequencies, but heavy filtering tends to increase the supply impedance at frequencies that have good rejection. The solution that I arrived at was to use a single ferrite bead, along with a 10uF and 0.1uF decoupling capacitor to keep the high frequency impedance low. This minimizes any high frequency noise on the supply lines, but maintains a very low power supply impedance across frequency. Any low frequency noise is mostly controlled by the LDOs and the power supply rejection ratio of the IC itself.

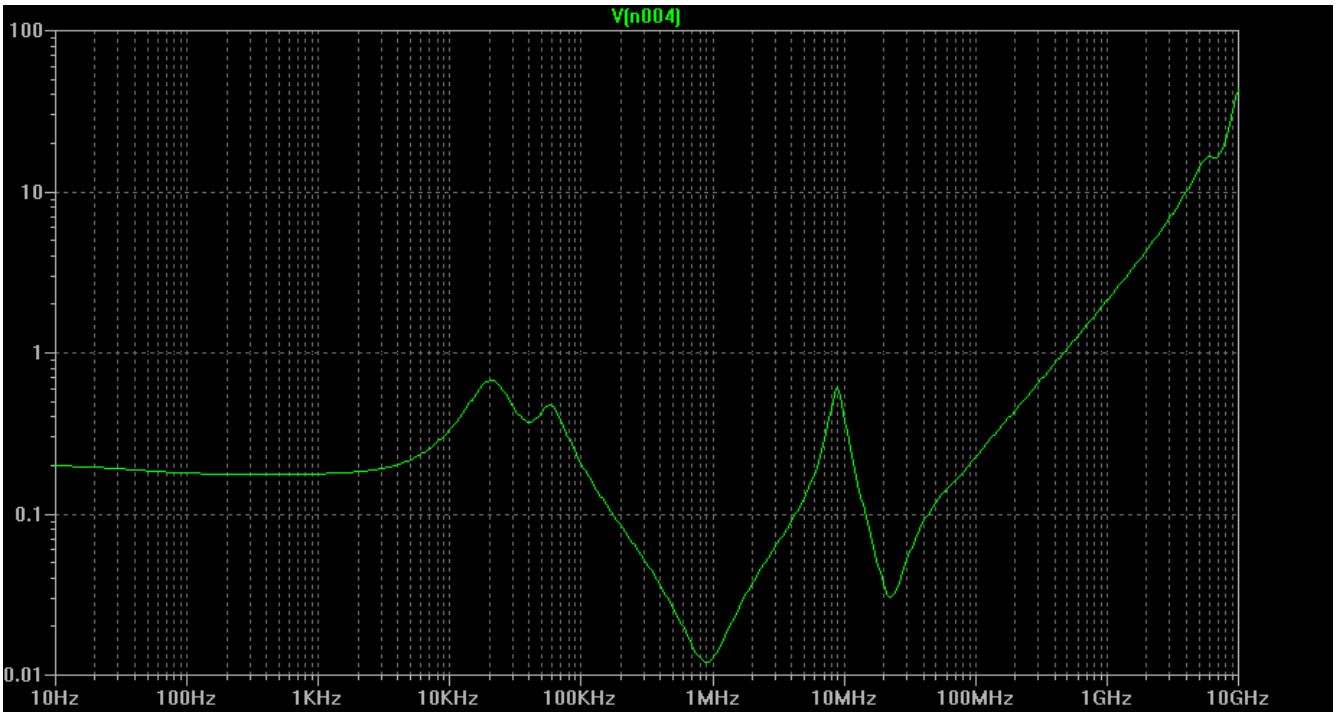

Illustration 3.6: Power supply impedance through final decoupling network.

2. Analog Section

Getting the analog part of the design finalized was probably the most time consuming part of the Super Audio Board design overall. The overall goal was just to mostly maintain the codec's performance specs:

1. THD+N of ~100dB
2. Dynamic range of 114dB
3. Excellent flatness to >20kHz

I had already chosen the CS4272 to be the audio codec, and it requires input and output buffers, so the next step was to try to find the right opamp that would drive the codec's differential inputs and outputs and not degrade the signal appreciably.

This isn't an easy problem for a few reasons. The first is that the CS4272 has differential inputs and outputs, so either two single ended amplifiers are required for each channel, or a differential amplifier is needed. The second is that most opamps designed for this type of application work best with dual supply rails or a single supply greater than 10V. The CS4272 already needs a +5V supply, and the digital supply needed to be +3.3V for compatibility with the Teensy. Another supply rail just for the input and output buffers would mean adding a lot more complexity (and cost) to the power supply to generate a clean +10-12V rail.

I was able to find a few amplifiers that looked like they would be a good fit for this application. The first is the TI LME49721 low voltage audio opamp. The second is the TI THS4521 fully differential amplifier. The CS4272 datasheet recommended input and output buffers all use single-ended output opamps, but I decided to go with the fully differential part for the following reasons:

1. Output flexibility
    a. The CS4272 datasheet schematic, and the eval board from Cirrus both only provide single-ended outputs to the user.
    b. Some users might want differential outputs to connect to their own high quality audio gear.
    c. Users who only want a single-ended output can simply leave the negative side of the differential output disconnected, and only use the positive side and ground.
2. Output level
    a. With only a single 5V power supply, a fully differential signal can easily achieve a 5V peak-to-peak output level (the output range of the CS4272 itself) without any significant distortion.
    b. A single-ended opamp needs higher supply voltages before it can achieve the same output levels.
3. Common mode rejection
    a. The CS4272 recommended input buffer relies entirely on the CS4272 itself for common mode rejection (rejection of noise that's the same on both the positive and negative parts of the differential signal)
    b. A differential input buffer will add a second level of common mode rejection for this type of noise.

With the main components chosen, it was now time to actually design the input and output buffers.

The input buffers shown in the CS4272 datasheet are a pair of opamps driving a moderate sized capacitor that is connected directly across the differential inputs of the codec. The capacitor across the input terminals appears to be fairly common for audio ADCs; the datasheet for the THS4521 actually includes several example applications schematics with audio ADCs that have the exact same topology.

The opamp feedback topology of the recommended input buffer circuit in the CS4272 datasheet (figure 12 in the datasheet) is a topology that is optimized for driving capacitive loads. This topology effectively reduces the opamps bandwidth, which gives it a low-pass filter type of frequency response, but there isn't any specific filtering in the circuit. Figure 79 in the THS4521 datasheet shows a similar circuit driving the exact same capacitive load, but using a single differential amplifier instead of two

single-ended op-amps.

Because the capacitor on the ADC input terminals is the same in both schematics, I felt confident that the fully differential topology would work well, and was able to directly use the schematic from the THS4521 datasheet, modified for a gain of 1, instead of 0.27 (Illustration 3.7).

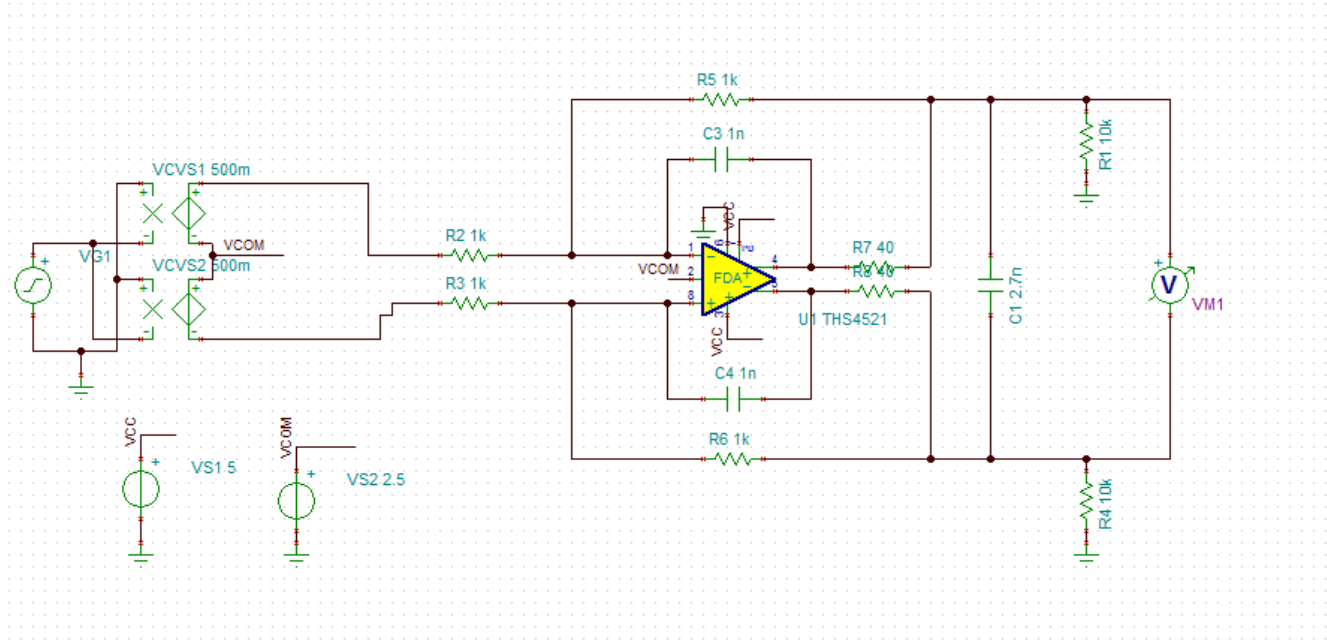

Illustration 3.7: Input buffer schematic

The only downside to this circuit is that it only provides 1k Ohm of input resistance, so there may be some signal level lost if the driving circuit does not have low output impedance.

Normally ADCs are preceded by an anti-alias filter to prevent noise and other unwanted signals above the Nyquist frequency from folding back into the sampled spectrum. In this case, the input buffer schematic shown above acts as the anti-alias filter. Because the CS4272 uses a delta-sigma architecture for both ADC and DAC functions, the actual sample rate is 6.144MHz, so the anti-alias filter only needs to have good rejection by 3MHz. The very high Nyquist frequency allows the very simple topology to work and still have good performance.

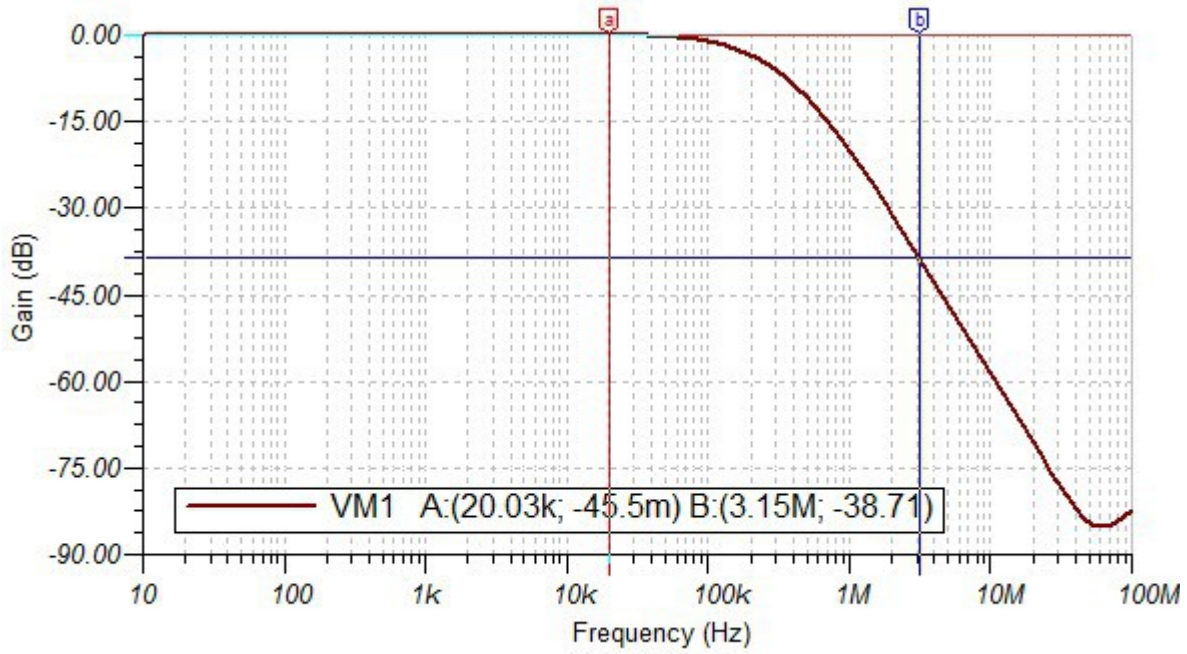

Illustration 3.8: Simulated input buffer amplitude response showing excellent passband flatness (<0.05dB @ 20kHz) and good rejection at the Nyquist frequency (almost 40dB).

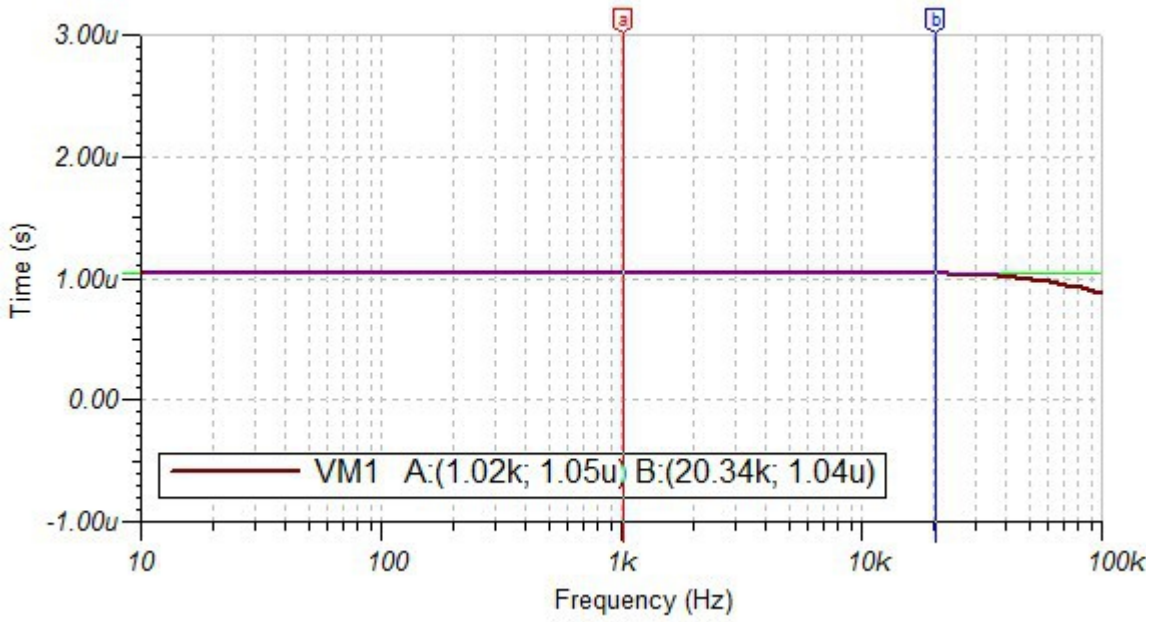

Illustration 3.9: Simulated input buffer group delay showing excellent flatness across the passband.

The output buffer schematic shown in the CS4272 datasheet is a multi-feedback (MFB) opamp filter topology that also converts the differential output signal into a single-ended signal. Unfortunately,

none of the circuit in the datasheet is usable in a differential topology, so the output filter needed to be re-designed from scratch.

A single filter stage isn't a huge problem as long as you know where to start. In this case, the most important thing is to maintain the integrity of the signal as it passes through the filter. Because of the high oversampling rate of the converter, we don't need to worry too much about rejecting images in the DAC output, so the filter just needs to have good passband amplitude and group delay flatness. Bessel filters have maximally flat group delay and slow amplitude roll-off, so they are the perfect starting point.

The next step is to decide on a filter topology. The common single-ended Sallen-Key topology is out because it uses feedback to the non-inverting opamp input which would not be easy to implement in a differential topology (if it's possible at all). Another common topology is the biquad, but that requires multiple opamps to achieve full transfer function control. Lastly, there is the multiple-feedback (MFB) topology which lends itself quite easily to differential designs.

Designing any given topology of active filter with low noise and distortion can be a big challenge. I was able to find a really good application note from TI (SBOA114) that walks through a process for designing MFB filters with low noise and distortion, even taking into account the opamps noise characteristics.

The only other requirement for the filter is that it has high enough input impedance to not load the CS4272 outputs excessively. The CS4272 datasheet mentions a resistance of 3k ohms. For the filter I chose to give this a bit of headroom and went with 5.1k ohm resistors. The rest of the design process is very similar to the examples in sections 5 and 6 of the TI app note. The final filter is shown in Illustration 3.10.

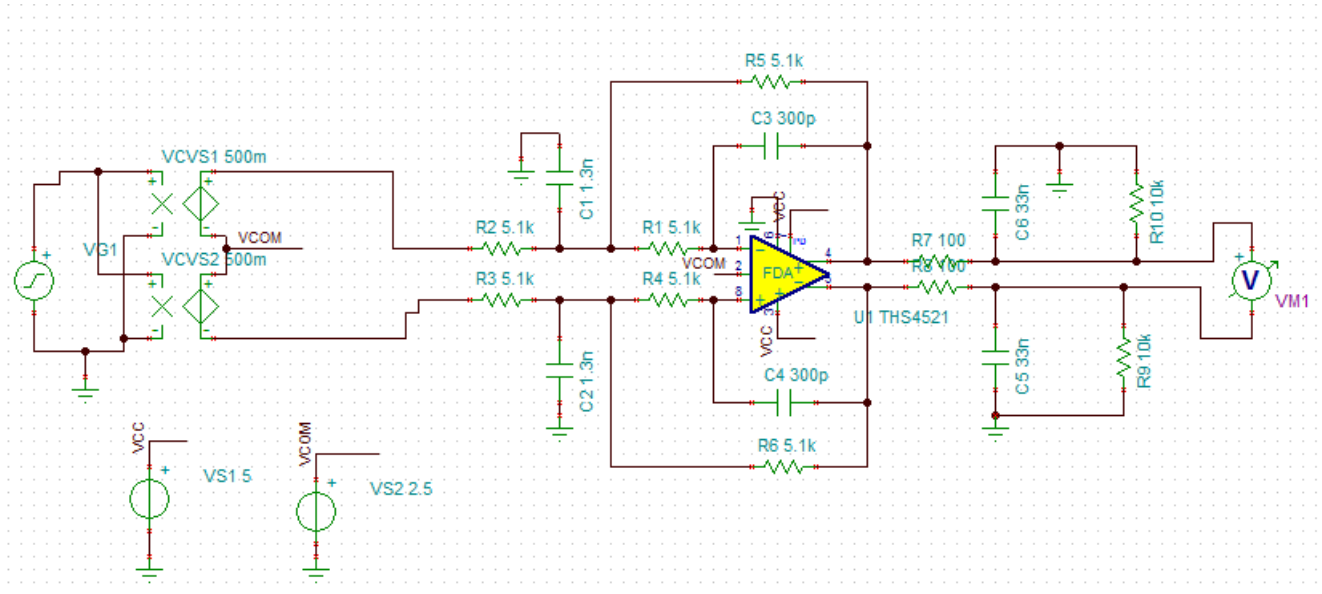

Illustration 3.10: Final output buffer schematic

Because the ideal filter components have to be replaced by components that are actually available, some of the capacitor values are slightly different than their ideal values. The filter still has excellent amplitude and phase response, however. The amplitude response has less than 1dB of roll-off at 20kHz, and the group delay is within 1% (there is slight peaking in the group delay because of the non-ideal values).

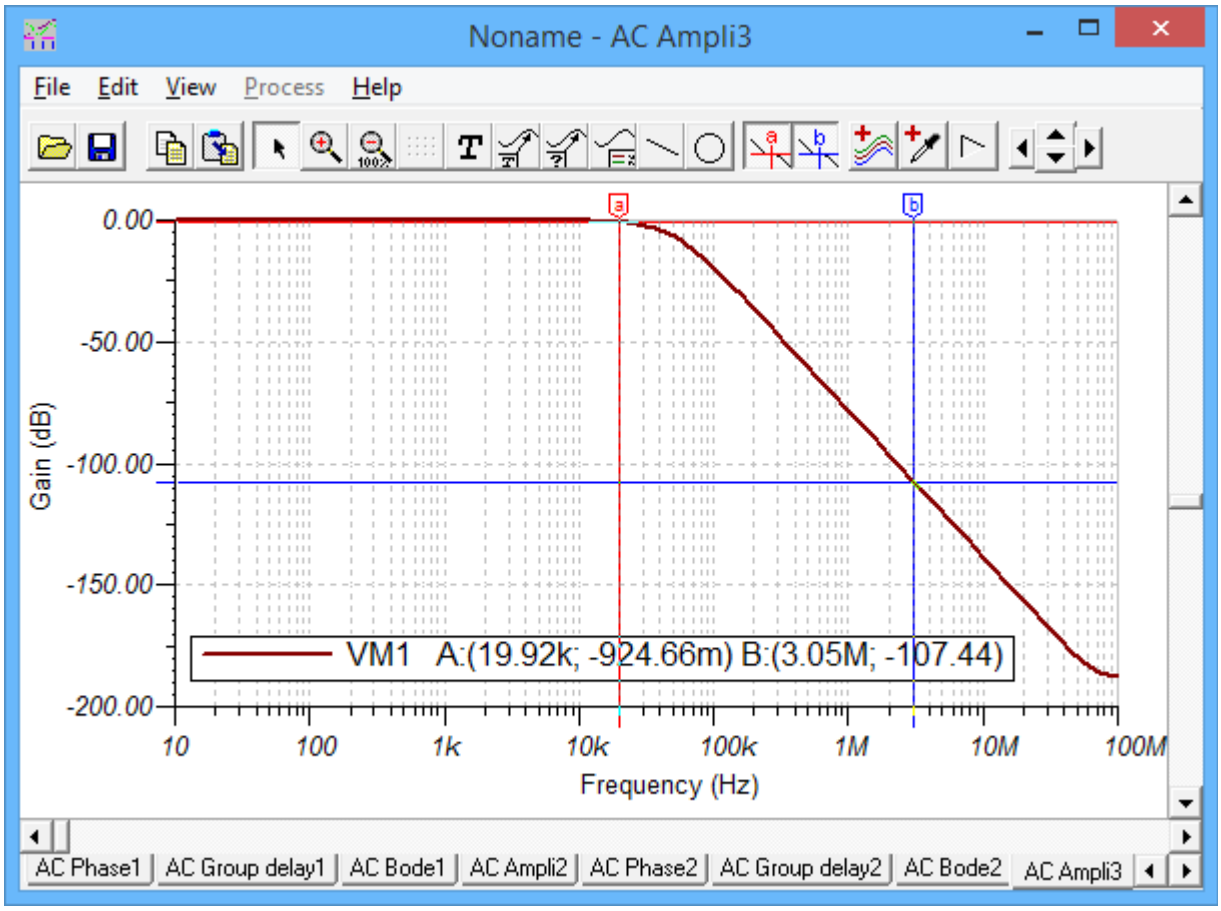

Illustration 3.11: Output buffer amplitude response

As was the case for the ADC, the DAC output filter can have a slow amplitude roll-off because the output sample rate is so much higher than the highest signal (3.1MHz vs 20kHz). This allows the filter to be fairly low order (only a third order filter in this case) and still have a large amount of rejection at the image frequencies above 3.1MHz.

One other thing that is needed with differential amplifiers is some definition of the common mode voltage. Differential amplifiers need both differential negative feedback and common mode feedback to fully define the output voltage. Both the CS4272 and the THS4521 have internal common mode feedback that will tend to center the differential signals around approximately Vcc/2 or 2.5V. Unfortunately, the CS4272 common mode voltage, at 0.48*Vcc, is slightly different than the THS4521 common mode voltage at 0.5*Vcc.

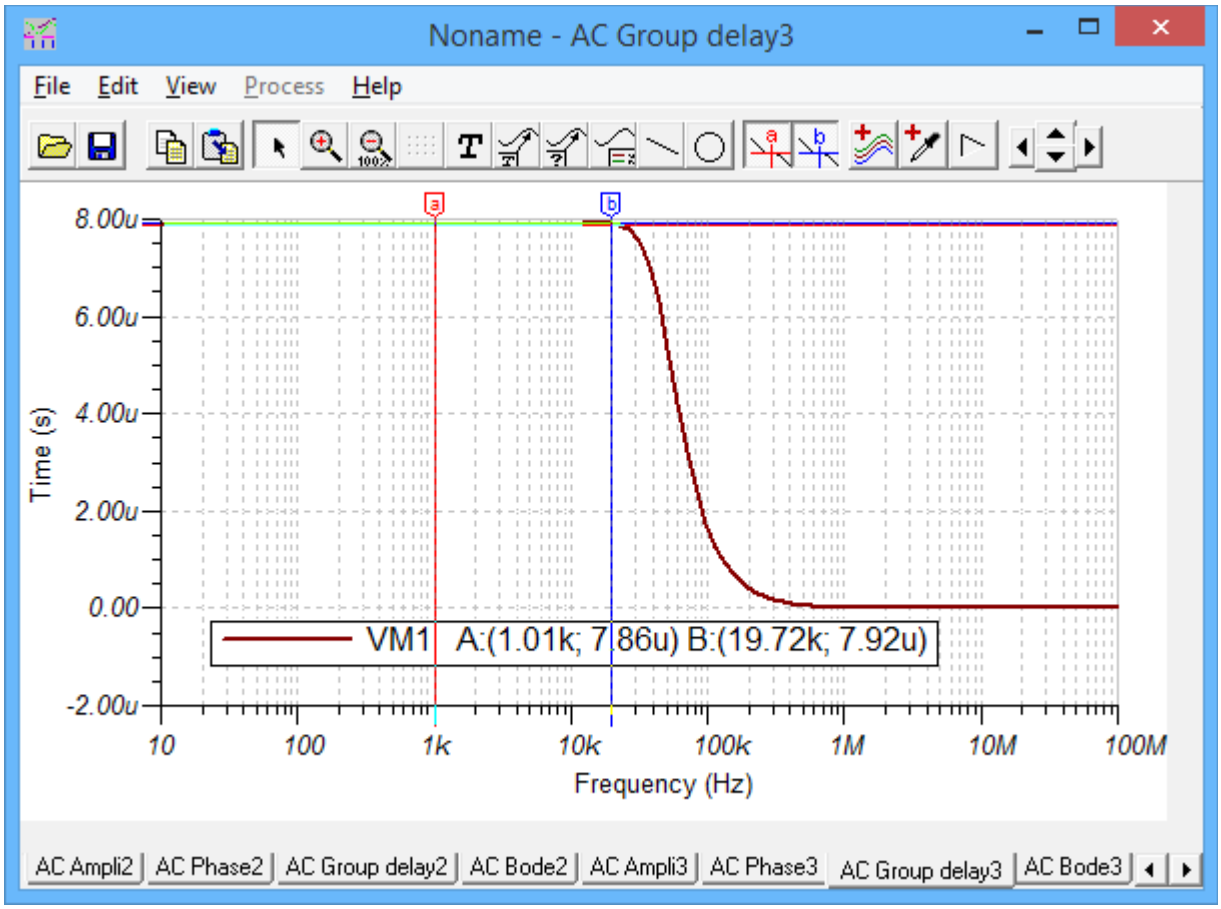

Illustration 3.12: Output buffer group delay

On the input buffer side, this will only result in a slightly reduced signal swing, because the differential signals will reach the absolute limit of the CS4272 input earlier due to the common mode offset. On the output buffer side, the difference in common mode voltages will result in a bit of DC current through the output buffer feedback resistors. However, to absolutely maximize performance, the CS4272 has a common mode voltage output that can be used to drive the common mode voltage input of the THS4521s. A dual, low-noise opamp is used to buffer the common mode output of the CS4272 for the input and output buffers.

The final step for both the input and output buffers is to go through DC blocking capacitors. The DC blocks are required to allow the signals at the opamps to be centered at 2.5V, while the signals delivered to the user are centered at 0V (ground). There are only two requirements for the DC blocking capacitors:

1. The capacitors create a high pass response, so they need to be big enough so that the filter rolls off below the lowest signal frequency (in this case 20Hz).

2. The capacitors need to be big enough to avoid generating any extra distortion.

For most audio applications, requirement #1 is really all that matters. However, for really high quality audio, the capacitors can start to introduce distortion. The best audio capacitors for this application (high capacitance) are aluminum electrolytic capacitors, but even they can be an issue if improperly sized. The distortion is caused by minute changes in capacitance with the voltage applied across the capacitor. This effect can be minimized by making sure that very little voltage appears across the capacitor itself. Because the impedance of a capacitor drops with increasing frequency or increasing capacitance (X = 1/(j*w*C)), the voltage across the capacitor drops with increasing frequency or increasing capacitance. This means that the distortion can be minimized with a really big capacitor, but usually 100uF – 500uF is more than enough (and a bigger capacitor can start introducing problems of its own).

3. Digital sections

Compared with the power supply and analog parts of the board, the digital section is quite simple. The fastest digital line (the bit clock), with the CS4272 at a 192kHz sample rate, is only 12.288MHz, so there isn't too much effort required to make sure that everything works and doesn't interfere with the analog parts of the board.

The biggest additions to this part of the board are the isolators that keep the controller (ie, Teensy, Raspberry Pi, etc) electrically separated from the codec and analog parts of the board. This helps to prevent ground loops from corrupting the audio as long as the power supply is isolated.

The only trick here was to find an isolator fast enough for the fastest speeds on the I2S interface side, and a bi-directional isolator for the I2C interface. Silicon Labs has an excellent line of isolators that are fast, and some that support bidirectional I2C interfaces. Both require minimal external parts.

Unfortunately, the fast digital isolators are unidirectional, so the I2S bus master had be chosen at design time. For the best performance, the codec is the bus master because it uses the crystal oscillator to derive the bus clocks (integer divide only), and therefore should have excellent jitter performance. The only downside to this arrangement is that only three sample rates are available: 48kHz, 96kHz, and 192kHz. These are fairly standard sample rates in professional audio applications, but most consumer music is delivered with a 44.1kHz sample rate, so any music playback will likely require resampling.

50 ohm series terminations were added to the I2S bus lines to minimize RF issues due to fast rise times. The fast isolator, the SI8662, helpfully has inputs and outputs that are nominally 50 ohms, so only a single resistor was needed for each line on the driver side.

Using OSHPark.com's 4-layer board stackup and a ground plane on the 1st internal layer, a 50 ohm microstrip line is approximately 10 mils wide, so it was easy to keep the digital lines close to the right impedance. I also made sure to route the lines without any hard corners (max 45 degree corners) to minimize radiation. It shouldn't be too much of an issue at these interface speeds, but it's good to be

safe, especially with sensitive analog circuits close by.

4. References

1. CS4272 datasheet. Retrieved from http://www.cirrus.com/en/pubs/proDatasheet/CS4272_F1.pdf
2. CDB4272 datasheet (CS4272 eval board). Retrieved from http://www.cirrus.com/en/pubs/rdDatasheet/CDB4272-2.pdf
3. THS4521 datasheet. Retrieved from http://www.ti.com/lit/ds/symlink/ths4524.pdf
4. Texas Instruments App Note SBOA114, “Design Methodology for MFB Filters in ADC Interface Applications”. Retrieved from http://www.ti.com/lit/an/sboa114/sboa114.pdf