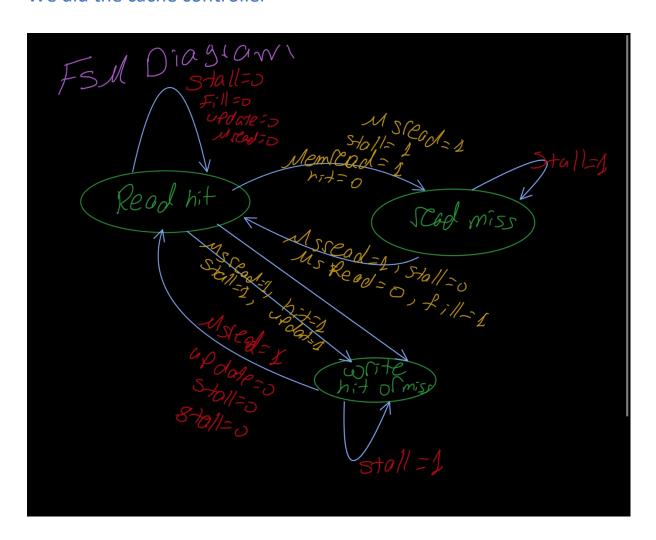
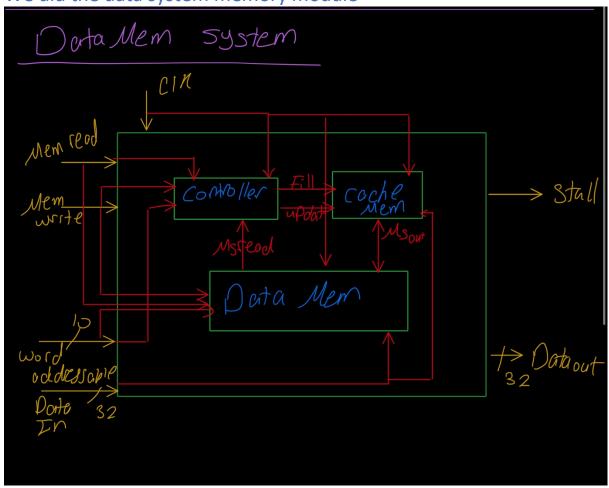
Lab 10

Experiment 3: We did the cache controller



Experiment 4:

We did the data system memory module

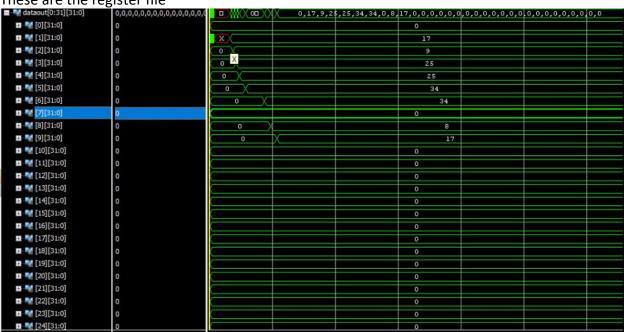


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ScreenShots for simulation:

1)

These are the register file

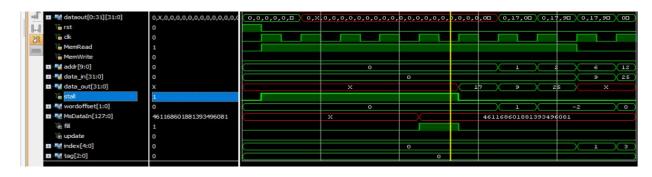


2)

There are the cache

☐ ■ data_out[31:0]	X		Х			7	9) 2	5	х
MsDataIn[127:0]	461168601881393496081		х	X		4611	16860188	139349	081	
cache[0:31][0:3][31:0]	(17,9,25,X),(X,X,X,X),(X,X,X,	(X,X,X,X),(X,X,X,X)	(),(X,X,X,X),(X,X,X	(X,X,X,X)	(17	9,25	,X) , (X,	(,x,x),	(x,x)	D,X,X,X),(X,X
[0][0:3][31:0]	00000011,00000009,0000001	XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX	0000000,00000000,00	0000000	0	00000	11,0000	0009,00	00001	19,000000000
II [0][31:0]	17		x					17		
1 4 [1][31:0]	9		х					9		
[2][31:0]	25		x					2.5		
3 [3][31:0]	x			х						

3) This is the stall signal and the PC results



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4)

PCmux[31:0]	8	4	8		12	16	20	(28
PCout[31:0]	4	(X	4		X 8	12	16	20
cout1_ripple1	0							
cout1_ripple2	0							
☐ Ints_out[31:0]	8323	(51)	8323		(4202755)	8397187	2155059	(30)
readdata 1[31:0]	0			0			X 17	X 25