THE AMERICAN UNIVERSITY IN CAIRO

100 YEARS

lab report 3

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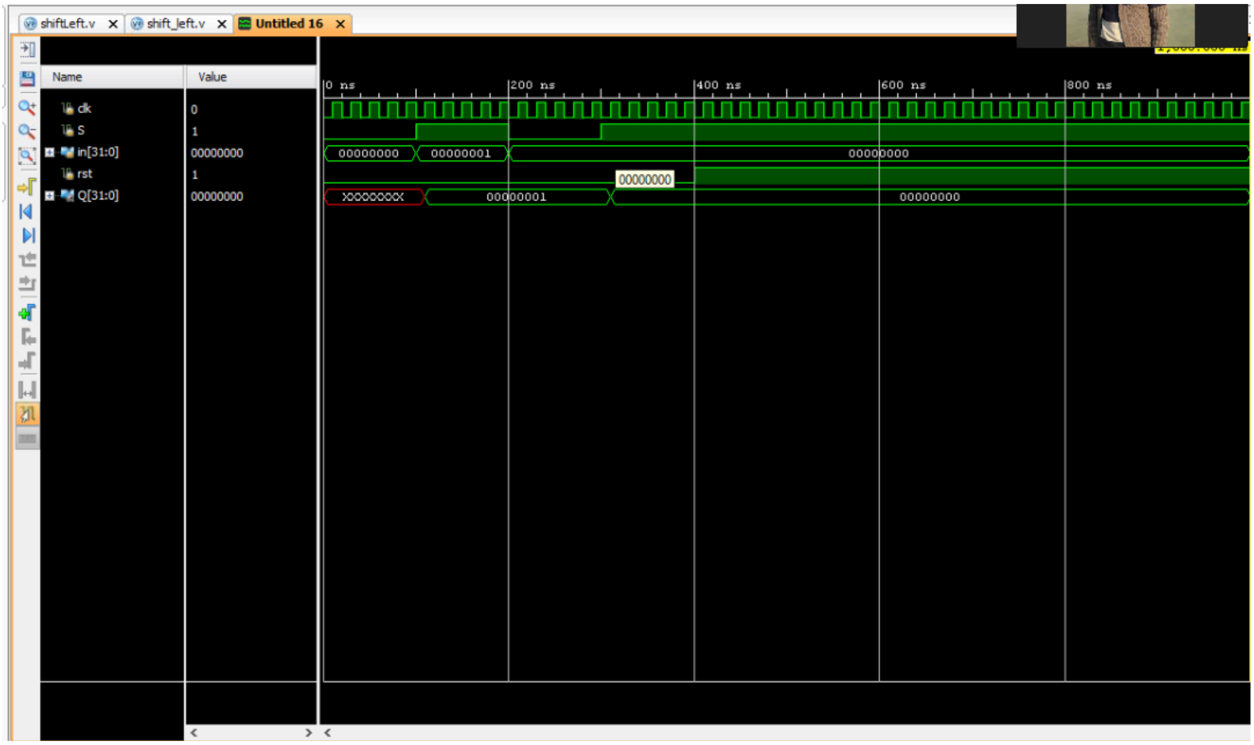
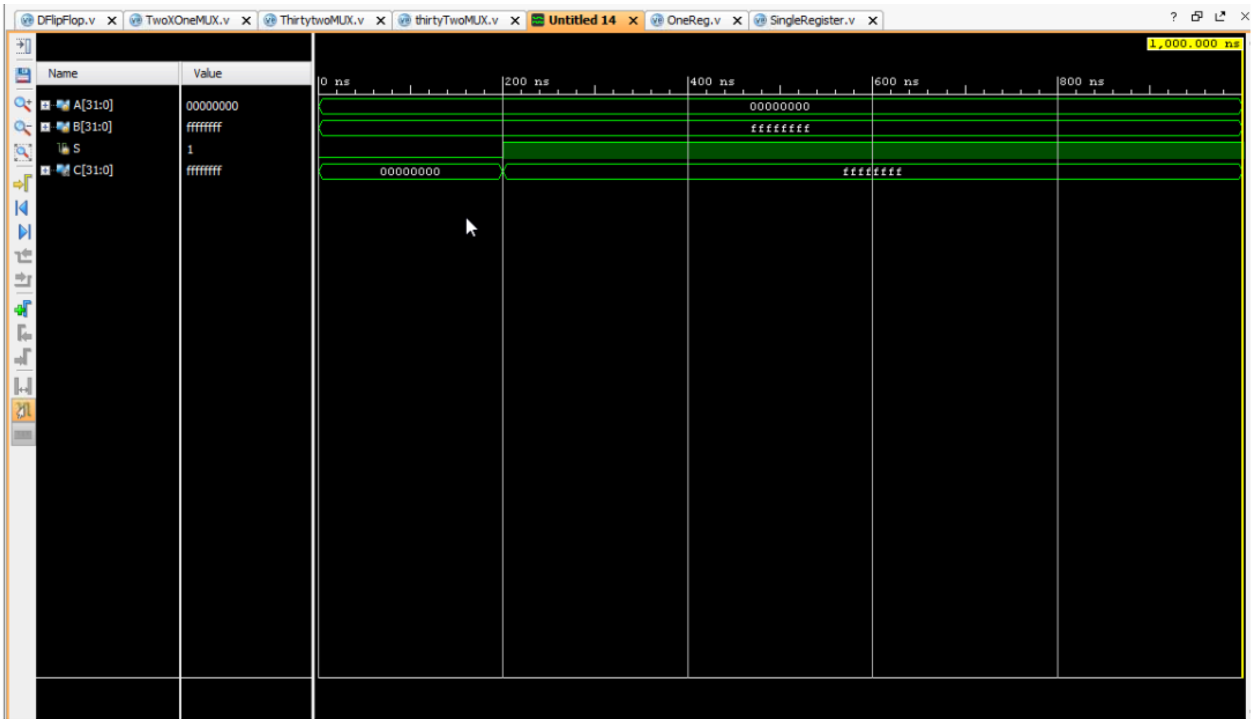
Results:

Exp1:



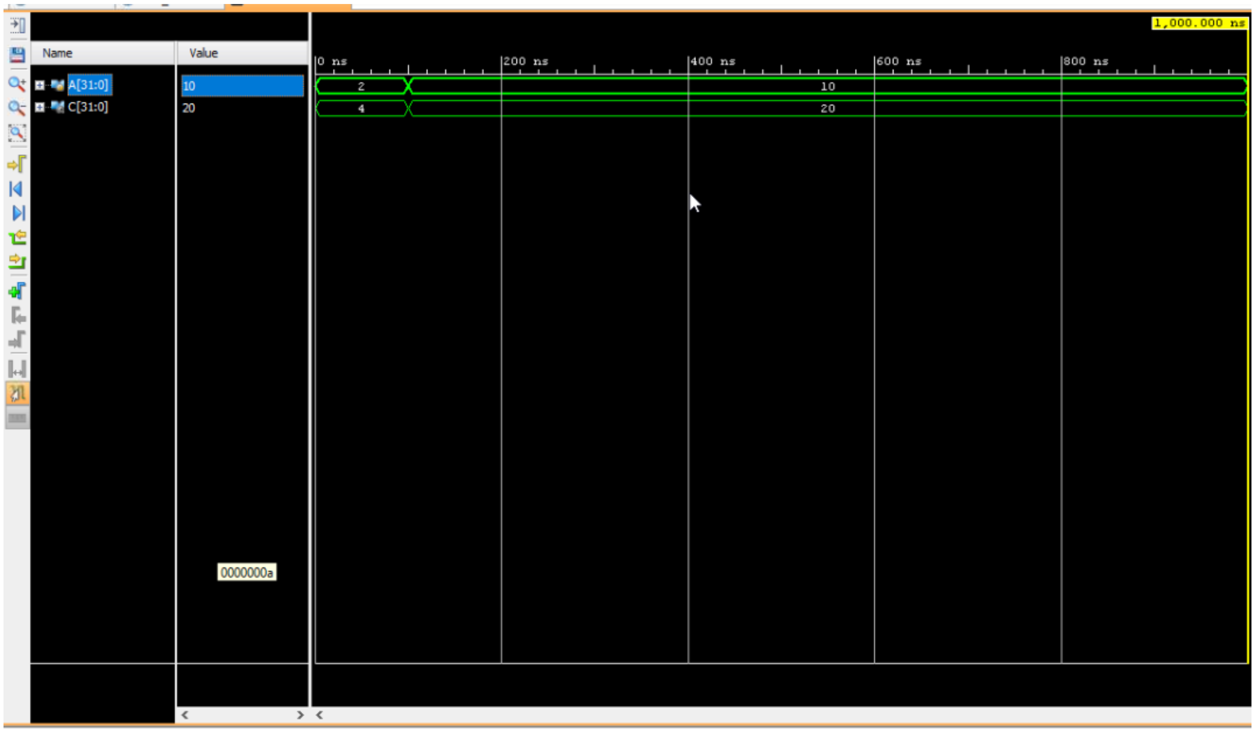
Name	Value
dk	0
S	1
in[31:0]	00000000
rst	1
Q[31:0]	00000000

Ex2

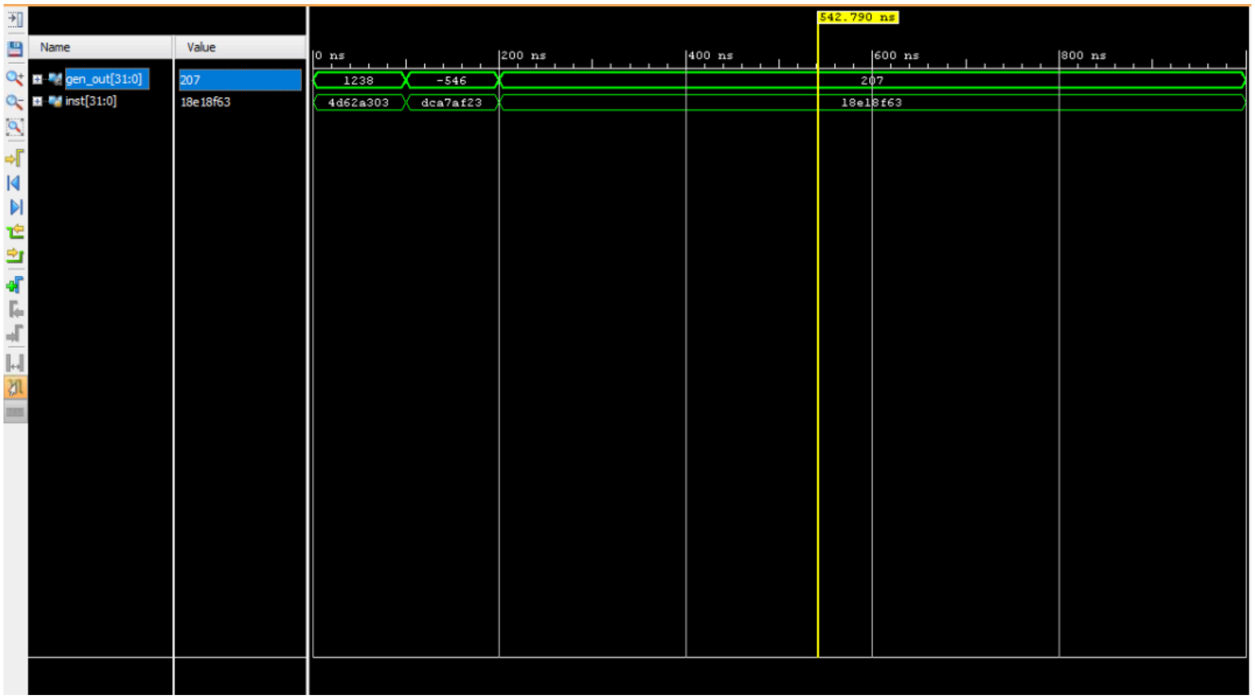


Name	Value
A[31:0]	00000000
B[31:0]	ffffffff
S	1
C[31:0]	ffffffff

Ex3:


1,000.000 ns
Name
Value
A[31:0]
10
C[31:0]
20
0000000a
0 ns
200 ns
400 ns
600 ns
800 ns
2
10
4
20

Ex4:


542.790 ns
Name
Value
gen_out[31:0]
207
inst[31:0]
18e18f63
0 ns
200 ns
400 ns
600 ns
800 ns
1238
-546
207
4d62a303
dca7af23
18e18f63

Question 1:
I add the case If it is 01, then shift to left

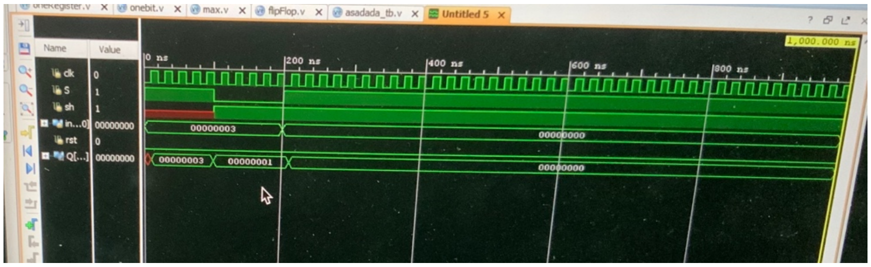
```
` `timescale 1ns / 1ps



module OneReg(input clk,input S,input sh,input [31:0] in,input rst, output
reg[31:0] Q );
 wire [1:0] Sl;
 assign  SL= {S,sh};
 wire[31:0] out;
genvar i;
generate
for (i=0;i<=31;i=i+1)
begin
    onebitReg mod1 (in[i],S,clk,rst,out[i]);
    end
   endgenerate


 always @(*)
 begin
 case(SL)
 2'b01: Q={1'b0,Q[31:1]};
 default: Q=out;
 endcase
 end
endmodule
```

Testbench:

```
// file: asadada_tb.v
// author: @andrewhany
// Testbench asadada_tb

`timescale 1ns / 1ps

module registertesting() ;

reg clk;
reg S;
reg sh;
reg [31:0] in;
reg rst;
wire [31:0] Q ;
OneReg  regis(clk, S,sh, in, rst,Q);
```

```
initial
begin
clk = 0;
 forever #10
clk=~clk;
end

initial
 begin

 S=1;
 in=3;
 rst=0;

 #100
 S=0;
 sh=1;
 #100
 S=1;
 in=0;




end
endmodule
```

Simulation:

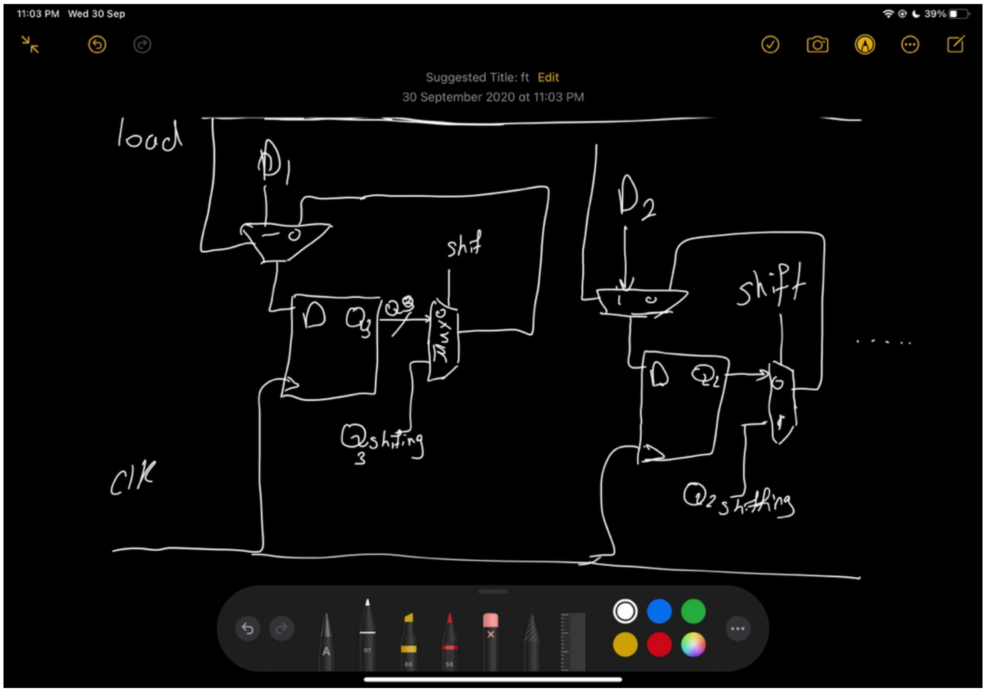


Name	Value
clk	0
S	1
sh	1
in...0]	00000000
rst	0
Q[...]	00000000

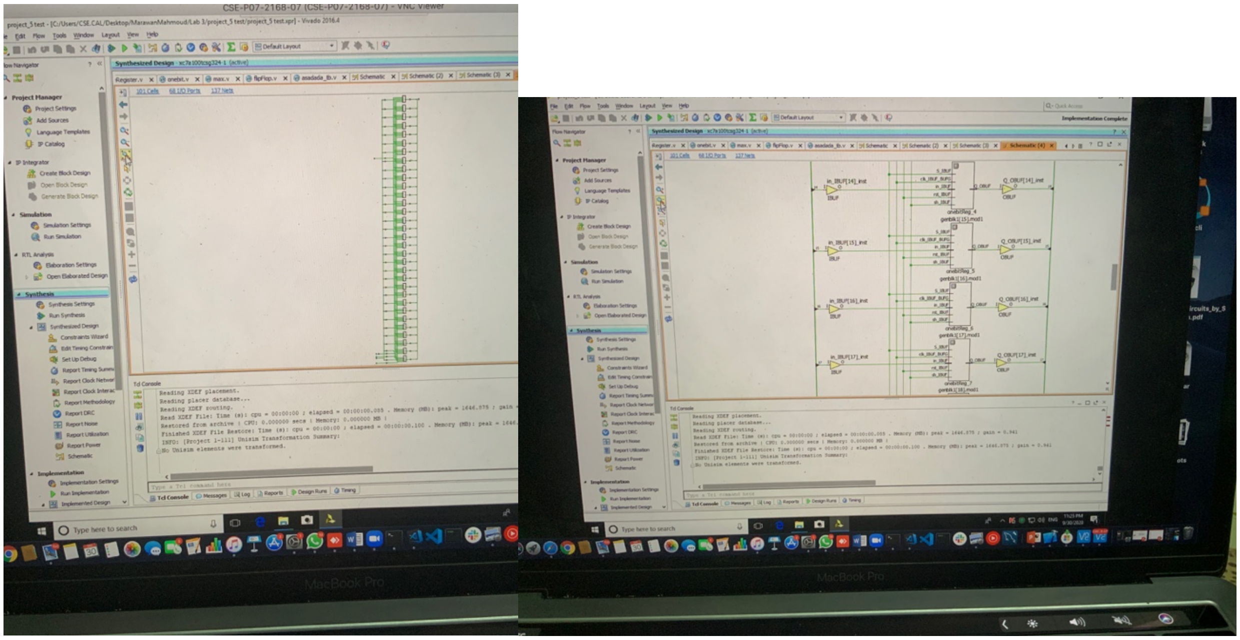
When I make the load by 1, I entered the value 3, when I make the load by zero and the shifting flag with 1, it shifts it to the right 011 to 001

Question 2:

- I tried to mak it by hand, to figure out the logic
- Here if the load = 1 then it will read a new data
- If it is load ==0, then we load at shif flag if it is 1 then we shift the Q and pass it to the flipFlop, otherwise it will pass the normal Q.



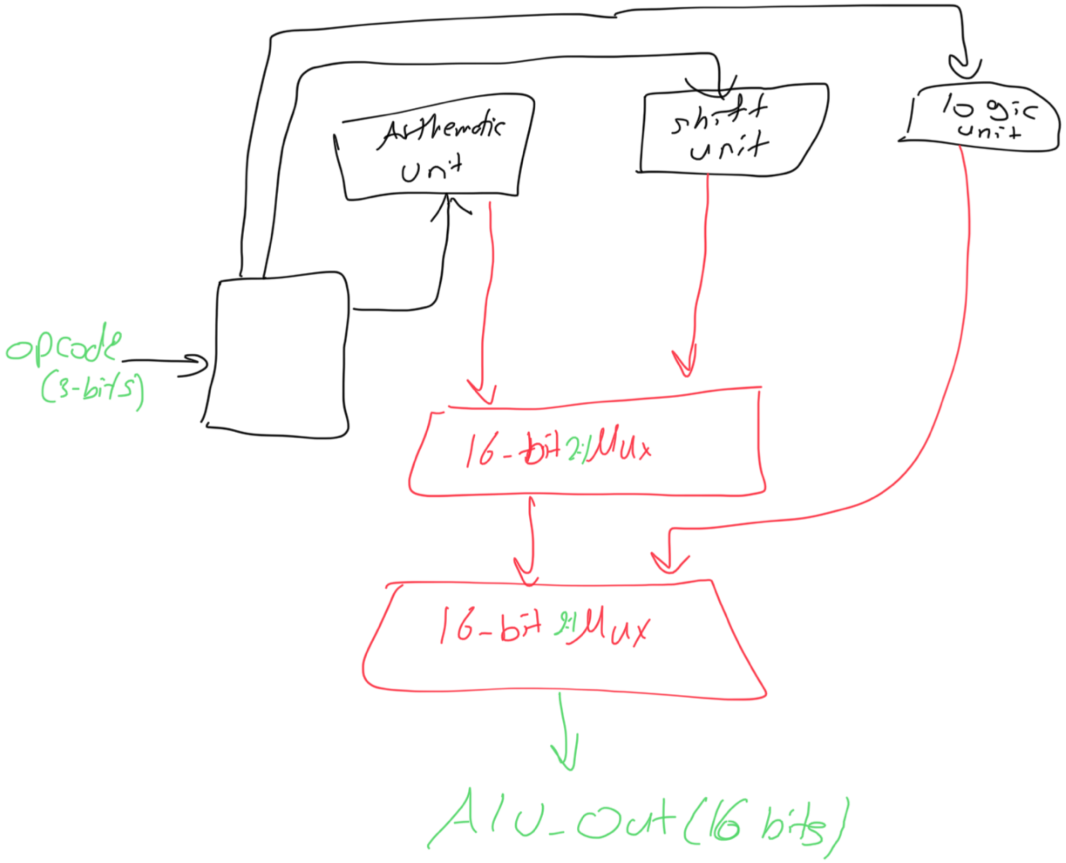
Schematic:



```
Reading XDEF placement.
Reading placer database...
Reading XDEF routing.
Read XDEF File: Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.085 . Memory (MB): peak = 1646.875 ; gain =
Restored from archive | CPU: 0.000000 secs | Memory: 0.000000 MB |
Finished XDEF File Restore: Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.100 . Memory (MB): peak = 1646.
INFO: [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.
```

Question 3:

- To support only 8 operation, so what we need is 3 bits only from the opcode


Arthemetic unit
shift unit
logic unit
opcode (3-bits)
16-bit 2:1 Mux
16-bit 2:1 Mux
AlU_Out (16 bits)