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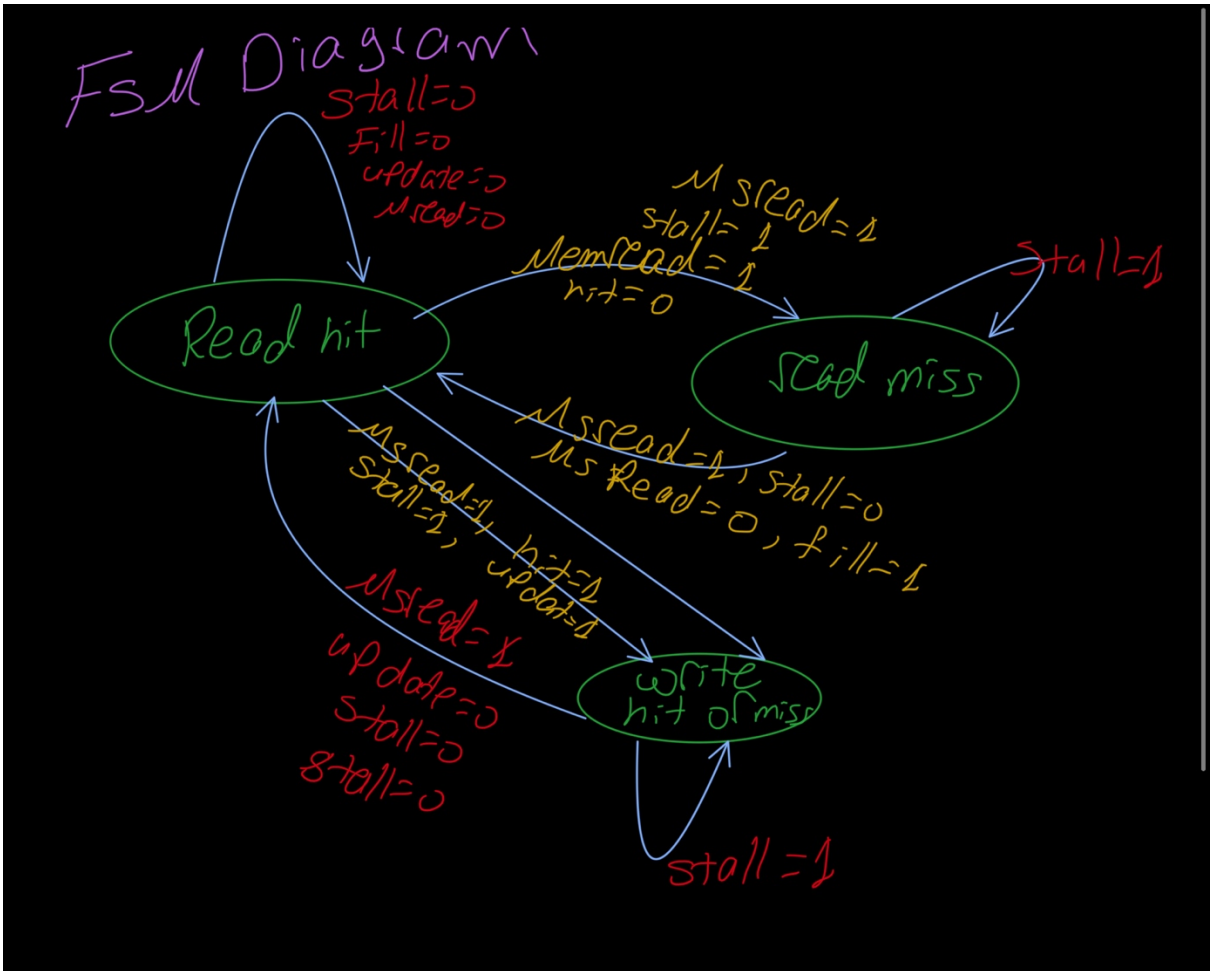
Lab 10

Experiment 3:

We did the cache controller



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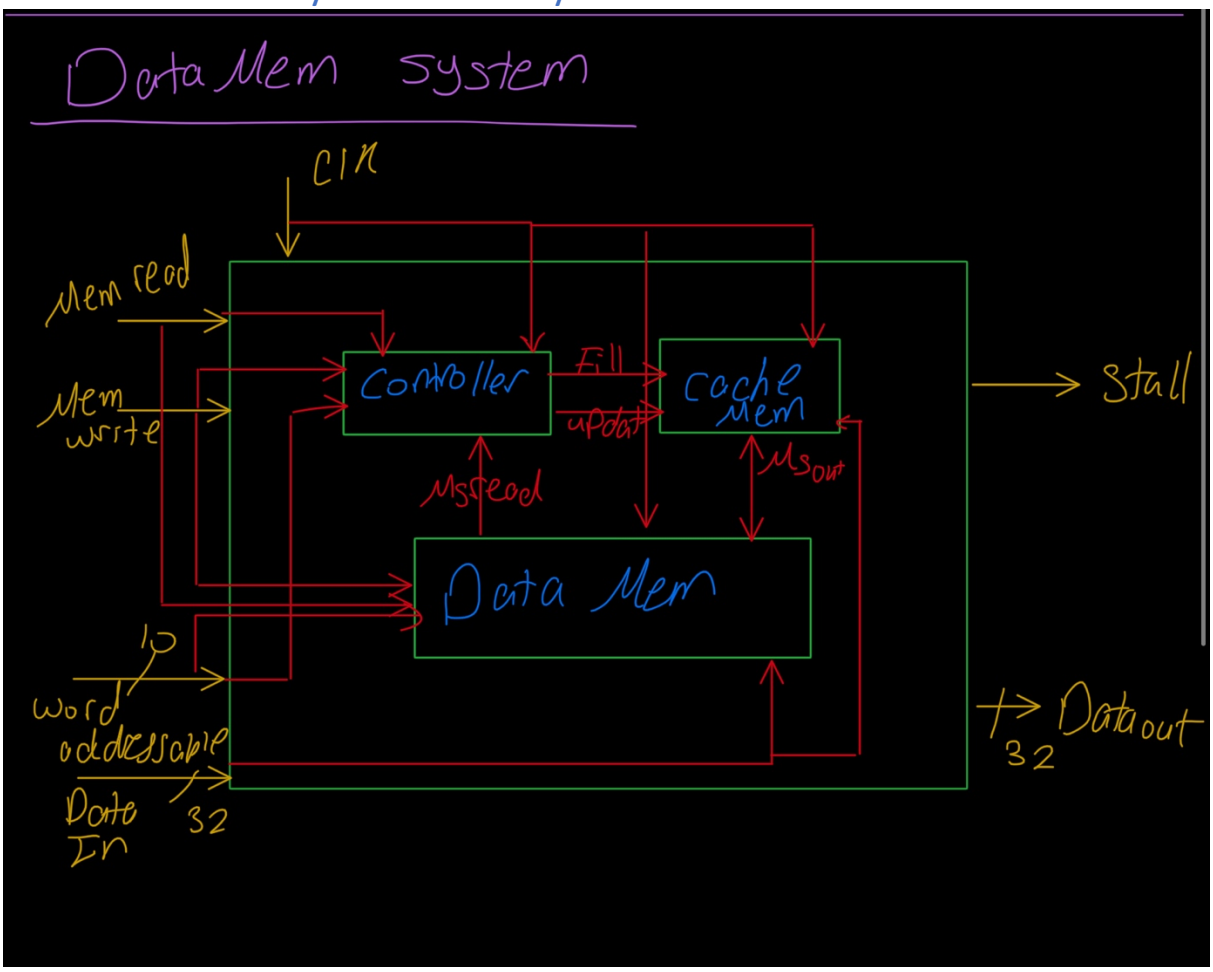
Experiment 4:

We did the data system memory module



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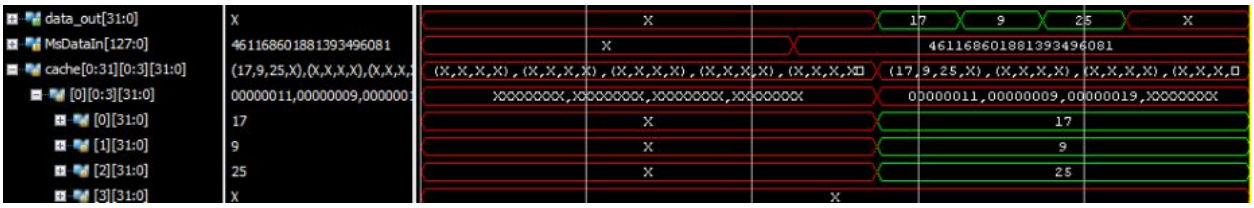
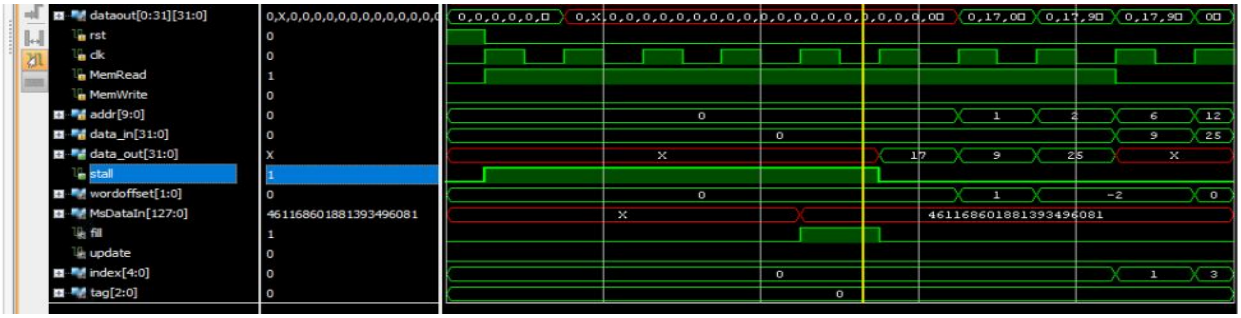
ScreenShots for simulation:

1)
These are the register file

2)
There are the cache



3) This is the stall signal and the PC results



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4)