Engineering Portfolio

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Bachelor's of Engineering
Electrical Engineering
Toronto Metropolitan University (Formerly Ryerson)

Power Electronics | Power Systems | Embedded Systems | Digital Circuit Design
Energy Management | Signal Processing | Control Systems | Renewable Energy

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Table of Contents

About Me

I am Andrew Arizaga, an Electrical Engineering student at *Toronto Metropolitan University* with a minor in Computer Science and Mathematics. Combining theoretical knowledge from my studies with practical experience from internships, I specialize in designing innovative solutions in embedded systems, power systems, and power electronics.

Previous Experience:

- **Assistant Energy Management Engineering Intern – City of Brampton**
  Worked on energy optimization projects, including LED retrofits and EV charging station installations. Assisted in analyzing HVAC systems and utility data using Excel automation to identify patterns and improve resource allocation.

- **Hardware Engineer Intern – Cence Power**
  Worked on designing and testing PCBs for high- and low-voltage systems using KiCAD and Altium. Contributed to integrating IoT-enabled energy monitoring systems and tested inventory management workflows for improved efficiency.

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Project 1 - Smart Power Management System Using Microcontroller

The **Smart Power Management System** improves energy efficiency by automating the control of lights and appliances based on **room occupancy** and **iris recognition**. The system is powered by an **ESP32-WROOM-32D microcontroller**, programmed in **C** using the **Espressif IoT Development Framework (ESP-IDF)**. It integrates **IR sensors** for real-time occupancy detection and advanced **iris recognition algorithms** for secure and personalized automation. Firmware development was carried out in **PlatformIO**, ensuring precise data handling and seamless operation of the sensors and relays.

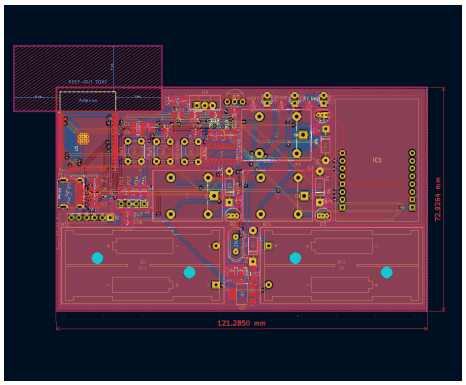

Figure 1: Custom PCB Layout Design for Project 1.

A **custom PCB**, designed in **KiCAD**, consolidates both **through-hole** and **surface-mount (SMD) components**, including **voltage regulators** for stable power delivery. The board layout prioritizes efficient power distribution, low signal interference, and scalability for future IoT integration. This combination of hardware and software creates a robust and adaptable system for managing energy consumption in smart home environments.

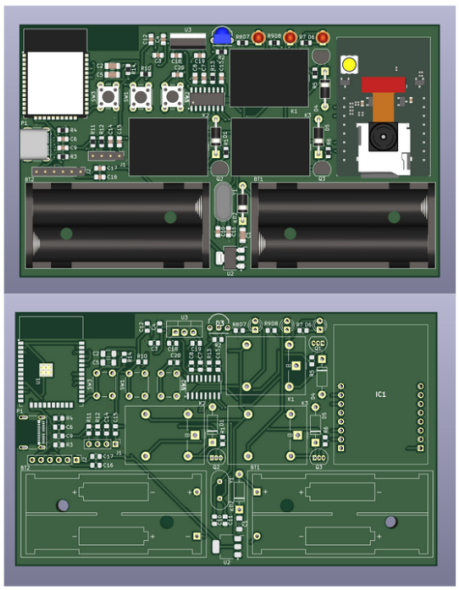

Figure 2: 3D- Model of Prototype with and without components.

The system automates appliance control during unoccupied periods, optimizing energy usage and reducing waste. It employs **IR sensors** for real-time occupancy detection and uses the **I2C protocol**, with lines like **SDA (data)** and **SCK (clock)**, for efficient communication between sensors and relays. This ensures accurate data handling and reliable control, critical for real-time smart home automation.

For iris recognition, the system integrates **SPI communication**, utilizing **MISO (Master In, Slave Out)** and **MOSI (Master Out, Slave In)** for secure, high-speed data exchanges. Low-power modes further reduce energy consumption during idle periods. Challenges such as reliable performance in low-light conditions were addressed through **sensor calibration** and **firmware enhancements**, ensuring robust and consistent operation.

The modular design supports seamless integration with existing **IoT ecosystems** and aligns with industry standards for automation. Future upgrades include **IoT connectivity**, **voice recognition**, and **PCB miniaturization** to enhance scalability and usability.

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Project 2 - Face & Voice Recognition AutoDoor Using Microcontroller

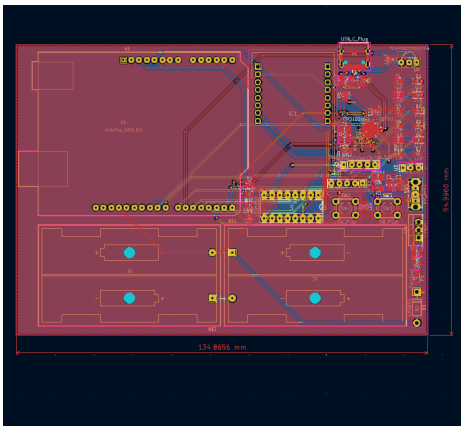

Figure 3: Custom PCB Prototype with PCB Layout

This project showcases an **advanced automation system** integrating **facial recognition** and **voice command processing** for secure, contactless access control. Designed for residential and commercial applications, the system uses an **ESP32-CAM module** for real-time facial recognition and a **serial voice recognition module** to process predefined commands. A motorized door mechanism, powered by a **5-wire unipolar stepper motor** and controlled via the **ULN2003 driver module**, ensures smooth and reliable operation.

The embedded software was written in **C** using **PlatformIO**, enabling modular and reusable code for both the **ESP32-CAM** and **Arduino Uno**. Optimized algorithms for facial recognition minimize processing time, while the voice recognition module uses **adaptive thresholds** for accurate command detection under varying conditions. A **state-machine approach** was implemented to manage system states, ensuring synchronized hardware interactions. Debugging and optimization were carried out using **serial monitors** and **logic analyzers**, enhancing real-time responsiveness and system reliability.

The custom **4-layer PCB**, designed in **KiCad 7**, integrates critical components such as the **L7805 voltage regulator**, bypass capacitors, and modular headers to support additional sensors and peripherals. **Power planes** and **segregated signal layers** minimize interference and ensure reliable operation under high-load scenarios. Strategically placed **decoupling capacitors** and **grounding planes** stabilize power delivery during simultaneous motor operations and data processing. Testing and simulation validated the board's performance, ensuring **thermal efficiency**, signal clarity, and operational reliability.

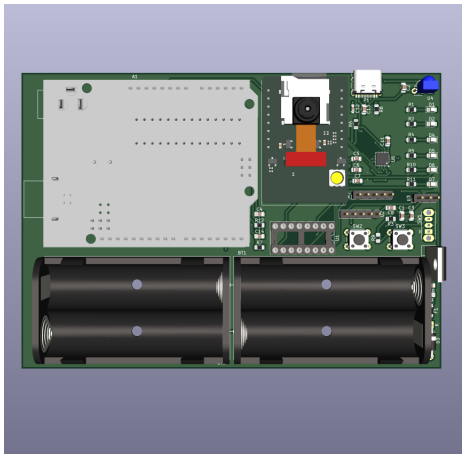

Figure 4: 3D-Model with Arduino and ULN2003 Motor Driver

This project resulted in a fully functional prototype that demonstrates expertise in **embedded systems**, **IoT communication**, and **hardware-software integration**. Future upgrades include integrating **RFID modules** for enhanced access control, **IoT connectivity** for remote monitoring, and further **PCB miniaturization** to improve scalability. With applications in **smart homes**, **secure workplaces**, and **accessible public facilities**, the system highlights the ability to create innovative, real-world engineering solutions.

Project 3 - Python Program for Ladder Iterative Load Flow

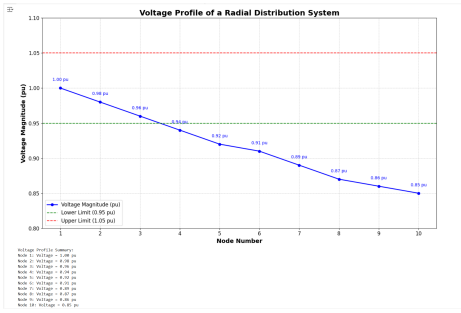

Figure 5: Visualization of Load Flow Results.

This project involved designing and implementing a **Python-based application** to analyze radial three-phase power distribution systems using the **Ladder Iterative Load Flow algorithm**. The software computes **voltage profiles**, **power flows**, and **system losses** with high accuracy, providing a robust solution for academic and professional use in **power systems engineering**. The goal was to automate load flow analysis, ensuring scalability, modularity, and efficiency for large datasets.

The program processes **IEEE-standard input data** from Excel files, which include information about **buses**, **branches**, and line impedances. Results are exported into an **IEEE-compliant Excel format**, ensuring compatibility with widely used power system tools. The core **Ladder Iterative Load Flow algorithm** iteratively balances active and reactive power at each bus while calculating voltages and power flows efficiently. **Error handling mechanisms** detect invalid or missing data, providing clear, actionable feedback to users.

The software was developed in **Python**, utilizing libraries such as **pandas** for data manipulation, **numpy** for numerical computations, and **openpyxl** for Excel input/output operations. Its modular architecture includes components for **input validation**, **algorithm execution**, and **output generation**, supporting scalability and maintainability. An optional **graphical user interface (GUI)** built with tkinter simplifies user interaction by enabling file uploads, real-time execution, and result visualization. The codebase is hosted on **GitHub**, facilitating collaboration and version control.

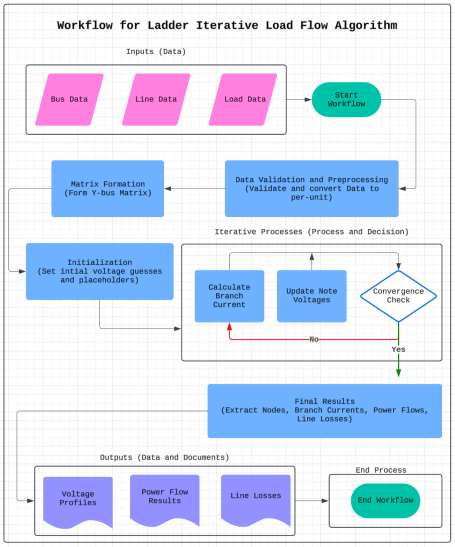

Figure 6: Workflow Diagram.

Extensively tested against **IEEE standard datasets**, the program demonstrated high accuracy and reliability. A Python-based **unittest framework** was used to validate input/output handling and algorithm convergence. Future enhancements include integrating with **hardware components** for **real-time monitoring** and adding **cloud-based computation** to enable distributed processing. This project showcases expertise in **power systems engineering**, **Python programming**, and **modular software design**, providing a scalable solution for modern engineering challenges.

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Project 4 - FPGA-Based General-Purpose Processor Design

I designed and implemented a **simple general-purpose processor** using **Quartus II**, **VHDL**, and an **Altera FPGA board**. This project combined **combinational and sequential logic** to create a fully functional hardware system capable of executing various operations. It demonstrated my proficiency in **digital system design**, **hardware programming**, and **problem-solving**, as well as my ability to optimize digital components.

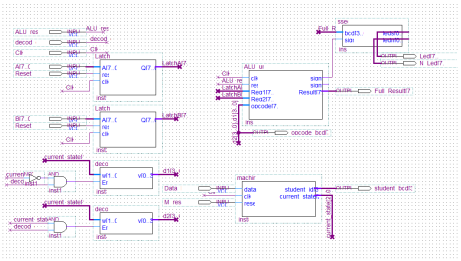
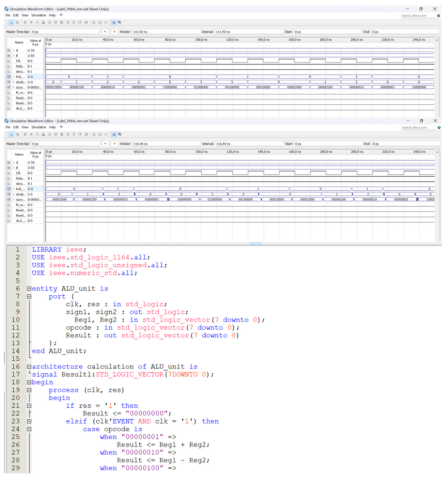


Figure 7: Block Diagram of the Processor Architecture

The processor's **Arithmetic and Logic Unit (ALU)** was designed to perform operations such as **addition**, **subtraction**, and **bitwise AND/OR/XOR**, processing **8-bit binary inputs** with precision. Its functionality was controlled by a programmable **8-bit Opcode**, generated via a **3x8 decoder**. To ensure efficient data flow, I designed a pipeline architecture connecting **input registers**, the **ALU**, and **output modules**. The control unit, implemented as a **Finite State Machine (FSM)** in **VHDL**, managed instruction sequencing with synchronized fetch and execute cycles. Troubleshooting included analyzing **state transitions** and refining **control signals** for reliable operation.



```
LIBRARY ieee;
USE ieee.std_logic_1164.all;
USE ieee.std_logic_unsigned.all;
USE ieee.numeric_std.all;

entity ALU_unit is
    port (
        clk, res : in std_logic;
        sign1, sign2 : out std_logic;
        Reg1, Reg2 : in std_logic_vector(7 downto 0);
        opcode : in std_logic_vector(7 downto 0);
        Result : out std_logic_vector(7 downto 0)
    );
end ALU_unit;

architecture calculation of ALU_unit is
signal Result1:STD_LOGIC_VECTOR(7DOWNTO 0);
begin
    process (clk, res)
    begin
        if res = '1' then
            Result <= "00000000";
        elsif (clk'EVENT AND clk = '1') then
            case opcode is
                when "00000001" =>
                    Result <= Reg1 + Reg2;
                when "00000010" =>
                    Result <= Reg1 - Reg2;
                when "00000100" =>
```

Figure 8: Simulation Results or FPGA Implementation

I designed **8-bit registers** and integrated **D-type and T-type flip-flops** to manage synchronous clocking and asynchronous resets, ensuring stable operation and minimizing timing errors. For real-time output visualization, I programmed **7-segment displays** to showcase ALU results, splitting the **8-bit outputs** into two **4-bit signed values**. Custom **sign-handling logic** ensured accurate representation of positive and negative results.

Using **Quartus II**, I synthesized and simulated each processor component, validating functionality through timing and logic tests. Debugging with the **Waveform Editor** helped optimize **propagation delays** and address **glitches** in critical paths, such as the decoder. Resource optimizations on the FPGA were achieved through **Boolean algebra** and modular **VHDL coding practices**.

This project highlights my expertise in **digital processor design**, integrating tools like **VHDL**, **FSMs**, and **flip-flop architectures** to create a robust and efficient system. It also underscores my ability to troubleshoot and optimize hardware, positioning me as a strong candidate for roles in **digital systems design**, **embedded systems engineering**, and **hardware development**.

Project 5 - Academic Intervention Analysis Report

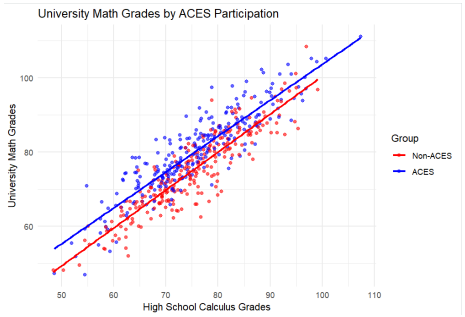


Figure 9: Visualization of Performance Trends.

This project applied **Propensity Score Analysis (PSA)** to evaluate the **Academic Career Enrichment Support (ACES) program**, designed to support first-year engineering students at **Toronto Metropolitan University (TMU)**. PSA is a statistical methodology used to address **confounding variables** in observational studies, providing a rigorous framework to estimate causal effects without randomized controlled trials. The ACES program bridges gaps in **STEM education** by offering **tutoring**, **mentoring**, and tailored resources to improve academic success.

Data for the analysis was sourced from **SQL databases**, incorporating **student demographics**, **high school grades**, and **university outcomes**. Propensity scores were estimated using **logistic regression** in **R**, with alternative techniques like **random forests** employed to capture nonlinear relationships. Covariate balance between treated (ACES participants) and untreated groups was evaluated using **Standardized Mean Differences (SMDs)**, **variance ratios**, and graphical tools such as **Love plots**, ensuring unbiased comparisons.

The program's impact was quantified through metrics like the **Average Treatment Effect (ATE)** and the **Average Treatment Effect on the Treated (ATT)**. Results were visualized in **Power BI**, highlighting **student performance trends**, **program effectiveness by region**, and **intervention intensity correlations**. Dashboards featured **dynamic filters** and **drill-down capabilities**, enabling stakeholders to derive actionable insights. Data preprocessing and cleaning were conducted in **Excel**, while final reports were compiled using **Microsoft Word** and **LaTeX** to ensure professionalism and clarity.

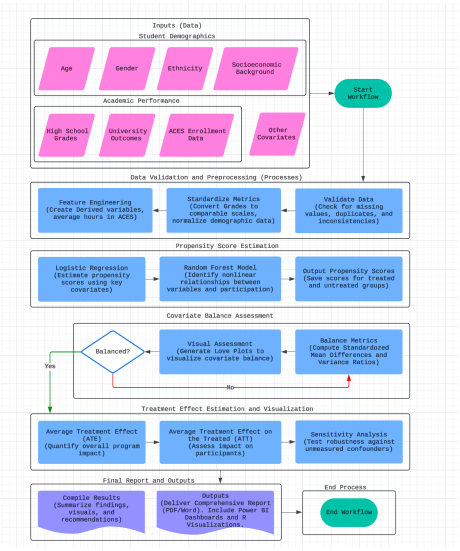


Figure 10: Workflow Diagram for PSA, Data Validation.

This project demonstrated expertise in **statistical modeling**, **data analysis**, and **visualization tools** such as **R**, **SQL**, and **Power BI**. By validating the effectiveness of the ACES program, the analysis provided actionable recommendations to improve academic support. Future applications include extending PSA to **longitudinal studies**, integrating advanced **machine learning algorithms**, and generalizing findings to broader contexts.

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Project 6 - Toronto Metropolitan Baja Racing – Manufacturing Lead

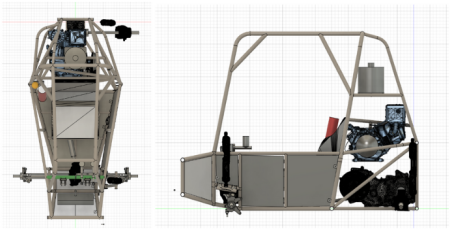

Figure 11: Chassis Design in SolidWorks.

As the **Manufacturing Lead** for the **TMU Baja Racing Team**, I led the design, simulation, and fabrication of a **high-performance chassis** for an off-road **Baja SAE competition vehicle**. The project demanded expertise in **structural analysis**, **manufacturing optimization**, and **technical documentation**, ensuring compliance with **Baja SAE standards** while achieving superior performance and safety.

The chassis was developed in **SolidWorks**, focusing on a **lightweight yet durable frame** optimized for **weight distribution** and **modularity**. **Finite Element Analysis (FEA)** was conducted to assess **stress**, **deformation**, and **failure modes** under various conditions, including **front, rear, and side impacts**. These simulations validated the chassis's ability to withstand **collisions** and **high torque loads** during rugged terrain navigation and acceleration.

Fabrication involved the use of **Fusion 360** for validating angles, clearances, and assembly feasibility. I supervised the **welding and assembly process**, ensuring precise alignment of components and compliance with **ergonomic standards** for driver safety. High-strength materials and advanced **welding techniques** were employed to enhance durability under **extreme environmental conditions**.

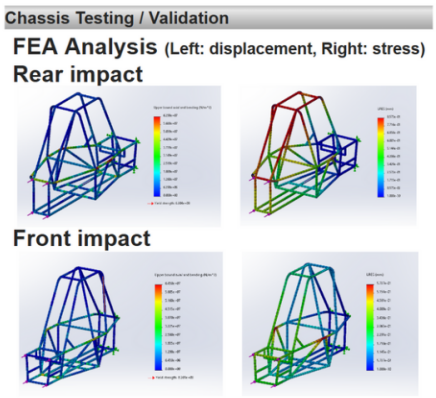

Figure 12: Finite Element Analysis in SolidWorks.

Field testing assessed the chassis's **impact resistance**, **torsional rigidity**, and **structural performance** under real-world scenarios, including rugged terrain simulations. Detailed **technical drawings** were prepared to streamline procurement and ensure compatibility with supplier standards, balancing **cost-effectiveness**, **structural integrity**, and **weight efficiency**. Collaboration with team members across mechanical and electrical subsystems ensured seamless integration, further contributing to the vehicle's overall performance. This project highlights my ability to lead **cross-functional teams**, integrate **simulation and manufacturing processes**, and deliver innovative solutions. By combining **CAD design**, **FEA simulations**, and **hands-on fabrication**, I successfully delivered a competition-ready chassis that met all **Baja SAE safety and performance evaluations**.

Thank You!

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