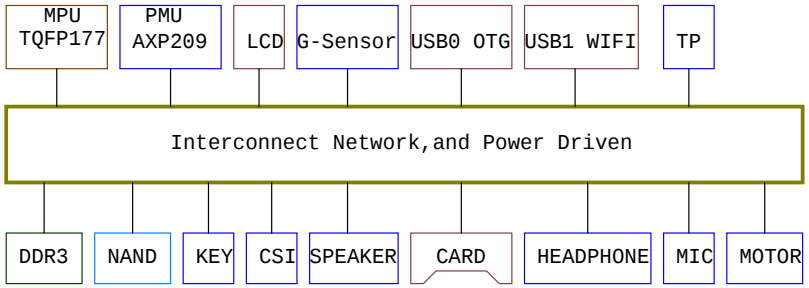
COVER

BLOCK

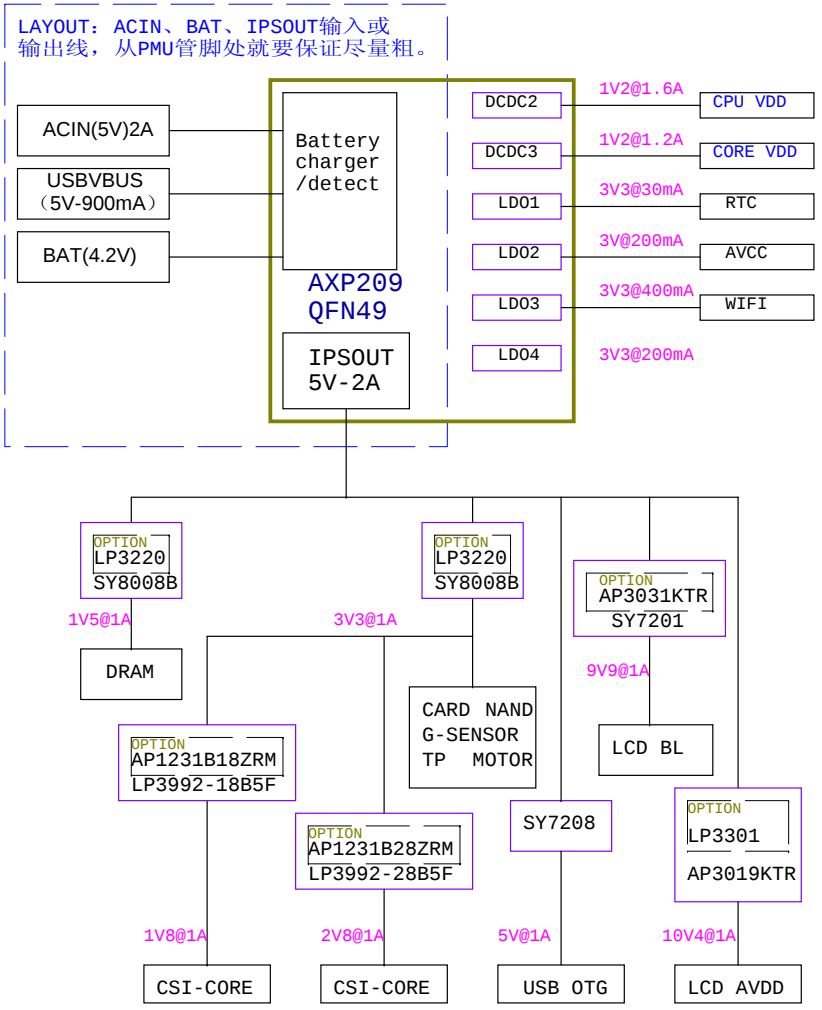


GPIO ASSIGNMENT

CPU	Define	Function
PB0	TWI0_SCK	TWI0
PB1	TWI0_SDA	
PB2	PWM0	LCD
PB3	GPIO-OUT	TP-WAKE-RST
PB4	NC	
PB10	GPIO-OUT	CSI-STY
PB15	TWI1_SCK	TWI1
PB16	TWI1_SDA	
PB17	TWI2_SCK	TWI2
PB18	TWI2_SDA	
PG0	INPUT	SD0-DET-N
PG1	GPIO-IN	USB0-VBUSDET
PG2	GPIO-IN	USB0-IDDET
PG3	GPIO-OUT	CSI-STY-1
PG4	GPIO-OUT	CSI-RST-1
PG9	GPIO-OUT	MT-EN
PG10	GPIO-OUT	PA-SHDN
PG11	EINT	TP-INT
PG12	GPIO-OUT	USB0-DRV
PMU	Define	Function
GPIO0	GPIO-OUT	LCD-PWR
GPIO1	GPIO-OUT	LCD-BL-EN
GPIO2	GPIO-OUT	CSI-PWR-EN
GPIO3	GPIO-OUT	CSI-RST

特别提醒：
1: PG0 / PG1 / PG2这三个PIN脚只具有INPUT/中断/专有功能
2: PMU的GPIO0/1/2/3这四个PIN脚只做GPIO-OUTPUT功能
3: PG10 /PG11 /PG12这三个PIN脚的功能不可改变

POWER TREE



Schematics Index

01 COVER
02 CPU
03 POWER
04 MEMORY
05 DISPLAY
06 MISC
07 WIFI

REVISION HISTORY

Revision	Description	Date	Drawn	Checked	Approved
APP3_PAD_DDR3_V1_22	version 1.22		YT		
APP3_PAD_DDR3_V1_23	version 1.23	2012.03.28	YT		

Title	APP3_PAD_DDR3	
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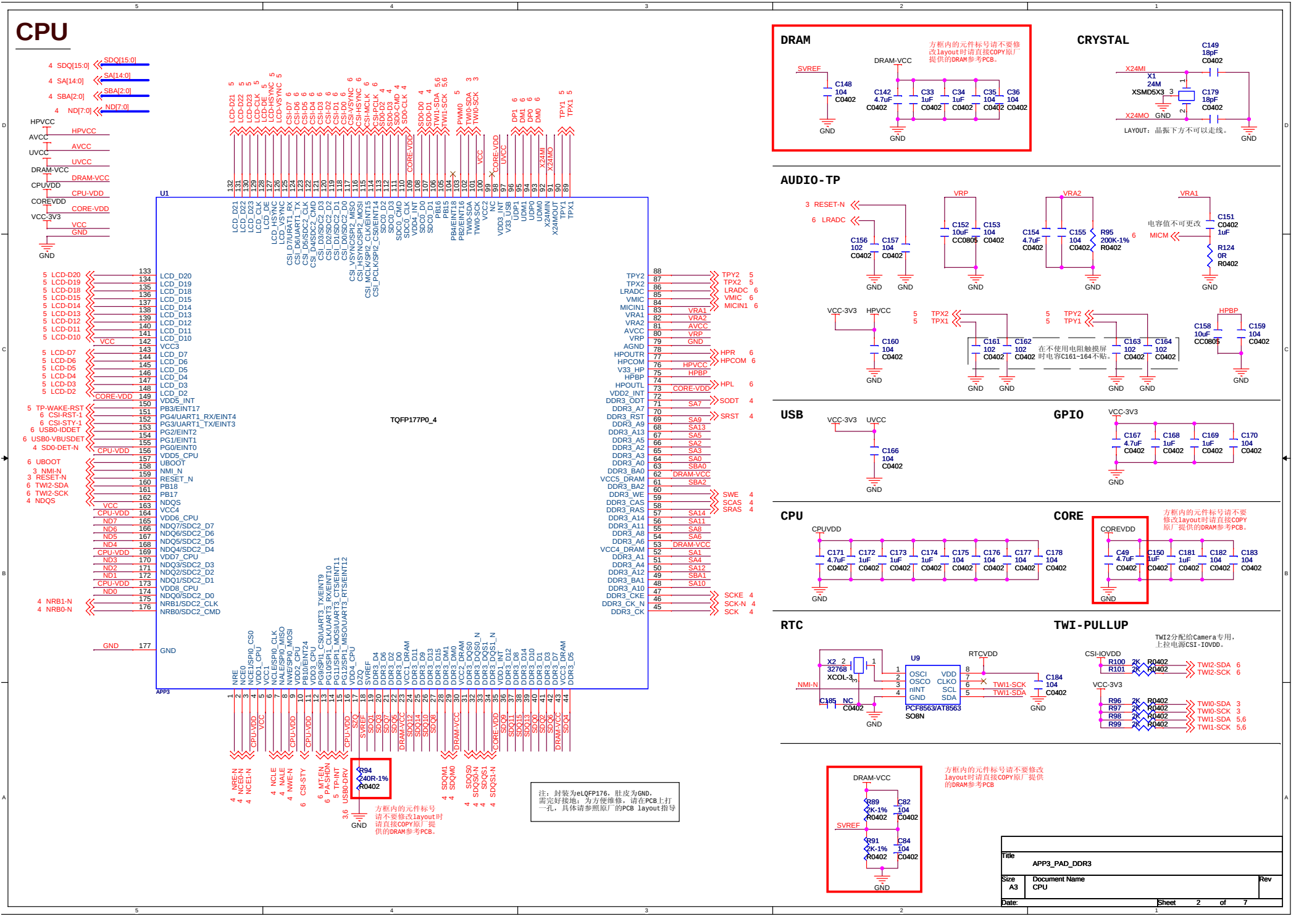
CPU



DRAM

CRYSTAL

AUDIO-TP

USB

GPIO

CPU

CORE

RTC

TWI-PULLUP

方框内的元件标号请不要修改layout时请直接COPY原厂提供的DRAM参考PCB

Title	APP3_PAD_DDR3	
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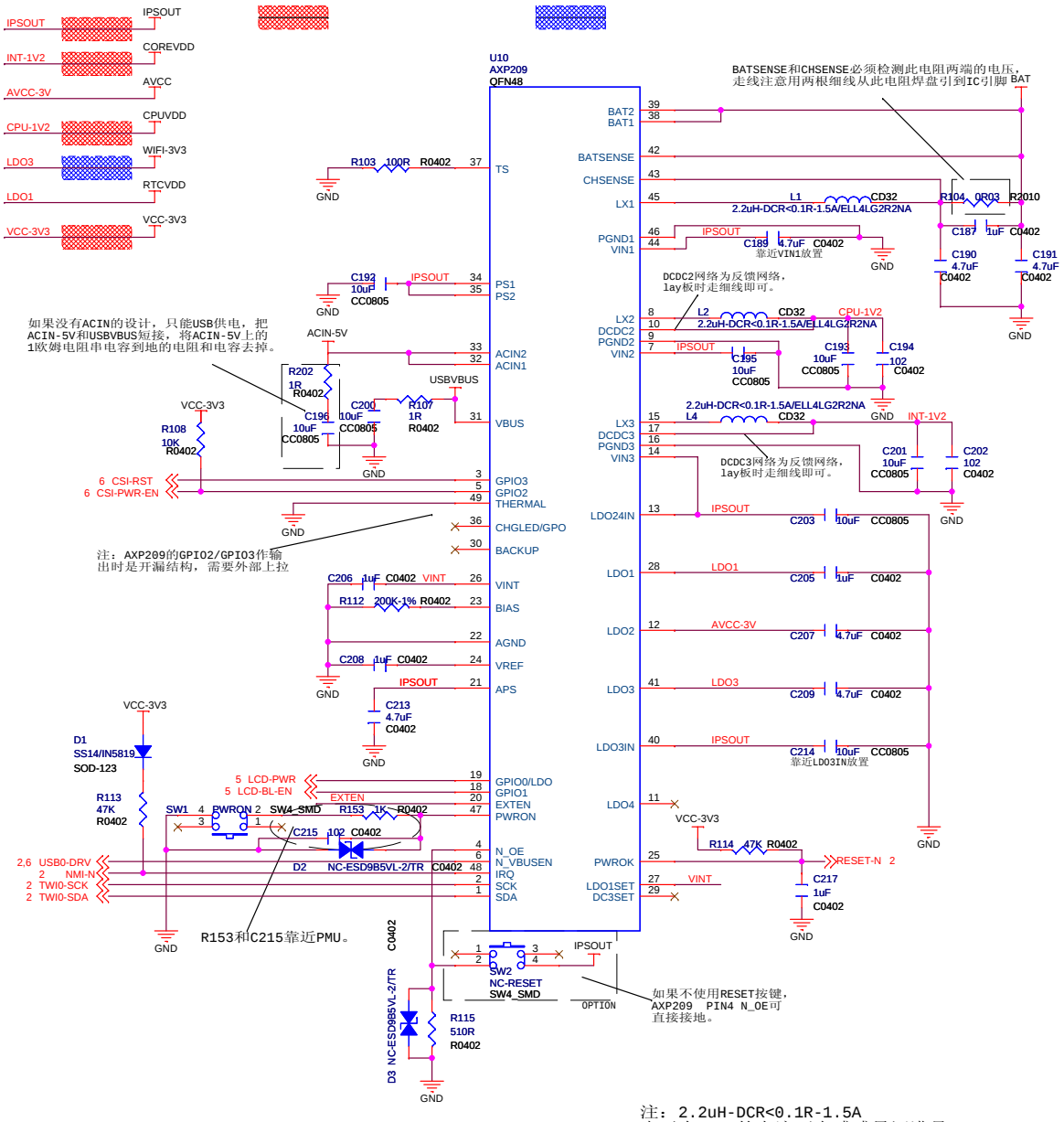
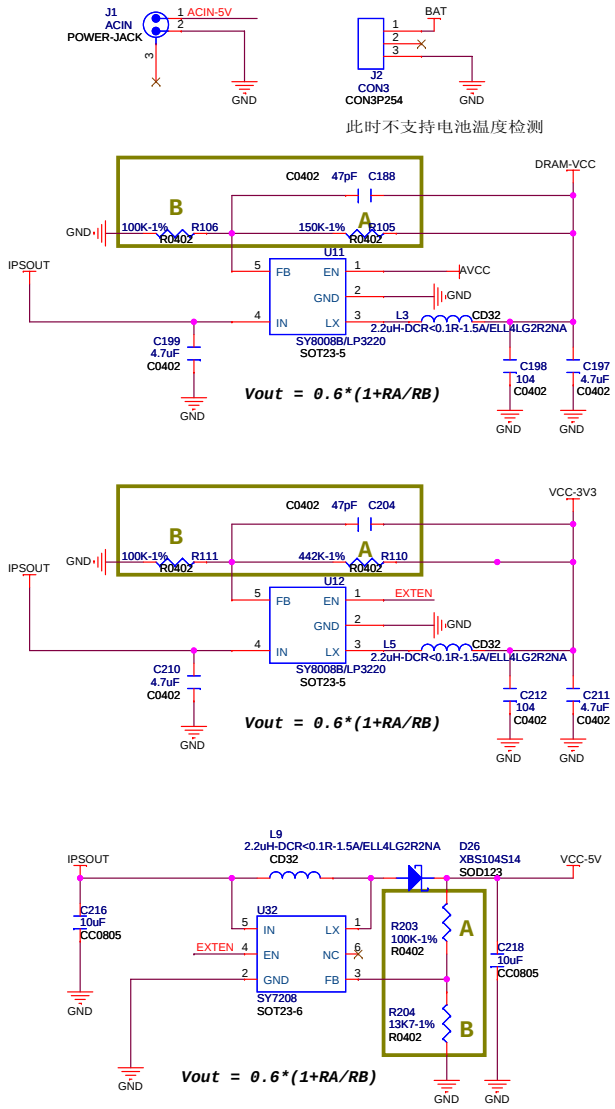
POWER

POWER LINE:Width>=80mil POWER LINE:Width>=50mil





注：2.2uH-DCR<0.1R-1.5A
表示在1.5A的电流下电感感量还满足2.2uH，
DCR<0.1R表示电感直流电阻要小于0.1欧姆。

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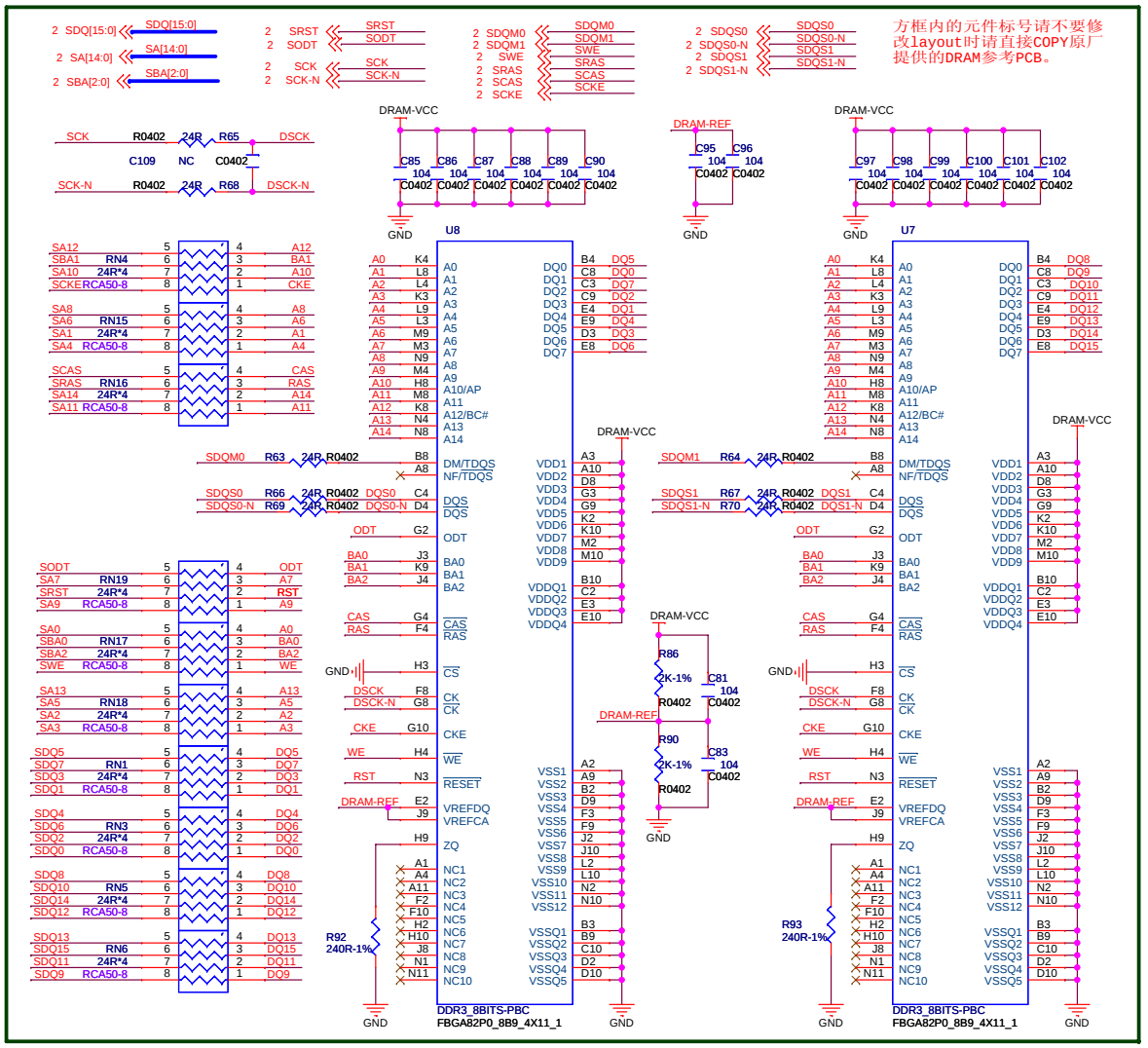
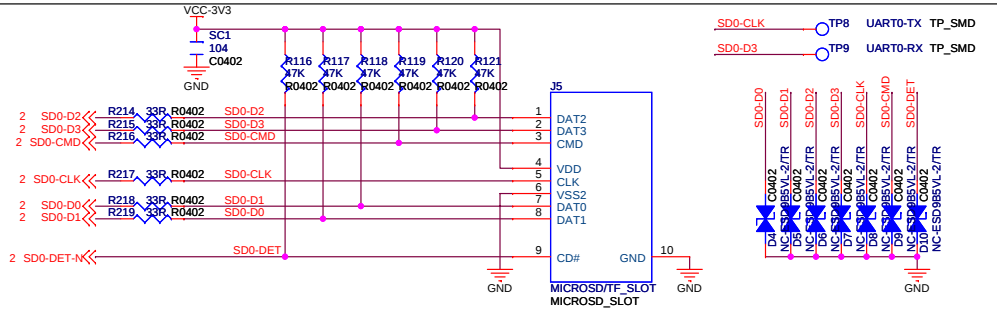
MEMORY

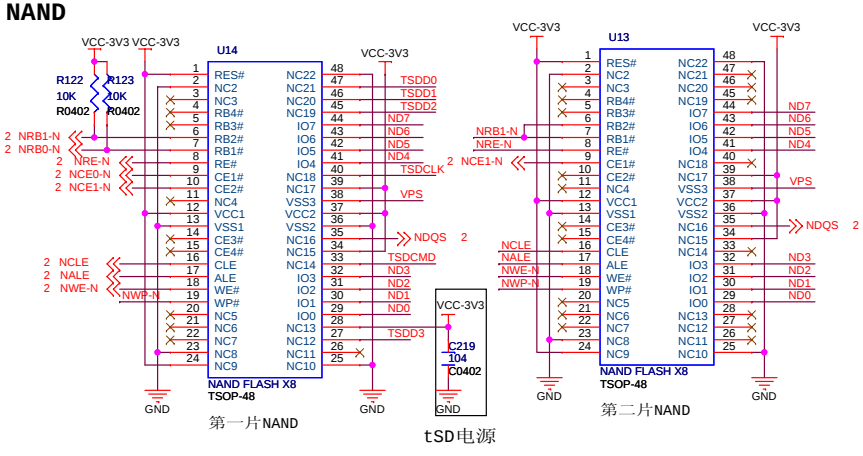
DDR3



CARD

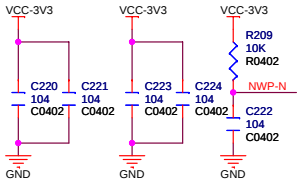


NAND



tSD电源

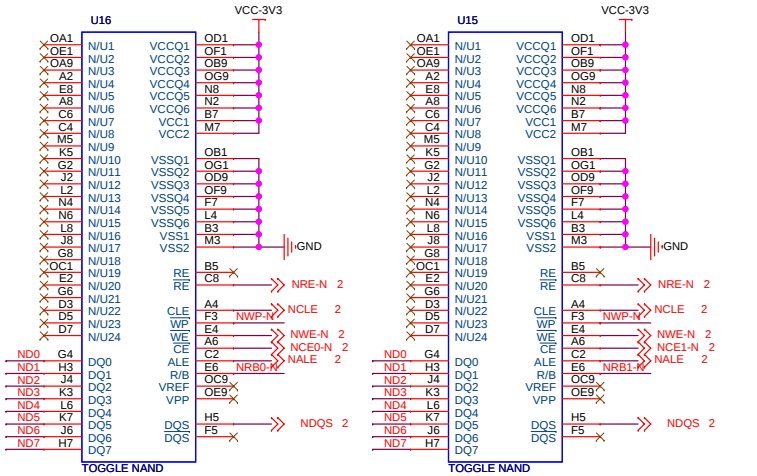
注：只贴一片NAND FLASH时，请贴在U14



注：VPS的上下拉，具体请参见所用NAND FLASH的datasheet。

此种连接方式兼容tSD和TSOP NAND。

注：只贴一片TOGGLE NAND时，请贴在U16



PCB上TOGGLE NAND与TSOP NAND双layout
(U14与U16双LAY，U13与U15双LAY)

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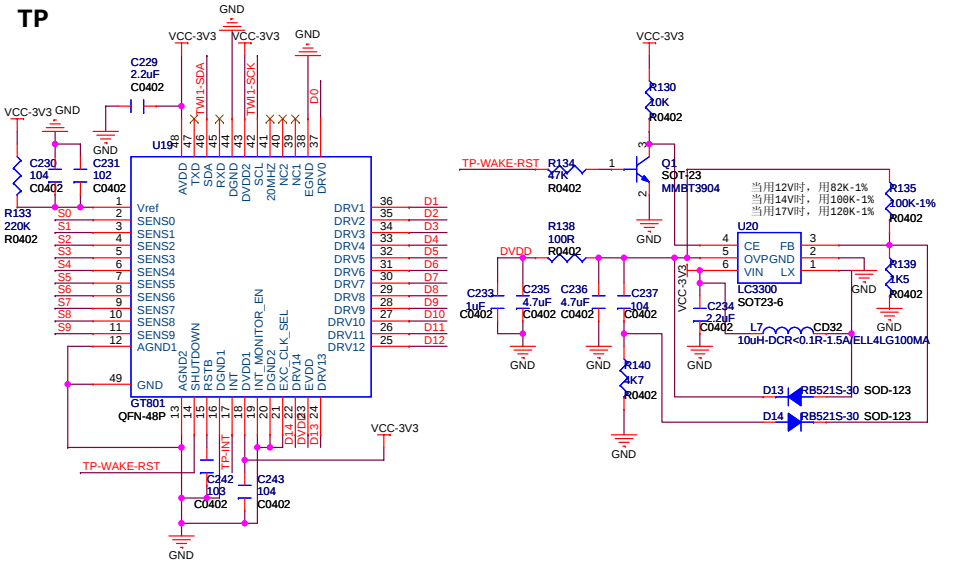
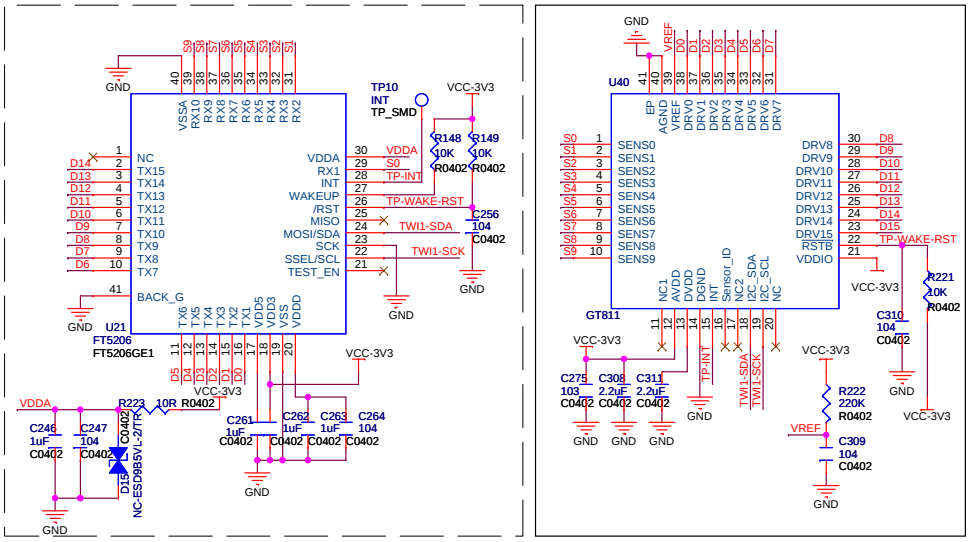
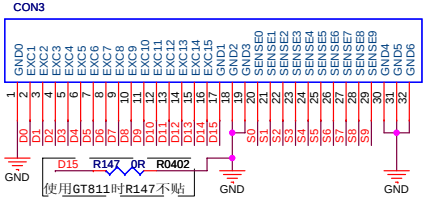
DISPLAY

TP

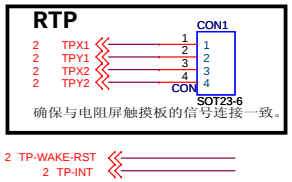


PCB上双LAYOUT

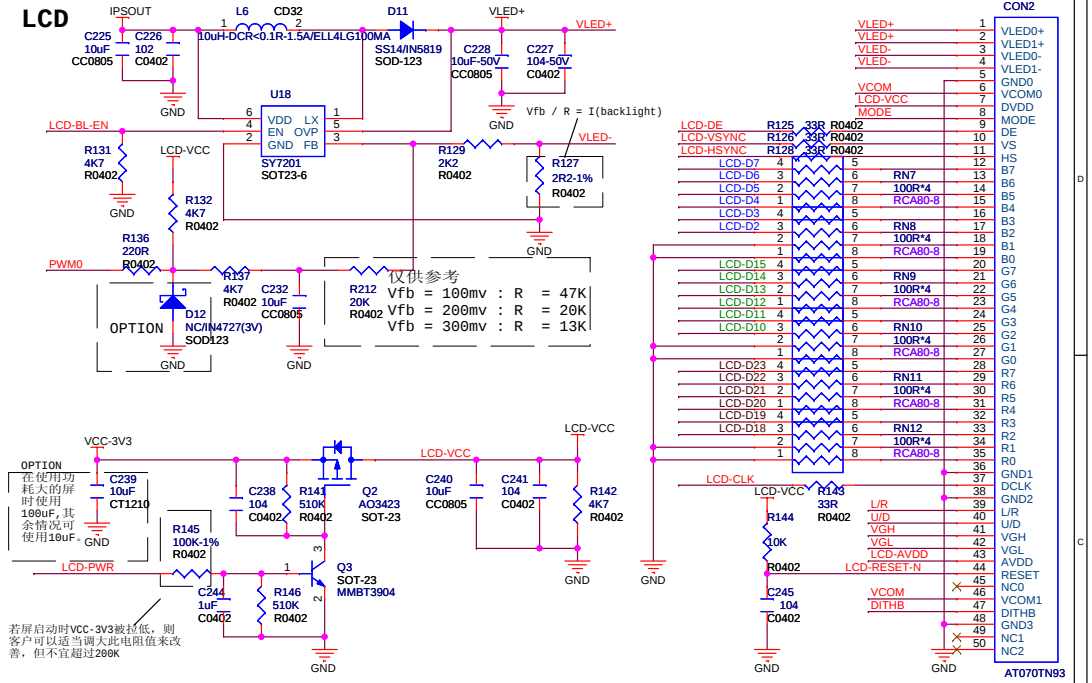


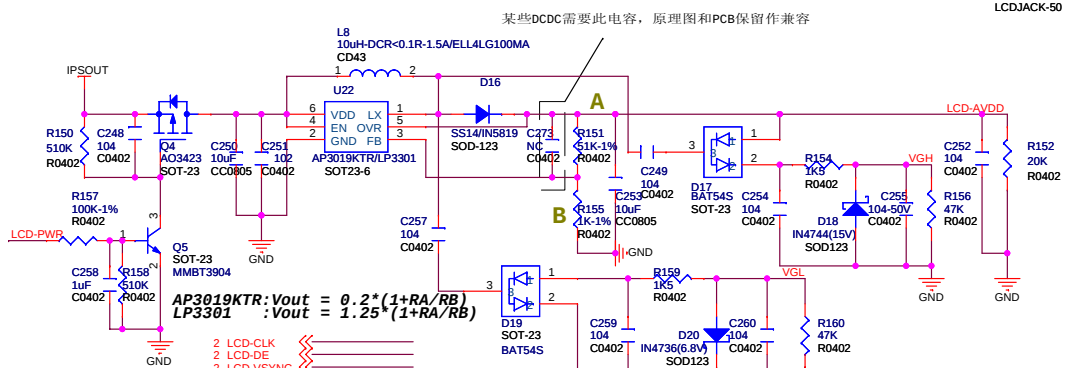


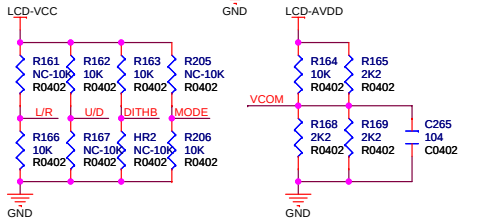
RTP



LCD







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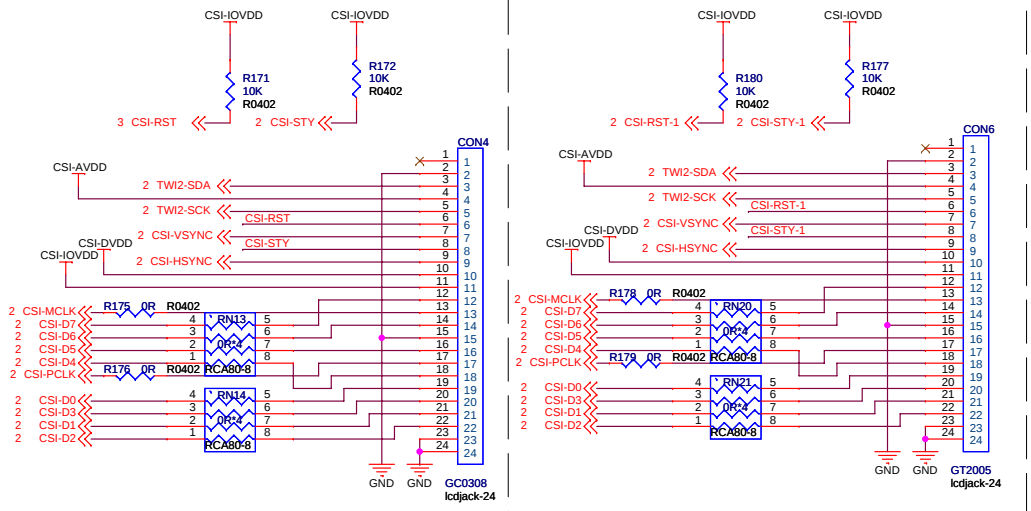
MISC

CSI

30W-前置低分辨率

OPTION

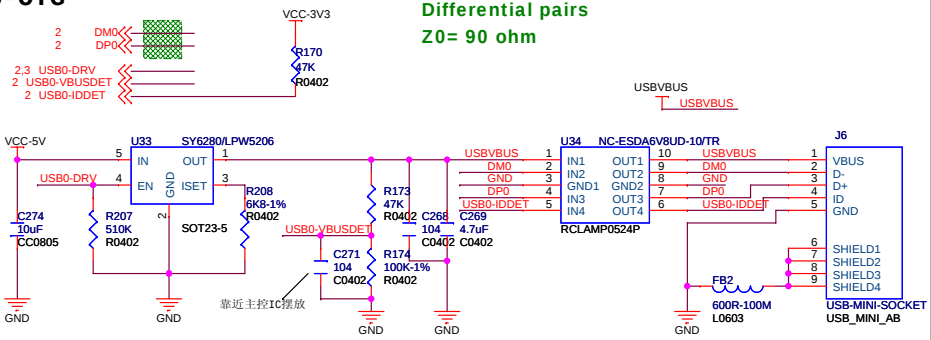
200W-后置高分辨率

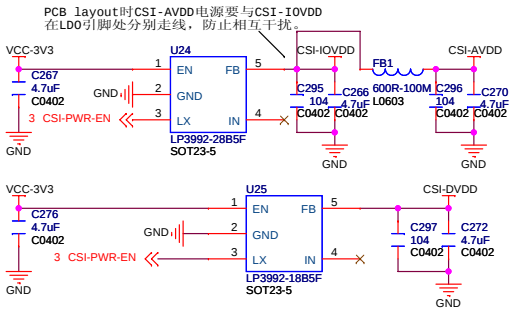


A.LAYOUT时，请保证摄像头成像方向与LCD显示一致
B.若选用其他模组，请检查CSI-IOVDD,CSI-AVDD,CSI-DVDD的
具体电压值以及负载能力能够满足

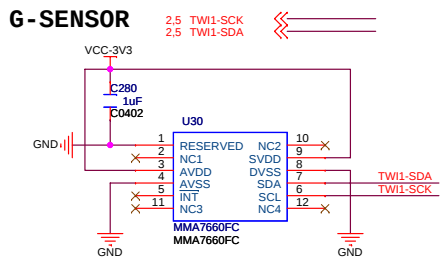
USB-OTG

Differential pairs
Z0= 90 ohm

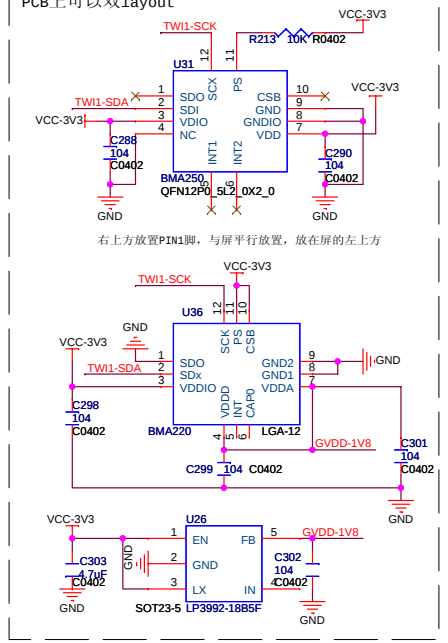




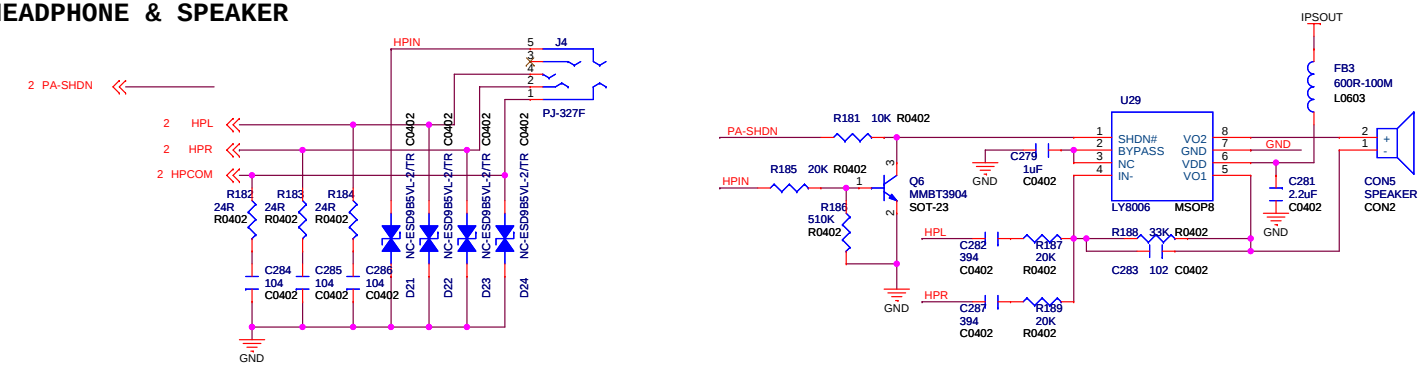
G-SENSOR



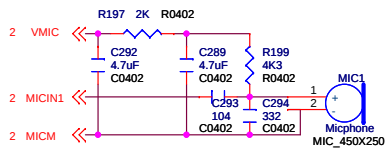
PCB上可以双layout



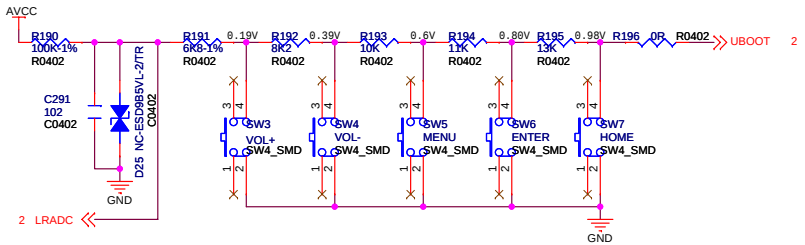
HEADPHONE & SPEAKER



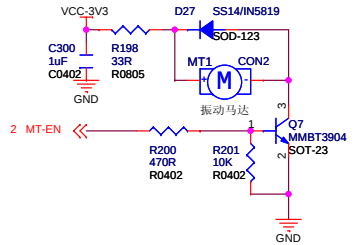
MIC



KEY



MOTOR



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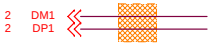
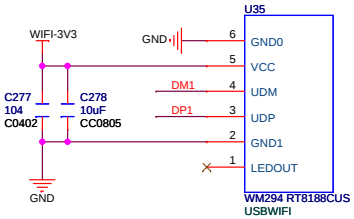
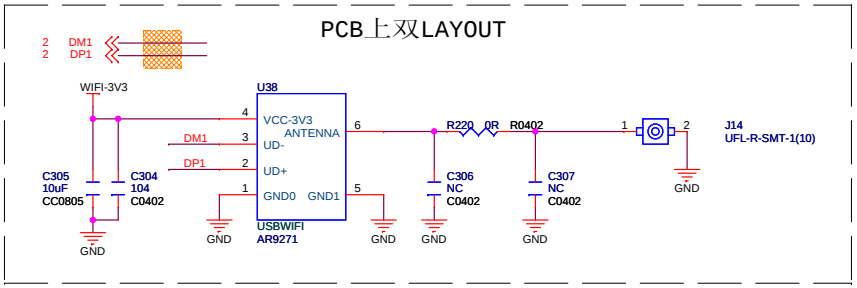
WIFI





PCB上双LAYOUT



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