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Design Questions

Question 1:
What is the minimum required DAC sample rate to achieve the frequency output requirements? Hint: look up the Nyquist Sampling Theorem.

According to the Nyquist sampling theorem, the sample rate must always be at least double the highest frequency. So in our case the top end of the frequency is 20 kHz which would give us a sampling rate of 40,000 samples per second.

Question 2:
At the DAC's maximum serial clock frequency, what is the maximum single-channel sample rate using the write-and-update command while still meeting the delay-after update requirement? Reference which parameters in the data sheet are needed to determine this specification. Hint: determine the data period first.

The max clock frequency of 50Hz results in a clock time of 20 nano seconds which goes through 32 cycles and as a result ends up at 640 nanoseconds. Taking into account the 1.9 microseconds required by the data sheet, the total time will now be 2.54 microsceonds which gives a max sample rate of 396 KHz.

Question 3:
What sample rate does your design use? How does this affect the appearance of the DAC output at higher frequencies?

Our design uses a sample rate of 48.8 KHz, which will cause higher frequencies to appear more easily.

Question 4:
What are the GPIO signals used to connect to the pins of the DAC interface? Use the expansion board schematic and the GPIO documentation page on Blackboard.

The correct pins appear to be

GPIO_[9] which is DAC_in

GPIO_[8] which is DAC clock signal

GPIO_[11] which is DAC LDAC

GPIO_[10] which is DAC sync singal

Question 5:
For your mono-channel output, which DAC command does your design use?

We use the DAC command 0011 which is write to and update DAC channel n

Question 6:
How do you control the NCO such that each sample is sent to the DAC correctly?

We have a counter which enables every 1024th clock cycle which means the data is sent the same rate at 48.8 KHz which is the same rate it is processed.

Question 7:
Find the equation in the NCO datasheet that shows how to calculate sine frequency versus phase increment. Since your sample rate is the effective clock rate of the NCO, what range of phase increments do you need to meet the output frequency specification?
To meet the 20 Hz requirement the lower frequency must be 819.67 Hz and the upper cap at 20 KHz must output at a frequency of 819.67 KHz
Response Requirments

Requirement 1:
Discuss how your design controls the LPM_SHIFTREG IP block

As previously stated we had a counter that would go every 1024th cycle through the DAC. Serving a dual purpose, the counter would also shift every bit of the 32 bit to the right with a 0. Each bit requires its own shift meaning there are 32 bit shifts.

Requirement 2:
Describe the functionality of each module used in the design. Your signal names should make sense relative to their function and correspond to the signal names used in the block diagram.

values - Detects movement in the motor and changes the frequency and amplitude

sync_clock - syncs the input to the clock

slow_down - counts from 0 to 1024 for use in the DAC reading

multi - allows the NCO generated sine wave to grow or decrease in size because of the amplitude

shiftreg - Takes the result of the sine wave and sends it to the DAC in 32 bits which is done by a shift register.

NCO_Lab3 - generates a sine wave based on the input frequency

Requirement 3:
Summarize how each group member contributed to the completion of this lab.

Jon - Began programming the lab

Andrew - Finished programming of the lab and report