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Design Questions

Question 1:
How many states did you use for each machine? How did you choose what these states were? Consider using sub-states to achieve the multi-cycle delay before transitioning out of a state (e.g. left_signal_three_lights_0, left_signal_three_lights_1, left_signal_three_lights_2).

The brake machine has 3 states in total. idle, break1, and break2
The turn signal machine has 22 states in total. IDLE, ERROR_STATE, left with 10 sub-states, and right with 10 sub-states.
The states names were given in the assignment and the sub-state names were reasonable names.

Question 2:
How many bits did you use in the counter to generate the 3Hz clock?

In order to get the clock from 50 MHz we used division by the powers of two to get 23 bits. From $2^{24} = 16777216$, multiplying by 3 we get 50331648 which is close to 50 MHz

Question 3:
Which I/O signals that you need on the DE1-SoC development board are active-low?

The buttons and hex displays are the only active low components we used in this lab.

Question 4:
How did you verify that you correctly implemented the Verilog state machine syntax in the Quartus software?

We were able to verify the state machine diagram by bringing up the state machine diagram feature in Quartus.