

Figure 3-11 Connections between the GPIO header and Cyclone V FPGA

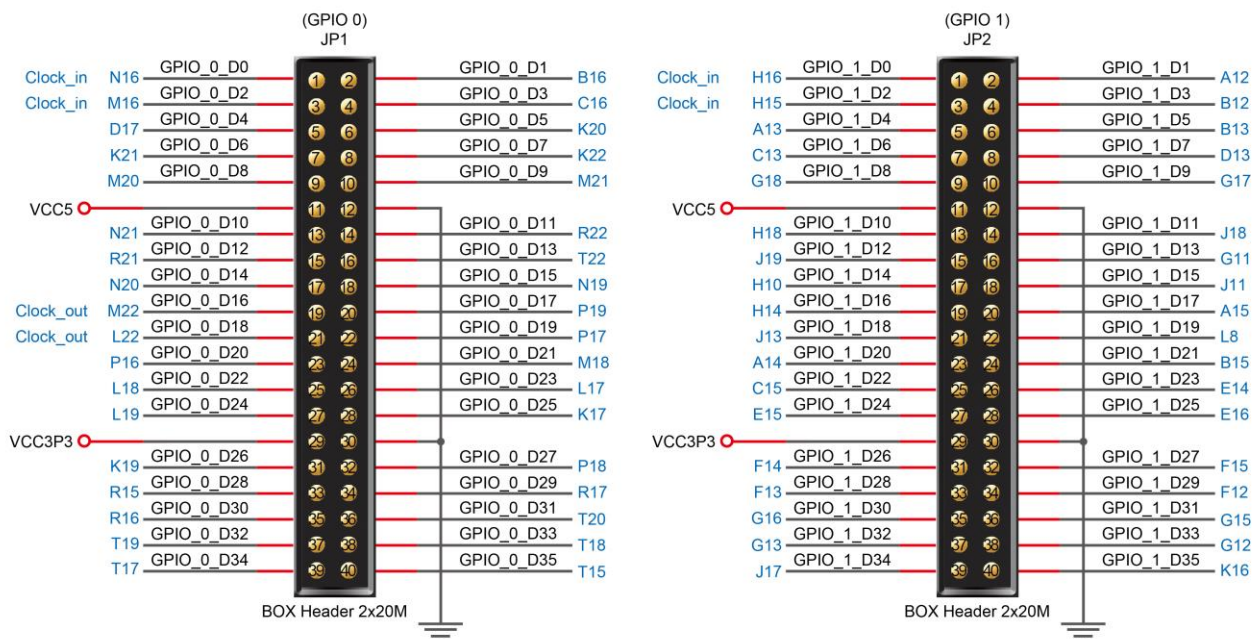


Figure 3-12 I/O distribution of the expansion headers

Table 3-7 Pin Assignment of Expansion Headers

Signal Name	FPGA Pin No.	Description
GPIO_0_D0	PIN_N16	GPIO Connection 0[0]
GPIO_0_D1	PIN_B16	GPIO Connection 0[1]
GPIO_0_D2	PIN_M16	GPIO Connection 0[2]
GPIO_0_D3	PIN_C16	GPIO Connection 0[3]
GPIO_0_D4	PIN_D17	GPIO Connection 0[4]
GPIO_0_D5	PIN_K20	GPIO Connection 0[5]
GPIO_0_D6	PIN_K21	GPIO Connection 0[6]