Durham University

EXAMINATION PAPER

Examination Session:	Year:	Exam Code:
May	2015	COMP1071WE01

Title: Computer Systems

Time Allowed:	2 hours	
Additional Material provided:		
Materials Permitted:		
Calculators Permitted:	No	Models Permitted:
Visiting Students may use dictionaries: Yes		

Instructions to Candidates:	Answer FOUR questions. (TWO from Section A and ONE from Section B and ONE from Section C) ANSWER EACH SECTION IN A SEPARATE ANSWER BOOK

Revision:	

Section A Machine Architecture and Digital Electronics (Dr. M. Bordewich)

Question 1

Consider the Karnaugh map given below for a Boolean function F on four inputs A, B, C and D.

CD \ AB	00	01	11	10
00	1	0	0	1
01	1	0	1	1
11	0	1	1	1
10	1	0	0	1

(a) Express the Boolean function F represented by the Karnaugh map above in **unsimplified** "Sum of Products" form. **[2 Marks]**

(b) List the rules for drawing loops on a Karnaugh map, then copy out the Karnaugh map above, and draw a correct set of loops on it. **[9 Marks]**

(c) Give a simplified formula for this Boolean function, based on the loops you have drawn on the Karnaugh map. **[3 Marks]**

(d) Draw a circuit diagram that gives an appropriate circuit for the function F using 2-input AND and OR gates, and NOT gates. **[2 Marks]**

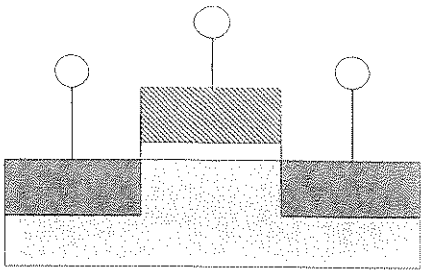
(e) If we assume that individual logic gates are combinational circuits, give **three** rules a larger circuit must satisfy in order to be a **combinational circuit**. For each rule, give an example of a circuit that fails to be a combinational circuit only by failing to satisfy that rule. **[6 Marks]**

(f) Discuss both to what extent a multiplexor circuit created from tristate gates may be considered a combinational circuit and may not be considered a combinational circuit. **[3 Marks]**

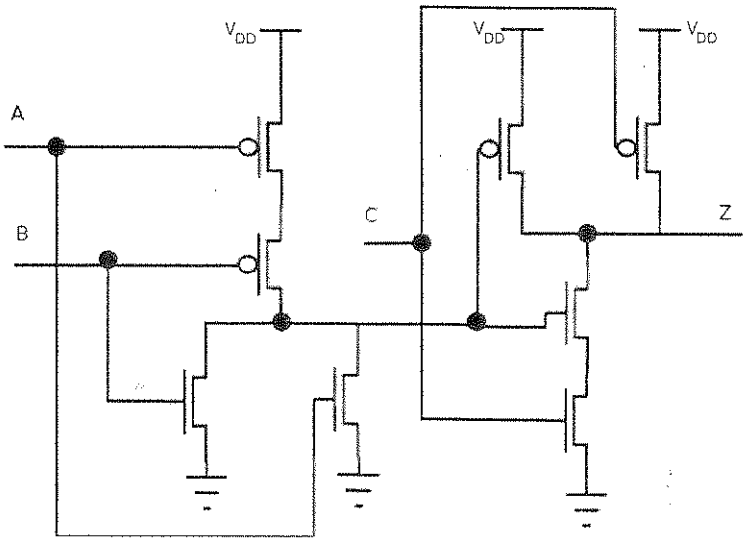
continued

Question 2

(a) Describe in detail how an nMOS transistor works, in both its on state and off state. Include in your description an annotated copy of the diagram below. **[10 Marks]**



(b) Give a truth table showing the output Z of the transistor circuit below for each possible value of the inputs A, B and C. **[6 Marks]**



(c) Express Z (the output of the circuit above) as an **unsimplified** "Sum of Products" Boolean formula in A, B and C, based upon your truth table from part (b). **[3 Marks]**

(d) Simplify your expression for Z as far as possible, showing your working. **[3 Marks]**

(e) Draw a combinational circuit for Z using AND, OR and NOT gates, based on your simplified formula from part (d). **[3 Marks]**

continued

Question 3

(a) In a single-precision floating point representation the three components are represented by 1, 8 and 23 bits, and an offset of 127 is used. What are the three components of the floating point representation of a number? Explain how to interpret a binary floating point representation, and convert the single-precision floating point

$$0100\,0101\,0111\,1100\,1000\,0000\,0000\,0000$$

to a decimal. **[8 Marks]**

(b) Draw a circuit diagram of a full adder for adding two bits with possible carry-in. **[2 Marks]**

(c) Draw a circuit diagram of a 4-bit ripple adder, made from full adder components. **[1 Marks]**

(d) What is twos-complement representation? Express the decimal numbers 37 and -54 in 8-bit twos-complement binary representation. **[4 Marks]**

(e) How can twos-complement representation be used in the design of a space-efficient simple arithmetic logic unit (ALU)? Demonstrate your answer by sketching a simple ALU that can perform addition, subtraction, bit-wise AND and bit-wise OR using any of the following components: adders, bit-wise NOT gates, bit-wise AND gates, bit-wise OR gates, and 2-1 multiplexors. Identify the settings of the control inputs that give each function. **[10 Marks]**

continued

Question 4

(a) Describe each of the essential elements of the Little Man Computer (LMC) model of a CPU. **[5 Marks]**

(b) The LMC uses direct, absolute addressing. Describe the difference between **direct, indirect, immediate** and **indexed** addressing. **[4 Marks]**

(c) The standard instruction set of the LMC is:

Mnemonic	Description	Mnemonic	Description
LDA	Load	IN	Input
STO	Store	OUT	Output
ADD	Add	BR	Branch
SUB	Subtract	BRZ	Branch on zero
HLT	Halt or Stop	BRP	Branch on positive

Where each instruction (except IN, OUT and HLT) takes a 2 digit address, e.g. ADD 60 looks up the value in mailbox 60 and adds it to the current total in the calculator. This instruction set is now augmented with an additional index register X, and with the additional instructions:

Mnemonic	Description
LDA@	Load with indexed addressing
STO@	Store with indexed addressing
ADD@	Add with indexed addressing
SUB@	Subtract with indexed addressing
LDX	Load a value into register X
DEC	Decrement register X
INC	Increment register X
BRPX	Branch if X positive
BRZX	Branch if X is zero

Illustrate how indexed addressing can be used by giving assembly code for the augmented LMC so that when run the LMC takes user inputs $n, x_1, x_2, \ldots, x_n$, and stores values $x_1, \ldots, x_n$ in some set of sequential mailboxes (order is not important). Note that the first input n is the number of subsequent inputs to store. **[6 Marks]**

this question is continued on the next page

(d) Describe how the program from (c) could be implemented in the standard LMC, i.e. using only direct absolute addressing, give a name for this type of code, and discuss the disadvantages of the resulting program compared to the program from (c). **[5 Marks]**

(e) Describe, including a small example, how indirect addressing can be used to access a larger memory than can be directly addressed, and discuss how much memory the LMC model could access using indirect addressing. **[5 Marks]**

End of Section A

Section B Operating Systems (Dr M. Gadouleau)

Question 5

(a) Describe 'prepaging', including its purpose and its potential drawback. **[3 Marks]**

(b) Using the page reference string below, show the total page faults for each of the replacement algorithms below that would occur with a three-frame reference memory allocation. Assume that the frames are originally empty.

Page reference string: 4,2,6,1,3,5,4,1,2,1,5,4,2,1,6

i. First in First Out (FIFO)

ii. Optimal (OPT)

iii. Least Recently Used (LRU)

[9 Marks]

(c) Assume a set of processes P1, P2, P3, and P4 arrive at different times in the ready queue. The table below shows the burst time, the priority (smallest priority number implies highest priority) and arrival time for each of the processes.

Process	Burst time	Priority	Arrival Time
P1	6	1	0
P2	2	3	2
P3	8	0	4
P4	4	2	6

Draw a Gantt chart illustrating the timing of the execution of the processes for each of the following scheduling algorithms:

i. First-Come, First-Served (FCFS)

ii. Pre-emptive Priority (PP)

iii. Shortest Job First (SJF)

iv. Shortest Remaining Time First (SRTF)

[8 Marks]

(d) When considering CPU scheduling, what do we mean by starvation? Which CPU scheduling algorithms from part (c) may leave processes vulnerable to starvation? Justify your answer. **[5 Marks]**

continued

Question 6

(a) A disk drive has 100 cylinders indexed from 0 to 99. The current cylinder request being serviced is at cylinder 84. The previous cylinder request serviced was 60.

The disk queue has the following cylinder requests pending:

$$86, 17, 3, 50, 51, 70, 75, 43.$$

For each of the four algorithms, draw a disk scheduling diagram to show disk head movement.

i. First Come First Served (FCFS)

ii. Shortest Seek Time First (SSTF)

iii. LOOK

iv. Circular LOOK (C-LOOK)

[8 Marks]

(b) Using the diagrams in part (a), calculate the seek time for each of the four disk scheduling algorithms. **[4 Marks]**

(c) When talking about disk scheduling, what do we mean by **starvation**? Which algorithm(s) in part (a) may cause starvation? For each algorithm that causes starvation, provide an example. **[6 Marks]**

(d) Disk access time is dependent on rotational latency and seek time. Briefly describe:

i. seek time

ii. rotational latency

[2 Marks]

(e) What is **thrashing** and why does it occur in demand-page memory management systems? **[2 Marks]**

(f) Explain how a page fault frequency scheme can be used to control thrashing. **[3 Marks]**

End of Section B

Section C Introduction to networks (Dr T. Breckon)

Question 7

(a) List the three bottom layers of the OSI reference model. Describe the role of each of them as follows.

i. Explain what kind of data structure it deals with.

ii. Mention at least one relevant algorithm/protocol.

iii. Say what its purpose is (without describing it in detail).

[10 Marks]

(b) Draw a schematic diagram of a router and explain where the translations between packets and frames occur. **[5 Marks]**

(c) Consider the simple Positive Acknowledgement with Retransmission protocol with a S(ender) and a R(eceiver). Assume that whenever S got a valid ack(nowledgement) for a successfully received frame, that ack arrived well before the timeout of S occurred. Fill in the gaps (indicated by square symbols) in the following scenario:

S sends frame 1; □; R doesn't get anything; □; S sends frame □; R gets valid frame □ and processes it; R sends ack □; □; timeout of S; S sends frame □; R gets valid frame □ and □; R sends ack □; S gets valid ack □; S sends frame □; R gets valid frame □ and □; R sends ack □; S gets valid ack □; S sends frame □;.....

[10 Marks]

Question 8

(a) Explain the simplest Positive Acknowledgement with Retransmission protocol.

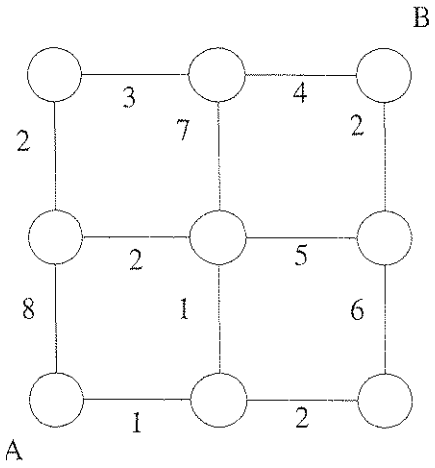
i. Describe both sender's and receiver's algorithms (you may want to use pseudocode).

ii. Argue that no frames are lost, duplicated or received in a wrong order.

[10 Marks]

(b) List the layers of both OSI and TCP/IP models and show the correspondence between layers. **[5 Marks]**

(c) Consider the following simple network with nine routers. Apply the Dijkstra shortest path algorithm to find a path from router A to router B. (Give worked out details such as the tentative and permanent labels at each iteration.)



[10 Marks]

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