Durham University

EXAMINATION PAPER

Examination Session:	Year:	Exam Code:
May/June	2016	COMP1071-WE01

Title:

COMPUTER SYSTEMS

Time Allowed:	2 hours	
Additional Material provided:	None	
Materials Permitted:	None	
Calculators Permitted:	Yes	Models Permitted: Casio FX-83 GTPLUS or Casio FX-85GTPLUS
Visiting Students may use dictionaries: Yes		

Instructions to Candidates:	Answer FOUR questions. (TWO from Section A, ONE from Section B and ONE from Section C)

Revision:

Section A Machine Architecture and Digital Electronics (Dr M. Bordewich)

Question 1

(a) Explain what is meant by the *architecture*, *micro-architecture* and the *state* of a CPU. **[6 Marks]**

(b) A MIPS CPU has 32 general purpose registers $0, $at, $v0-$v1, $a0-$a3, $t0-$t9, $s0-$s8, $k0-$k1, $gp, $sp and $ra. State the conventional usage of registers $v0-$v1, $a0-$a3, $t0-$t9, $s0-$s8, $sp and $ra, noting the difference between s and t registers as you do so. **[6 Marks]**

(c) Explain what the *stack* is and how it is used. **[5 Marks]**

(d) If the stack pointer starts with the (hexadecimal) value `7fffeffc`, give the new value for the stack pointer after lines 1-6 of the code below have been executed, and also after all the lines of code have been executed. **[4 Marks]**

```
1: myfunction:
2: or $a0, $0, $a1
3: addi $sp, $sp, -8
4: sw $t1, 4($sp)
5: sw $ra, 0($sp)
6: jal testfunction
7: lw $ra, 0($sp)
8: lw $t1, 4($sp)
9: addi $sp, $sp, 8
10: slt $v0, $v0, $t1
11: jr $ra
```

(e) Describe the type of addressing that is used in line 8, stating in detail what line 8 does. **[4 Marks]**

Question 2

You are asked to design a circuit taking a 4-bit input ABCD representing a hexadecimal number 0-F, and outputting a signal Y to drive the middle horizontal element of a 7-segment LED display. (Therefore the output should be 1 for inputs representing values 2,3,4,5,6,8,9,A,B,D,E or F, and 0 for inputs 0,1,7 or C.)

(a) Give a Boolean expression for Y in sum of products form. **[2 Marks]**

(b) Explain how a Karnaugh map is constructed and used. **[6 Marks]**

(c) Give a Karnaugh map for Y and use it to produce a simpler Boolean expression for Y. **[8 Marks]**

(d) You are now told that you are only going to get inputs representing decimal digits 0-9, although the input is still 4 bits. Explain how this might affect your analysis, and use an appropriate Karnaugh map to provide a Boolean formula for Y in this new situation. **[6 Marks]**

(e) You are finally told that you will be presented with a 64-bit binary number, which you can represent either in hexadecimal or in decimal using several 7-segment displays. Which number format would you choose? Justify your answer. **[3 Marks]**

continued

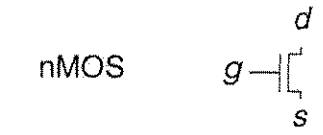
Question 3

(a) Explain in detail what is meant by the *logic level* of a gate or circuit in the context of digital electronics. **[5 Marks]**

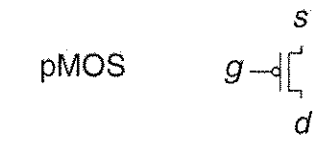
(b) Why are logic levels used? Are there any disadvantages to using logic levels? **[4 Marks]**

(c) Explain the difference in function between an nMOS and a pMOS transistor as depicted below. **[2 Marks]**

nMOS



pMOS



(d) Sketch a circuit made only from nMOS and pMOS transistors, a ground connection, a high voltage supply, two inputs A and B, output Y and lines connecting them, such that Y takes the value of A NOR B. **[6 Marks]**

(e) What does it mean to say that 'NOR gates alone form a functionally complete set'? **[2 Marks]**

(f) Sketch a circuit using only NOR gates that has two inputs A and B and output Y such that Y takes the value of A $\oplus$ B (A exclusive OR B). **[6 Marks]**

Question 4

(a) Explain in detail how DRAM works. Specify the role of the MDR, the MAR, the word lines and bit lines. Include a high level diagram of a DRAM array, as well as a diagram of a single bit of DRAM storage. **[15 Marks]**

(b) What are the advantages and disadvantages of DRAM over SRAM? **[2 Marks]**

(c) What is the *width* of a MAR, and what limitation does the width of the MAR determine? **[2 Marks]**

(d) Briefly describe two different techniques for mitigating memory access delays in a CPU. **[6 Marks]**

End of Section A

continued

Section B Operating Systems
(Dr M. Gadouleau and Dr M. Johnson)

Question 5

(a) Assume a set of processes P1, P2, P3, and P4 arrive at different times in the ready queue. Table 1 below shows the burst time, the priority (smallest priority number implies highest priority), and the arrival time for each of the processes.

Process	Burst Time	Priority	Arrival Time
P1	8	1	0
P2	2	2	2
P3	3	1	5
P4	1	4	6

Table 1: Processes table

Draw a Gantt chart illustrating the execution of the processes for each of the following scheduling algorithms:

i. Shortest Remaining Time First

ii. Shortest Job First

iii. Round Robin (time slice of 2 time units) **[6 Marks]**

(b) For each algorithm from part (a), explain whether it could pre-empt a running process. **[3 Marks]**

(c) Using the Gantt charts in part (a) calculate the average waiting time for each of the three algorithms. Show all your working. **[3 Marks]**

(d) Briefly describe the five possible process states. **[5 Marks]**

(e) As a process executes, it changes state. Using a diagram, show the event triggers that will cause a process to enter into each of the states described in part (d). **[8 Marks]**

Question 6

(a) Using the page reference string below, find the total number of page faults that would occur with a three frame reference memory allocation for each of the page replacement algorithms listed below. Assume that the frames are initially empty.

Page reference string: $5, 0, 1, 2, 0, 3, 0, 4, 2, 3, 0, 3$

i. First In First Out (FIFO)

ii. Least Recently Used (LRU)

Show your working. **[8 Marks]**

(b) Consider a disk with 200 cylinders (from 0 to 199). Suppose the head is on cylinder 63. It then receives requests for I/O to blocks in cylinders

$$108, 169, 47, 131, 12, 125, 75, 77.$$

Calculate the seek time for each of the following disk scheduling algorithms.

i. First Come First Served (FCFS)

ii. Shortest Seek Time Firm (SSTF)

iii. Cyclic Scan (C-SCAN)

iv. Cyclic Look (C-LOOK) **[6 Marks]**

(c) Briefly describe the three widely used methods for allocating disk space to a file. **[9 Marks]**

(d) Disk access time is dependent on rotational latency and seek time. Briefly describe:

i. seek time,

ii. rotational latency. **[2 Marks]**

End of Section B **continued**

Section C Networks
(Dr T. Breckon)

Question 7

(a) Describe the purpose of packet routing within a computer network and outline the key steps of a routing algorithm in common use within the internet. **[8 Marks]**

(b) Outline the operation of controlled access to the shared communication media within the operation of a computer network using:

i. a wired physical layer connection (e.g. Ethernet), **[4 Marks]**

ii. a wireless physical layer connection (e.g. Wifi). **[6 Marks]**

(c) Describe one method for binary data encoding used at the physical layer within the protocol stack and state any limitations of this method. **[4 Marks]**

(d) Describe three properties of a connection oriented network data transmission. **[3 Marks]**

Question 8

(a) Describe the key concepts of a protocol stack within the context of computer networking. **[6 Marks]**

(b) Describe the use of frames within the Data Link Layer of a protocol stack. **[6 Marks]**

(c) Outline each of the following data framing methods used within the Data Link Layer of a protocol stack.

i. byte count, **[3 Marks]**

ii. byte stuffing, **[3 Marks]**

iii. bit stuffing. **[3 Marks]**

(d) Outline the operation of flow control at the Data Link Layer of a protocol stack using positive acknowledgements and retransmission. **[4 Marks]**

END OF PAPER