Durham University

EXAMINATION PAPER

Examination Session:	Year:	Exam Code:
May/June	2014	1 0 1 0 7 1 / 0 1

Title: **Computer Systems**

Time Allowed:	2 hours
Examination Material Provided:	None
Additional Materials Permitted:	None
Instructions:	Answer FOUR questions. (TWO from Section A and ONE from Section B and ONE from Section C) ANSWER EACH SECTION IN A SEPARATE ANSWER BOOK Calculators are NOT allowed Erasmus/Visiting students can use a dictionary

Revision:	

ED01/2014

Section A Machine Architecture and Digital Electronics (Dr. M. Bordewich)

Question 1

You are designing an automatic ordering system for a cafe which has 11 dishes on its menu. When a client presses a button for one of these dishes, the signal is represented as a 4-bit binary number as follows: 0000: roast beef, 0001: asparagus tart (V), 0010: sausages, 0011: cheese sandwich (V), 0100: chicken pie, 0101: steak pie, 0110: grilled mushroom (V), 0111: quiche (V), 1000: salad (V), 1001: meatballs, 1010: tomato soup (V). You wish to create a (combinational) circuit which takes four inputs A,B,C and D which together encode this 4-bit number, and has one output F indicating whether the dish is suitable for a vegetarian (indicated with a (V)). The output should be 1 if the signal represents a vegetarian dish. In **all** other cases the output should be 0.

(a) Express the Boolean function F, given above, in unsimplified "sum of products" form. **[3 Marks]**

(b) Draw a Karnaugh map for this truth table and use it to produce a simpler formula for the same Boolean function. You should describe the construction of the Karnaugh map and process used to produce a simplified formula, and show your working on this example. **[10 Marks]**

(c) Draw a circuit diagram that gives an appropriate circuit for the function F using 2-input AND and OR gates and NOT gates. **[2 Marks]**

(d) It is now decided that the output value does not matter for inputs representing numbers that do not correspond to dishes (since there are 16 possible input states and only 11 dishes). For input values representing dishes the value must be 1 or 0 as before. Explain how this could affect your calculations so far and produce a simpler formula for a Boolean function that satisfies this new requirement. **[5 Marks]**

(e) Draw a circuit diagram that gives an appropriate circuit for the revised function from part (d) using 2-input AND and OR gates and NOT gates. **[2 Marks]**

this question is continued on the next page

(f) If the contamination and propagation delay of AND, OR and NOT gates is given by $t_{cd}(\text{AND}) = 30, t_{cd}(\text{OR}) = 25, t_{cd}(\text{NOT}) = 20$ and $t_{pd}(\text{AND}) = 60, t_{pd}(\text{OR}) = 50$ and $t_{pd}(\text{NOT}) = 30$, what is the contamination and propagation delay of your final circuit? Show your working. **[3 Marks]**

Question 2

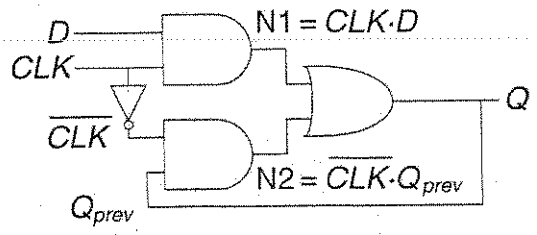
(a) Define precisely what is meant by the term **combinational circuit** and give an example of a circuit consisting entirely of AND, OR and NOT gates that:

i. is a combinational circuit

ii. is not a combinational circuit, and explain why. **[6 Marks]**

(b) Give a circuit diagram for a 2-1 multiplexor using tristate buffers, explain why this circuit is not a combinational circuit and describe why such a circuit might be used instead of a correct combinational circuit for a multiplexor. **[6 Marks]**

(c) With reference to the circuit below, explain what is meant by 'race conditions' in a circuit. **[4 Marks]**



(d) For a single physical logic gate in a circuit define the **propagation delay** (PD) and the **contamination delay** (CD) and give a reason why these may be different from each other. **[3 Marks]**

(e) Give values of the propagation and contamination delay of AND, OR and NOT gates such that in the circuit above:

i. if each logic gate operates within bounds given by its contamination and propagation delay, then $\overline{CLK}$ is guaranteed to rise to 1 before Q_{prev} drops to 0. **[2 Marks]**

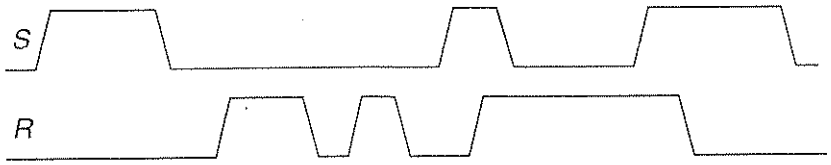
ii. if each logic gate operates within bounds given by its contamination and propagation delay, then Q_{prev} is guaranteed to drop to 0 before $\overline{CLK}$ rises to 1. **[2 Marks]**

iii. if each logic gate operates within bounds given by its contamination and propagation delay, then either outcome could occur. **[2 Marks]**

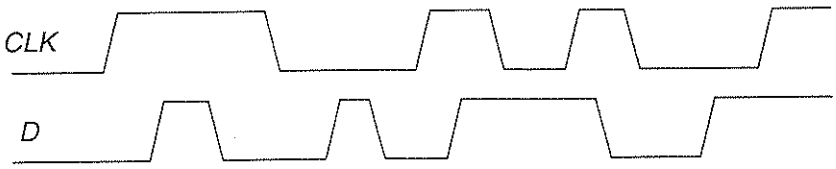
continued

Question 3

(a) Give a circuit diagram for an SR-latch using logic gates. **[3 Marks]**



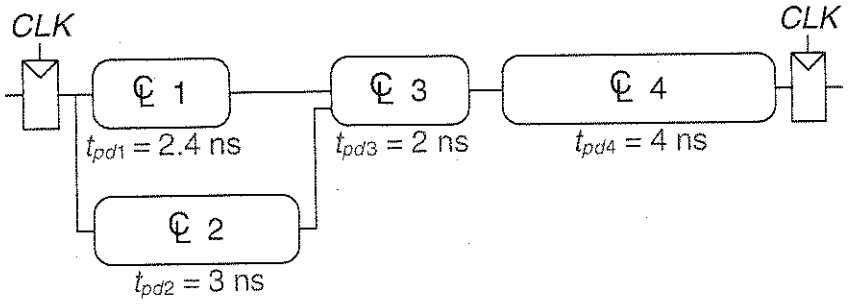
(b) For the first input wave form given above, draw the output Q of an SR-latch. **[2 Marks]**



(c) Describe concisely the behaviour of a D-latch and, for the second input wave form given above, draw the output Q of a D-latch. **[3 Marks]**

(d) Describe concisely the behaviour of a flip-flop and, for the second input wave form given above, draw the output Q of a flip-flop. **[3 Marks]**

(e) For a register (bank of flip-flops), define the times $t_{\text{setup}}, t_{\text{hold}}, t_{\text{ccq}}$ and t_{pcq}. **[4 Marks]**



(f) For the circuit segment shown above, derive a lower bound on the cycle time T_c, the time between clock ticks, if $t_{\text{setup}} = 0.2$ns, $t_{\text{hold}} = 0.4$ns, $t_{\text{ccq}} = 0.3$ns, $t_{\text{pcq}} = 0.5$ns and the propagation delays of the combinational logic elements are as given in the diagram. **[2 Marks]**

(g) Explain what pipelining of a sequential circuit is, and show how it can be used to allow a faster clock in the circuit above using (i) one, and (ii) three additional registers. In each case quantify the minimum permissible cycle time T_c. **[8 Marks]**

continued

Question 4

(a) A MIPS CPU has 32 general purpose registers $0, $at, $v0-$v1, $a0-$a3, $t0-$t9, $s0-$s8, $k0-$k1, $gp, $sp and $ra. Give the conventional usage of registers $v0-$v1, $a0-$a3, $t0-$t9, $s0-$s8, $sp and $ra, noting the difference between s and t registers as you do so. **[6 Marks]**

(b) Explain what the stack is and how it is used. **[5 Marks]**

I am writing an assembly function **compare** that will take two arguments in $a0 and $a1 and will return a value 1 if the $a1th triangular number is less than $a0 and return a 0 otherwise. I am making use of another function **triangular** which takes one argument $a0 and returns the $a0th triangular number. I know nothing about this function except that it follows convention. My code is below.

```
1: compare:
2: or $t0, $0, $a0
3: or $a0, $0, $a1
4: addi $sp, $sp, -4
5: sw $ra, 0($sp)
6: jal triangular
7: lw $ra, 0($sp)
8: addi $sp, $sp, 4
9: slt $v0, $v0, $t0
10: jr $ra
```

(c) What is the purpose of lines 4,5,7 and 8? **[2 Marks]**

(d) What mistake have I made with this function call? **[2 Marks]**

(e) Using a selection for the assembly instructions below, give MIPS assembly code for the function **triangular**. Recall that the n^{th} triangular number is equal to the sum $1 + 2 + \ldots n$.

add $rd, $rs, $rt	addi $rs, $rt, immediate
sub $rd, $rs, $rt	lw $rs, immediate($rt)
and $rd, $rs, $rt	sw $rs, immediate($rt)
or $rd, $rs, $rt	lui $rs, immediate
slt $rd, $rs, $rt	ori $rs, immediate
beq $rs, $rt, label	beq $rs, immediate, label
jal label	jr $rd

[10 Marks]

End of Section A

continued

Section B Operating Systems (Dr. M. Gadouleau)

Question 5

(a) Describe the five possible states a process may enter. **[5 Marks]**

(b) Assume a set of processes P1, P2, P3, and P4 arrive at different times in the ready queue. The table below shows the burst time, the priority (smallest priority number implies highest priority) and arrival time for each of the processes.

Process	Burst time	Priority	Arrival Time
P1	4	3	0
P2	5	2	2
P3	8	0	3
P4	3	1	5

Draw a Gantt chart illustrating the timing of the execution of the processes for each of the following scheduling algorithms:

i. Non-Pre-emptive Priority (NPP)

ii. Shortest Job First (SJF)

iii. First-Come, First-Served (FCFS)

iv. Shortest Remaining Time First (SRTF)

[8 Marks]

(c) Using the Gantt charts in part (b) calculate the average waiting time for each algorithm. (Show all your work.)

[4 Marks]

(d) Which CPU scheduling algorithms from part (b) may leave processes vulnerable to starvation? Justify your answer.

[4 Marks]

(e) When considering page replacement algorithms, what is Belady's anomaly? Give two examples of page replacement algorithms: one that suffers from the anomaly and one that does not. **[4 Marks]**

Question 6

(a) Using the page reference string below, show the total page faults for each of the replacement algorithms listed i) to iii) that would occur with a three-frame reference memory allocation. Which one produces the fewest faults and why? Assume that the frames are originally empty.

Page reference string: 4,5,2,1,3,3,1,5,4,2

i. First In First Out (FIFO)

ii. Optimal (OPT)

iii. Least Recently Used (LRU)

[10 Marks]

(b) A disk drive has 100 cylinders indexed from 0 to 99. The current cylinder request being serviced is at cylinder 30. The previous cylinder request serviced was 65.

The disk queue has the following cylinder requests pending: 17, 40, 55, 88, 71, 2, 3, 31.

For each of the three algorithms below, draw a disk scheduling diagram to show disk head movement.

i. SCAN

ii. Shortest Seek Time First (SSTF)

iii. LOOK

[6 Marks]

(c) Using the diagrams in part (b), calculate the seek time for each of the three disk scheduling algorithms. **[3 Marks]**

(d) Three major methods for allocating disk space to files are widely used. Describe each method briefly. **[6 Marks]**

End of Section B

continued

Section C Networks (Dr. S. Dantchev)

Question 7

(a) Explain the roles of the data-link layer and the network layer in the context of the OSI reference model. You should include: the data structure each layer deals with; design issues; some relevant algorithms/protocols; and how the two layers interact with one another.

[10 Marks]

(b) Explain what the core of the count-to-infinity problem is. Give an example of how this problem could occur. **[5 Marks]**

(c) Consider the simple PAR protocol with a S(ender) and a R(eceiver). Assume that whenever S got a valid ack(nowledgement) for a successfully received frame, that ack arrived well before the timeout of S occurred. Fill in the gaps (i.e. explain what has happened) in the following scenario.

S sends frame 0; _____; S gets valid ack 1; S sends frame __; R gets valid frame __ and processes it; R sends ack __; _____; timeout of S; S sends frame __; R gets valid frame __ and _____; R sends ack __; S gets valid ack __; S sends frame __; R gets a corrupted frame and _____; S gets valid ack __; S sends frame __;.....

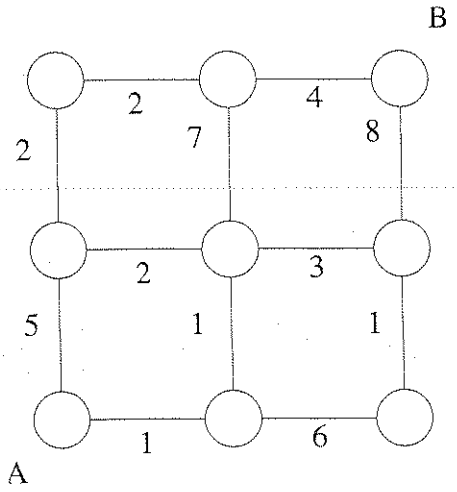
[10 Marks]

Question 8

(a) Explain the three concepts that are central to the OSI reference model: services, interfaces and protocols. How were these components designed in the TCP/IP model and how did this impact on the model itself? **[10 Marks]**

(b) Briefly explain the acknowledgements in both the Selective Repeat protocol and the Go Back N protocol. What is the main advantage of the former over the latter? **[5 Marks]**

(c) Consider the following simple network with nine routers. Apply the Dijkstra shortest path algorithm to find a path from router A to router B. (Give full details, such as the tentative and permanent labels at each iteration.)



[10 Marks]

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