Lecture 4 ISA Exercises

Q1:

```
1       addi $t0, $zero, $zero
2 loop: add $t2, $t0, $t5
3       lw $t3, 0($t2)
4       add $t2, $t0, $t6
5       lw $t4, 0($t2)
6       add $t3, $t3, $t4
7       add $t2, $t0, $t7
8       sw $t3, 0($t2)
9       addi $t0, $t0, 4
10      slti $t2, $t0, 200
11      bne $t2, $zero, loop
```

Assume the loop is only executed for one iteration.

1) Calculate the total number of data memory accesses made during execution of the code.

2) Calculate the CPI of this program. Assume every load instruction takes 3 cycles, every store instruction takes 2 cycles, and all other instructions take 1 cycle. Also assume that instructions are executed in sequence (one after the other).

3) Assuming a clock period of 500 ns, what is the execution time of this program?

Solution:

1) Number of Data Memory References = number of load (lw) and store (sw) instructions = 3 for one iteration of the loop

2) Total number of instructions executed = 11 instructions

1 addi instruction before the loop label → 1 × 1 cycle = 1 cycle
2 lw instructions → 2 × 3 cycles = 6 cycles
1 sw instruction → 1 × 2 cycles = 2 cycles
4 addi instructions → 4 × 1 cycle = 4 cycles
1 add instruction→1 × 1cycle=1 cycle
1 slti instruction→1 × 1cycle = 1 cycles
1 bne instruction → 1 × 1 cycle = 1 cycles
Latency of the program = 1+6+2+4+1+1+1 = 16 cycles
CPI = (16 cycles) / (11 instructions) = 1.45 cycles/instruction.

3) Execution Time = cycles × clock period = 16 cycles × 500 ns = 8 μs

Q2:
Answer the following points about properties and characteristics of various Instruction Set Architectures.

- Is latency dependent on the ISA (assume non-pipelined CPU)? Explain.

Solution: In terms of instruction execution, RISC instructions have a lower latency when compared to CISC instructions. Latencies can be detected at the instruction level, for example, branch delay slots expose the latencies of branches at the ISA level ("branch delay slots" will be discussed later in the class). Therefore, the answer is Yes.

- Which of the following metrics is dependent on the ISA: performance, die area, energy efficiency, code size? Why?

Solution: All are dependant on ISA

- Overall performance is dependent on ISA. MIPS (million instructions per second) metric favors RISC as instructions are simpler.
- ISA has an impact on die area as CISC architectures are more complex in their design and usually have larger die sizes when compared to RISC.
- RISC based processors incorporate less clocks per instructions. So energy per instruction is reduced.
- RISC based architecture will have larger code size when compared to CISC based architecture when implementing the same logic.

Q3:
Which of the following attributes of a machine are properties of its ISA:
(1) The machine does not have a subtract instruction.
(2) The ALU of the machine does not have a subtract unit.
(3) The machine does not have condition codes.
(4) A 5-bit immediate can be specified in an ADD instruction.
(5) It takes n cycles to execute an ADD instruction.
(6) There are 8 general purpose registers.
(7) A 2-to-1 mux feeds one of the inputs to ALU.
(8) The register file has one input and two output ports

Answer: (1)(3)(4)(6)

Q4:
In the MIPS ISA, which instruction(s) do not change the program counter?
A. bneq B. add C. j D. none

Answer: D