Lecture 10 Memory Hierarchy and Cache Exercises

Q1:
Assume:
- A processor has a 32KB direct mapped cache
- The cache access uses physical addresses only
- A physical address is 48 bits long
- Each block holds 64 bytes of data
- Tag overhead includes the valid bit and tag bits

How much is the tag overhead in percent?

Solution:
The total number of cache blocks = 32KB / 64B = 512
Number of bits in index = log2(512) = 9
Number of bits in byte offset = log2(64) = 6
Number of bits in tag = 48 – 9 – 6 = 33
Tag overhead = (33+1)/(8*64) * 100% = 6.6%

Q2:
Assuming the base CPIbase (no stall) of a pipeline is 1. A program has 25% of load/store instructions. The processor only has one level of cache, i.e., an L1 instruction cache and an L1 data cache. Cache miss rate and penalty are as following:

- L1 instruction cache: %miss = 2%, tmiss = 30 cycles
- L1 data cache: %miss = 30%, tmiss = 30 cycles

What is the CPI?

Solution:
CPI = CPIbase + (%cache_access%miss * CPImiss)
CPI = 1 + (100%*2%*30 cycles/insn) + (25%*30%*30 cycles/insn)
= 1 + 0.6 + 2.25
= 3.85