Name PID

UNIVERSITY OF CALIFORNIA, SAN DIEGO

Electrical and Computer Engineering Department

ECE 65 – Fall 2021

Components and Circuits lab

Final Exam

Closed books, five double-sided cheat sheets, and calculators are allowed

Electronic devices are not allowed.

Please put all answers in the provided sheets.

Be sure to write your name and PID on **all pages**.

Please do not begin until told.

Show your work.

Good luck.

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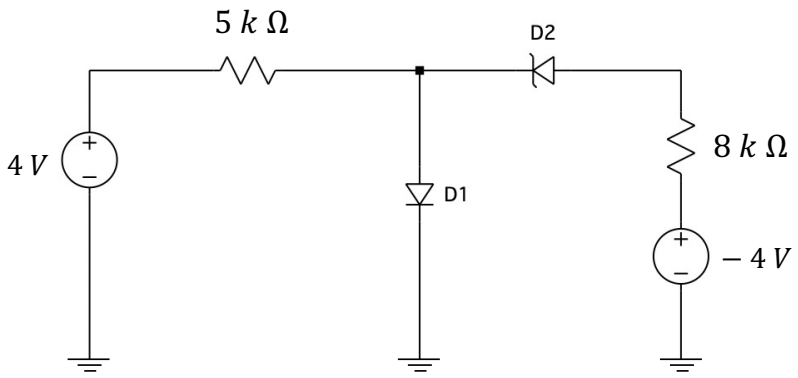
Problem 1. (5 points)

In the below circuit, can the Zener diode operate in the Zener region? The other PN junction diode can be assumed to be ON or OFF (include the analysis of both).

Assume $V_{D0} = 0.7\ V$. Choose a value between $3V$ and $5V$ and use it as V_Z. For example, you can select and use $V_Z = 5\ V$.



Show your work.

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Problem 2. (5 points)

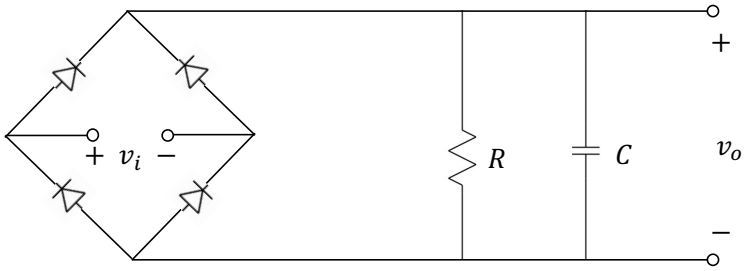
In the below circuit, sketch $v_o(t)$ for

i. $V_i(t) = 10\sin(2\pi \times f \times t)$, where $f = 1\ kHz$, $c = 1\ \mu F$ and $R = 100\ k\Omega$

ii. $V_i(t) = 10\sin(2\pi \times f \times t)$, where $f = 1\ kHz$, $c = 1\ \mu F$ and $R = 100\ \Omega$

A rough sketch for the waveform of $v_o(t)$ is enough. **Label the peak value of $\boldsymbol{v_o(t)}$**. If the output waveform is different for part (i) and (ii), your sketch should be an indicator of this difference.

Assume $V_{D0} = 0.7\ V$.



Show your work.

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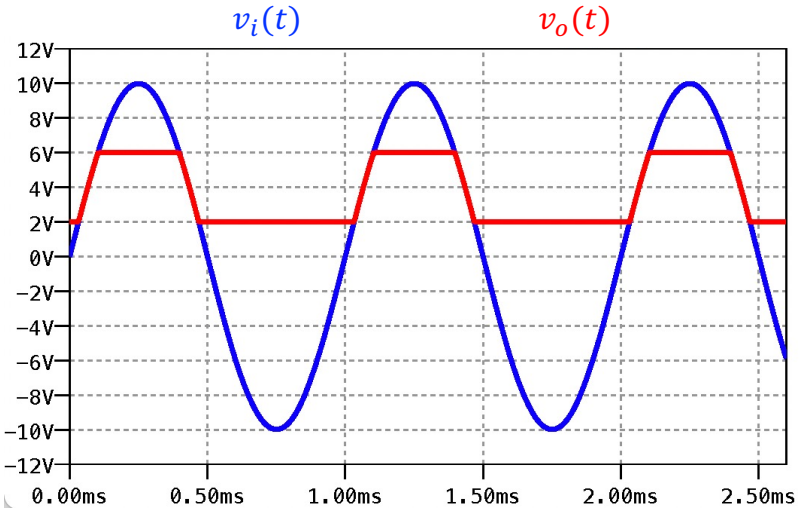
Problem 3. (10 points)

a) Design a diode circuit that would generate the output waveform, $v_o(t)$, shown in the below graph when the input signal $v_i(t) = 10\sin(\omega t)$ is applied to the circuit.

You can use regular PN junction diodes ($V_{D0} = 0.7\ V$), Zener diodes (any desired V_Z), and resistor(s) in your design. Make sure to label v_i and v_o on your circuit diagram.



b) Parametrically solve your designed circuit to find the transfer function and draw the transfer function graph. (find the relationship between v_o and v_i for different ranges of v_i and plot v_o vs v_i)

Show your work.

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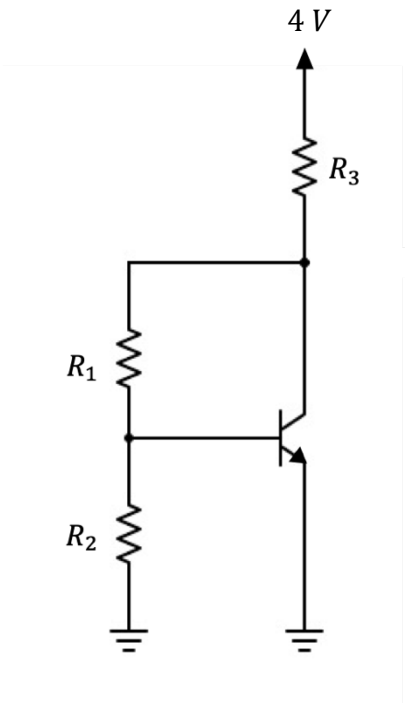
Problem 4 (10 points)

Design the following circuit to have $I_C = 2\ mA$ and $V_C = 1$ V.

Assume $\beta = 100$, $V_D = 0.7$ V, and $V_{sat} = 0.2$V.

The resistors must have finite non-zero values.



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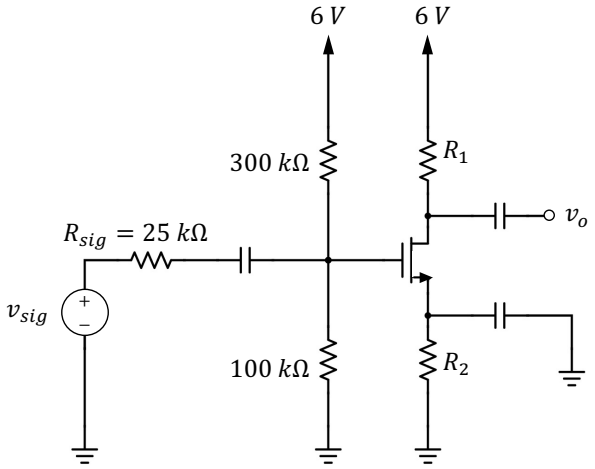
Problem 5 (15 points)

For this problem, neglect the early effect in the bias and signal circuits, assume the capacitors are short for the signal circuit and $V_t = 0.5\,V$.



a) Design the above amplifier circuit such that
   - The transistor is biased at $I_D = 0.5$ mA and $V_{OV} = 0.5\,V$.
   - The open-loop voltage gain is -10 V/V.

b) Draw the small signal equivalent circuit.

c) If v_{sig} is a sinusoidal signal with peak amplitude $\hat{v}_{sig}$, find the maximum allowable value of $\hat{v}_{sig}$ for which the transistor remains in saturation. What is the corresponding amplitude of the output signal voltage?

d) If we limit $\hat{v}_{sig}$ to 40 mV, what value can R_D be increased to while maintaining saturation region operation? (I_D and V_{OV} will not change.)

Show your work.

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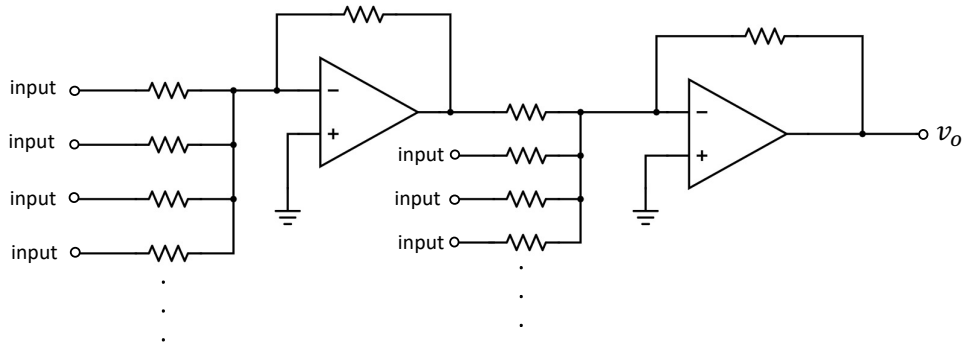
Problem 6 (5 points)

Using the general weighted summer op-amp circuit provided below, design an op-amp circuit that provides

$$v_o = 2v_1 + v_2 - 4v_3$$

where, v_1, v_2, and v_3 are the inputs.



Show your work.

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