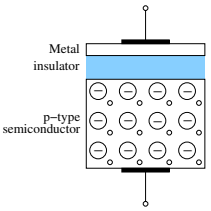
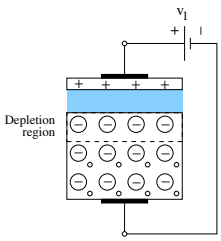
IV. Metal-Oxide Field-Effect Transistors (MOSFET)

4.1 Device Operation

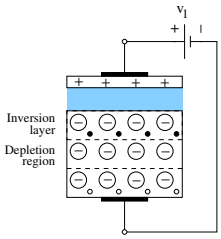
Consider a hypothetical semiconductor as is shown. It is constructed similar to a parallel-plate capacitor, *i.e.,* a layer of insulator is sandwiched between a metal plate and a p-type semiconductor. The p-type semiconductor includes mobile holes (majority carriers) and stationary, negatively-charged dopant ions.



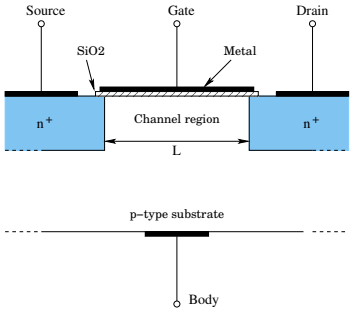
If voltage, v_1, is applied to this device with the positive terminal attached to the metal plate, electric charges, $Q = Cv_1$, appear on both terminals of this device. Because the metal plate is positively charged and the electric field is strongest in the vicinity of the insulator/p-material interface, mobile holes in this regions are repelled, forming a "depletion" region.



If v_1 is increased above a threshold value, V_t, electric field becomes strong enough to pull electrons (minority carriers) to the insulator/p-material interface. As the holes had been repelled from this region, an "inversion layer" is formed which contains electrons in the conduction band. This layer or "channel" is a "virtual" n-type material.



A simplified structure of a metal-oxide field-effect transistor (MOSFET or MOS for short) is shown. The device is fabricated on a p-type substrate (or Body). Two heavily doped n-type regions (Source and Drain) are created in the substrate. A thin (fraction of micron) layer of SiO_2, which is an excellent electrical insulator, is deposited on the p-type material in between the source and drain regions. Metal is deposited on the insulator to form the Gate of the device (thus, metal-oxide semiconductor). Metal contacts are also made to the source, drain, and body region.



The length of the channel region, L, is the the smallest feature of the transistor on the chip surface. The drain and source regions are typically much wider (picture is zoomed on the channel region). The width of the device W (dimension into the page) is also much larger than L.

The region between the source and the drain (p-type body, the oxide insulator layer and the gate metal) resembles the hypothetical parallel-plate capacitor above. As discussed, if a voltage greater than some threshold value is applied between the gate and the body, an

inversion layer will forms The inversion layer is a virtual n-type "channel" connecting the source to the drain. Both source and drain regions are heavily doped to provide a source of free electrons and assist in the formation of this inversion layer. This device is called a "n-channel" enhancement MOS or NMOS for short.

Let's first consider the case when no channel is formed. If we apply a voltage between the drain and the source NO current flows as n/p/n regions between the drain and the source look like two diodes back to back. This case is called the MOS cut-off mode.

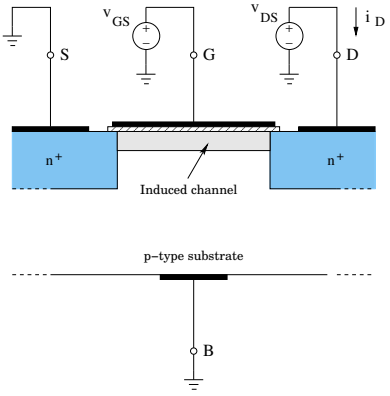
Note that we need to ensure that drain/body and source/body diodes are reverse biased so that no current can flow from the drain to the body or from the source to the body. For now, we assume that the source is connected to the body and $v_{DS} \geq 0$ for this purpose. We will examine implications of this assumption later.

We denote the threshold voltage for the formation of the channel as V_t. We apply a voltage v_{GS} to the NMOS ($v_{GS} = v_{GB}$). As long as $v_{GS} < V_t$, no channel is formed, the MOS is in cut-off and no current can flow from drain to source ($i_D = 0$).

When, $v_{GS} \geq V_T$, the virtual n-type channel is formed. As both drain and source region are also n-type, formation of this channel provide a n-type path for the current to flow from the drain to the source. The total charge in the channel is $|Q| = CV_{OV}$. $V_{OV} = v_{GS} - V_t$ is called the "overdrive" voltage. C is the capacitance of the gate/body structure:

$$|Q| = C\,V_{OV} \qquad \text{with} \qquad C = \frac{\epsilon_{ox}}{t_{ox}}\,WL = C_{ox}WL$$

where C_{ox} is the capacitance per unit area. ϵ_{ox} and t_{ox} are, respectively, the permittivity and the thickness of the insulator region.



Now, if we apply a voltage v_{DS} to the device an electric field of $E = v_{DS}/L$ appears along the channel. Electrons in the channel move from the source to drain with a drift velocity of

$$v_{drift} = \mu_n |E| = \mu_n \frac{v_{DS}}{L}$$

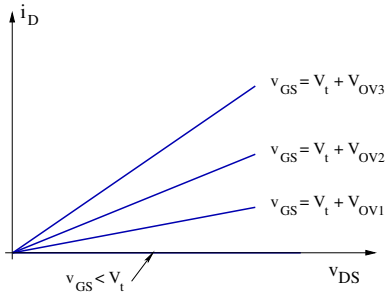
where μ_n is the mobility of electrons. The resulting current, i_D is:

$$i_D = \frac{dQ}{dt} = \frac{dQ}{dx} \times \frac{dx}{dt} = \frac{|Q|}{L} \times v_{drift} = \frac{|Q|}{L}\,\mu_n\,\frac{v_{DS}}{L}$$

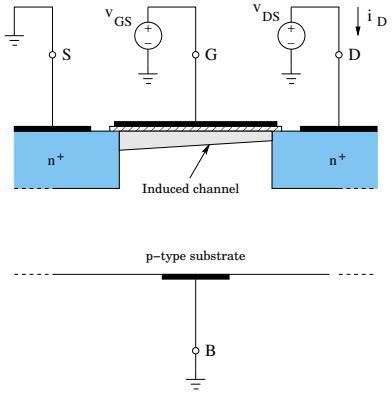
$$i_D = \mu_n C_{ox}\,\frac{W}{L} V_{OV} v_{DS}$$

$$i_D = g_{DS} v_{DS} \qquad \text{and} \qquad g_{DS} = \mu_n C_{ox}(W/L)V_{OV}$$

Effectively, the device acts like a resistor. Its conductance, g_{DS}, is controlled by V_{OV}. For this case plot of i_D versus v_{DS} is a straight line with a slope of g_{DS}. For $V_{OV} < 0$ no channel exists (zero conductance).



The above description is correct only for small values of v_{DS} as in that case, $v_{GD} = v_{GS} - v_{DS} \approx v_{GS}$ and the induced channel is fairly uniform (*i.e.,* has the same width near the drain as it has near the source). If we increase v_{DS} (keeping v_{GS} the same), $v_{GD} = v_{GS} - v_{DS}$ becomes smaller than v_{GS}. As such, the size of the channel near the drain becomes smaller than its size near the source, as is shown. This is called the "Triode" mode.



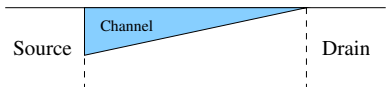
In this configuration, the charge per unit length near the source is $C_{ox}WV_{OV}$ (similar to that of a straight channel). The charge per unit length near the drain, however, is reduced to $C_{ox}W(V_{OV} - v_{DS})$. The average charge per unit length in the channel is:

$$\frac{|Q|}{L} = 0.5[C_{ox}WV_{OV} + C_{ox}W(V_{OV} - v_{DS})] = 0.5C_{ox}W(2V_{OV} - v_{DS})$$

$$i_D = \frac{|Q|}{L}\mu_n\frac{v_{DS}}{L} = \mu_n C_{ox}\frac{W}{L}(2V_{OV}v_{DS} - v_{DS}^2)$$

Note that for small v_{DS}, the above equation for i_D reduces to the one for a straight channel.

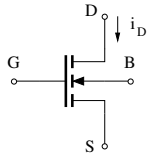
When $v_{DS} = V_{OV}$, the depth of the channel at the drain becomes effectively zero. It is said that the channel is "pinched" off. At this point ($v_{DS} = V_{OV}$):

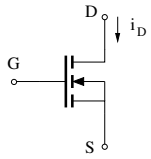


$$i_D = 0.5\mu_n C_{ox}\frac{W}{L}(2V_{OV}V_{OV} - V_{OV}^2)V_{OV} = 0.5\mu_n C_{ox}\frac{W}{L}V_{OV}^2$$

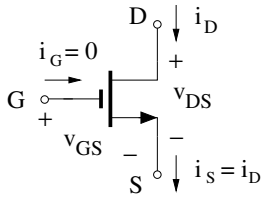
If v_{DS} is increased further, the channel pinched-off point remains very close to the drain and i_D remains approximately constant, given by the expression above. This case of $v_{DS} \geq V_t$ is called the "Saturation" mode.

The circuit symbol for an NMOS is shown on the right. The NMOS physical structure is symmetric, *i.e.,* drain and source positions can be exchanged without any change in device properties. Similarly, the source and the drain are indistinguishable on the circuit symbol and the arrow is placed on the body (pointing inward as it is p-type). For most applications, the body is connected to the source, leading to a 3-terminal element. In this case, the source and the drain are not interchangeable. A simplified circuit symbol for this configuration is usually used as is shown below (with the arrow on the source, pointing outward as it is n-type). Directions of currents and voltages are chosen such that they are all ≥ 0





An NMOS is a 3-terminal device with six parameters (3 voltages and 3 currents). Similar to a BJT, two parameters (i_S and v_{GD}) can be written in terms of the other four. Since $i_G = 0$ ($i_S = i_D$), an NMOS has three parameters and its iv characteristics equation is in the form of $i_D = f(v_{DS}, v_{GS})$.



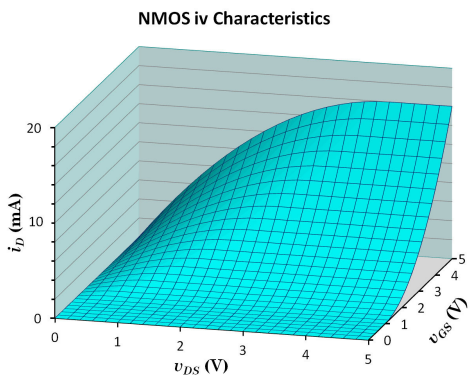
Note that $i_D = f(v_{DS}, v_{GS})$ is a surface in the 3D-space of (i_D, v_{GS}, v_{DS}) as is shown below (left). Projection of this surface on the i_D-v_{DS} plane (with v_{GS} pointing into the paper) is shown on the right. The three modes of operation of a MOS are identified on this figure:

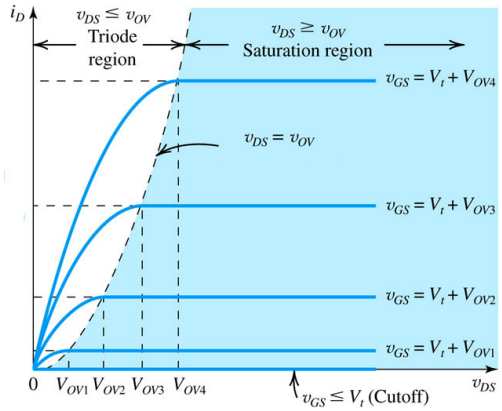
1) Cut-off mode in which no channel exists ($V_{OV} < 0$ for NMOS) and $i_D = 0$ for any v_{DS}.

2) Triode mode in which the channel is formed but not pinched off ($V_{OV} \geq 0$ and $v_{DS} \leq V_{OV}$).

3) Saturation mode in which the channel is formed and pinched off ($V_{OV} \geq 0$ and $v_{DS} \geq V_{OV}$).

Cut-off:	$V_{OV} < 0$,		$i_D = 0$
Triode:	$V_{OV} \geq 0$	& $v_{DS} \leq V_{OV}$	$i_D = 0.5\mu_n C_{ox} \dfrac{W}{L} [2V_{OV}v_{DS} - v_{DS}^2]$
Saturation:	$V_{OV} \geq 0$	& $v_{DS} \geq V_{OV}$	$i_D = 0.5\mu_n C_{ox} \dfrac{W}{L} V_{OV}^2(1 + \lambda v_{DS})$



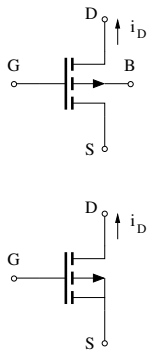


Channel-Length Modulation: In saturation, the channel is pinched off and the pinch-off point remains "approximately" at the drain. If the pinch-off point remains exactly at the drain, i_D would be constant. In reality, i_D increases slightly when v_{DS} is increased. This effect is called "channel-length modulation." If we extrapolate NMOS iv lines in the saturation mode, they will all intersect the horizontal axis at $-V_A$. (similar to the Early effect in BJTs). Channel-length modulation effect is included in the saturation mode i_D equation through the $(1 + \lambda v_{DS})$ term with channel-modulation parameter, $\lambda \equiv 1/V_A$. Note that V_A is much larger than the threshold voltage.

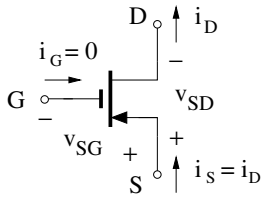
Body Effect: Recall that the drain-body and source-body pn junctions should be reverse biased. In deriving NMOS iv characteristics, we had assumed that the body and the source are connected. It is not straight forward to connect the body of every MOS to its source in an IC chip. The common practice is to attach the body of the chip to the smallest voltage available from the power supply (zero or negative). In this manner, drain-body and source-body junctions of all NMOS would be reverse biased. The impact of this approach is to lower the threshold voltage for the MOS devices slightly. This is called the body effect. Body effect can degrade device performance. For analysis here, we will assume that body effect is negligible.

p-Channel Enhancement-Type MOSFET (PMOS)

The physical structure of a PMOS is identical to an NMOS except that the semiconductor types are interchanged, *i.e.,* body & gate are made of n-type material, source & drain are made of p-type material, and a p-channel is formed. As the sign of charge carriers is reversed, all voltages and currents in a PMOS have opposite signs compared to those of an NMOS. In order to get positive values for voltages and currents in a PMOS, the convention is that the drain current is flowing out of the drain and subscripts for voltages are reversed (as is shown).



Since the threshold voltage in a PMOS is negative, the overdrive voltage is defined as $V_{OV} = v_{SG} - |V_{tp}|$. The channel-length modulation coefficient is also positive and defined as $\lambda_p = 1/V_{Ap}$. With these conventions, the iv equations for a PMOS are:



Cut-off:	$V_{OV} < 0,$			$i_D = 0$
Triode:	$V_{OV} \geq 0$	&	$v_{SD} \leq V_{OV}$	$i_D = 0.5\mu_n C_{ox} \dfrac{W}{L} (2V_{OV} v_{SD} - v_{SD}^2)$
Saturation:	$V_{OV} \geq 0$	&	$v_{SD} \geq V_{OV}$	$i_D = 0.5\mu_n C_{ox} \dfrac{W}{L} V_{OV}^2 (1 + \lambda v_{SD})$

4.2 Solving MOS circuits in DC

A MOS is very similar to a BJT in that the applied voltage v_{GS} controls i_D flowing through the drain-source circuit. As such, we can solve a MOS circuit utilizing a method similar to that used for BJTs: Write down GS-KVL and DS-KVL, assume the MOS is in a particular state, solve the circuit with the corresponding MOS equation and validate the assumption.

There are some differences, however:

1) A MOS is controlled with v_{GS} and $i_G = 0$. As such, typically no resistor is necessary in the gate circuit (as opposed to an R_B which was necessary for a BJT).

2) When MOS is in cut-off, $i_D = 0$. However, $i_D = 0$**, does not mean that MOS is in cut-off.** This is a very important property that is utilized in the design of CMOS logic gates (discussed in the next section).

To see this, assume that a MOS is in triode. Condition of $i_D = 0$ gives:

$$i_D = 0.5\mu_n C_{ox} \frac{W}{L} [2V_{OV}v_{DS} - v_{DS}^2] = 0 \quad \rightarrow \quad v_{DS} = 0$$

Thus, i_D **can be zero if a MOS is in the triode mode <u>and</u>** $v_{DS} = 0$**.**

We can also reach this conclusion by noting that when a MOS is in cut-off no channel exists and thus $i_D = 0$. However, if MOS is ON and a channel exists, i_D would be zero if no voltage is applied between the drain and the source terminals to drive i_D. Because $v_{DS} = 0 < V_{OV}$, this MOS has to be in triode.

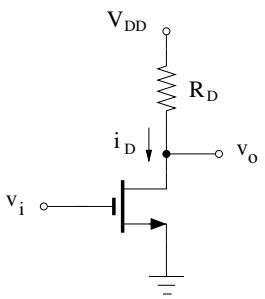
3) MOS iv equations are quadratic. Often, we find two roots in solving a MOS circuit with one being unphysical. Furthermore, it is usually easier to check for the saturation mode than the triode mode (as we see below).

Example: In the circuit below, $R_D = 1$ k and $V_{DD} = 12$ V. Compute v_o for $v_i = 0$, 6, and 12 V ($\mu_n C_{ox}(W/L) = 0.5$ mA/V^2, $V_t = 2$ V, and $\lambda = 0$).

Part A: $v_i = 0$ V.

GS-KVL: $v_{GS} = v_i = 0 < V_t \quad \rightarrow \quad$ NMOS in cut-off $\quad i_D = 0$

DS-KVL: $V_{DD} = R_D i_D + v_{DS} \quad \rightarrow \quad v_o = v_{DS} = V_{DD} = 12$ V



Part B: $v_i = 6$ V.

GS-KVL: $v_{GS} = v_i = 6 \quad \rightarrow \quad V_{OV} = v_{GS} - V_t = 6 - 2 = 4$ V

Since $V_t > 0$, MOS is ON. Assume the NMOS is in saturation (with $\lambda = 0$):

$$i_D = 0.5\mu_n C_{ox} \frac{W}{L} V_{OV}^2 = 0.5 \times 0.5 \times 10^{-3} \times (4)^2 = 4.0 \text{ mA}$$

DS-KVL: $V_{DD} = R_D i_D + v_{DS}$

$$12 = 10^3 \times 4 \times 10^{-3} + v_{DS} \quad \rightarrow \quad v_o = v_{DS} = 8 \text{ V}$$

Since $v_{DS} = 8 > V_{OV} = 4$ V, out assumption of MOS in saturation is justified.

Part C: $v_i = 12$ V.

GS-KVL: $v_{GS} = v_i = 12 \quad \rightarrow \quad V_{OV} = v_{GS} - V_t = 12 - 2 = 10$ V

Since $V_t > 0$, the NMOS is ON. Assume the NMOS is in saturation (with $\lambda = 0$):

$$i_D = 0.5\mu_n C_{ox} \frac{W}{L} V_{OV}^2 = 0.5 \times 0.5 \times 10^{-3} \times (10)^2 = 25.0 \text{ mA}$$

DS-KVL: $V_{DD} = R_D i_D + v_{DS}$

$$2 = 10^3 \times 24 \times 10^{-3} + v_{DS} \quad \rightarrow \quad v_o = v_{DS} = -13 \text{ V}$$

Since $v_{DS} = -13 < V_{OV} = 10$ V, our assumption of saturation mode is NOT justified.

Assume the NMOS is in triode:

$$i_D = 0.5\mu_n C_{ox} \frac{W}{L} [2V_{OV} v_{SD} - v_{SD}^2] = 0.5 \times 0.5 \times 10^{-3} \times (20 v_{SD} - v_{SD}^2)$$

DS-KVL: $12 = 10^3 i_D + v_{DS}$

The above two equations in two unknown can be solved by substituting for i_D into DS-KVL:

$$12 = 10^3 \times 0.25 \times 10^{-3} \times (20 v_{SD} - v_{SD}^2) + v_{DS}$$

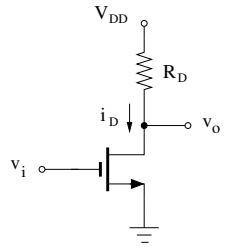
$$v_{DS}^2 - 24 v_{DS} + 48 = 0 \quad \rightarrow \quad v_{DS} = 21.8 \text{ V} \qquad \text{and} \qquad v_{DS} = 2.2 \text{ V}$$

The first root $v_{DS} = 21.8 > V_{OV} = 10$ V is not acceptable for a MOS in triode. The second root is the correct one as $v_{DS} = 2.2 < V_{OV} = 10$ V.

Thus $v_o = v_{DS} = 2.2$ V.

4.3 MOS transfer function

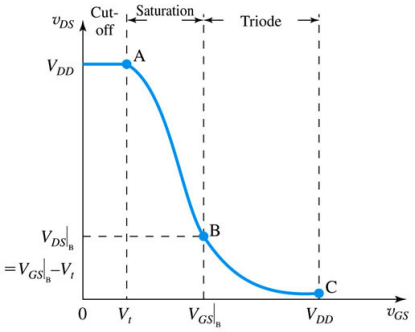
We will find the transfer function of a MOS by examining the circuit below.



GS-KVL: $v_{GS} = v_i$

DS-KVL: $V_{DD} = R_D i_D + v_{DS}$

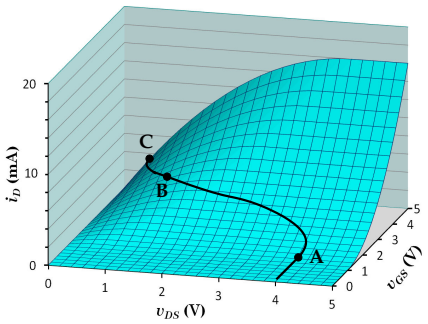
Starting at $v_i = 0$, we find $v_{GS} = 0 < V_T$ and the NMOS is in cut-off with $v_o = V_{DD}$. The NMOS remains in cut-off as long as $v_i = v_{GS} < V_t$.

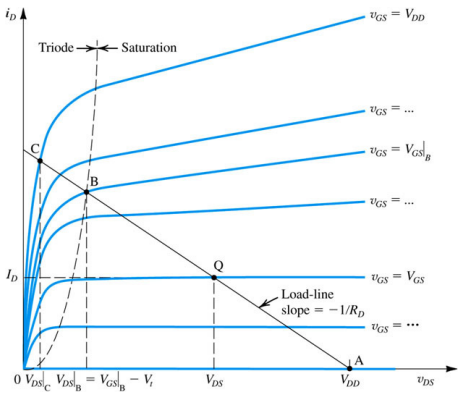


When $v_i = v_{GS} = V_t$ (point A in the figure), the NMOS turns ON (*i.e.,* a channel is formed). If we increase v_i slightly beyond this point, $V_{OV} = v_{GS} - V_t = v_i - V_t$ is positive but small. Thus, i_D would be small leading to $v_{DS} = V_{DD} - R_D i_D$ be close to V_{DD}. As such to the right of point A, $v_{DS} > V_{OV}$ and the NMOS is in saturation.

As we increase v_i (further to the right of point A), V_{OV} increases leading to a larger i_D and a smaller v_{DS}. At some point $v_{DS} = V_{OV}$ and the NMOS enters the triode mode (point B). For larger v_i (and V_{OV}), i_D increases (and $v_o = v_{DS}$ decreases) but not as fast as it was in the saturation mode as is shown.

We can observe this behavior by considering the 3-D iv characteristic surface of the MOS (figure below left). The DS-KVL, $V_{DD} = R_D i_D + v_{DS}$, represents a "plane" in this 3-D space which is parallel to the v_{GS} axis. The intersection of the DS-KVL plane and the NMOS iv surface is the operating path of the NMOS (shown below with points A, B, and C identified). The figure below (right) is the projection of this 3-D structure onto the $i_D v_{DS}$ plane with v_{GS} pointing into the paper. The projection of the KVL plane and the operating path of the NMOS overlaps and is the load line in this figure.





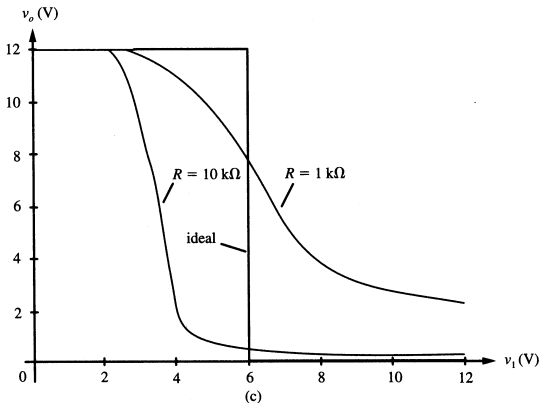
Note that if we look at the 3-D picture from the top with i_D axis pointing out of the paper, we should see the transfer function of the NMOS.

The NMOS transfer function provides an insight into MOS functional circuits. In the saturation mode, v_o has an approximately linear dependence on v_i (similar to a BJT in the active mode). A MOS in saturation can be utilized in amplifier circuits (discussed later).

MOS switches and RTL logic gates can be constructed by using the transition from cut-off to triode (similar to BJT in cut-off/saturation modes). There are, however, some differences with similar BJT circuits:

An NMOS remains in cut-off for $v_i < V_t$ and value of V_t can be set through the manufacturing process (as opposed to $v_I < V_{D0} = 0.7$ V for a BJT).

When a BJT is in saturation, $v_o = V_{sat}$ and is independent of the transistor and/or circuit parameters. When a MOS is in triode, v_o and i_D depend on MOS parameters as well as the value of R_D. As can be seen from the figure, a larger R_D leads to a lower v_o in the low state and a "rapid" transition from cut-off to triode.



While it may appear the a large R_D is require to get "good" transfer function for a logic gate, large R_D reduces gate switching times considerably. NMOS digital gates are not used today because of the CMOS technology offers a far superior circuit.

4.4 Complementary MOS (CMOS)

Complementary MOS technology employs pairs of NMOS and PMOS. CMOS devices are more difficult to fabricate than NMOS ones. However, most of MOS circuits are based on CMOS technology today because of the excellent properties of CMOS circuits (both analog and digital).

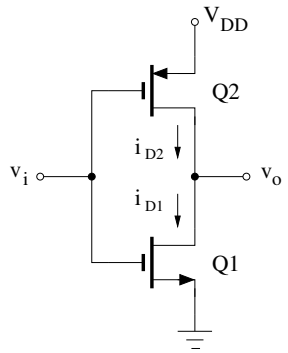
The basic idea is to replace R_D in the NMOS inverter circuit above with a PMOS. Recall that in the NMOS inverter circuit, the transfer function would resembles an ideal inverter for large R_D (low v_o in triode mode, rapid transistor from high to low state). The PMOS is configured such that when v_i is high (v_o is low), it would act as an effectively infinite resistor. Furthermore, When v_i is low (v_o is high), the PMOS acts as a small resistor thus allowing a high switching speed.

Two fundamental properties of CMOS logic gates are:

- A Low state of 0 and a High state of V_{DD}, thereby allowing for a maximum voltage swing. These states are independent of MOS device parameters. As a result, the gate has a wide noise margin.
- Zero static power consumption. *i.e.,* $i_D = 0$ when the gate is in one the two states. i_D is non-zero only during transition from state to another.

CMOS Inverter

We consider the response of the inverter to $v_i = 0$ (low) and $v_i = V_{DD}$ (high). Note that $v_o = v_{DS1} = V_{DD} - v_{DS2}$



GS1-KVL: $v_i = v_{GS1} \quad \rightarrow \quad v_{GS1} = v_i$

GS2-KVL: $v_{DD} = v_{SG2} + v_i \quad \rightarrow \quad v_{SG2} = V_{DD} - v_i$

DS-KVL: $V_{DD} = v_{SD2} + v_{DS1}$

KCL: $i_{D1} = i_{D2}$

Case 1: $v_i = 0$

Since $v_{GS1} = v_i = 0 < V_{tn}$, NMOS will be in cut-off. Therefore, $i_{D1} = 0$. Since $v_{SG2} = V_{DD} - v_i = V_{DD} > |V_{tp}|$, PMOS will be ON.

$$\begin{array}{lcll} v_{GS1} = v_1 = 0 < V_{tn} & \rightarrow & \text{Q1 is OFF} & \rightarrow \quad i_{D1} = 0 \\ v_{SG2} = V_{DD} - v_i = V_{DD} > |V_{tp}| & \rightarrow & \text{Q2 is ON} & \quad\; i_{D2} = 0 \end{array}$$

where we used KCL and $i_{D1} = 0$ to get $i_{D2} = 0$.

Since PMOS (Q2) is ON and $i_{D2} = 0$, PMOS should be in triode and $v_{SD2} = 0$ (see discussion of page 4-6)

$$\begin{array}{lcll} v_{GS1} = v_1 = 0 < V_{tn} & \rightarrow & \text{Q1 is OFF} & \rightarrow \quad i_{D1} = 0 \\ v_{GS2} = V_{DD} - v_i = V_{DD} > |V_{tp}| & \rightarrow & \text{Q2 is ON} & \quad\; i_{D2} = 0 \quad \rightarrow \quad v_{SD2} = 0 \end{array}$$

Then, $v_o = V_{DD} - v_{SD2} = V_{DD}$.

The above analysis is valid as long as $v_i < V_{tn}$ (Q1 OFF & Q2 ON) and v_o remains at $v_o = V_{DD}$.

Case 2: $v_i = V_{DD}$

Since $v_{GS1} = v_i = V_{DD} > V_{tn}$, NMOS will be ON. Since $v_{SG2} = V_{DD} - v_i = 0 < |V_{tp}|$, PMOS will be in cut-off and $i_{D2} = 0$.

$$\begin{aligned} v_{GS1} = v_1 = V_{DD} > V_{tn} \quad &\rightarrow \quad \text{Q1 is ON} \\ v_{GS2} = v_i - V_{DD} = 0 < |V_{tp}| \quad &\rightarrow \quad \text{Q2 is ON} \quad \rightarrow \quad i_{D2} = 0 \end{aligned}$$

By KCL, $i_{D2} = 0$ implies $i_{D1} = 0$. Now, NMOS (Q1) is ON and $i_{D1} = 0$. Thus, NMOS should be in triode with $v_{DS1} = 0$.

$$\begin{aligned} v_{GS1} = v_1 = V_{DD} > V_{tn} \quad &\rightarrow \quad \text{Q1 is ON} \qquad i_{D1} = 0 \quad \rightarrow \quad v_{DS1} = 0 \\ v_{GS2} = v_i - V_{DD} = 0 < |V_{tp}| \quad &\rightarrow \quad \text{Q2 is ON} \quad \rightarrow \quad i_{D2} = 0 \end{aligned}$$

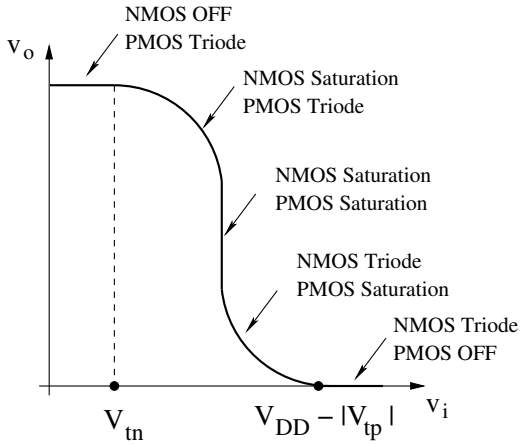
Then $v_o = v_{DS1} = 0$.

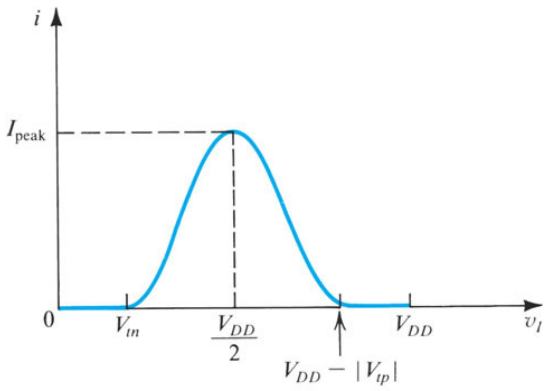
The above analysis is valid as long as $v_i > V_{DD} - |V_{tp}|$ (Q1 ON & Q2 OFF) v_o remains at $v_o = 0$.

In sum, when $v_i = 0$, $v_o = V_{DD}$ and when $v_i = V_{DD}$, $v_o = 0$. Therefore, this is an inverter (or a NOT gate). Note that 1) the low and high states were NOT set by transistor parameters, and 2) $i_{D1} = i_{D2} = 0$ and the gate has zero power consumption when in either state.

The transfer function of a CMOS inverter is shown below. From our analysis, when $v_i < V_{tn}$, NMOS is OFF and PMOS is in triode. When v_i becomes larger than V_{tn}, NMOS moves from cut-off to saturation (PMOS still in triode). Increasing v_i further leads to both MOS to be in saturation. The, NMOS transistor moves to triode. Finally, when $v_i > V_{DD} - |V_{tp}|$ NMOS is in triode and PMOS is in cut-off.

When $V_{tn} < v_i < V_{DD} - |V_{tp}|$ both MOS are ON (and one is in saturation), a current i_D would flow during the transition between high and low states (as shown below).

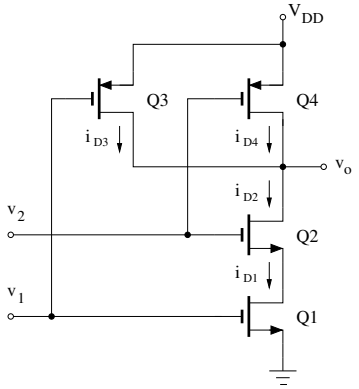




For a "matched" pair of MOS (*i.e.*, $V_{tn} = |V_{tp}|$, $\mu_n(W/L)_n = \mu_p(W/L)_p$) the transfer function would be symmetric about $v_i = 0.5V_{DD}$, $v_o = 0.5V_{DD}$ point. In this case, the maximum value of i_D that flows during the transition occurs when $v_i = 0.5V_{DD}$ and $v_o = 0.5V_{DD}$.

CMOS NAND Gate

As we saw in the CMOS inverter analysis, transistors in a CMOS logic circuit would be either in triode with $i_D = 0$ and $v_{DS} = 0$ or would be in cut-off. As such, in the solution below: 1) we will use GS-KVLs to find which transistors are OFF (and their $i_D = 0$), 2) we will use KCL to show that all i_D are zero, 3) we will look for any MOS that is ON with $i_D = 0$. These transistors should have $v_{DS} = 0$. 4) From the v_{DS} values, we will compute v_o.



GS1-KVL: $v_i = v_{GS1} \quad \rightarrow \quad v_{GS1} = v_i$

GS2-KVL: $v_2 = v_{GS2} + v_{DS1} \quad \rightarrow \quad v_{GS2} = v_2 - v_{DS1}$

GS3-KVL: $v_{DD} = v_{SG3} + v_1 \quad \rightarrow \quad v_{SG3} = V_{DD} - v_1$

GS3-KVL: $v_{DD} = v_{SG4} + v_2 \quad \rightarrow \quad v_{SG4} = V_{DD} - v_2$

DS-KVL: $V_{DD} = v_{SD4} + v_{DS2} + v_{DS1}$

DS-KVL: $v_{SD3} = v_{SD4}$

KCL: $i_{D1} = i_{D2} = i_{D3} + i_{D4}$

$v_o = v_{DS1} + v_{DS2} = V_{DD} - v_{SD3} = V_{DD} - v_{SD4}$

$\underline{v_1 = 0,\ v_2 = 0}$ We first find v_{GS} and state of all transistors:

$v_{GS1} = v_1 = 0 < V_{tn} \quad \rightarrow$ Q1 is OFF $\rightarrow \quad i_{D1} = 0$

$v_{GS2} = v_2 - v_{DS1} = -v_{DS1} \quad \rightarrow$ Q2 is ?

$v_{SG3} = V_{DD} - v_1 = V_{DD} > |V_{tp}| \quad \rightarrow$ Q3 is ON

$v_{SG4} = V_{DD} - v_2 = -V_{DD} > |V_{tp}| \quad \rightarrow$ Q4 is ON

While v_{DS1} can be mathematically negative and still satisfy DS-KVL above, NMOS operation requires $v_{DS} \geq 0$. Thus, Q2 should be OFF (however, this is not used in analysis below).

By KCL $i_{D2} = i_{D1} = 0$ and $i_{D3} + i_{D4} = i_{D1} = 0$. Since $i_D \geq 0$ for both PMOS and NMOS, the last equation can be only satisfied if $i_{D3} = i_{D4} = 0$. We add values of i_D to the table above and look for transistors that are ON and have $i_D = 0$. These transistors (Q3 and Q4) have to be in triode mode with $v_{SD3} = v_{SD4} = 0$.

$v_{GS1} = v_1 = 0 < V_{tn}$	$\rightarrow$	Q1 is OFF	$\rightarrow$	$i_{D1} = 0$	
$v_{GS2} = v_2 - v_{DS1} = -v_{DS1}$	$\rightarrow$	Q2 is ?		$i_{D2} = 0$	
$v_{SG3} = V_{DD} - v_1 = V_{DD} > \|V_{tp}\|$	$\rightarrow$	Q3 is ON		$i_{D3} = 0$	$\rightarrow \quad v_{SD3} = 0$
$v_{SG4} = V_{DD} - v_2 = -V_{DD} > \|V_{tp}\|$	$\rightarrow$	Q4 is ON		$i_{D4} = 0$	$\rightarrow \quad v_{SD4} = 0$

Finally, we find $v_o = V_{DD} - v_{SD3} = V_{DD}$. So, when both inputs are low, the output is HIGH.

We can check and see if our agreement for Q2 OFF is correct. Assume Q2 is ON. This requires $v_{GS2} > V_{tn}$. Since $i_{D2} = 0$ and Q2 is ON, $v_{DS2} = 0$ (Q2 in triode). But $v_o = v_{DS1} + v_{DS2} = V_{DD}$ leading to $v_{DS1} = V_{DD}$ and $v_{GS2} = v_2 - v_{DS1} = 0 - V_{DD} = -V_{DD} < V_{tn}$, a contradiction of of Q2 being ON. Therefore, Q2 should be OFF.

$\underline{v_1 = 0,\ v_2 = V_{DD}}$

$$
\begin{array}{lcll}
v_{GS1} = v_1 = 0 < V_{tn} & \rightarrow & \text{Q1 is OFF} & \rightarrow \quad i_{D1} = 0 \\
v_{GS2} = v_2 - v_{DS1} = V_{DD} - v_{DS1} & \rightarrow & \text{Q2 is ?} & \\
v_{SG3} = V_{DD} - v_1 = V_{DD} > |V_{tp}| & \rightarrow & \text{Q3 is ON} & \\
v_{SG4} = V_{DD} - v_2 = 0 < |V_{tp}| & \rightarrow & \text{Q4 is OFF} & \rightarrow \quad i_{D4} = 0
\end{array}
$$

In this case, the state of Q2 is unknown. By KCL $i_{D2} = i_{D1} = 0$. Also, $i_{D3} + i_{D4} = i_{D1} = 0$ leading to $i_{D3} = 0$. We add values of i_D to the table above and look for transistors that are ON and have $i_D = 0$. This transistor (Q3) have to be in triode mode with $v_{SD3} = 0$.

$$
\begin{array}{lcllll}
v_{GS1} = v_1 = 0 < V_{tn} & \rightarrow & \text{Q1 is OFF} & \rightarrow \quad i_{D1} = 0 & & \\
v_{GS2} = v_2 - v_{DS1} = V_{DD} - v_{DS1} & \rightarrow & \text{Q2 is ?} & \quad\ \ i_{D2} = 0 & & \\
v_{SG3} = V_{DD} - v_1 = V_{DD} > |V_{tp}| & \rightarrow & \text{Q3 is ON} & \quad\ \ i_{D3} = 0 & \rightarrow & v_{SD3} = 0 \\
v_{SG4} = V_{DD} - v_2 = 0 < |V_{tp}| & \rightarrow & \text{Q4 is OFF} & \rightarrow \quad i_{D4} = 0 & &
\end{array}
$$

Finally, we find $v_o = V_{DD} - v_{SD3} = V_{DD}$. So, when v_1 is LOW and v_2 is HIGH, the output is HIGH.

We can go back and find the state of Q2. We will find Q2 to be OFF (left as an exercise).

$\underline{v_1 = V_{DD},\ v_2 = 0}$

$$
\begin{array}{lcll}
v_{GS1} = v_1 = V_{DD} > V_{tn} & \rightarrow & \text{Q1 is ON} & \\
v_{GS2} = v_2 - v_{DS1} = -v_{DS1} < V_{tn} & \rightarrow & \text{Q2 is OFF} & \rightarrow \quad i_{D2} = 0 \\
v_{SG3} = V_{DD} - v_1 = 0 < |V_{tp}| & \rightarrow & \text{Q3 is OFF} & \rightarrow \quad i_{D3} = 0 \\
v_{SG4} = V_{DD} - v_2 = V_{DD} > |V_{tp}| & \rightarrow & \text{Q4 is ON} &
\end{array}
$$

We used $v_{DS1} \geq 0$ to find the state of Q2. By KCL $i_{D1} = i_{D2} = 0$. Also, $i_{D3} + i_{D4} = i_{D2} = 0$ leading to $i_{D4} = 0$. We add values of i_D to the table above and look for transistors that are ON and have $i_D = 0$. These transistors (Q1 and Q4) have to be in triode mode with $v_{DS1} = v_{SD4} = 0$.

$$
\begin{array}{lcllll}
v_{GS1} = v_1 = V_{DD} > V_{tn} & \rightarrow & \text{Q1 is ON} & \quad\ \ i_{D1} = 0 & \rightarrow & v_{DS1} = 0 \\
v_{GS2} = v_2 - v_{DS1} = -v_{DS1} < V_{tn} & \rightarrow & \text{Q2 is OFF} & \rightarrow \quad i_{D2} = 0 & & \\
v_{SG3} = V_{DD} - v_1 = 0 < |V_{tp}| & \rightarrow & \text{Q3 is OFF} & \rightarrow \quad i_{D3} = 0 & & \\
v_{SG4} = V_{DD} - v_2 = V_{DD} > |V_{tp}| & \rightarrow & \text{Q4 is ON} & \quad\ \ i_{D4} = 0 & \rightarrow & v_{SD4} = 0
\end{array}
$$

Finally, $v_o = V_{DD} - v_{SD4} = V_{DD}$. So, when v_1 is HIGH and v_2 is LOW, the output is HIGH.

$\underline{v_1 = V_{DD},\ v_2 = V_{DD}}$

$$
\begin{array}{lll}
v_{GS1} = v_1 = V_{DD} > V_{tn} & \rightarrow & \text{Q1 is ON} \\
v_{GS2} = v_2 - v_{DS1} = V_{DD} - v_{DS1} & \rightarrow & \text{Q2 is ?} \\
v_{SG3} = V_{DD} - v_1 = 0 < |V_{tp}| & \rightarrow & \text{Q3 is OFF} \quad \rightarrow \quad i_{D3} = 0 \\
v_{SG4} = V_{DD} - v_2 = 0 < |V_{tp}| & \rightarrow & \text{Q4 is OFF} \quad \rightarrow \quad i_{D4} = 0
\end{array}
$$

By KCL $i_{D2} = i_{D1} = i_{D3} + i_{D4} = 0$. We add values of i_D to the table above and look for transistors that are ON and have $i_D = 0$. As can be seen in equations below, Q1 is ON and $i_{D1} = 0$. Thus, $v_{DS1} = 0$. We use this value to find that Q2 should also be ON.

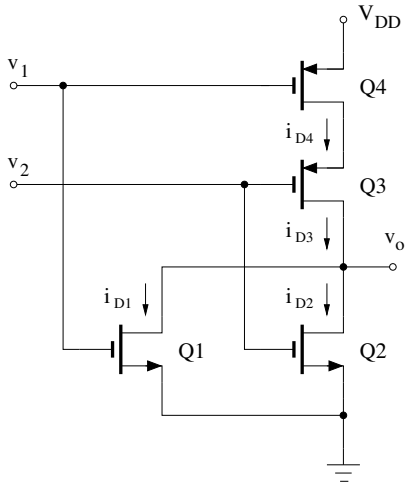
$$
\begin{array}{llllll}
v_{GS1} = v_1 = V_{DD} > V_{tn} & \rightarrow & \text{Q1 is ON} & i_{D1} = 0 & \rightarrow & v_{DS1} = 0 \\
v_{GS2} = v_2 - v_{DS1} = V_{DD} - v_{DS1} = V_{DD} > V_{tn} & \rightarrow & \text{Q2 is ON} & i_{D2} = 0 & \rightarrow & v_{DS2} = 0 \\
v_{SG3} = V_{DD} - v_1 = 0 < |V_{tp}| & \rightarrow & \text{Q3 is OFF} \quad \rightarrow \quad i_{D3} = 0 & & & \\
v_{SG4} = V_{DD} - v_2 = 0 < |V_{tp}| & \rightarrow & \text{Q4 is OFF} \quad \rightarrow \quad i_{D4} = 0 & & &
\end{array}
$$

Finally, $v_o = v_{DS1} + v_{DS1} = 0$. So, when v_1 is HIGH and v_2 is HIGH, the output is LOW.

From the "truth table," the output of this gate is LOW only if both input states are HIGH. Therefore, this is a NAND gate.

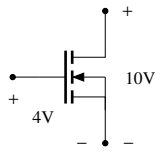
CMOS NOR Gate

Exercise: Show that this is a NOR gate.

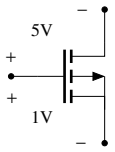


4.5 Exercise Problems

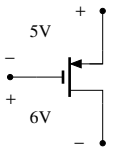
Problems 1 to 4. Find i_D ($\mu_n C_{ox}(W/L)_n = \mu_p C_{ox}(W/L)_p = 0.4$ mA/V^2, $\lambda = 0$, $V_{tn} = 3$ V and $V_{tp} = -3$ V).



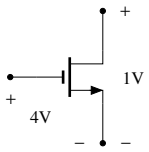
Problem 1



Problem 2



Problem 3



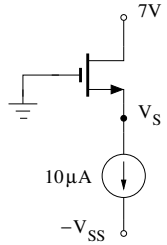
Problem 4

Problem 5. Find V_S ($\mu_n C_{ox}(W/L)_n = 0.5$ mA/V^2, $\lambda = 0$, and $V_{tn} = 0.8$ V).

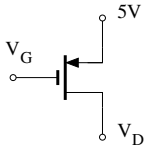
Problem 6. Consider this PMOS with $\mu_p C_{ox}(W/L)_p = 0.6$ mA/V^2, $\lambda = 0$, and $V_{tp} = -1$ V. A) For what values of V_G, PMOS will be ON?, B) Find the range of V_D for which PMOS is in triode (answer in terms of V_G). C) Find the range of V_D for which PMOS is in saturation (answer in terms of V_G). D) If PMOS is in saturation with $i_D = 75$ μA, find V_{OV}, V_G and the corresponding range of V_D.

Problem 7. Find i_D and v_{DS} ($\mu C_{ox}(W/L) = 0.4$ mA/V^2, $\lambda = 0$, and $V_t = 3$ V).

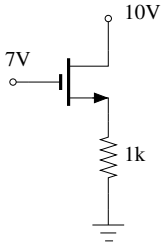
Problem 8. Find v_{SG}, i_D, and v_{SD} ($\mu_p C_{ox}(W/L)_p = 0.4$ mA/V^2, $\lambda = 0$, and $V_{tp} = -3$ V).



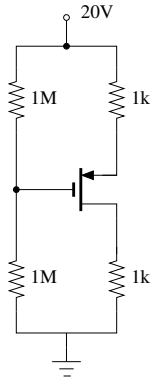
Problem 5



Problem 6



Problem 7



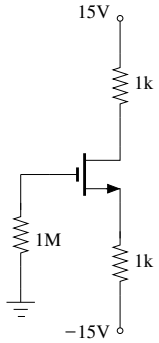
Problem 8

Problem 9. Find v_{GS}, i_D, and v_{DS} ($\mu_n C_{ox}(W/L)_n = 0.4$ mA/V^2, $\lambda = 0$, and $V_{tn} = 3$ V).

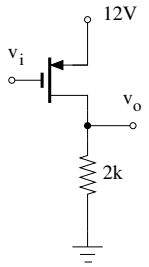
Problem 10. Find v_o for $v_i = 0$ V ($\mu_p C_{ox}(W/L)_p = 0.5$ mA/V^2, $\lambda = 0$, and $V_{tp} = -2$ V).

Problem 11. Find R such that PMOS is in saturation with $V_{OV} = 0.6$ V ($\mu_p C_{ox} = 1$ mA/V^2, $(W/L) = 10/0.18$, $\lambda = 0$, and $V_{tp} = -0.4$ V).

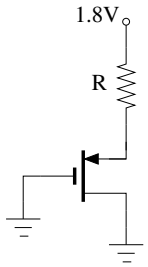
Problem 12. Design the circuit below (*i.e.,* find R_S and R_D) in order to get $i_D = 0.25$ mA and $V_D = 0$. ($\mu_n C_{ox} = 60$ μA/V^2, $W/L = 100/3$, $\lambda = 0$, and $V_t = 1$ V).



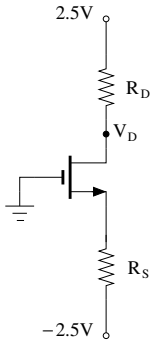
Problem 9



Problem 10



Problem 11



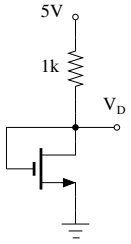
Problem 12

Problem 13. Find V_D ($\mu_n C_{ox}(W/L) = 0.5$ mA/V^2, $\lambda = 0$, and $V_t = 0.8$ V).

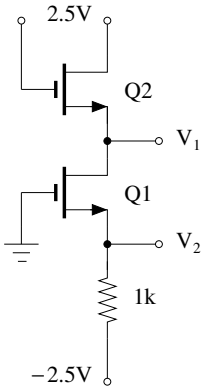
Problem 14. Find V_1 and V_2 ($\mu_n C_{ox}(W/L) = 5$ mA/V^2, $\lambda = 0$, and $V_t = 1$ V).

Problem 15. Find i_D and v_{DS} for A) ignoring channel-length modulation ($\lambda = 0$) and B) including channel-length modulation ($\lambda = 0.05$ V^{-1}). NMOS has $\mu_n C_{ox}(W/L) = 1$ mA/V^2 and $V_t = 0.4$ V.

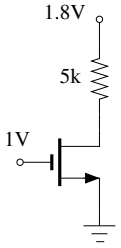
Problem 16. Show that this circuit is a NOR gate with a LOW state of 0.2 V and a HIGH state of 12 V ($\mu_n C_{ox}(W/L)_n = 0.5$ mA/V^2, $V_t = 1$ V).



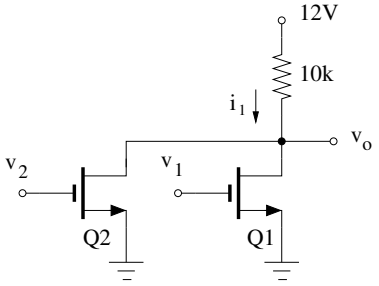
Problem 13



Problem 14



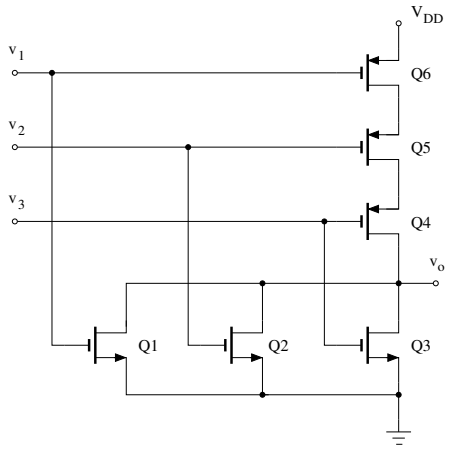
Problem 15



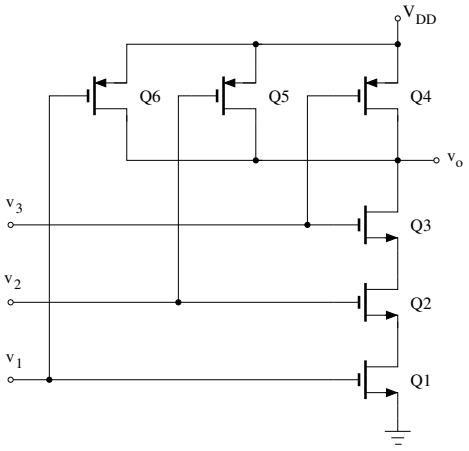
Problem 16

Problem 17. Show that this is a three-input NOR gate.

Problem 18. Show that this is a three-input NAND gate.



Problem 17

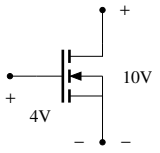


Problem 18

4.6 Solution to Selected Exercise Problems

Problem 1. Find i_D ($\mu_n C_{ox}(W/L)_n = \mu_p C_{ox}(W/L)_p = 0.4$ mA/V^2, $\lambda = 0$, $V_{tn} = 3$ V and $V_{tp} = -3$ V).

This is a NMOS transistor with $v_{GS} = 4$ V and $v_{DS} = 10$ V.



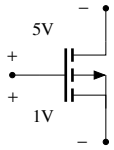
$V_{OV} = V_{GS} - V_{tn} = 1$ V $\qquad\qquad$ $V_{OV} > 0 \quad \rightarrow \quad$ MOS is ON

$v_{DS} = 10 > V_{OV} = 1$ V $\quad \rightarrow \quad$ MOS is in saturation

$i_D = 0.5\mu_n C_{ox}(W/L)_n V_{OV}^2 = 0.5 \times 0.4 \times 10^{-3}(1)^2 = 0.2$ mA

Problem 2. Find i_D ($\mu_n C_{ox}(W/L)_n = \mu_p C_{ox}(W/L)_p = 0.4$ mA/V^2, $\lambda = 0$, $V_{tn} = 3$ V and $V_{tp} = -3$ V).

This is a PMOS transistor with $v_{SG} = -1$ V and $v_{GD} = 5$ V.



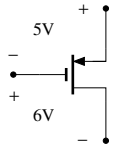
$V_{OV} = V_{SG} - |V_{tp}| = -4$ V

$V_{OV} < 0 \quad \rightarrow \quad$ MOS is OFF $\quad \rightarrow \quad i_D = 0$

Note $v_{SD} = v_{SG} + v_{GD} = -1 + 5 = +4$ V.

Problem 3. Find i_D ($\mu_n C_{ox}(W/L)_n = \mu_p C_{ox}(W/L)_p = 0.4$ mA/V^2, $\lambda = 0$, $V_{tn} = 3$ V and $V_{tp} = -3$ V).

This is a PMOS transistor with $v_{SG} = 5$ V and $v_{GD} = 6$ V.



$V_{OV} = V_{SG} - |V_{tp}| = 2$ V $\qquad\qquad$ $V_{OV} > 0 \quad \rightarrow \quad$ MOS is ON

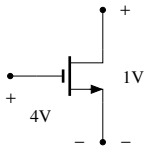
$v_{SD} = v_{SG} + v_{GD} = 5 - (-6) = 11$ V

$v_{SD} = 11 > V_{OV} = 2$ V $\quad \rightarrow \quad$ MOS is in saturation

$i_D = 0.5\mu_p C_{ox}(W/L)_p V_{OV}^2 = 0.5 \times 0.4 \times 10^{-3}(2)^2 = 0.8$ mA

Problem 4. Find i_D ($\mu_n C_{ox}(W/L)_n = \mu_p C_{ox}(W/L)_p = 0.4$ mA/V^2, $\lambda = 0$, $V_{tn} = 3$ V and $V_{tp} = -3$ V).

This is a NMOS transistor with $v_{GS} = 4$ V and $v_{DS} = 1$ V.



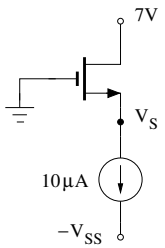
$$V_{OV} = V_{SG} - V_{tn} = 1 \text{ V} \qquad V_{OV} > 0 \quad \rightarrow \quad \text{MOS is ON}$$

Since $v_{DS} = 1 = V_{OV} = 1$ V, NMOS is at the boundary of saturation and triode modes ("edge of saturation"). We can use either formulas for i_D. Saturation is simpler:

$$i_D = 0.5\mu_n C_{ox}(W/L)_n V_{OV}^2 = 0.5 \times 0.4 \times 10^{-3}(1)^2 = 0.2 \text{ mA}$$

Problem 5. Find V_S ($\mu_n C_{ox}(W/L)_n = 0.5$ mA/V^2, $\lambda = 0$, and $V_{tn} = 0.8$ V).

Since $i_D = 10$ μA, NMOS should be ON. Assume NMOS in saturation:

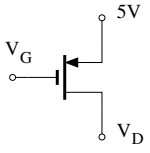


$$i_D = 0.5\mu_n C_{ox}(W/L)_n V_{OV}^2$$
$$10 \times 10^{-6} = 0.5 \times 0.5 \times 10^{-3} V_{OV}^2 \quad \rightarrow \quad V_{OV} = 0.2 \text{ V}$$
$$v_{GS} = V_{OV} + V_{tn} = 1 \text{ V}$$
$$v_{GS} = V_G - V_S = 0 - V_S \quad \rightarrow \quad V_S = -1 \text{ V}$$
$$v_{DS} = V_D - V_S = 7 - (-1) = 8 \text{ V}$$

Since $v_{DS} = 8 > V_{OV} = 0.2$ V, assume of MOS in saturation is correct and $V_S = -1$ V.

Problem 6. Consider this PMOS with $\mu_p C_{ox}(W/L)_p = 0.6$ mA/V^2, $\lambda = 0$, and $V_{tp} = -1$ V. A) For what values of V_G, PMOS will be ON?, B) Find the range of V_D for which PMOS is in triode (answer in terms of V_G). C) Find the range of V_D for which PMOS is in saturation (answer in terms of V_G). D) If PMOS is in saturation with $i_D = 75$ μA, find V_{OV}, V_G and the corresponding range of V_D.

Note: $v_{SG} = 5 - V_G$, $v_{SD} = 5 - V_D$, and $V_{OV} = v_{SG} - |V_{tp}| = 4 - V_G$:



Part A: For PMOS to be ON:

$$V_{OV} \geq 0 \quad \rightarrow \quad 4 - V_G \geq 0 \quad \rightarrow \quad V_G \leq 4 \text{ V}$$

Part B: For PMOS to be in triode:

$$v_{SD} \le V_{OV}$$
$$5 - V_D \le 4 - V_G \quad \rightarrow \quad V_D \ge V_G + 1$$

Part C: For PMOS to be in saturation:

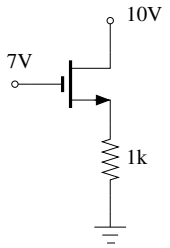
$$v_{SD} \ge V_{OV}$$
$$5 - V_D \ge 4 - V_G \quad \rightarrow \quad V_D \le V_G + 1$$

Part D:

$$75 \times 10^{-6} = i_D = 0.5\mu_p C_{ox}(W/L)_p V_{OV}^2 = 0.5 \times 0.6 \times 10^{-3} V_{OV}^2 \quad \rightarrow \quad V_{OV} = 0.5 \text{ V}$$
$$v_{SG} = V_{OV} + |V_{tp}| = 1.5 \text{ V}$$
$$v_{SG} = 5 - V_G = 1.5 \text{ V} \quad \rightarrow \quad V_G = 3.5 \text{ V}$$

and from the result of part C, we get $V_D \le V_G + 1 = 4.5$ V.

Problem 7. Find i_D and v_{DS} ($\mu C_{ox}(W/L) = 0.4$ mA/V^2, $\lambda = 0$, and $V_t = 3$ V).



GS-KVL: $7 = v_{GS} + 10^3 i_D = V_{OV} + V_t + 10^3 i_D \quad \rightarrow \quad 4 = V_{OV} + 10^3 i_D$

DS-KVL: $10 = v_{DS} + 10^3 i_D$

Obviously, NMOS cannot be in cut-off because if $i_D = 0$, GS-KVL gives $V_{OV} = 4 > 0$. Assume NMOS in saturation:

$$i_D = 0.5\mu_n C_{ox}(W/L)_n V_{OV}^2$$

GS-KVL: $4 = V_{OV} + 10^3 \times 0.5 \times 0.4 \times 10^{-3} V_{OV}^2$

$$0.2V_{OV}^2 + V_{OV} - 4 = 0 \quad \rightarrow \quad V_{OV} = -7.62 \text{ V} \quad \text{and} \quad V_{OV} = 2.62 \text{ V}$$

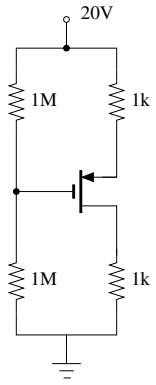
Negative root is unphysical (we need $V_{OV} > 0$). Thus, $V_{OV} = 2.62$ V ($v_{GS} = 5.62$ V) and

GS-KVL: $4 = V_{OV} + 10^3 i_D \quad \rightarrow \quad i_D = 1.38$ mA

DS-KVL: $10 = v_{DS} + 10^3 i_D \quad \rightarrow \quad v_{DS} = 8.62$ V

Since $v_{DS} = 8.62 > V_{OV} = 2.62$ V, our assumption of NMOS in saturation is justified.

Problem 8. Find v_{SG}, i_D, and v_{SD} ($\mu_p C_{ox}(W/L)_p = 0.4$ mA/V^2, $\lambda = 0$, and $V_{tp} = -3$ V).



Since $i_G = 0$, the two 1 MΩ resistors form a voltage divider and $V_G = 20 \times (10^6)/(10^6 + 10^6) = 10$ V.

SG-KVL: $20 = 10^3 i_D + v_{SG} + V_G = 10^3 i_D + V_{OV} + |V_{tp}| + V_G$

$\rightarrow \quad 20 - 3 - 10 = 7 = V_{OV} + 10^3 i_D$

SD-KVL: $20 = 10^3 i_D + v_{SD} + 10^3 i_D = v_{SD} + 2 \times 10^3 i_D$

Obviously, PMOS cannot be in cut-off because if $i_D = 0$, SG-KVL gives $V_{OV} = 7 > 0$. Assume PMOS in saturation:

$$i_D = 0.5\mu_p C_{ox}(W/L)_p V_{OV}^2$$

GS-KVL: $7 = V_{OV} + 10^3 \times 0.5 \times 0.4 \times 10^{-3} V_{OV}^2$

$$0.2V_{OV}^2 + V_{OV} - 7 = 0 \quad \rightarrow \quad V_{OV} = -8.92 \text{ V} \quad \text{and} \quad V_{OV} = 3.92 \text{ V}$$

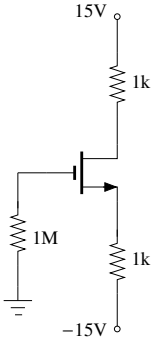
Negative root is unphysical (we need $V_{OV} > 0$). Thus, $V_{OV} = 3.92$ V ($v_{SG} = 6.92$ V) and

SG-KVL: $7 = V_{OV} + 10^3 i_D \quad \rightarrow \quad i_D = 3.08$ mA

SD-KVL: $20 = v_{SD} + 2 \times 10^3 i_D \quad \rightarrow \quad v_{SD} = 13.8$ V

Sine $v_{SD} = 13.8 > V_{OV} = 3.92$ V, our assumption of PMOS in saturation is justified.

Problem 9. Find v_{GS}, i_D, and v_{DS} ($\mu_n C_{ox}(W/L)_n = 0.4$ mA/V^2, $\lambda = 0$, and $V_{tn} = 3$ V).



GS-KVL: $15 = 10^3 i_D + v_{GS} + 10^6 i_G = 10^3 i_D + V_{OV} + V_{tn} + 0$

$\rightarrow \quad 12 = V_{OV} + 10^3 i_D$

DS-KVL: $15 = 10^3 i_D + v_{DS} + 10^3 i_D - 15$

$\rightarrow \quad 30 = 2 \times 10^3 i_D + v_{DS}$

NMOS cannot be in cut-off because if $i_D = 0$, GS-KVL gives $V_{OV} = 12 > 0$. Assume NMOS in saturation:

$$i_D = 0.5\mu_n C_{ox}(W/L)_n V_{OV}^2$$

GS-KVL: $12 = V_{OV} + 10^3 \times 0.5 \times 0.4 \times 10^{-3} V_{OV}^2$

$$0.2V_{OV}^2 + V_{OV} - 12 = 0 \quad \rightarrow \quad V_{OV} = -10.64 \text{ V} \quad \text{and} \quad V_{OV} = 5.64 \text{ V}$$

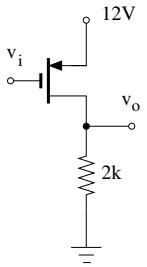
Negative root is unphysical (we need $V_{OV} > 0$). Thus, $V_{OV} = 5.64$ V ($v_{GS} = 8.64$ V) and

GS-KVL: $\quad 12 = V_{OV} + 10^3 i_D \quad \rightarrow \quad i_D = 6.36$ mA

DS-KVL: $\quad 30 = v_{DS} + 2 \times 10^3 i_D \quad \rightarrow \quad v_{DS} = 17.28$ V

Sine $v_{DS} = 17.28 > V_{OV} = 5.64$, our assumption of NMOS in saturation is justified.

Problem 10. Find v_o for $v_i = 0$ V ($\mu_p C_{ox}(W/L)_p = 0.5$ mA/V^2, $\lambda = 0$, and $V_{tp} = -2$ V).



$$v_{SG} = 12 - 0 = 12 \text{ V}$$
$$V_{OV} = v_{SG} - |V_{tp}| = 12 - 2 = 10 \text{ V}$$

Since $V_{OV} > 0$, assume PMOS in saturation:

$$i_D = 0.5\mu_p C_{ox}(W/L)_p V_{OV}^2 = 0.5 \times 0.5 \times 10^{-3} \times (10)^2 = 25 \text{ mA}$$

DS-KVL: $\quad 12 = v_{SD} + 2 \times 10^3 i_D \quad \rightarrow \quad v_{SD} = -38$ V

Since $v_{SD} = -38 < V_{OV}$, PMOS is NOT in saturation. Assume PMOS in triode:

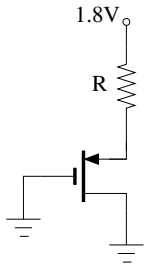
$$i_D = 0.5\mu_p C_{ox}(W/L)_p(2v_{SD}V_{OV} - v_{SD}^2)$$

DS-KVL: $\quad 12 = v_{SD} + 2 \times 10^3 i_D = v_{SD} + 2 \times 10^3 \times 0.5 \times 0.5 \times 10^{-3} \times (20v_{SD} - v_{SD}^2)$

$$\rightarrow \quad 0.5v_{SD}^2 - 11v_{SD} + 12 = 0 \quad \rightarrow \quad v_{SD} = 20.8 \text{ V} \quad \text{and} \quad v_{SD} = 1.15 \text{ V}$$

$v_{SD} = 20.8$ V is unphysical ($v_{SD} \geq V_{OV} = 10$ V). Thus, $v_o = 12 - v_{SD} = 10.85$ V.

Problem 11. Find R such that PMOS is in saturation with $V_{OV} = 0.6$ V ($\mu_p C_{ox} = 0.1$ mA/V^2, $(W/L) = 10/0.18$, $\lambda = 0$, and $V_{tp} = -0.4$ V).



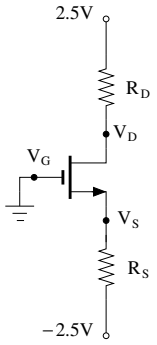
$$i_D = 0.5\mu_p C_{ox}(W/L)V_{OV}^2 = 0.5 \times 0.1 \times 10^{-3} \times (10/0.18) \times (0.6)^2 = 1 \text{ mA}$$

SG-KVL: $\quad 1.8 = Ri_D + v_{SG} = 10^{-3}R + V_{OV} + |V_{tp}|$

$$1.8 = 10^{-3}R + 0.6 + 0.4 \quad \rightarrow \quad R = 800\ \Omega$$

SD-KVL: $\quad 1.8 = Ri_D + v_{SD} \quad \rightarrow \quad v_{SD} = 1 > V_{OV} = 0.6$ V, $\quad$ in saturation

Problem 12. Design the circuit below (*i.e.,* find R_S and R_D) in order to get $i_D = 0.25$ mA and $V_D = 0$. ($\mu_n C_{ox} = 60\ \mu$A/V^2, $W/L = 100/3$, $\lambda = 0$, and $V_t = 1$ V).



Since $i_D > 0$, NMOS is ON. Assume saturation:

$$i_D = 0.5\mu_n C_{ox}(W/L)V_{OV}^2$$
$$0.25 \times 10^{-3} = 0.5 \times 60 \times 10^{-6}(100/3)V_{OV}^2 \quad \rightarrow \quad V_{OV} = 0.5 \text{ V}$$
$$v_{GS} = V_{OV} + V_t = 0.5 + 1 = 1.5 \text{ V}$$
$$v_{GS} = V_G - V_S = 0 - V_S \quad \rightarrow \quad V_S = -1.5 \text{ V}$$
$$v_{DS} = V_D - V_S = 0 - (-1.5) = 1.5 \text{ V}$$

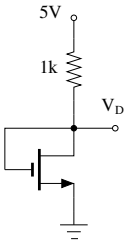
Since $v_{DS} = 1.5 > V_t = 1$ V, assumption of NMOS in saturation is justified.

GS-KVL: $0 = v_{GS} + R_S i_D - 2.5 = 1.5 + 0.25 \times 10^{-3} R_S - 2.5 \quad \rightarrow \quad R_S = 4.0$ k

DS-KVL: $2.5 = R_D i_D + V_D = 0.25 \times 10^{-3} R_D + 0 \quad \rightarrow \quad R_D = 10$ k

Problem 13. Find V_D ($\mu_n C_{ox}(W/L) = 0.5$ mA/V^2, $\lambda = 0$, and $V_t = 0.8$ V).

Since the gate is connected to the drain, $v_{DS} = v_{GS}$. This leads to $v_{DS} = v_{GS} > v_{GS} - V_t = V_{OV}$. Thus, this transistor is always in saturation. This configuration is called a diode-connected transistor.

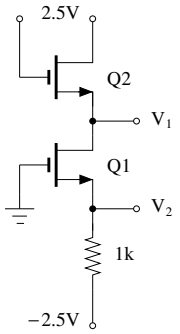


Proceed to the solution with $v_{DS} = v_{GS} = V_{OV} + V_t$:

$$i_D = 0.5\mu_n C_{ox}(W/L)V_{OV}^2$$
DS-KVL $$5 = 10^3 i_D + v_{DS} = 10^3 \times 0.5 \times 0.5 \times 10^{-3} V_{OV}^2 + V_{OV} + 0.8$$
$$0.25V_{OV}^2 + V_{OV} - 4.2 = 0 \quad \rightarrow \quad V_{OV} = -6.56 \text{ V} \quad \text{and} \quad V_{OV} = 2.56 \text{ V}$$

Negative root is unphysical (we need $V_{OV} > 0$). Thus, $V_{OV} = 2.56$ V and $V_D = v_{DS} = v_{GS} = V_{OV} + V_t = 3.36$ V.

Problem 14. Find V_1 and V_2 ($\mu_n C_{ox}(W/L) = 5$ mA/V^2, $\lambda = 0$, and $V_t = 1$ V).



By KCL: $i_{D1} = i_{D2} = i_D$. Assume both in saturation

$$i_D = i_{D1} = 0.5\mu_n C_{ox}(W/L)V_{OV1}^2$$

GS1-KVL: $$0 = V_{GS1} + 10^3 i_D - 2.5$$

$$0 = V_{OV1} + 1 + 10^3(0.5 \times 5 \times 10^{-3} V_{OV1}^2) - 2.5$$

$$2.5V_{OV1}^2 + V_{OV1} - 1.5 = 0$$

$$\rightarrow \quad V_{OV1} = -1.0 \text{ V} \quad \text{and} \quad V_{OV} = 0.60 \text{ V}$$

Negative root is unphysical (we need $V_{OV} > 0$). Thus, $V_{OV1} = 0.6$ V ($v_{GS1} = 1.6$ V).

Since $i_{D1} = i_{D2}$, transistors have the same $\mu_n C_{ox}(W/L)$, and are both in saturation, $V_{OV2} = V_{OV1} = 0.6$ V and $v_{GS2} = v_{GS1} = 1.6$ V

$$v_{GS1} = V_{G1} - V_{S1} = 0 - V_{S1} \quad \rightarrow \quad V_2 = V_{S1} = -v_{GS1} = -1.6 \text{ V}$$

$$v_{GS2} = V_{G2} - V_{S2} = 2.5 - V_{S2} \quad \rightarrow \quad V_1 = V_{S2} = 2.5 - v_{GS2} = 0.90 \text{ V}$$

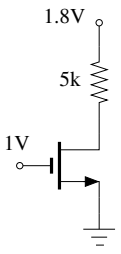
$$v_{DS1} = V_{D1} - V_{S1} = V_1 - V_2 = 0.90 - (-1.6) = 2.5 \text{ V}$$

$$v_{DS2} = V_{D2} - V_{S2} = 2.5 - V_1 = 2.5 - 0.90 = 1.6 \text{ V}$$

Since $V_{OV1} = V_{OV2} = 0.6 > 0$ and $V_{DS1} = 2.5 > V_{OV1} = 0.6$ as well as $V_{DS2} = 1.6 > V_{OV2} = 0.6$, our assumption of both MOS in saturation is justified,.

Problem 15. Find i_D and v_{DS} for A) ignoring channel-length modulation ($\lambda = 0$) and B) including channel-length modulation ($\lambda = 0.05$ V^{-1}). NMOS has $\mu_n C_{ox}(W/L) = 1$ mA/V^2 and $V_t = 0.4$ V.

Part A: $\lambda = 0$



$$i_D = 0.5\mu_n C_{ox}(W/L)_n V_{OV1}^2 = 0.5 \times 10^{-3}(0.6)^2 = 0.180 \text{ mA}$$

DS-KVL: $$1.8 = 5 \times 10^3 i_D + v_{DS} \quad \rightarrow \quad v_{DS} = 0.90 \text{ V}$$

Since $v_{DS} = 0.9 > V_{OV} = 0.6$ V, assumption of NMOS in saturation is justified.

Part B: $\lambda = 0.05\ \text{V}^{-1}$

$$i_D = 0.5\mu_n C_{ox}(W/L)_n V_{OV1}^2(1+\lambda v_{DS}) = 0.180\times 10^{-3}(1+0.05v_{DS})$$

DS-KVL: $1.8 = 5\times 10^3 i_D + v_{DS}$

$$1.8 = 0.9(1+0.05v_{DS}) + v_{DS} \quad \rightarrow \quad v_{DS} = 0.86\ \text{V}$$

$$i_D = 0.180\times 10^{-3}(1+0.05v_{DS}) = 0.188\ \text{mA}$$

Note that by ignoring channel-length modulation, the relative error in i_D and v_{DS} is $\approx \lambda v_{DS}$ (for this problem, $\lambda v_{DS} = 0.05\times 0.90 = 4.5\%$).

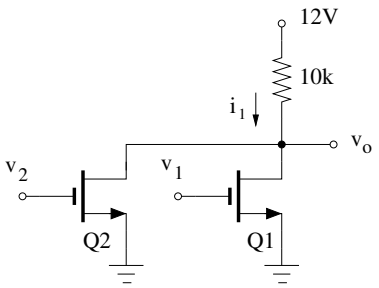
Problem 16. Show that this circuit is a NOR gate with a LOW state of 0.2 V and a HIGH state of 12 V ($\mu_n C_{ox}(W/L)_n = 0.5\ \text{mA/V}^2$, $V_t = 1$ V).

GS-KVL $v_{GS1} = v_1, \qquad v_{GS2} = v_2$

DS-KVL $12 = 10^4 i_1 + v_o$

KCL $i_1 = i_{D1} + i_{D2}$

$v_o = v_{DS1} = v_{DS2}$



Case 1: $v_1 = v_2 = 0.2$. Since $v_{GS1} = 0.2 < V_t = 1$ and $v_{GS2} = 0.2 < V_t = 1$, both transistors are in cut-off: $i_{D1} = i_{D2} = 0$. Then, $i_1 = i_{D1} + i_{D2} = 0$ and from DS-KVL, $v_o = 12$ V.

So, When $v_1 = 0.2$ (LOW) and $v_2 = 0.2$ (LOW), Q1 and Q2 are OFF and $v_o = 12$ V (HIGH).

Case 2: $v_1 = 0.2, v_2 = 12$ V. Since $v_{GS1} = 0.2 < V_t = 1$, Q1 is in cut-off and $i_{D1} = 0$. Since $v_{GS2} = 12 > V_t = 1$, Q2 is not in cut-off. Assume Q2 is in saturation ($V_{OV2} = v_{GS2} - V_t = 11$ V). Then:

$$i_{D2} = 0.5\mu_n C_{ox}(W/L)_n V_{OV2}^2 = 0.5\times 0.5\times 10^{-3}(11)^2 = 30\ \text{mA}$$

$$v_{DS2} = v_o = 12 - 10^4(i_{D2} + i_{D1}) = -288\ \text{V}$$

Since $v_{DS2} = -288 < v_{OV2} = 11$ V, Q2 is not in saturation. Assume Q2 is in triode:

$$i_{D2} = 0.5\mu_n C_{ox}(W/L)_n(2v_{DS2}V_{OV2} - v_{DS2}^2) = 0.25\times 10^{-3}(22v_{DS2} - v_{DS2}^2)$$

$$12 = 10^4 i_{D2} + v_{DS2} \quad \rightarrow \quad 12 = 2.5[22v_{DS2} - v_{DS2}^2] + v_{DS2}$$

$$-2.5v_{DS2}^2 + 56v_{DS2} - 12 = 0 \quad \rightarrow \quad V_{DS2} = 22.2\ \text{V} \quad \text{and} \quad V_{DS2} = 0.22\ \text{V}$$

First root is not physical ($v_{DS2} = 22.2 > V_{OV2} = 11$ V). $v_{DS2} = 0.2$ V is correct as $v_{DS2} = 0.22 < V_{OV} = 11$ V (our assumption of Q2 in triode is justified).

So, when $v_1 = 0.2$ (LOW) and $v_2 = 12$ V (HIGH), Q1 is OFF, Q2 is in triode and $v_o = 0.2$ V (LOW).

Case 3: $v_1 = 12, v_2 = 0.2$ V. This is similar to case 2. By symmetry:

When $v_1 = 12$ V (HIGH) and $v_2 = 0.2$ (LOW), Q1 is in triode, Q2 is OFF, and $v_o = 0.2$ V (LOW).

Case 4: $v_1 = 12, v_2 = 12$ V. Since $v_{GS1} = 12 > V_t = 1$, and $v_{GS2} = 12 > V_t = 1$, both transistors are ON ($V_{OV1} = V_{OV2} = 11$ V). Since the two transistors are identical, $v_{GS1} = v_{GS2}$ and $v_{DS1} = v_{DS2}$, both are in the same state and $i_{D1} = i_{D2} = 0.5i_1$ (we only need to analyze one of them). Assume both transistors are in triode:

$$i_{D1} = i_{D2} = 0.5\mu_n C_{ox}(W/L)_n[2v_{DS2}V_{OV2} - v_{DS2}^2] = 0.25 \times 10^{-3}[22v_{DS2} - v_{DS2}^2]$$
$$12 = 10^4(2i_{D2}) + v_{DS2} \quad \rightarrow \quad 12 = 5[22v_{DS2} - v_{DS2}^2] + v_{DS2}$$
$$-5v_{DS2}^2 + 121v_{DS2} - 12 = 0 \quad \rightarrow \quad V_{DS2} = 22.1 \text{ V} \quad \text{and} \quad V_{DS2} = 0.11 \text{ V}$$

First root is not physical ($v_{DS2} = 22.1 > V_{OV2} = 11$). $v_{DS2} = 0.11$ V is correct as $v_{DS2} = 0.11 < v_{GS2} - V_t = 12 - 1 = 11$ (our assumption of Q2 in triode is justified). By KVL: $v_o = v_{DS1} = v_{DS2} = 0.11$ V.

So, When $v_1 = 12$ V (HIGH) and $v_2 = 12$ V (HIGH), Q1 and Q2 are in triode and $v_o = 0.1$ V (LOW).

Since the output is HIGH only when both inputs are LOW, this is NOR gate.