Name PID

UNIVERSITY OF CALIFORNIA, SAN DIEGO

Electrical and Computer Engineering Department

ECE 65 – Spring 2023

Components and Circuits lab

Final Exam Solutions

- Closed books, three one-sided cheat sheets, and calculators are allowed.
- Electronic devices are not allowed.
- Please put all answers in the provided sheets.
- You can use the back of every page as a scratch paper.
- Please scan your answers and cheat sheets and submit them to Gradescope by 2:30 pm.

Please do not begin until you are told to do so.

Show your work and good luck!

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Problem 1.

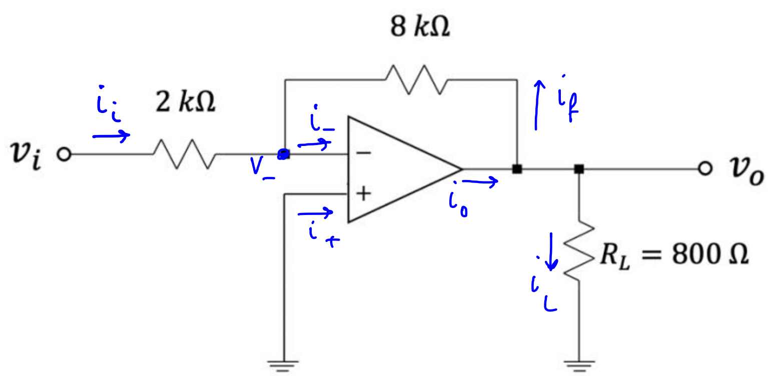
Consider the following op-amp circuit. Assume an ideal op-amp.

Choose the op-amp saturation voltage, maximum output current, and a sinusoidal input voltage such that the output voltage would be distorted because of op-amp's maximum output current.

a) What are your selected saturation voltage, maximum output current, and input voltage?

b) Analyze the circuit and show why the output voltage is distorted.

c) Draw the input and output waveforms.



There is more than one correct answer to this problem.

Show your work.

op-amp is ideal: $i_+ = i_- = 0$

there is negative feedback: $V_+ = V_- = 0$

KCL at the inverting input terminal: $i_i + i_f = i_- = 0$

$$\frac{V_i - V_-}{2k\Omega} + \frac{V_o - V_-}{8k\Omega} = 0 \rightarrow \frac{V_i}{2k\Omega} + \frac{V_o}{8k\Omega} = 0 \Rightarrow \frac{V_o}{V_i} = -\frac{8}{2} = -4\ V/V$$

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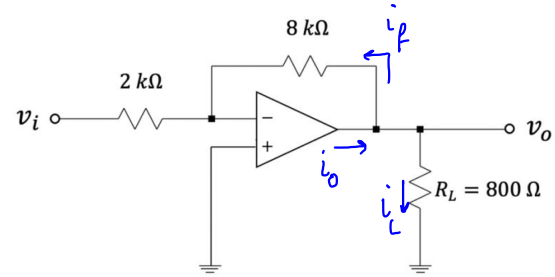


$v_o = -4 v_i$ when we have linear amplification

KCL at the output node: $i_o = i_f + i_L$

$$i_f = \frac{V_o - V_-}{8k} = \frac{V_o}{8k} \quad , \quad i_L = \frac{V_o}{0.8k}$$

$$i_o = \frac{V_o}{8k} + \frac{V_o}{0.8k} = \frac{11}{8} V_o \quad (mA)$$

choose some values for V_{sat}, I_{omax} and choose v_i:

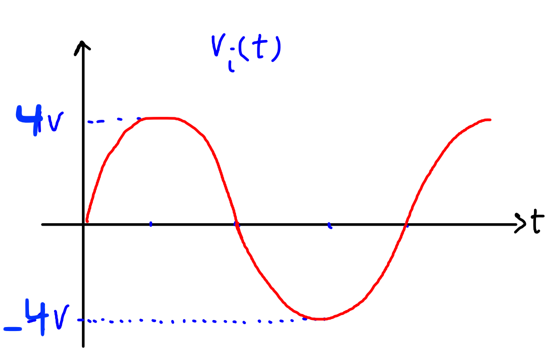
$$V_{sat} = \pm 25 \,,\quad \hat{V}_i = 4\ V \rightarrow |\hat{V}_o| = 16\ V < V_{sat}$$

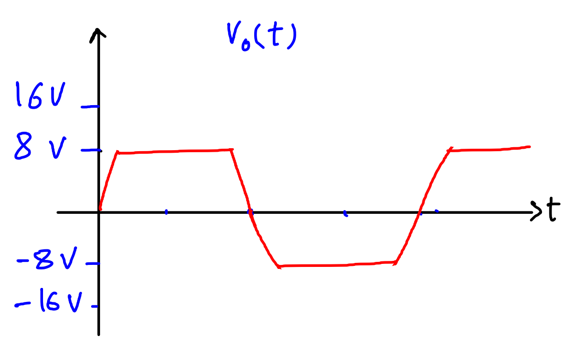
linear amplification will not be limitted by the saturation voltage.

Assume $I_{omax} = 11\,mA$. To have $\hat{V}_o = 16V$, we need $\hat{i}_o = 22\,mA$, which can not be supplied

The output voltage will be distorted because of the op-amp max output current.

$$i_{o\,max} = \frac{11}{8} V_{o\,max} = 11\ mA \rightarrow V_{o\,max} = \frac{8 \times 11}{11} = 8\ (V)$$





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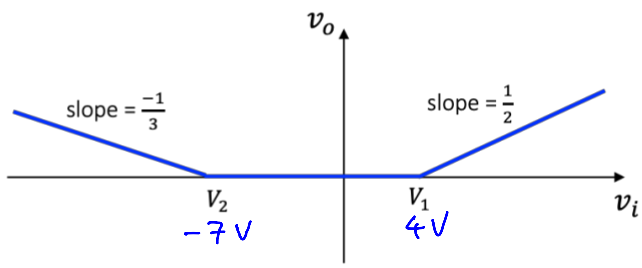
Problem 2.

In the below transfer characteristics (transfer function) graph, $V_1 = 4\ V,\ V_2 = -7\ V$



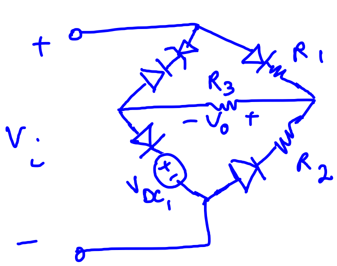
a) Design a diode waveform shaping circuit that would have the above transfer function.
   - You can use PN junction diodes with $V_{D0} = 0.7$ V, Zener diodes with $V_z = 2.3$ V, DC voltage sources and resistors in your design.
   - You should indicate the resistor values and the DC voltage sources' values in your design.
   - Make sure to include the input voltage source in your circuit schematic and label the output terminals.
   - Make sure that at least one Zener diode and one DC voltage source are used in your design.

b) Parametrically solve your circuit. That means find the relationship between v_i and v_o and the range of v_i.

Write complete equations and show your work.

From the transfer characteristic graph:

$$V_o = \begin{cases} \frac{1}{2}V_i - 2, & V_i \geq 4V \\ 0, & -7 < V_i < 4V \\ \frac{-1}{3}V_i - \frac{7}{3}, & V_i \leq -7V \end{cases}$$



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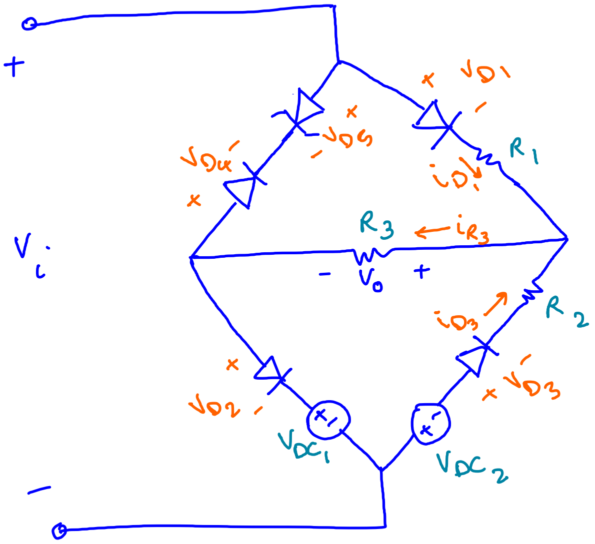

$$V_o = \begin{cases} \frac{1}{2}V_i - 2, & V_i \geqslant 4V \\ 0, & -7 < V_i < 4V \\ -\frac{1}{3}V_i - \frac{7}{3}, & V_i \leqslant -7V \end{cases}$$

Case 1: D_1 & D_2 ON, D_3 & D_4 & D_5 off

Case 2: D_1 & D_2 off, D_3 & D_4 ON and D_5 in Zener

Case 3: All diodes are off

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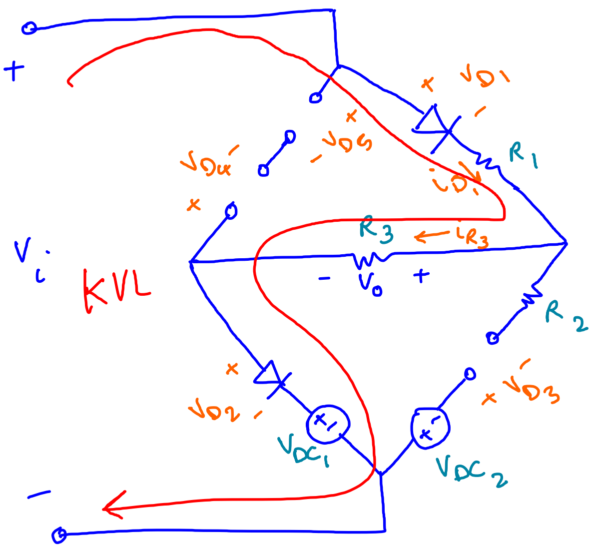

Case 1: D_1 & D_2 ON

D_3 & D_4 & D_5 off

$V_{D_1} = V_{D_2} = 0.7\ V \qquad i_{D_1} \geq 0, \; i_{D_2} \geq 0$

$V_{D_3} < V_{D_o}, \; V_{D_4} < V_{D_o}, \; -V_2 < V_{D_3} < V_{D_o}$

$i_{D_3} = i_{D_4} = i_{D_5} = 0$

KVL: $V_i = V_{D_1} + R_1 \, i_{D_1} + i_{D_1} \times R_3 + V_{D_2} + V_{DC_1}$

$$V_i = 0.7 + R_1 \, i_{D_1} + i_{D_1} \times R_3 + 0.7 + V_{DC_1}$$

$$i_{D_1} = \frac{V_i - 1.4 - V_{DC_1}}{R_1 + R_3}$$

$$i_{D_1} \geq 0 \longrightarrow V_i \geq 1.4\ V + V_{DC_1}$$

$$V_o = R_3 \times i_{D_1} = \frac{R_3}{R_1 + R_3} V_i - \frac{R_3}{R_1 + R_3}\left(1.4 + V_{DC_1}\right)$$

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$$\begin{cases} V_i \geq 1.4\,V + V_{DC_1} \\ \\ V_o = \frac{R_3}{R_1+R_3} V_i - \frac{R_3}{R_1+R_3}(1.4 + V_{DC_1}) \end{cases}$$

comparing the above conditions with the ones obtained from the graph we can find V_{DC_1} and choose values for R_1 and R_3.

From the graph: $V_o = \frac{1}{2} V_i - 2$ when $V_i \geq 4V$

$$1.4\,V + V_{DC_1} = 4\,V \longrightarrow V_{DC_1} = 2.6\,V$$

$$\frac{R_3}{R_1+R_3} = \frac{1}{2}$$, choose $R_3 = 1\,k\Omega$, $R_1 = 1\,k\Omega$

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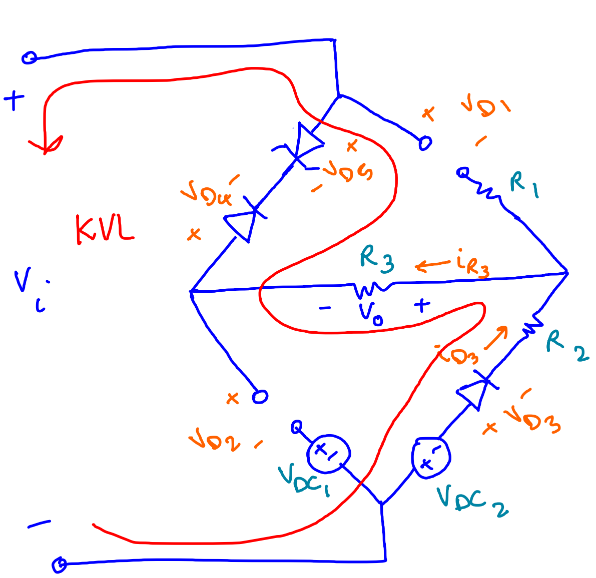

Case 2 : D_1 & D_2 off

D_3 & D_4 ON and D_5 in Zener

$V_{D_3} = V_{D_4} = 0.7\ V \qquad i_{D_3} \geq 0, \ i_{D_4} \geq 0$

$V_{D_5} = -V_Z \ , \quad i_{D_5} \leq 0$

$V_{D_1} < V_{D_0} \ , \ V_{D_2} < V_{D_0}$

$i_{D_1} = i_{D_2} = 0$

KVL : $V_i = V_{D_5} - V_{D_4} - i_{R_3} \times R_3 - i_{D_3} \times R_2 - V_{D_3} - V_{DC_2}$

$V_{D_5} = -V_Z = -2.3\ V \ , \quad V_{D_4} = 0.7 \ , \quad V_{D_3} = 0.7\,V$

$i_{R_3} = i_{D_3}$

$$V_i = -2.3V - 0.7\ V - i_{D_3} \times R_3 - i_{D_3} \times R_2 - 0.7V - V_{DC_2}$$

$$i_{D_3} = \frac{-V_i - 3.7V - V_{DC_2}}{R_3 + R_2}$$

$$i_{D_3} \geq 0 \rightarrow V_i \leq -3.7V - V_{DC_2}$$

$$V_o = R_3\, i_3 = \frac{-R_3}{R_3 + R_2} V_i - \frac{R_3}{R_3 + R_2}\left(3.7 + V_{DC_2}\right)$$

$$\begin{cases} V_i \leq -3.7V - V_{DC_2} \\ \\ V_o = \dfrac{-R_3}{R_3+R_2} V_i - \dfrac{R_3}{R_3+R_2}\left(3.7 + V_{DC_2}\right) \end{cases}$$

comparing the above conditions with the ones obtained from the graph we can find V_{DC_2} and choose a value for R_2.

From the graph: $V_o = -\frac{1}{3} V_i - \frac{7}{3}$ when $V_i \leq -7V$

$$-3.7 - V_{DC_2} = -7 \longrightarrow V_{DC_2} = 3.3\ V$$

$$\frac{-R_3}{R_2+R_3} = \frac{-1}{3} \quad \text{and } R_3 = 1\,k\Omega \longrightarrow R_2 = 2\,k\Omega$$

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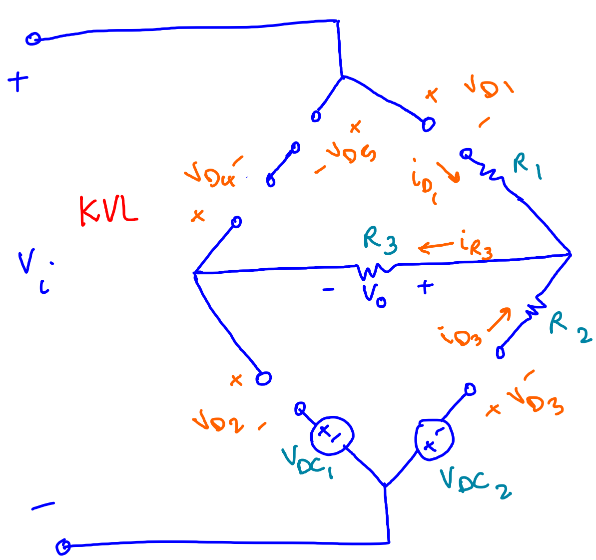

Case 3:

All diodes are off.

$V_{D_1} < V_{D_0}$, $V_{D_2} < V_{D_0}$, $V_{D_3} < V_{D_0}$

$-V_2 < V_{D_5} < V_{D_0}$

$i_{D_1} = i_{D_2} = i_{D_3} = i_{D_4} = i_{D_5} = 0$

This is the only other case, so for this case $-7 < V_i < 4$.

$$i_{R_3} = i_{D_1} + i_{D_3} = 0$$

$$V_o = R_3 \, i_{R_3} = 0$$

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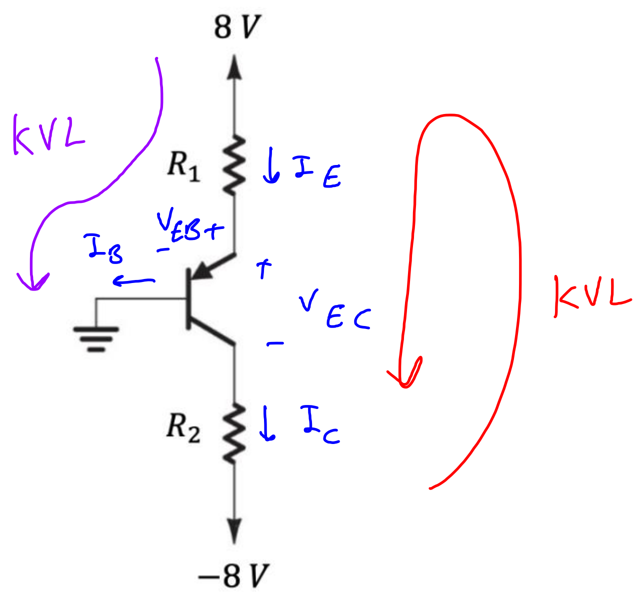
Problem 4.

Deign the following circuit to have the BJT operate in the saturation mode.

Assume $\beta = 200,\ V_{sat} = 0.2\ V$, and $V_{D0} = 0.7\ V$



Show your work.

BJT is in saturation : $V_{EC} = V_{sat} = 0.2\ V$

KVL: $8V = R_1 I_E + V_{EB} \longrightarrow 8V = R_1 I_E + 0.7 \longrightarrow R_1 I_E = 7.3\ V$

KVL: $8\ V = R_1 I_E + V_{EC} + R_2 I_C - 8\ V$

$16\ V - 0.2\ V = R_1 I_E + R_2 I_C \longrightarrow \underbrace{R_1 I_E}_{7.3\ V} + R_2 I_C = 15.8\ V$

$\Longrightarrow R_2 I_C = 8.5\ V$

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$$R_1 I_E = 7.3\ V$$

$$R_2 I_C = 8.5\ V$$

$$I_C < \beta I_B \longrightarrow I_B > \frac{1}{\beta} I_C$$

$$I_B + I_C > \frac{1}{\beta} I_C + I_C$$

$$I_E > \frac{\beta + 1}{\beta} I_C$$

$$I_E > \frac{201}{200} I_C \longrightarrow I_E > 1.005\ I_C$$

We can choose $I_C = 1\ mA$ and $I_E = 1.2\ mA$

$$R_1 I_E = 7.3\ V \longrightarrow R_1 = \frac{7.3\ V}{1.2\ mA} = 6.08\ k\Omega$$

$$R_2 I_C = 8.5\ V \longrightarrow R_2 = \frac{8.5\ V}{1\ mA} = 8.5\ k\Omega$$

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Problem 4.

Design the following amplifier circuit for $\boldsymbol{I_D = 8\ mA}$.

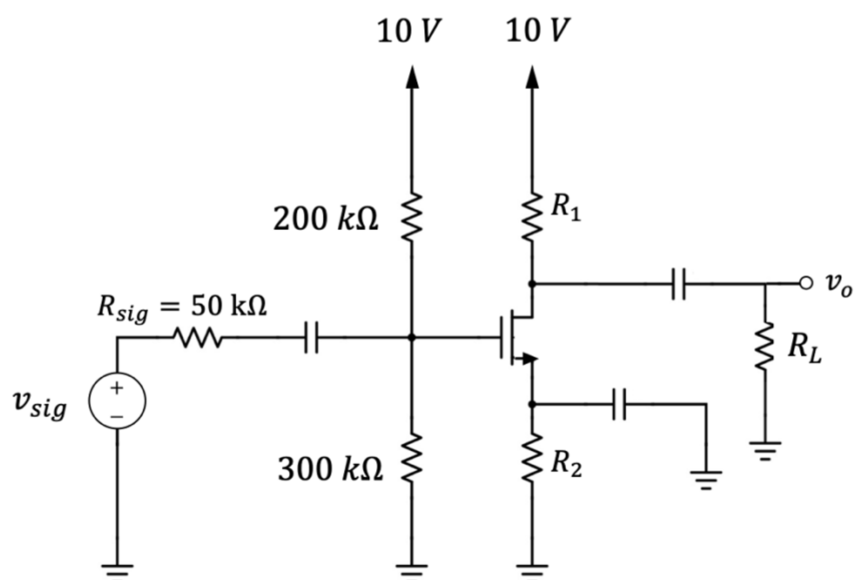
a) Design the circuit and find the Bias point.

b) Find the small signal parameters and draw the signal circuit.

c) Assume $R_L = 1\ k\Omega$ and V_{sig} is a triangular wave with a peak-to-peak amplitude of $400\ mV$ and DC voltage of zero. Find and draw the instantaneous (total) drain to source voltage.

d) What is the maximum amplitude of the signal at the drain if a symmetrical signal swing is desired? What is the amplitude of the corresponding input signal?

Assume $V_t = 0.5\ V$, $\mu C_{ox}\frac{W}{L} = 4\ mA/V^2$, and $\lambda = 0$.



There is more than one correct answer to this problem.

Show your work.

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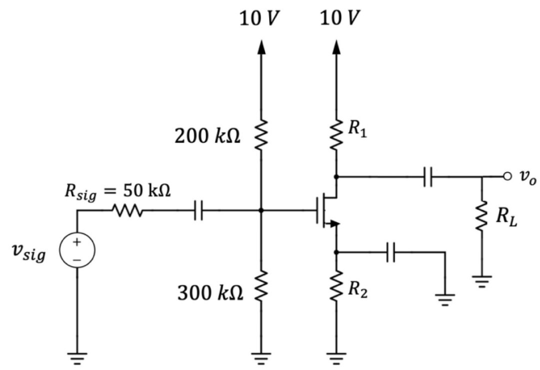
a)



$$V_G = \frac{300\,k\Omega}{500\,k\Omega} \times 10 = 6\ V$$

$I_D = 8\,mA$

NMOS is in saturation

$$I_D = \frac{1}{2} k_n V_{ov}^2$$

$$8\,mA = \frac{1}{2} \times 4\,m\frac{A}{V} \times V_{ov}^2 \Rightarrow V_{ov} = \sqrt{4} = 2\ V$$

$$V_{GS} - V_t = 2 \rightarrow V_{GS} = 2 + 0.5 = 2.5\ V$$

$$V_{GS} = V_G - V_S = 6 - V_S = 2.5 \Rightarrow V_S = 3.5\ V$$

$$V_S = R_2 \times I_D \Rightarrow R_2 = \frac{3.5}{8\,mA} = 437.5\ \Omega$$

$$\boxed{R_2 = 437.5\ \Omega}$$

NMOS must operate in saturation region. $\rightarrow V_{DS} > V_{OV}$

$$V_D - V_S > 2 \rightarrow V_D > 3.5 + 2 \rightarrow V_D > 5.5\ V$$

Select $V_D = 8\ V \rightarrow V_{DS} = 4.5\ V$

$$V_D = 10V - R_1 I_D \rightarrow 8 = 10 - R_1 \times 8\,mA \rightarrow R_1 = \frac{2\,V}{8\,mA} = 250\ \Omega$$

$$\boxed{R_1 = 250\ \Omega}$$

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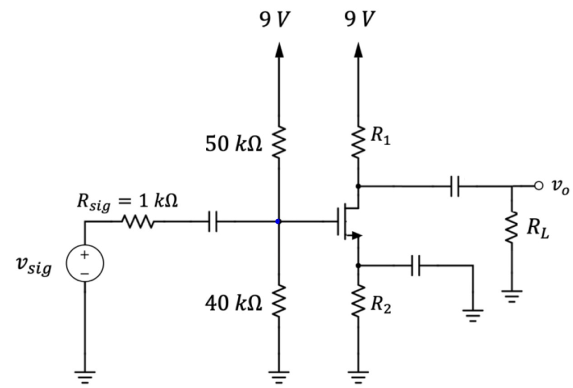
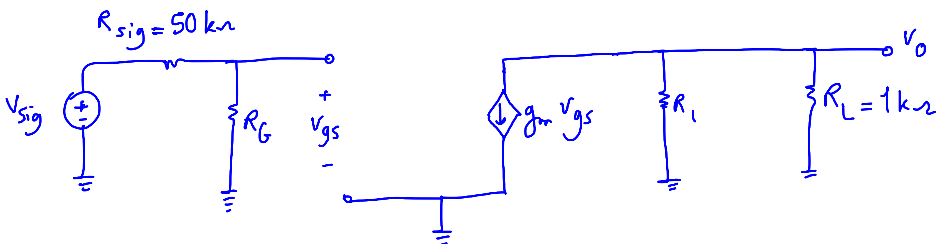
b)



$$g_m = \frac{2 I_D}{V_{oV}} = \frac{2 \times 8 mA}{2 V} = 8 \ mA/V$$

$$r_o \simeq \frac{1}{\lambda I_D} = \infty$$



c) $V_o = -g_m V_{gs} \ (R_1 \| R_L)$, $V_{gs} = \dfrac{R_G}{R_G + R_{sig}} V_{sig}$

$$V_o = V_d = V_{ds} = -g_m \ (R_1 \| R_L) \ \frac{R_G}{R_G + R_{sig}} \ V_{sig}$$

$R_G = 300 k\Omega \ \| \ 200 k\Omega = 120 \ k\Omega$, $\dfrac{R_G}{R_G + R_{sig}} = \dfrac{120 \ k\Omega}{170 \ k\Omega} \simeq 0.71$

$R_1 \| R_L = 0.25 \ k\Omega \ \| \ 1 k\Omega = 200 \ \Omega$, $V_{sig} \simeq 1.42 \ V_{gs}$

$$V_o = V_{ds} = \left(- 8 \ mA/V \times 0.2 \ k\Omega \times 0.71 \right) V_{sig} \simeq -1.136 \ V_{sig}$$

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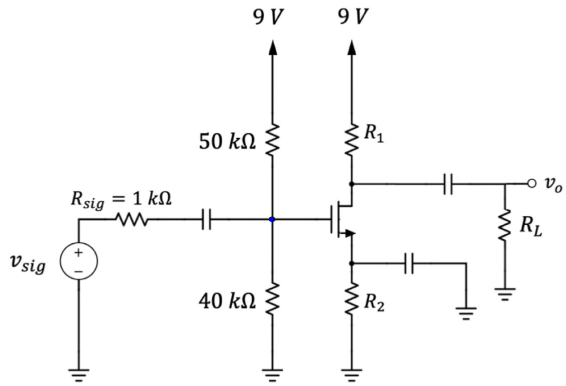
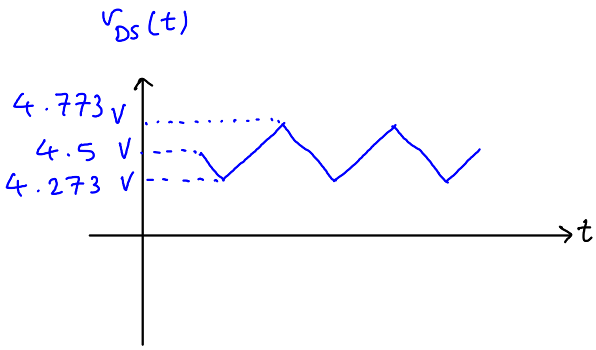


Total $v_{DS} = V_{DS} + v_{ds}$

$= 4.5\ V - 1.136\ v_{sig}$

$\hat{v}_{sig} = 200\ mV \rightarrow \hat{v}_{ds} = 227.2\ mV \simeq 0.227\ V$



d) $v_{DS} > v_{OV} \rightarrow V_{DS} - \hat{v}_{ds} > V_{GS} + \hat{v}_{gs} - V_t$

$v_{ds} = 1.136\ v_{sig} = 1.136 \frac{v_{sig}}{v_{gs}} \times v_{gs} = 1.136 \times 1.42\ v_{gs} \simeq 1.61\ v_{gs}$

$4.5 - \hat{v}_{ds} > 2.5 + \frac{\hat{v}_{ds}}{|A|}$

$2 > \hat{v}_{ds} + \frac{\hat{v}_{ds}}{1.61} \rightarrow \hat{v}_{ds} < 1.23\ V$

$\hat{v}_{ds} = 1.136\ \hat{v}_{sig} \Rightarrow \hat{v}_{sig} < 1.08\ V$