Name PID

UNIVERSITY OF CALIFORNIA, SAN DIEGO

Electrical and Computer Engineering Department

ECE 65 – Spring 2021

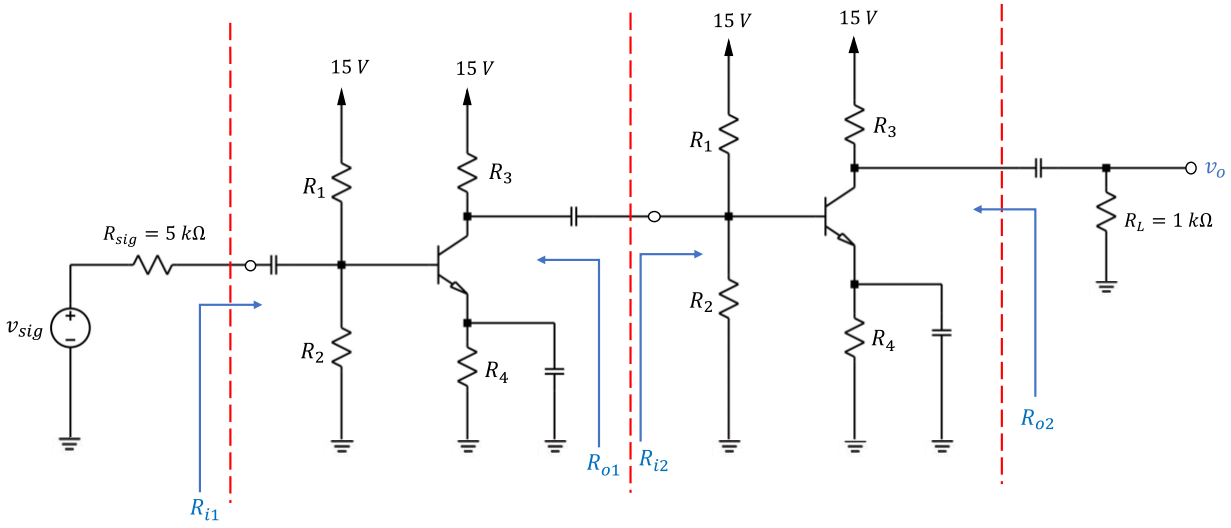
Components and Circuits lab

Midterm Exam3

You should submit your handwritten solutions in a PDF format to Gradescope by Tuesday, 6/1, at 11:59 pm (Pacific Time).

Name PID

In the design of the following two stage BJT amplifier, assume $\beta = 100$, $V_A = 100V$, $V_{D0} = 0.7V$ and $V_T = 25mV$. Also assume the capacitors are short in the signal circuit. Ignore the early effect in Bias circuit calculations.



a) Design the circuit (find the values of R_1, R_2, R_3, and R_4) such that
   - $I_{C1} = I_{C2} = 1\ mA$
   - The input resistances of the first and second stages, R_{i1} and R_{i2}, are both equal to $2\ k\Omega$.
   - The DC node voltages at the collector of transistor 1 and transistor 2 are both greater than 5 V.

Note that the same resistors, R_1, R_2, R_3, and R_4, are used in both stages. To show your work, answer the following questions.

b) Draw the circuit and add your calculated resistor values to the schematic.

c) What are the DC base, collector, and emitter node voltages in your designed circuit? Find them for both transistors.

d) What are the values of g_m, r_π, and r_o for each transistor?

e) Draw the signal circuit.

Name PID

f) What are the output resistances values for each stage (R_{o1}, R_{o2}) in your designed amplifier circuit?

g) What the total circuit voltage gain ($A = \frac{v_o}{v_{sig}}$)? You can either solve the signal circuit from part (e) or use the voltage amplifier model.

h) If $v_{sig} = 0.005\sin(2\pi \times 1000t)$ (V), draw the waveforms for the output voltage (v_o) and the instantaneous (total of AC and DC) collector and emitter node voltages in each transistor.

This is a design problem, so the answers will not be unique.

Show your work.