# UNIVERSITY OF CALIFORNIA, SAN DIEGO

Electrical and Computer Engineering Department

ECE 65 – Fall 2018

*Components and Circuits lab*

Final Exam

Closed books, up to seven double-sided cheat sheets and calculators are allowed

Electronic devices are not allowed.

Please put all your answers in the answer sheets. **Show your work**

Please do not begin until told. Good luck.

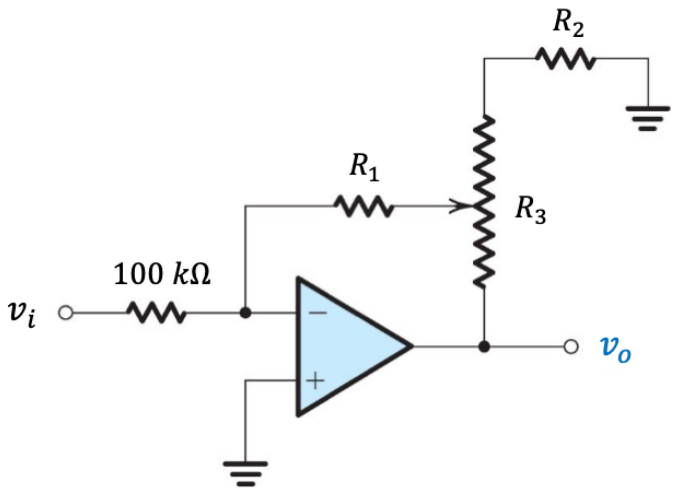
All electronic devices must be turned off and stored away in a backpack or a purse. Anyone caught with such a device on their person during the exam will be charged with academic dishonesty.

**Problem 1**. (10 points)

In the below circuit assuming that the op-amp is ideal,

a) Find $R_1$ and $R_2$ such that the gain can be varied from -1 V/V to -100 V/V using the $100\ k\Omega$ potentiometer $R_3$.

b) What voltage gain results when the potentiometer is set at its middle value?

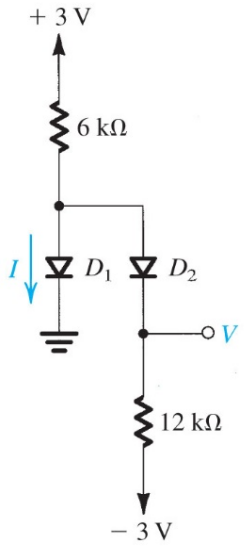


**Problem 2**. (part a: 7 points, part b: 3 points)

Show your analysis for at least two assumptions on the operation of the diodes.

a) Find the values of the labeled voltage ($V$) and current ($I$) in the below circuit.

Assume $V_{D0} = 0.7\ V$.



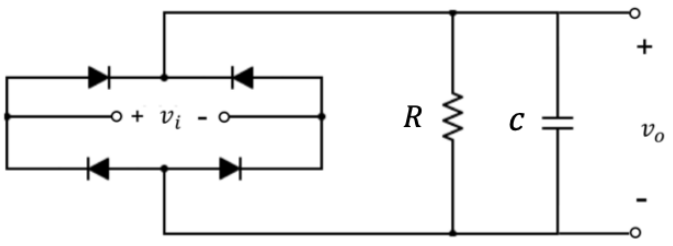

b) In the below circuit, sketch $v_o(t)$ for

i. $V_i(t) = 10\sin(2\pi \times f \times t)$, where $f = 1\ MHz$, $c = 1\ nF$ and $R = 100\ k\Omega$

ii. $V_i(t) = 10\sin(2\pi \times f \times t)$, where $f = 1\ MHz$, $c = 1\ nF$ and $R = 100\ \Omega$

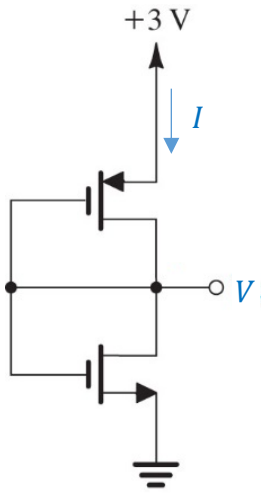
A rough sketch for the waveform of $v_o(t)$ is enough. **Label the peak value of $v_o(t)$**. If the output waveform is different for part (i) and (ii), your sketch should be an indicator of this difference.

Assume $V_{D0} = 0.7\ V$.



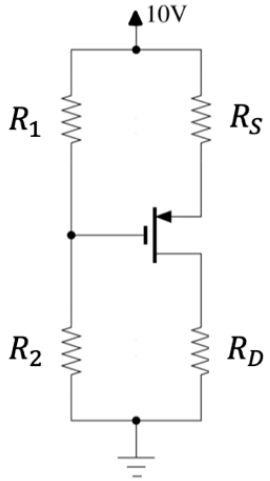
**Problem 3**. (10 points)

The MOS transistors in the following circuit have $|V_t| = 0.5\,V$, $\mu_n C_{ox} = 3\,\mu_p C_{ox} = 270\,\mu A/V^2$, $\lambda = 0$, $L = 1\,\mu m$, and $W = 3\,\mu m$ . Find the labeled current and voltage ( V and I ).




**Problem 4**. (10 points)

Design the below circuit so that the transistor operates in saturation with $V_{SD}$ biased 1-V from the edge of the saturation, with $I_D = 1\,mA$ and $V_D = 3\,V$. Use a $10\,\mu A$ current in the voltage divider. $|V_t| = 1\,V$, $k_p = 0.5\,mA/V^2$, $\lambda = 0$.



**Problem 5**. (part a: 3 points, part b: 3 points, part c: 1 point, part d: 3 points)

In the below amplifier circuit, $Q_1$ has $\beta_1 = 50$ and $Q_2$ has $\beta_2 = 200$. Neglect the early effect in the bias and signal circuits. ($V_{D0} = 0.7\ V, V_T = 25\ mV$).

a) Find the DC emitter currents of $Q_1$ and $Q_2$, as well as the DC voltages of $V_{B1}$ and $V_{B2}$.

b) Find the small signal parameters ( $g_m$ and $r_\pi$ ) for $Q_1$ and $Q_2$.

c) Draw the small signal equivalent circuit.

d) If a load resistance of $R_L = 100\ k\Omega$ is connected to the output terminal, and a signal source with $R_{sig} = 0$ is connected to the input terminal, Find the voltage gain of the circuit ($A = \frac{v_o}{v_{sig}}$). You can either find the input resistance, output resistance, and open loop voltage gain of each stage and use the voltage amplifier model to find the circuit voltage gain (A) or solve the signal equivalent circuit directly.

Hint: The input resistance of the second stage will act as the load resistor for the first stage.

For a common-collector amplifier you can use $A_{vo} = \frac{(1/g_m)\|r_\pi\|R_E\|r_o}{(1/g_m)\|r_\pi}$.