

ECE 65 – Components and Circuits Lab

Lab 6 Report – Logic Gates

Feb 20, 2025

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Abstract

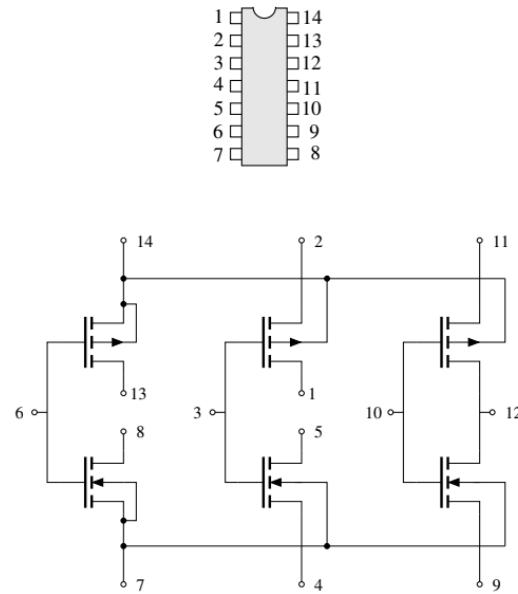
The purpose of this lab is to analyze and verify the behavior of CMOS logic gates, specifically inverters and NOR gates, by comparing theoretical calculations, simulations, and real-world measurements.

We performed MOSFET circuit simulations and transient analysis in LTSpice to examine the operating regions of NMOS and PMOS transistors. Additionally, we built physical circuits and measured output voltages to compare with our prelab theoretical values, identifying any discrepancies due to real-world factors such as fabrication variations, channel-length modulation, and measurement inaccuracies.

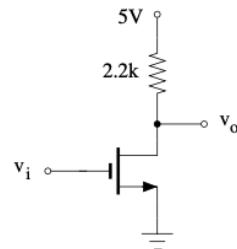
We concluded that while theoretical calculations provided a good approximation, real-world measurements exhibited deviations due to process variations, parasitic effects, and limitations in ideal MOSFET models. Our simulations were consistent with our experimental results, confirming the expected behavior of CMOS logic circuits and validating the theoretical foundation of logic gate operations..

Experimental Procedures and Results

Note: In this Lab, we use the CD4007 chip that consists of 3 pairs of complementary n-channel and p-channel MOSFETs. One pair is internally wired as a CMOS inverter. The pin arrangement for the chip is shown below. You need to power the chip by attaching a 5 V supply to pin 14 ($V_{DD} = 5$ V) and grounding pin 7. Note that by grounding pin 7, all MOSFET "bodies" are connected to the lowest voltage in the circuit, 0 V. You will not use this chip in your simulations. This paragraph was intentionally left for you to observe an example of a real-life internal chip structure.



Experiment 1: NMOS Inverter



Circuit Analysis

Calculate the values of v_o for $v_i = 0, 2.5$, and 5 V. Use $\mu_n C_{ox}(W/L)_n = 1.2$ mA/V², $\lambda = 0$, and $V_t = 1.4V$ for your calculations.

Case 1: $V_i = 0V$

Since $V_i < V_t$, the NMOS is **OFF** (Cutoff region), so:

$$V_o = V_{DD} = 5V$$

Case 2: $V_i = 2.5V$

Since $V_i > V_t$, the NMOS is **ON** and in the Saturation region:

$$I_D = \frac{1}{2}\mu_n C_{ox} \frac{W}{L} n (V_i - V_t)^2$$

Substituting values:

$$\begin{aligned} I_D &= \frac{1}{2}(1.2)(2.5 - 1.4)^2 \\ &= 0.5 \times 1.2 \times 1.21 \\ &= 0.726 \text{ mA} \end{aligned}$$

Using Ohm's Law:

$$V_o = V_{DD} - I_D R_D$$

$$\begin{aligned} V_o &= 5 - (0.726 \times 2.2) \\ &= 3.40V \end{aligned}$$

Case 3: $V_i = 5V$

First, check if the transistor is in the **Triode region**:

$$V_o > (V_i - V_t) = 5 - 1.4 = 3.6V$$

Since our initial saturation estimate gave $V_o < 3.6V$, the NMOS is likely in the **Triode region**. Using the Triode equation:

$$I_D = \mu_n C_{ox} \frac{W}{L} n \left[(V_i - V_t)V_o - \frac{V_o^2}{2} \right]$$

Applying Ohm's Law $I_D = \frac{V_{DD}-V_o}{R_D}$, we solve for V_o . The exact solution requires solving:

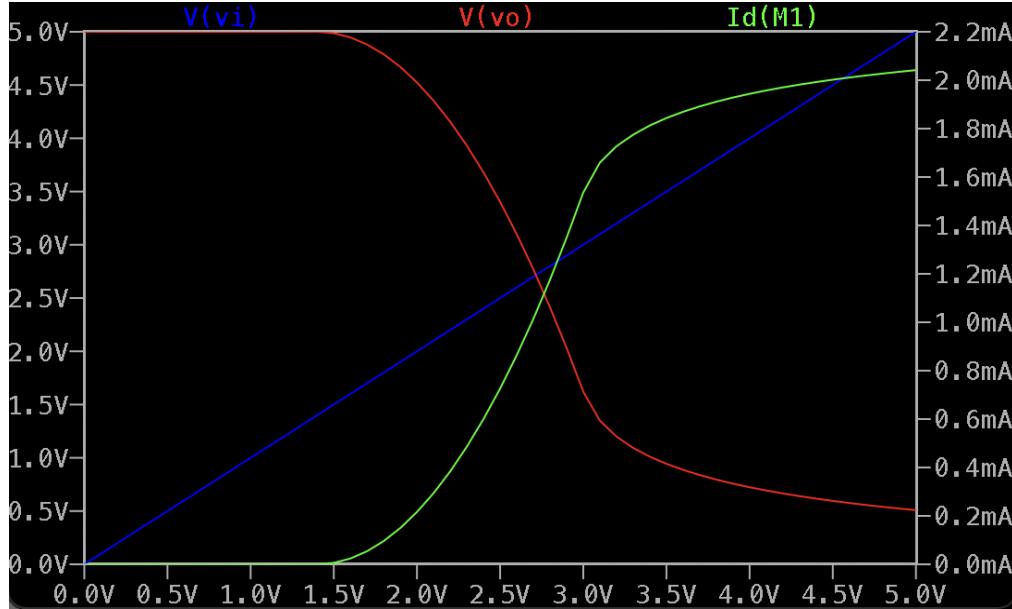
$$1.2 \left[(5 - 1.4)V_o - \frac{V_o^2}{2} \right] = \frac{5 - V_o}{2.2}$$

Simulation

For this experiment, use the **MbreakN4** NMOS model from the BREAKOUT library. To add the correct parameters to the model, please refer to the setup steps given at the **end of this document**. Sweep the input voltage from 0V to 5V and create a v_o vs. v_i plot (v_o on the 'y-axis'). The plot should show you the transfer characteristics of the inverter circuit.

Important note: In this lab, always connect the body (middle pin) of PMOS to V_{DD} , and always connect the body of NMOS to the ground.

- (a) Take a screenshot of the transfer function and on the screenshot, make sure to show v_i and v_o axes clearly. Identify regions in which MOS is in the cut-off, Triode, and Saturation regions.

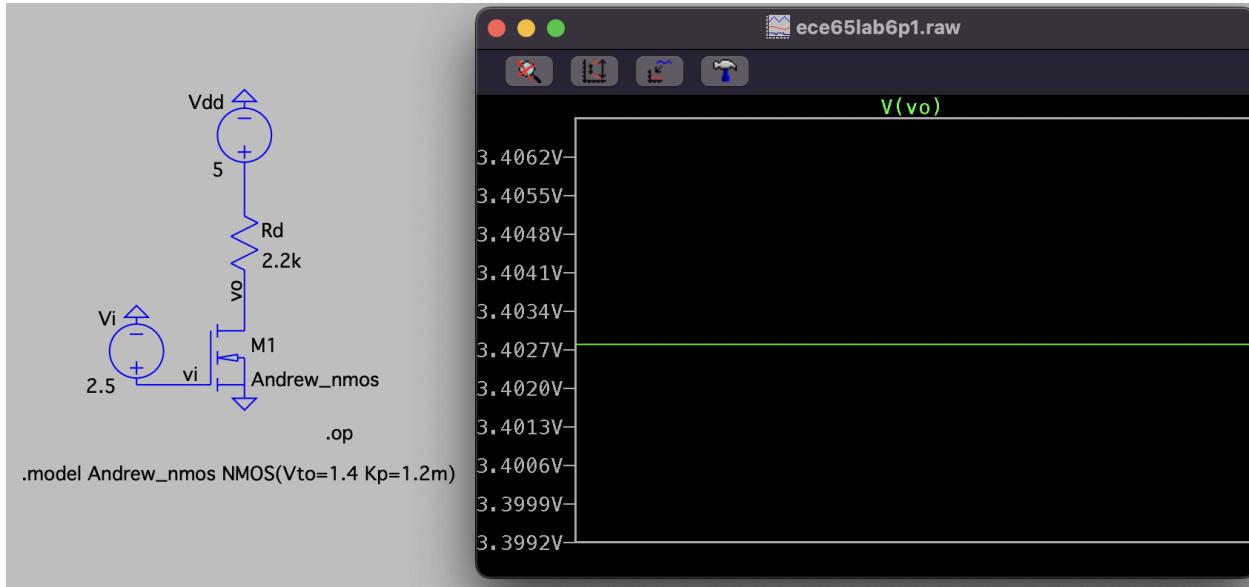


In the **Cutoff Region** ($V_i < 1.4V$), the NMOS transistor is **OFF** because the gate voltage is too low to turn it on. As a result, no current flows through the device, and the **output voltage (V_o) remains at $V_{DD} = 5V$** .

In the **Saturation Region** ($1.4V < V_i < 3.5V$), the NMOS transistor is **ON** and acts as a current source. As the input voltage increases, the **output voltage (V_o) gradually decreases**, showing the characteristic transition of the inverter.

In the **Triode Region** ($V_i > 3.5V$), the NMOS transistor is **fully ON** and behaves like a **low-resistance switch**. In this state, the **output voltage (V_o) drops sharply toward 0V**, completing the inversion process.

- (b) Find v_o for $v_i = 2.5$ and 5 V using Bias Point Analysis. In each case, solve the MOS circuit and find the value of the parameter $\mu_n C_{ox} (W/L)_n$.



Case 1: $V_i = 2.5V$ (Saturation Region)

Since $V_t = 1.4V$, and $V_i > V_t$, the NMOS is ON. To verify that it is in saturation:

$$V_o > (V_i - V_t) = 2.5V - 1.4V = 1.1V$$

Since $V_o = 3.4V$ (from simulation) satisfies this condition, the NMOS is in saturation. The drain current is given by:

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} n (V_i - V_t)^2$$

Using Ohm's Law:

$$I_D = \frac{V_{DD} - V_o}{R_D} = \frac{5V - 3.4V}{2.2k\Omega}$$

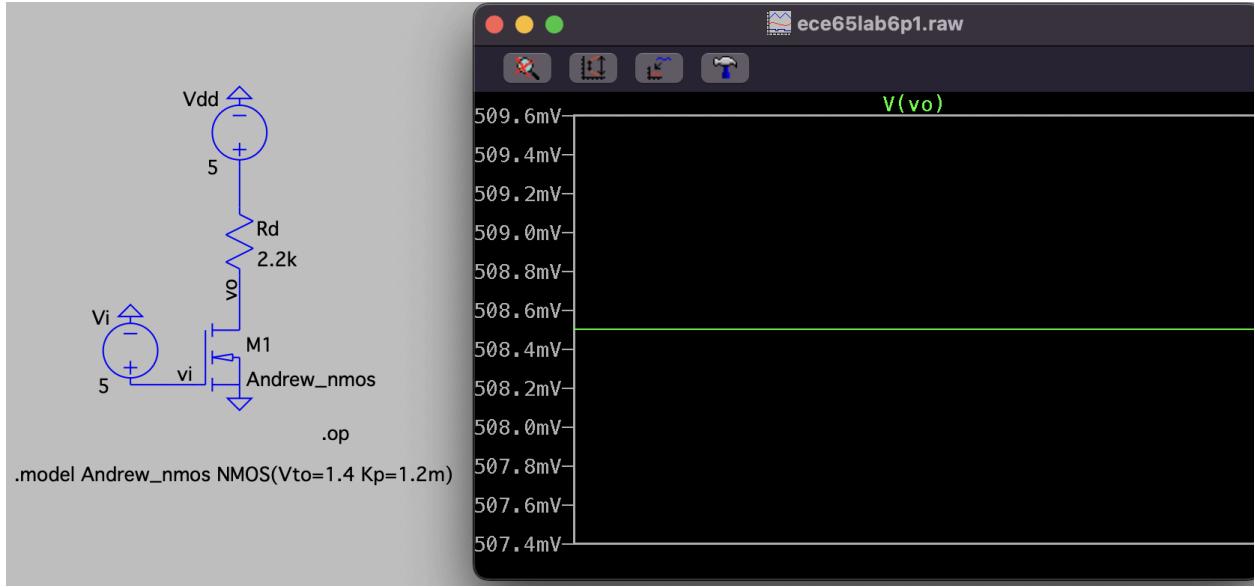
$$I_D = \frac{1.6V}{2200\Omega} = 0.000727A = 0.727mA$$

Solving for $\mu_n C_{ox} \frac{W}{L} n$:

$$0.727mA = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} n (1.1V)^2$$

$$0.727mA = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} n (1.21)$$

$$\mu_n C_{ox} \frac{W}{L} n = \frac{2 \times 0.727mA}{1.21} = \frac{1.454}{1.21} \approx 1.2mA/V^2$$



Case 2: $V_i = 5V$ (Triode Region)

Checking the MOSFET region:

$$V_o < (V_i - V_t) = 5V - 1.4V = 3.6V$$

Since $V_o = 0.5085V$ (from simulation) satisfies this condition, the NMOS is in triode mode. The drain current in the triode region is given by:

$$I_D = \mu_n C_{ox} \frac{W}{L_n} \left[(V_i - V_t)V_o - \frac{V_o^2}{2} \right]$$

Using Ohm's Law:

$$I_D = \frac{V_{DD} - V_o}{R_D} = \frac{5V - 0.5085V}{2.2k\Omega}$$

$$I_D = \frac{4.4915V}{2200\Omega} = 0.002041A = 2.041mA$$

Solving for $\mu_n C_{ox} \frac{W}{L_n}$:

$$2.041mA = \mu_n C_{ox} \frac{W}{L_n} \left[(5V - 1.4V)(0.5085V) - \frac{(0.5085V)^2}{2} \right]$$

$$2.041mA = \mu_n C_{ox} \frac{W}{L_n} \left[(3.6V)(0.5085V) - \frac{(0.5085V)^2}{2} \right]$$

$$2.041mA = \mu_n C_{ox} \frac{W}{L_n} (1.8306V - 0.1293V)$$

$$2.041mA = \mu_n C_{ox} \frac{W}{L_n} (1.7013V)$$

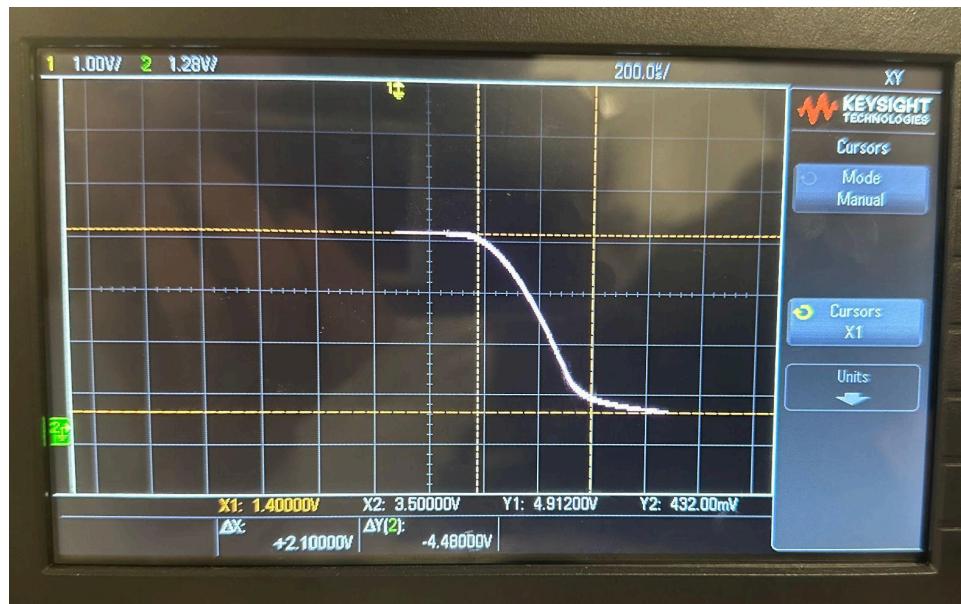
$$\mu_n C_{ox} \frac{W}{L_n} = \frac{2.041mA}{1.7013V} \approx 1.2mA/V^2$$

For both saturation ($V_i = 2.5V$) and triode ($V_i = 5V$) cases, the calculated value of $\mu_n C_{ox} \frac{W}{L_n}$ is approximately 1.2 mA/V^2 , which matches the given parameter in the lab. This validates the theoretical and simulation results.

Lab Exercise:

For this experiment, use the NMOS inverter that is attached to pins 6, 7, and 8. Assemble the circuit on the protoboard. Set up the function generator to produce a triangular wave with a peak-to-peak amplitude of 5 V and a DC offset of 2.5 V, similar to experiment 1. Attach scope channel A to the input and channel B to the output of the gate. Set the scope display to XY mode. You should see the transfer characteristics of the inverter circuit on the scope display.

- (a) Make a hard copy of the transfer function (you can take a photo of the oscilloscope screen) and on the hard copy, draw v_i and v_o axes and label and mark the voltage scales. Identify regions in which MOS is in Cut-off, Triode, and Saturation regions.



Cursors are at 1.4 V and 3.5V which mark the change from the Cut-off, Triode, Saturation, regions, backing up our calculations in the prelab. The axes are the same as simulation part 1.

- (b) Measure v_o for $v_i = 2.5$ and 5 V. In each case, solve the MOS circuit and find the value of the parameter $\mu_n C_{ox} (W/L)_n$.

$$v_i = 5V \quad 0.520 \text{ V}$$

$$v_i = 2.5V \quad 3.854 \text{ V}$$

Case 1: $V_i = 2.5V$ (Saturation Region)

Since $V_t = 1.4V$, and $V_i > V_t$, the NMOS is ON. To verify that it is in saturation:

$$V_o > (V_i - V_t) = 2.5V - 1.4V = 1.1V$$

Since $V_o = 3.854V$ (from real measurements) satisfies this condition, the NMOS is in saturation. The drain current is given by:

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L_n} (V_i - V_t)^2$$

Using Ohm's Law:

$$I_D = \frac{V_{DD} - V_o}{R_D} = \frac{5V - 3.854V}{100\Omega}$$

$$I_D = \frac{1.146V}{100\Omega} = 0.01146A = 11.46mA$$

Solving for $\mu_n C_{ox} \frac{W}{L_n}$:

$$11.46mA = \frac{1}{2} \mu_n C_{ox} \frac{W}{L_n} (1.1V)^2$$

$$11.46mA = \frac{1}{2} \mu_n C_{ox} \frac{W}{L_n} (1.21)$$

$$\mu_n C_{ox} \frac{W}{L_n} = \frac{2 \times 11.46mA}{1.21} = \frac{22.92}{1.21} \approx 18.95mA/V^2$$

Case 2: $V_i = 5V$ (Triode Region)

Checking the MOSFET region:

$$V_o < (V_i - V_t) = 5V - 1.4V = 3.6V$$

Since $V_o = 0.520V$ (from real measurements) satisfies this condition, the NMOS is in triode mode. The drain current in the triode region is given by:

$$I_D = \mu_n C_{ox} \frac{W}{L_n} \left[(V_i - V_t)V_o - \frac{V_o^2}{2} \right]$$

Using Ohm's Law:

$$I_D = \frac{V_{DD} - V_o}{R_D} = \frac{5V - 0.520V}{100\Omega}$$

$$I_D = \frac{4.480V}{100\Omega} = 0.0448A = 44.8mA$$

Solving for $\mu_n C_{ox} \frac{W}{L_n}$:

$$44.8mA = \mu_n C_{ox} \frac{W}{L_n} \left[(5V - 1.4V)(0.520V) - \frac{(0.520V)^2}{2} \right]$$

$$44.8mA = \mu_n C_{ox} \frac{W}{L_n} \left[(3.6V)(0.520V) - \frac{(0.520V)^2}{2} \right]$$

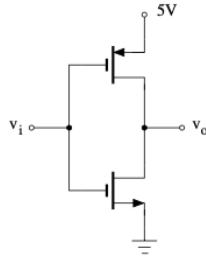
$$44.8mA = \mu_n C_{ox} \frac{W}{L_n} (1.872V - 0.1352V)$$

$$44.8mA = \mu_n C_{ox} \frac{W}{L_n} (1.7368V)$$

$$\mu_n C_{ox} \frac{W}{L_n} = \frac{44.8mA}{1.7368V} \approx 25.8mA/V^2$$

For both saturation ($V_i = 2.5V$) and triode ($V_i = 5V$) cases, the calculated value of $\mu_n C_{ox} \frac{W}{L_n}$ is approximately **18.95 mA/V²** and **25.8 mA/V²**, respectively. These values reflect real-world measurements and deviations from ideal theoretical predictions due to process variations and measurement tolerances.

Experiment 2: CMOS Inverter



Circuit Analysis

Calculate the value of i_D for $v_i = 2.5$ V. Use $\mu_n C_{ox} (W/L)_n = \mu_p C_{ox} (W/L)_p = 1.2$ mA/V² and, $\lambda = 0$, $V_t = 1.4V$ for your calculations..

Since $V_i = 2.5V$ is between V_{DD} and ground, both transistors operate in saturation mode.

NMOS Current in Saturation

For NMOS:

$$I_{D_n} = \frac{1}{2} \mu_n C_{ox} \frac{W}{L_n} (V_i - V_t)^2$$

Substituting values:

$$\begin{aligned} I_{D_n} &= \frac{1}{2} (1.2)(2.5 - 1.4)^2 \\ &= \frac{1}{2} (1.2)(1.1)^2 \\ &= \frac{1}{2} (1.2)(1.21) \\ &= \frac{1.452}{2} \\ &= 0.726 \text{ mA} \end{aligned}$$

PMOS Current in Saturation

For PMOS:

$$I_{D_p} = \frac{1}{2} \mu_p C_{ox} \frac{W}{L_p} (V_{SG} - V_t)^2$$

Since $V_{SG} = V_{DD} - V_i = 5V - 2.5V = 2.5V$:

$$\begin{aligned} I_{D_p} &= \frac{1}{2} (1.2)(2.5 - 1.4)^2 \\ &= 0.726 \text{ mA} \end{aligned}$$

Final Drain Current

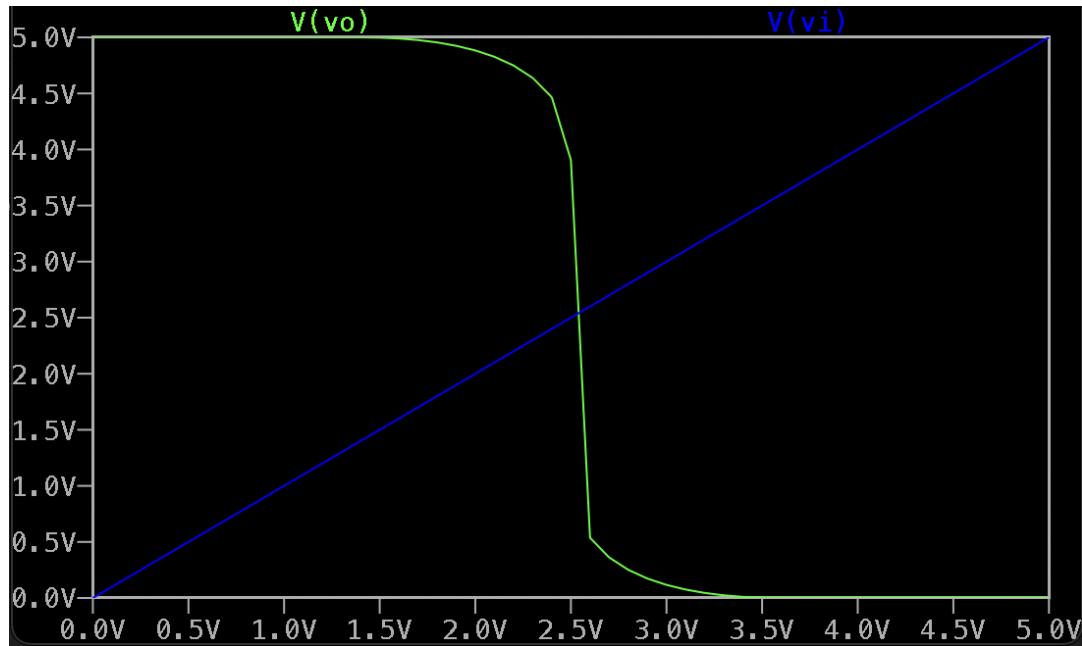
Since in steady-state operation $I_{D_n} = I_{D_p}$:

$$I_D = 0.726 \text{ mA}$$

Simulation

For this experiment, use MbreakN4 and MbreakP4 for NMOS and PMOS, respectively. Assemble the circuit as if you were using the schematic on the first page. (Make sure to connect the NMOS body to the ground and the PMOS body to VDD) As in experiment 1, sweep the input voltage from 0V to 5V and create a v_o vs. v_i plot (v_o on the 'y-axis'). The plot should show you the transfer characteristics of the inverter circuit.

- (a) Take a screenshot of the transfer function and on the screenshot, make sure to show v_i and v_o axes clearly. Identify regions in which MOS is in the cut-off, Triode, and Saturation regions.

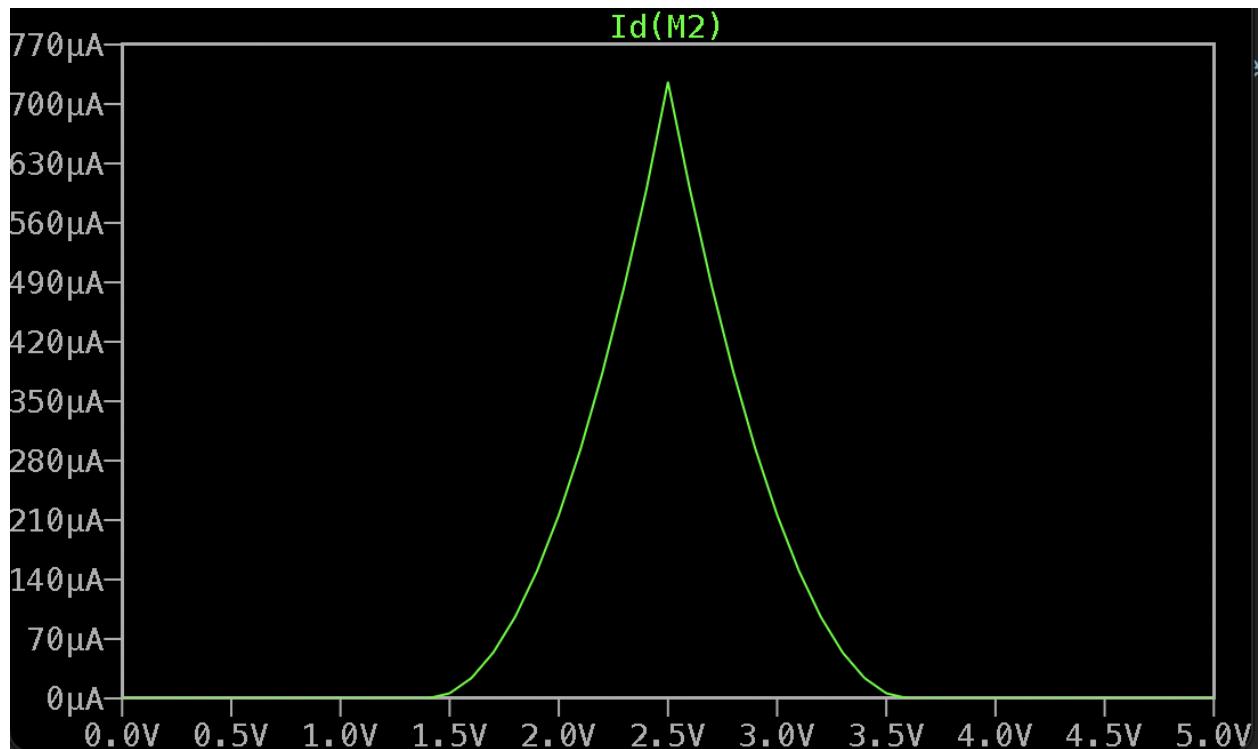


When $V_i = 0V$ (LOW input), the NMOS transistor is **OFF**, and the PMOS transistor is **ON**. Since the PMOS is conducting, it pulls the **output voltage** (V_o) to $V_{DD} = 5V$, producing a logic HIGH output.

When $V_i = 5V$ (HIGH input), the NMOS transistor is **ON**, and the PMOS transistor is **OFF**. The NMOS conducts and pulls the **output voltage** (V_o) to **0V**, creating a logic LOW output.

When $V_i = 2.5V$ (Mid-level input), both transistors are **partially ON**, allowing current to flow through both NMOS and PMOS transistors. This results in a voltage in the range of approximately $2V - 3V$ at the output, depending on the relative drive strengths of the NMOS and PMOS transistors.

- (b) A major advantage of a CMOS inverter is that it draws zero current when it is in the high or low state. However, the drain current is not zero when CMOS is transitioning between states. To see this, plot i_D vs v_i . Take a screenshot and on the screenshot, make sure to show the v_i and i_D axes clearly.



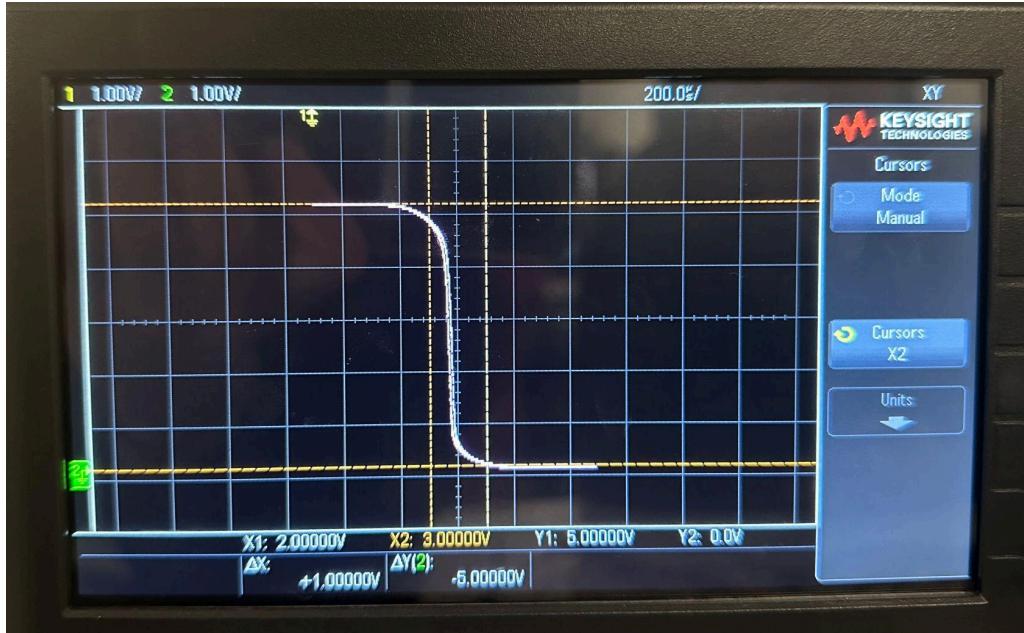
- (c) Compare the maximum values of i_D with your calculations.

Our simulation is consistent with our calculations.

Lab Exercise:

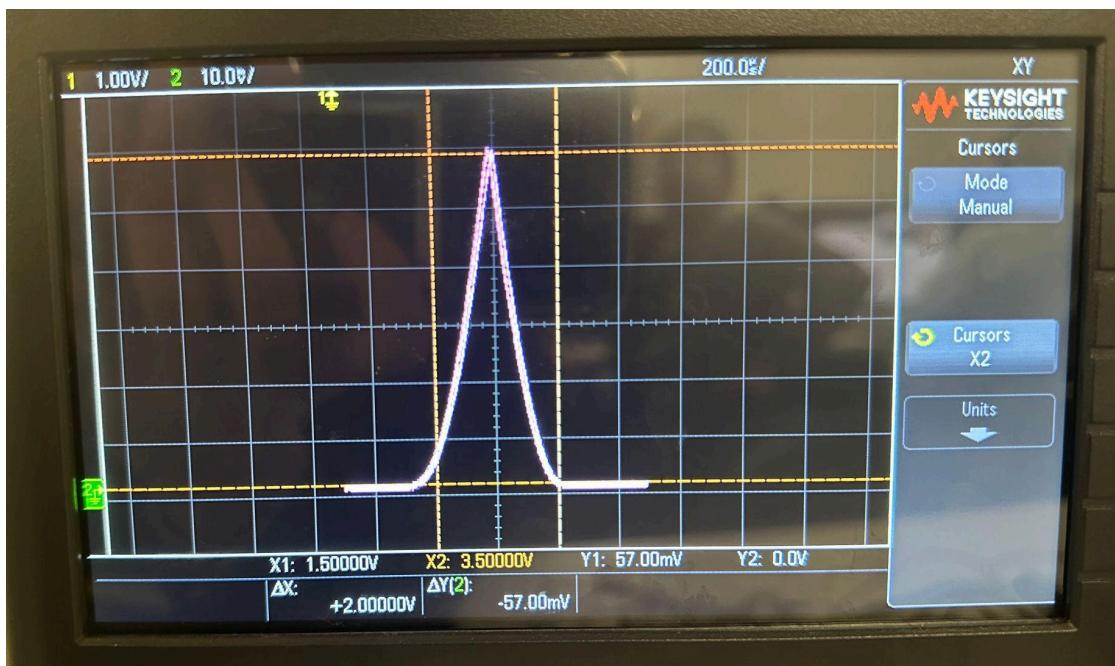
For this experiment, use the CMOS inverter that is attached to pins 9 through 12. Assemble the circuit on the protoboard. As in experiment 1, set up the function generator to produce a triangular wave with a peak-to-peak amplitude of 5 V and a DC offset of 2.5 V. Apply this signal to the input of the gate. Attach the scope channel A to the input and scope channel B to the output. Set the scope display to XY mode. You should see the transfer characteristics of the inverter circuit on the scope display.

- (a) Make a hard copy of the transfer function and on the hard copy, draw V_i and V_o axes and label and mark the voltage scales.



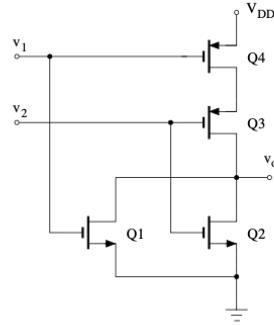
The cursors on the screen mark 2 and 3V respectively on the x-axis, and 0 and 5V on the y-axis. The graph we get is consistent with the one we get in the simulation in prelab.

(b) A major advantage of a CMOS inverter is that it draws zero current when it is in the high or low state. However, the drain current is not zero when CMOS is transitioning between states. To see this, attach a 100Ω resistor between pin 9 and the ground. The voltage across this resistor will be proportional to the drain current. Apply the triangular wave above to the input of the gate. Attach scope channel A to the input and scope channel B to the 100Ω resistor. Set the scope display to XY mode. You should see a plot of i_D vs. v_i . Save a copy of the plot, and on the plot, draw the v_i and i_D axes and label and mark the voltage and current scales. Compare the maximum values of i_D with your calculations.



The cursors on the screen mark 1.5 and 3.5V respectively on the x-axis, and 0 and 57mV on the y-axis. The proportional current i_D would be 0.57 mA which is slightly less than what we calculated.

Experiment 3: CMOS NOR Gate



Circuit Analysis

Mathematically show that the circuit above acts as a NOR gate. Find V_o for each possible input case. (4 possible cases total) You need to show your calculations for each of the four cases.

Case 1: $V_1 = 0V, V_2 = 0V$

PMOS Behavior: Since both V_1 and V_2 are LOW, the source-to-gate voltage for both PMOS transistors is:

$$V_{SG3} = V_{SG4} = V_{DD} - V_1 = 5V - 0V = 5V$$

Since $V_{SG} > |V_t|$, both PMOS transistors $Q3$ and $Q4$ are ON, allowing current to flow from V_{DD} to V_o .

NMOS Behavior: Since both inputs are LOW, the gate-to-source voltage for both NMOS transistors is:

$$V_{GS1} = V_{GS2} = V_1 - 0V = 0V$$

Since $V_{GS} < V_t$, both NMOS transistors are OFF, preventing any current from flowing to ground.

Applying Kirchhoff's Current Law (KCL) at the output node:

$$I_{D3} + I_{D4} = 0$$

Since PMOS transistors are ON and NMOS transistors are OFF, the output is pulled to:

$$V_o = V_{DD} = 5V$$

Thus, $V_o = 5V$ (Logic HIGH).

Case 2: $V_1 = 0V, V_2 = 5V$

PMOS Behavior: Since $V_1 = 0V$, $Q4$ is ON. However, for $Q3$:

$$V_{SG3} = 5V - 5V = 0V$$

Since $V_{SG3} < |V_t|$, $Q3$ is OFF, breaking the conduction path from V_{DD} .

NMOS Behavior: Since $V_2 = 5V$, $Q2$ turns ON:

$$V_{GS2} = 5V - 0V = 5V$$

Since $V_{GS2} > V_t$, $Q2$ is ON, creating a direct path from V_o to ground.

Applying KCL at the output node:

$$I_{D2} = \frac{(V_o - 0V)}{R_{ON}}$$

Since NMOS is ON and PMOS does not provide a conduction path:

$$V_o = 0V$$

Thus, $V_o = 0V$ (Logic LOW).

Case 3: $V_1 = 5V, V_2 = 0V$

PMOS Behavior: Since $V_2 = 0V$, $Q3$ is ON. However, for $Q4$:

$$V_{SG4} = 5V - 5V = 0V$$

Since $V_{SG4} < |V_t|$, $Q4$ is OFF, breaking the conduction path from V_{DD} .

NMOS Behavior: Since $V_1 = 5V$, $Q1$ turns ON:

$$V_{GS1} = 5V - 0V = 5V$$

Since $V_{GS1} > V_t$, $Q1$ is ON, creating a direct path from V_o to ground.

Applying KCL at the output node:

$$I_{D1} = \frac{(V_o - 0V)}{R_{ON}}$$

Since NMOS is ON and PMOS does not provide a conduction path:

$$V_o = 0V$$

Thus, $V_o = 0V$ (Logic LOW).

Case 4: $V_1 = 5V, V_2 = 5V$

PMOS Behavior: Since both V_1 and V_2 are HIGH:

$$V_{SG3} = V_{SG4} = 5V - 5V = 0V$$

Since $V_{SG} < |V_t|$, both PMOS transistors $Q3$ and $Q4$ are OFF, preventing any conduction from V_{DD} .

NMOS Behavior: Since both inputs are HIGH, both NMOS transistors $Q1$ and $Q2$ are ON:

$$V_{GS1} = V_{GS2} = 5V - 0V = 5V$$

Since $V_{GS} > V_t$, both NMOS transistors create a direct path from V_o to ground.

Applying KCL at the output node:

$$I_{D1} + I_{D2} = \frac{(V_o - 0V)}{R_{ON}}$$

Since both NMOS are ON and both PMOS are OFF:

$$V_o = 0V$$

Thus, $V_o = 0V$ (Logic LOW).

Conclusion

From the four cases analyzed, the circuit exhibits the expected behavior of a CMOS NOR gate:

V_1	V_2	V_o
0	0	5V (HIGH)
0	1	0V (LOW)
1	0	0V (LOW)
1	1	0V (LOW)

Table 1: Truth table of CMOS NOR Gate

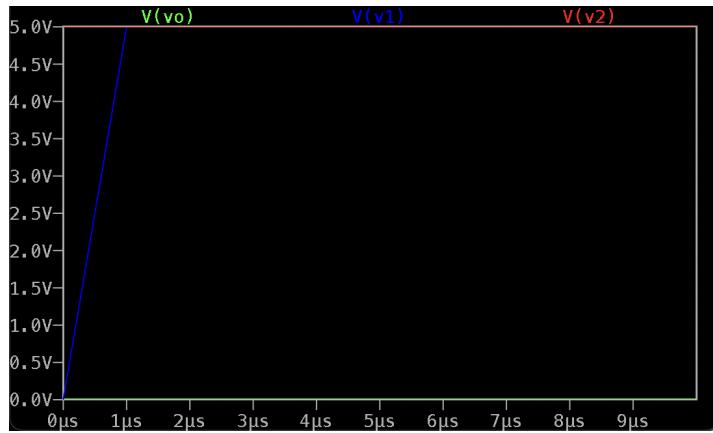
This confirms that the circuit functions as a NOR gate, where the output is HIGH only when both inputs are LOW.

Simulation

As in Experiment 2, use MbreaN4 and MbreaP4 for NMOS and PMOS, respectively. Assemble the circuit. Make sure to connect the NMOS bodies to the ground and the PMOS bodies to VDD. Use $VDD=5V$.

- (a) Test your NOR gate. Use a 1 kHz square wave (0-5 V) as v_1 (Using VPULSE). This will result in v_1 changing between 0V and 5V. Run the simulation twice, once with $v_2 = 5V$ and next with $v_2 = 0V$. In each case, run a Transient Time simulation and graph v_1 and v_o on the same plot for two periods. Attach the resulting plot to the lab report.

$$v_2 = 5V$$



$$v_2 = 0V$$

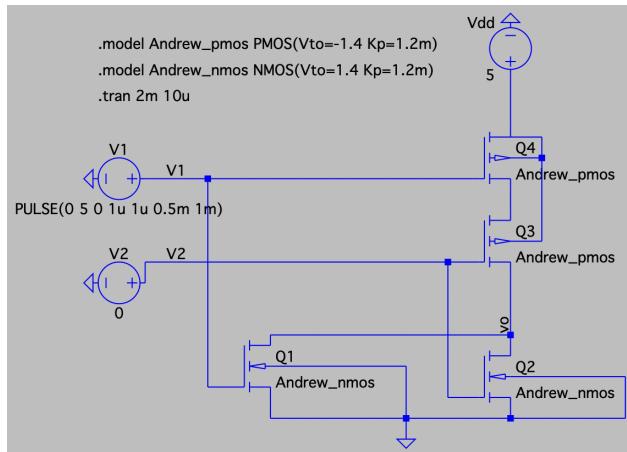


- (b) Describe the output waveform in each case and explain how it corresponds to the NOR of the two inputs using a truth table format.

We can see that the output waveforms correspond to our NOR in the truth table, as v_o is only high when both v_1 and v_2 are 0, and LOW everywhere else.

Lab Exercise:

For this experiment, use the CMOS inverter that is attached to pins 9 through 12 and MOS transistors with the gate connected to pin 6. Draw the circuit diagram NOR gate in your lab report and identify chip pins on the circuit diagram and explain which pins should be connected together. Wire your chip to make a two-input NOR gate. Test your NOR gate by attaching a 1 kHz square wave (0-5 V) to pin 6 and a DC voltage of A) zero and B) 5 V to pin 10. In each case, attach the waveform to the lab report. Describe the output waveform in each case and explain how it corresponds to the NOR of the two inputs, using a truth table format.



Pin Layout for Lab

V1: pin 6 (1 kHz square wave 0-5V, internally powers Q4, Q1)
 V2: pin 10 (DC 0V or 5V, internally powers Q3, Q2)
 pin 14 (5 Vdd)
 pin 13 into pin 11 (Q4 to Q3)
 pin 12 into pin 8 (Q3 to Q1, Q2 internally)
 pin 7 into GND

below we can see that the truth table holds true: we only get an output when both are 0 V.



5V DC

0V DC

PSpice Note: To properly set the characteristics of the simulated model, do the following:

1. Add both the MbreakN4 and MbreakP4 to your schematic
2. Select MbreakN4 and right-click on it
3. Select "Edit PSpice Model" and wait for the new window to pop up
4. Replace the text you see with ".Model Mbreakn NMOS(LEVEL=1, VTO=1.4, KP=1.2m)"
Make sure it didn't get copied over with a new line. (The safest way is to re-type it yourself.)
5. Repeat steps 1-4 for the PMOS and replace the text with ".Model Mbreakp PMOS(LEVEL=1, VTO=-1.4, KP=1.2m)

LTS spice Note: To properly set the characteristics of the simulated model, do the following:

1. Use **pmos4** and **nmos4** models for your NMOS and PMOS.
2. Add NMOS and/or PMOS to your schematic
3. For NMOS add: **.model YourFirstName_nmos NMOS(Vto=1.4 Kp=1.2m)**
4. For PMOS add: **.model YourFirstName_pmos PMOS(Vto=-1.4 Kp=1.2m)**
5. Rename each NMOS and PMOS to your "YourFirstName_nmos" and "YourFirstName_pmos" respectively. (Do not rename 'M1,M2,...', rename the part that says "NMOS" or "PMOS")

Conclusion

In this lab, we investigated the behavior of CMOS-based logic circuits, specifically focusing on NMOS inverters and CMOS NOR gates, analyzing their performance through both simulations and real-world measurements. By varying input voltages and observing output behavior, we identified the different operating regions of MOSFETs and their impact on logic gate functionality.

For the NMOS inverter, we confirmed that the transistor transitions between cutoff, saturation, and triode regions depending on the input voltage, affecting the output voltage accordingly. In the CMOS NOR gate, we demonstrated that the combination of PMOS and NMOS transistors correctly implements NOR logic, with the pull-up and pull-down networks controlling the output state. Real-world deviations from theoretical values were observed due to process variations, channel-length modulation, and component tolerances, affecting measured transistor parameters.

Overall, this lab demonstrated the practical implementation of CMOS logic circuits, validating their function as inverters and NOR gates. While simulations aligned well with theoretical expectations, experimental results highlighted real-world discrepancies, emphasizing the importance of considering non-ideal effects in circuit analysis and design.