Name: PID:

UNIVERSITY OF CALIFORNIA, SAN DIEGO

Electrical and Computer Engineering Department

ECE 65 – Spring 2019

Components and Circuits lab

Final Exam

Closed books, seven double-sided cheat sheets, and calculators are allowed

Electronic devices are not allowed.

Please put all answers in the answer sheets.

Write your name and PID on all pages.

Please do not begin until told. Show your work. Good luck.

All electronic devices including cell phones must be turned off and stored away in a backpack or a purse. Anyone caught with such a device on their person during the exam will be charged with academic dishonesty.

You can use the back of every page as a **scratch** paper.

The main pages are numbered. If you remove the staple, you should order the pages from page 1 to 16 and staple them before submitting your exam.

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Problem 1. (10 points)

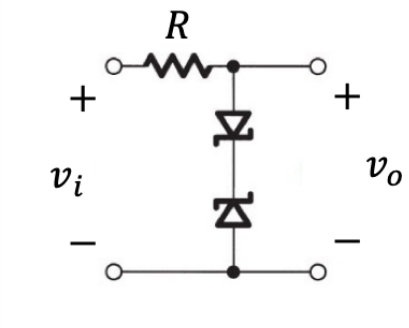
The diodes in the below circuit have $V_{D0} = 0.7\ V$, and $V_Z = 2.3\ V$.

a) Write the possible cases of the operation of the diodes.

b) For two of the possible cases, include the calculation of finding the relationship between v_o and v_i and the range of v_i for these two cases.

c) Sketch the output signal when $v_i = 4 \sin(\omega t)$.

Show your work.



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Problem 1.

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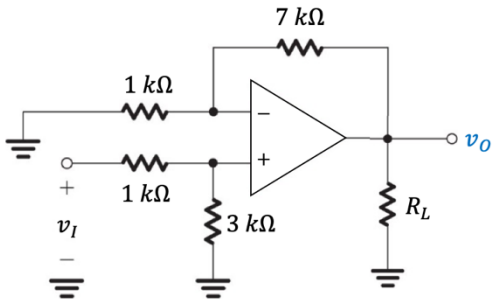
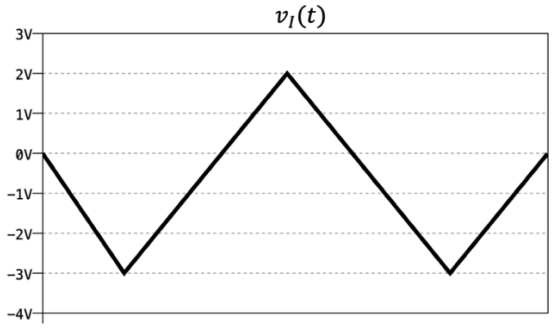
Problem 2. (12 points)

Assuming an ideal op-amp with $V_{sat} = \pm 16V$ and $I_{out_{max}} = \pm 25\ mA$ in the below circuit, answer the following questions.



a) **Find** (derive) an expression for the voltage gain. Assume $R_L = \infty$.

b) The input signal, $v_I(t)$ as shown below, is applied to the circuit. If $R_L = 1\ k\Omega$, **find** the output voltage and **sketch** it.



c) Assume a positive DC shift of 0.5 V is added to the above signal before applying it to the op-amp circuit.

i. Sketch the resulting input signal.

ii. With this new signal applied to the circuit, what is the lowest value of R_L that can be used to have an undistorted output voltage waveform?

iii. Design a diode waveform shaping circuit that can add the + 0.5 V DC shift to the signal given in part (b).

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Problem 2.

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Problem 2.

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Problem 2.

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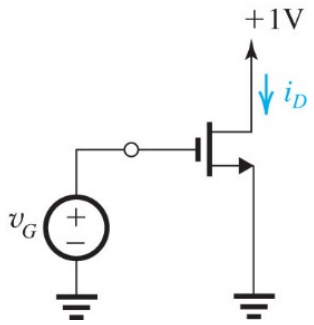
Problem 3. (6 points)

The NMOS in the below circuit has $V_t = 0.5\ V$ and $k_n = \mu_n C_{ox} \frac{W}{L} = 1\ mA/V^2$, and $\lambda = 0$.



a) Sketch (approximately) the graph of i_D vs v_G with v_G varying in the range of 0 to 2 V. Label your graph.

b) Write i_D equation(s) for the various portions of the resulting graph.

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Problem 3.

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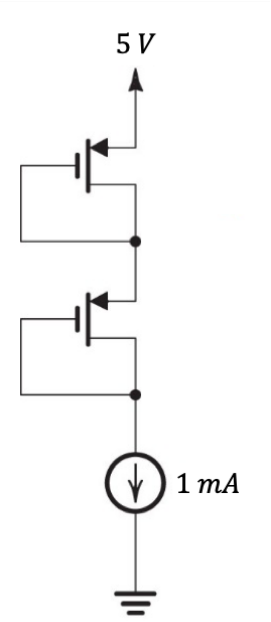
Problem 4. (10 points)

In the following circuit the transistors are characterized by $|V_t| = 1\ V$, $\mu\ C_{ox}\frac{W}{L} = 2\ mA/V^2$, and $\lambda = 0$.

a) Find the node voltages at the drain of both transistors.

b) Replace the current source with a resistor. Calculate the value of the resistor such that the current flowing through the resistor is equal to $1\ mA$.



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Problem 4.

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Problem 5. (12 points)

Answer the following questions for the below BJT amplifier circuit. Assume capacitors are short in the signal circuit. Use $V_T = 25\ mV$, $\beta = 100$, $V_{D0} = 0.7\ V$, and Ignore the early effect in the bias and signal circuits.

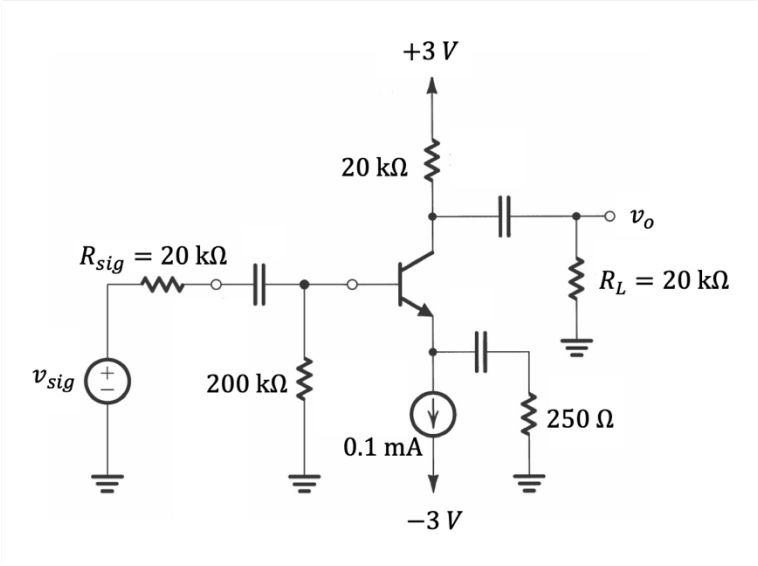
a) Find the Bias parameters of the amplifier circuit.

b) Find the small signal parameters of the amplifier.

c) Draw the small signal equivalent circuit.

d) Find the open loop voltage gain (A_{vo}), voltage gain (A_v), total circuit voltage gain (A), input resistance (R_i), and output resistance (R_o) of this circuit.

e) If the amplitude of the voltage signal at the base is to be limited to $10\ mV$, what is the largest amplitude of v_{sig}? What is the corresponding amplitude of the output voltage signal?



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Problem 5.

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