ECE 65 - *Components and Circuits lab*

Winter 2022

Midterm exam - Take-home test

You should submit your handwritten solutions in a PDF format to Gradescope by Sunday, 2/13, at 11:59 pm (Pacific Time).

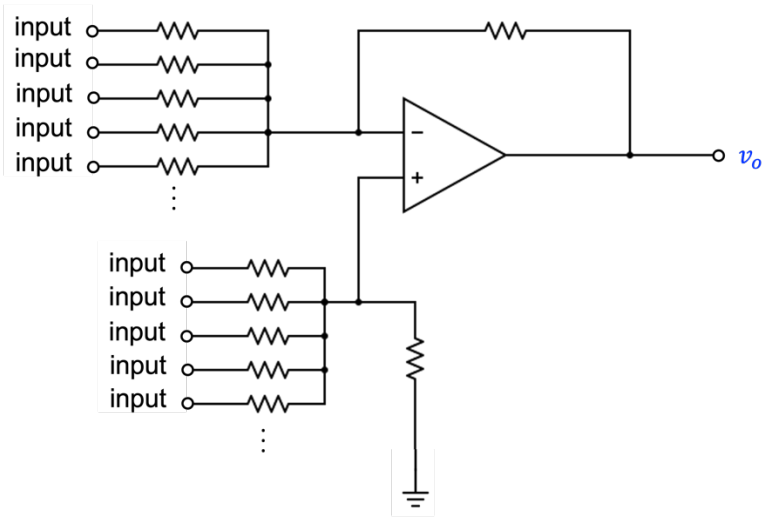
We recognize that final exams are stressful in the best of times, and this is an unusually hard time. Please remember that despite the stress, we are counting on you to uphold academic integrity while you complete your final exam. Regrettably, there have been instances in engineering classes this quarter where students have violated our principles of integrity by posting or seeking exam questions or answers online, or by consulting unauthorized resources. This is a gross violation of our principles of integrity and it will not be tolerated. To be fair to all students, I will report any integrity violations discovered during the final exam. Please make sure you understand and follow the academic integrity guidelines for the exam. An honest effort, no matter what the outcome, is something to be proud of, especially in these difficult times. Good luck on the exam. I am proud of your commitment and resilience in these difficult times.

Problem 1. (10 points)

Using the general structure of the op-amp circuit provided below, design an op-amp circuit that provides

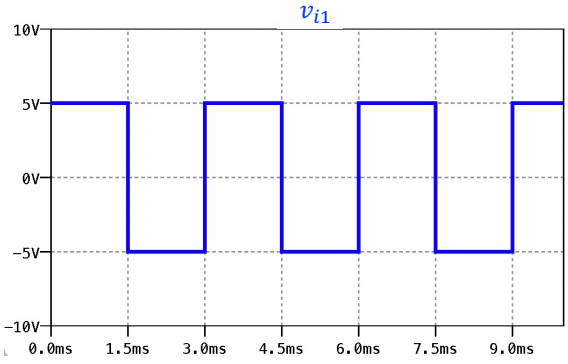
$$v_o = -5v_1 + v_2 + 3v_3$$

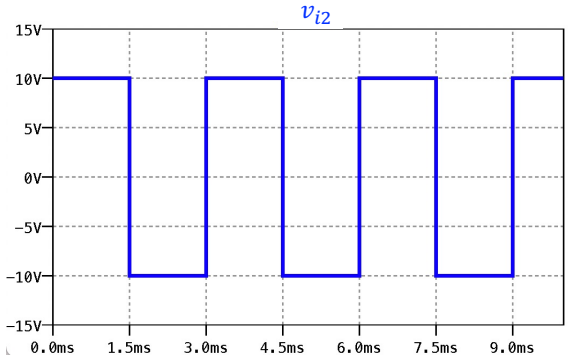
where v_1, v_2, and v_3 are the inputs. Assume ideal op-amps.

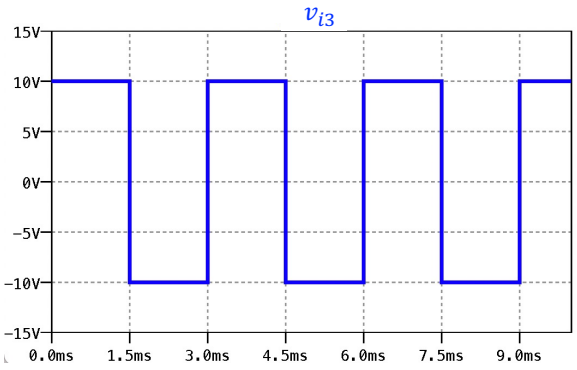


a. Draw your designed circuit and solve it to show that $v_o = -5v_1 + v_2 + 3v_3$.

b. If v_1, v_2, and v_3 are the signals shown below, sketch two cycles of $v_o(t)$. (a hand-drawn waveform is required.) Assume the op-amp is powered by $\pm 15\ V$ power supplies and assume $V_{sat} = \pm 13.5\ V$.







c. Simulate your designed circuit and plot $v_o(t)$ for 10 ms using the above v_1, v_2, and v_3 input signals. Use LF411 op-amps and $\pm 15V$ power supplies. Include the screenshots of your schematic and the output waveform in your submission.

Problem 2. (10 points)

Design a practical peak detector circuit to detect the peak amplitude of the input signal, $v_i = 0.3\sin(2\pi \times 100t)\ V$. (This is a sinusoidal signal with a peak amplitude of $V_P = 0.3\ V$). Assume $R_L = 100\ k\Omega$ (the resistor connected to the output node).

a. Choose a capacitor value such that after the first peak of the input signal, the output voltage does not go below 0.8 V_P. Show how you selected your capacitor value.

b. Draw your designed circuit.

c. Sketch the output waveform. An approximate graph is enough.

d. In a paragraph explain how your circuit works.

a. Simulate the circuit (use the circuit components you used in the ECE 65 labs) and plot the input and output waveforms for 100ms on the same graph. Include the screenshots of your schematic and waveforms in your submission.