# ECE 65: Components & Circuits Lab

Lecture 16

## CMOS NAND gates

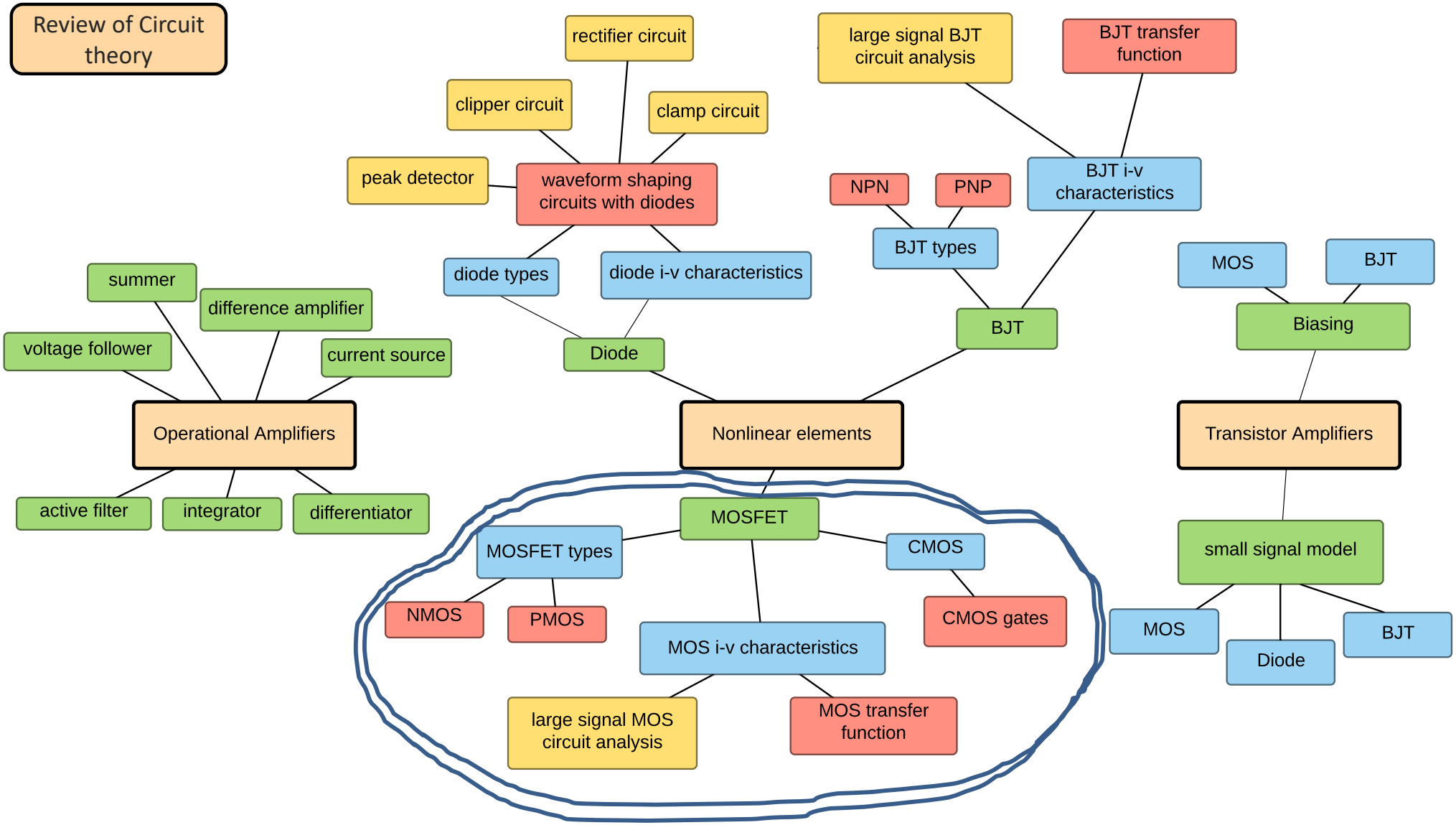
Reference notes: sections 4.4

Sedra & Smith (7th Ed): sections 5.1.8, 14.3

Saharnaz Baghdadchi

# Course map

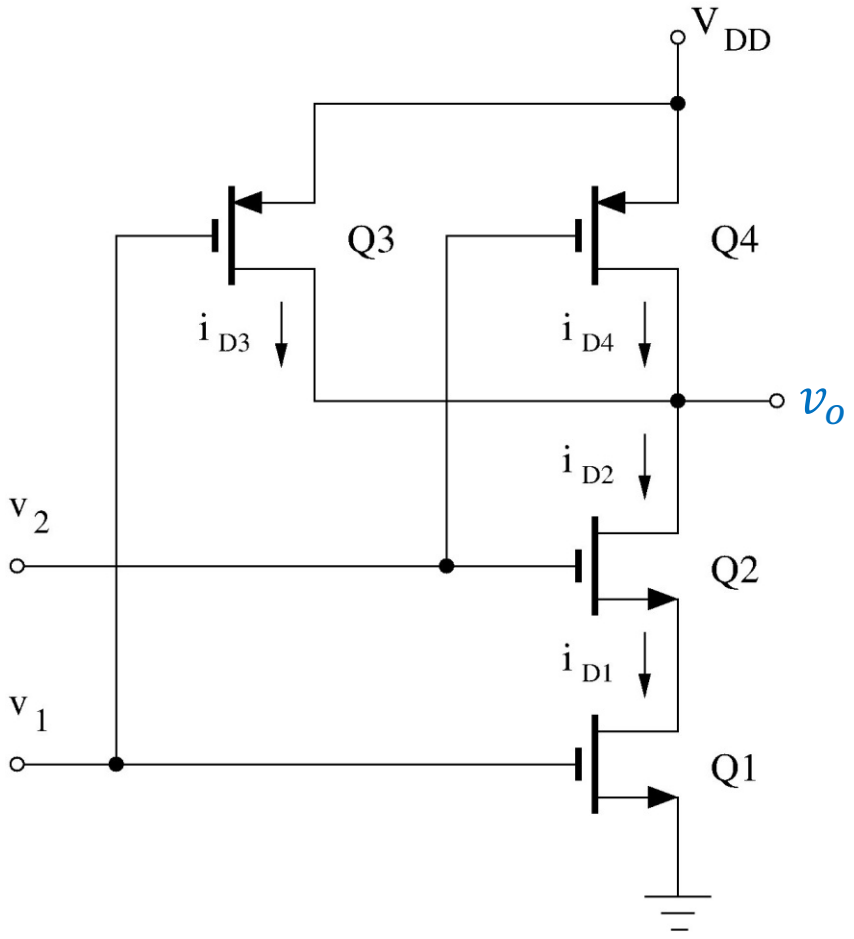
## 5. Metal Oxide Semiconductor Field Effect Transistor (MOSFET)



# CMOS NAND Gate

**Truth Table**

| | | |
|---|---|---|
| $v_1 = 0$ | $v_2 = 0$: | $v_o = V_{DD}$ |
| $v_1 = 0$ | $v_2 = V_{DD}$ : | $v_o = V_{DD}$ |
| $v_1 = V_{DD}$ | $v_2 = 0$ : | $v_o = V_{DD}$ |
| $v_1 = V_{DD}$ | $v_2 = V_{DD}$ : | $v_o = 0$ |



# Analysis of CMOS NAND Gate

GS1-KVL: $v_{GS1} = v_1$

GS2-KVL: $v_2 = v_{GS2} + v_{DS1}$

$\rightarrow \quad v_{GS2} = v_2 - v_{DS1}$

GS3-KVL: $V_{DD} = v_{SG3} + v_1$

$\rightarrow \quad v_{SG3} = V_{DD} - v_1$

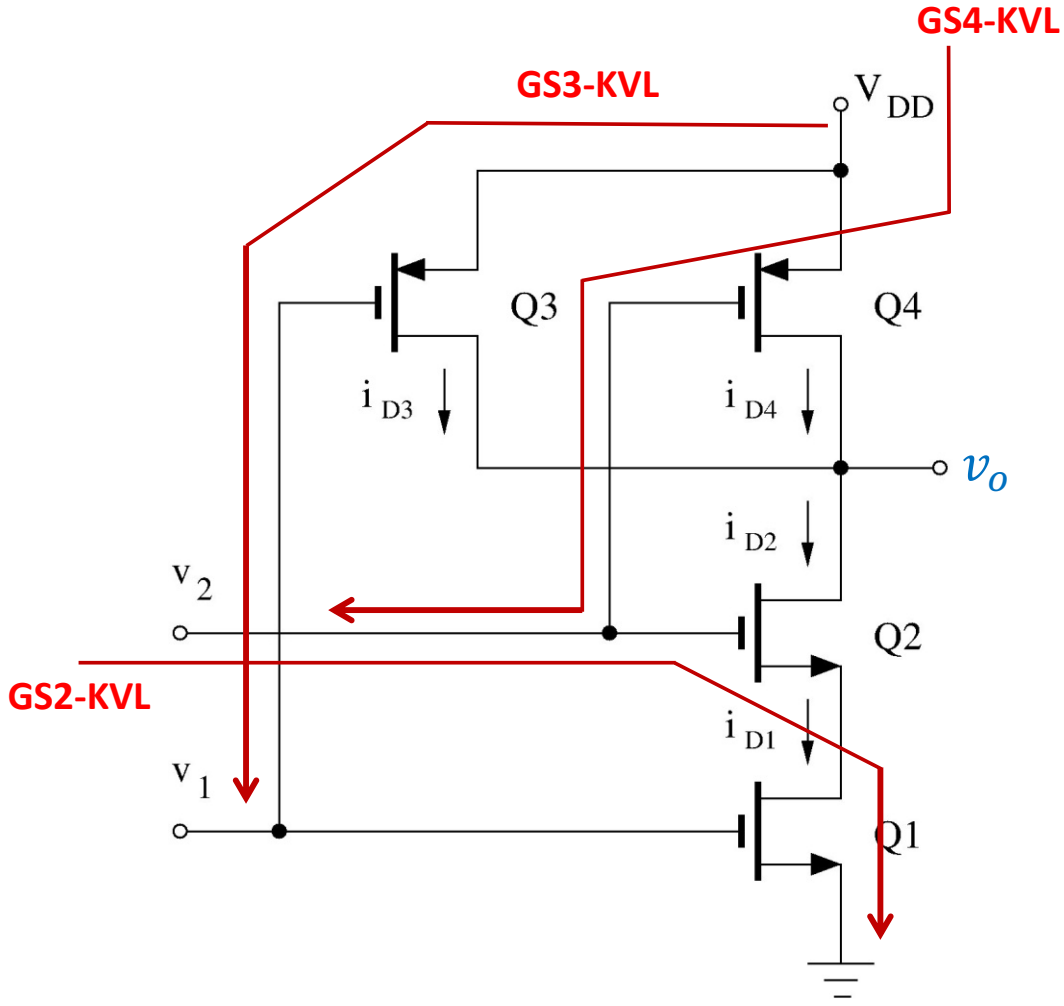
GS4-KVL: $V_{DD} = v_{SG4} + v_2$

$\rightarrow \quad v_{SG4} = V_{DD} - v_2$

DS-KVL: $V_{DD} = v_{SD4} + v_{DS2} + v_{DS1}$

$v_{SD3} = v_{SD4}$

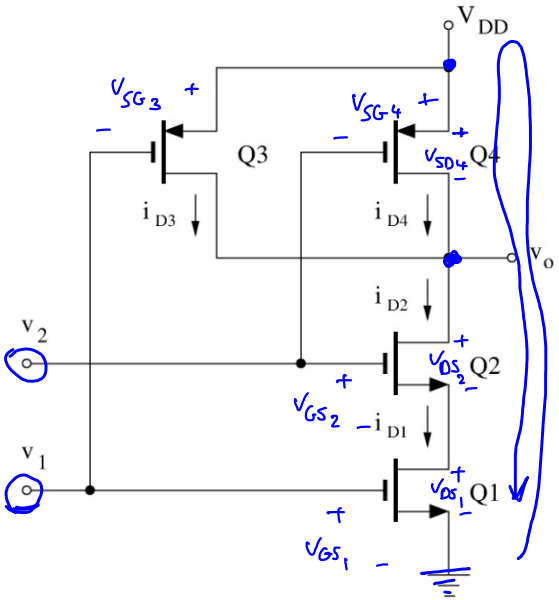
KCL: $i_{D1} = i_{D2} = i_{D3} + i_{D4}$




$v_o = v_{DS1} + v_{DS2}$

$v_o = V_{DD} - v_{SD4} = V_{DD} - v_{SD3}$

# Analysis of CMOS NAND Gate




**Case 1:** $v_1 = V_{DD}$ & $v_2 = 0$

$V_{GS_1} = V_1 = V_{DD} > V_{tn} \longrightarrow Q_1$ is ON

$V_{GS_2} = V_2 - V_{DS_1} = -V_{DS_1} < V_{tn} \longrightarrow Q_2$ is off $\longrightarrow i_{D_2} = 0$

$i_{D_1} = i_{D_2} = 0$

$\Longrightarrow Q_1$ is ON, $i_{D_1} = 0$ , $V_{DS_1} = 0$

$V_{SG_3} = V_{DD} - V_1 = 0 < |V_{tp}| \longrightarrow Q_3$ off $\longrightarrow i_{D_3} = 0$

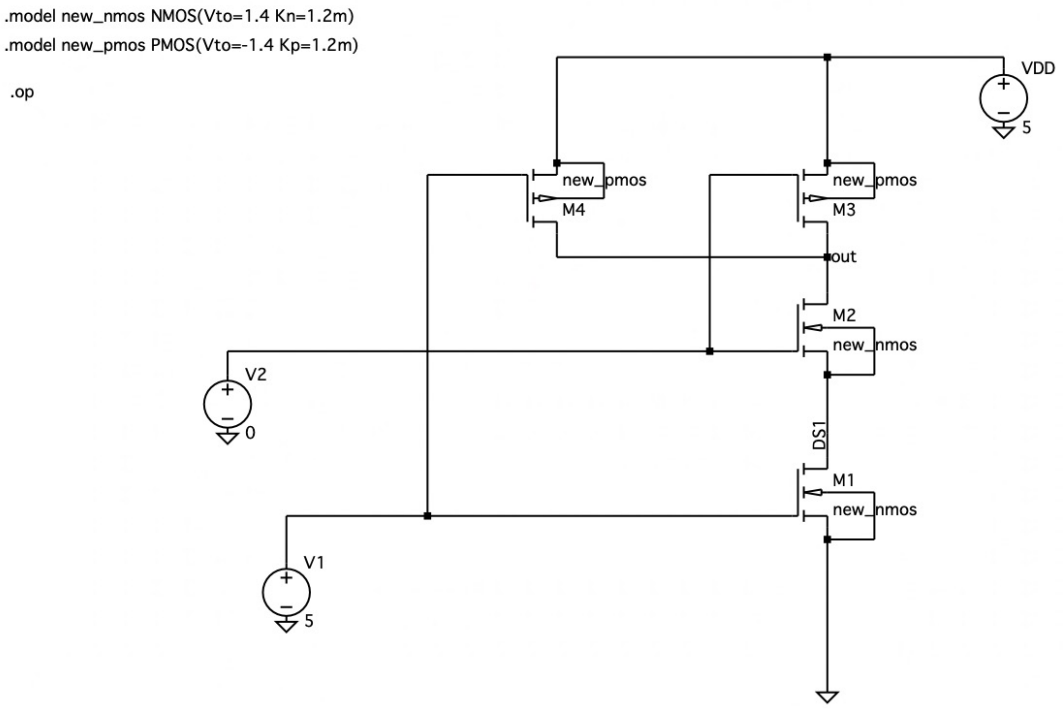
$V_{SG_4} = V_{DD} - V_2 = V_{DD} > |V_{tp}| \longrightarrow Q_4$ is ON

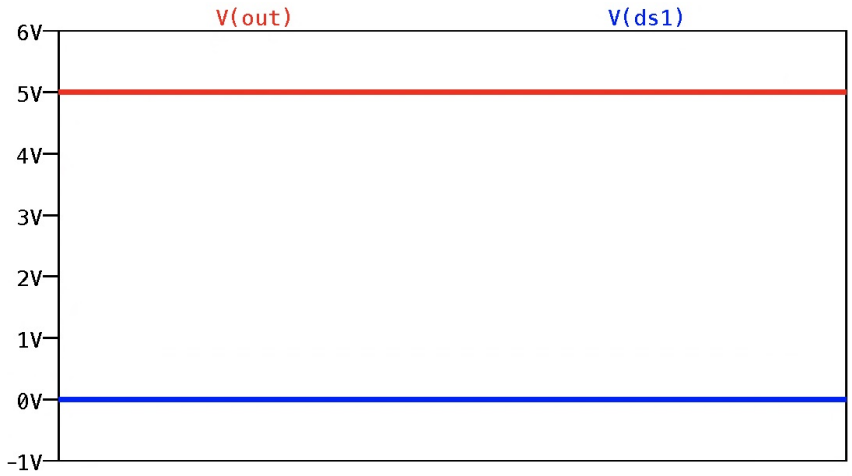
$i_{D_3} + i_{D_4} = i_{D_2} \longrightarrow i_{D_4} = 0$ , $Q_4$ is in Triode mode, $V_{SD_4} = 0$

$V_0 = V_{DD} - V_{SD_4} = V_{DD}$

# Analysis of CMOS NAND Gate

**Case 1:** $v_1 = V_{DD}$ & $v_2 = 0$



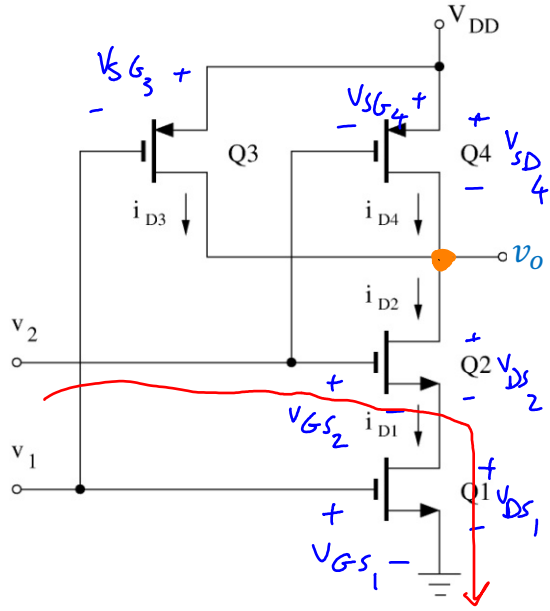



## Lecture 16 reading quiz

In the following two-input CMOS NAND gate, find the state of Q1 and Q4 when $v_1 = 0$ & $v_2 = 0$, and when $v_1 = 0$ & $v_2 = V_{DD}$ .

# Analysis of CMOS NAND Gate

**Case 2:** $v_1 = 0$ & $v_2 = 0$




$V_1 = V_{GS_1} = 0 \longrightarrow Q_1$ is off, $i_{D_1} = 0$

$GS_2$ KVL:

$V_{GS_2} = V_2 - V_{DS_1} = -V_{DS_1} < V_{tn} \longrightarrow Q_2$ is off, $i_{D_2} = 0$

For $Q_3$:

$SG_3$ KVL:

$V_{SG_3} = V_{DD} - V_1 = V_{DD} > |V_{tp}| \longrightarrow Q_3$ is ON, $i_{D_3} = 0 \longrightarrow V_{SD_3} = 0$

For $Q_4$:

KCL: $i_{D_3} + i_{D_4} = i_{D_2} = 0 \longrightarrow i_{D_3} = i_{D_4} = 0$

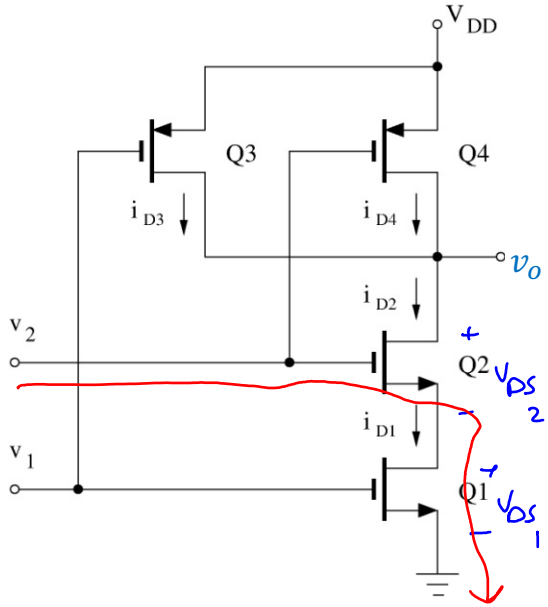
$SG_4$ KVL:

$V_{SG_4} = V_{DD} - V_2 = V_{DD} > |V_{tp}| \longrightarrow Q_4$ is ON, $i_{D_4} = 0 \longrightarrow V_{SD_4} = 0$

$\Rightarrow V_o = V_{DD}$

# Analysis of CMOS NAND Gate

**Case 2:** $v_1 = 0$ & $v_2 = 0$




Assume $Q_2$ is ON : $V_{GS_2} > V_{tn}$

$i_{D_2} = 0 \longrightarrow Q_2$ is in triode and, $V_{DS_2} = 0$

$\downarrow$

because $V_o = V_{DD} \longrightarrow V_{DS_1} = V_{DD}$

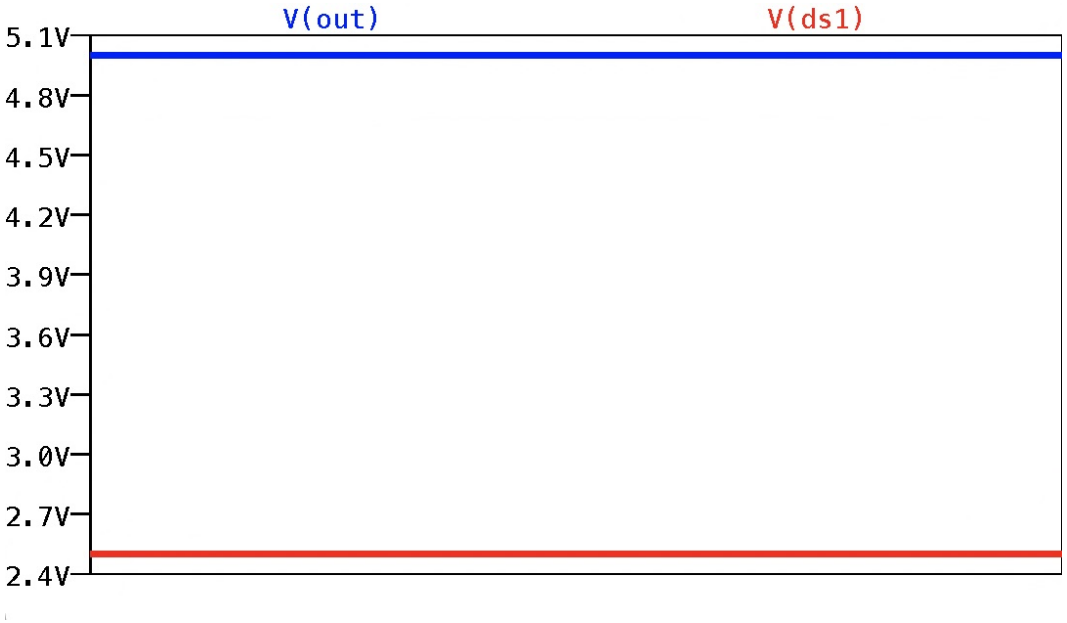
GS 2 KVL:

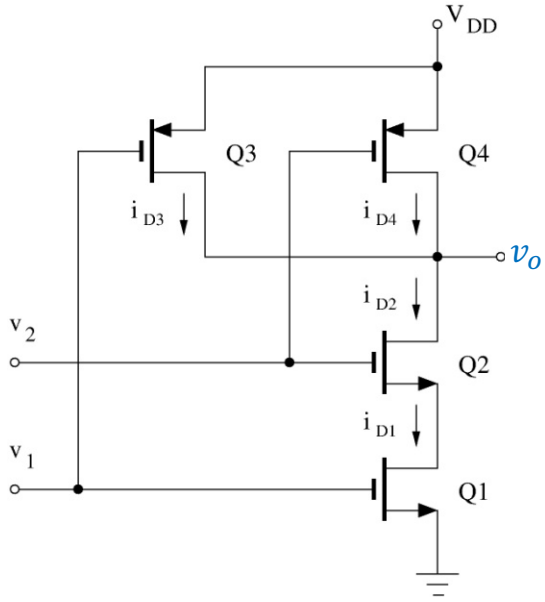
$V_{GS_2} = V_2 - V_{DS_1} = 0 - V_{DD} = -V_{DD} < V_{tn} \longrightarrow$ Assumption we not correct

$\Longrightarrow Q_2$ is off

# Analysis of CMOS NAND Gate

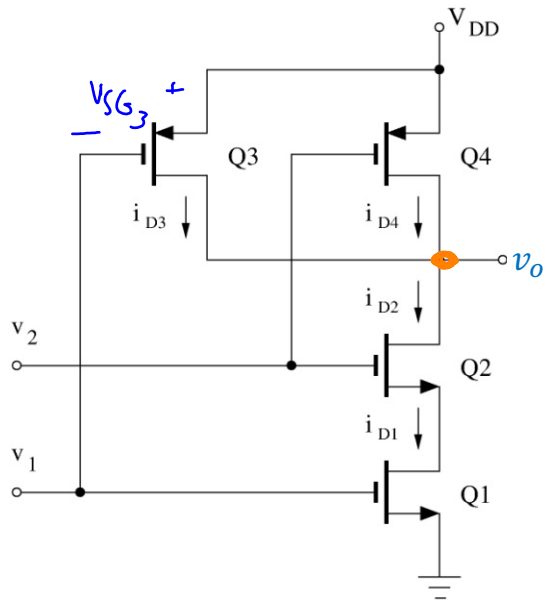
**Case 2:** $v_1 = 0$ & $v_2 = 0$



# Analysis of CMOS NAND Gate

**Case 3:** $v_1 = 0$ & $v_2 = V_{DD}$




$V_1 = V_{GS_1} = 0\ V \longrightarrow Q_1$ is off $\longrightarrow i_{D_1} = 0$

$V_{GS_2} = V_2 - V_{DS_1} = V_{DD} - V_{DS_1}$

$i_{D_2} = i_{D_1} = 0$

for $Q_3$:

$V_{SG_3} = V_{DD} - V_1 = V_{DD} > |V_{tp}| \longrightarrow Q_3$ is on, because $i_{D_3} = 0 \rightarrow Q_3$ is in triode

$\Rightarrow V_{SD_3} = 0$

for $Q_4$:

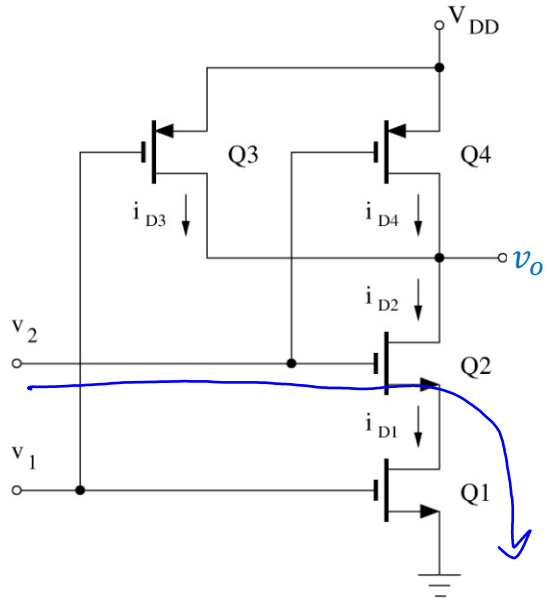
$V_{SG_4} = V_{DD} - V_2 = V_{DD} - V_{DD} = 0 < |V_{tp}| \longrightarrow Q_4$ is off $\longrightarrow i_{D_4} = 0$

KCL: $i_{D_3} + i_{D_4} = i_{D_2} = i_{D_1} = 0 \longrightarrow i_{D_3} = 0$

# Analysis of CMOS NAND Gate

**Case 3:** $v_1 = 0$ & $v_2 = V_{DD}$

$V_{SD_3} = 0 \longrightarrow V_o = V_{DD}$



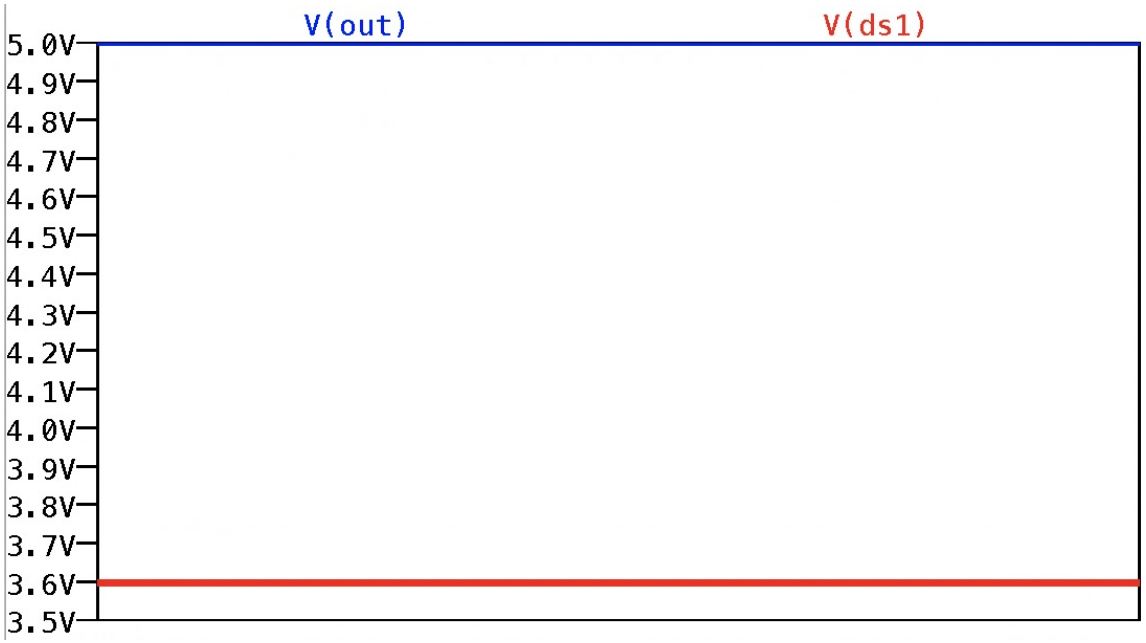

Assume $Q_2$ is ON $\longrightarrow V_{GS_2} > V_{tn}$

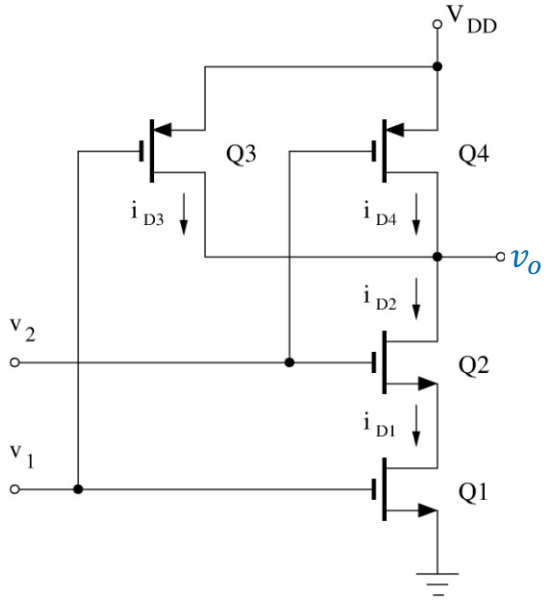
Since $i_{D_2} = 0 \longrightarrow V_{DS_2} = 0 \longrightarrow V_{DS_1} = V_{DD}$

$V_{GS_2} = V_2 - V_{DS_1} = V_{DD} - V_{DD} = 0 < V_{tn} \longrightarrow Q_2$ is off.

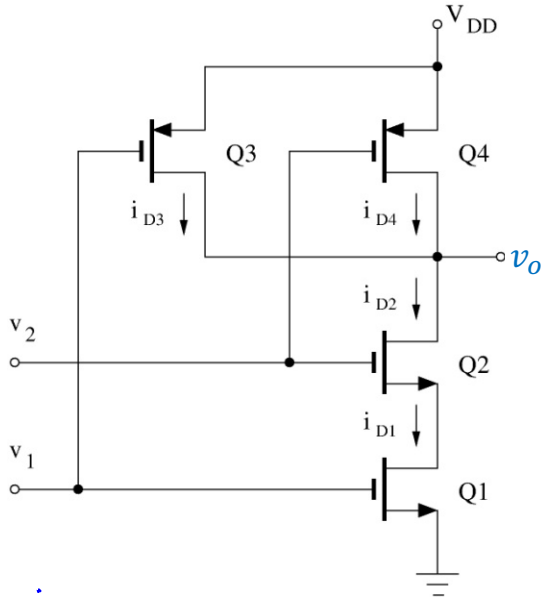
# Analysis of CMOS NAND Gate

**Case 3:** $v_1 = 0$ & $v_2 = V_{DD}$



# Analysis of CMOS NAND Gate




**Case 4:** $v_1 = V_{DD}$ & $v_2 = V_{DD}$

$V_1 = V_{GS_1} = V_{DD} > V_{tn} \longrightarrow Q_1$ is ON $\longrightarrow Q_1$ is in triode

$V_{DS_1} = 0$

$V_{GS_2} = V_2 - V_{DS_1} = V_{DD} - V_{DS_1} \longrightarrow Q_2$ is ON and in triode

$V_{DS_2} = 0$

$V_{SG_3} = V_{S_3} - V_{G_3} = V_{DD} - V_{DD} = 0 \longrightarrow Q_3$ is off $\longrightarrow i_{D_3} = 0$

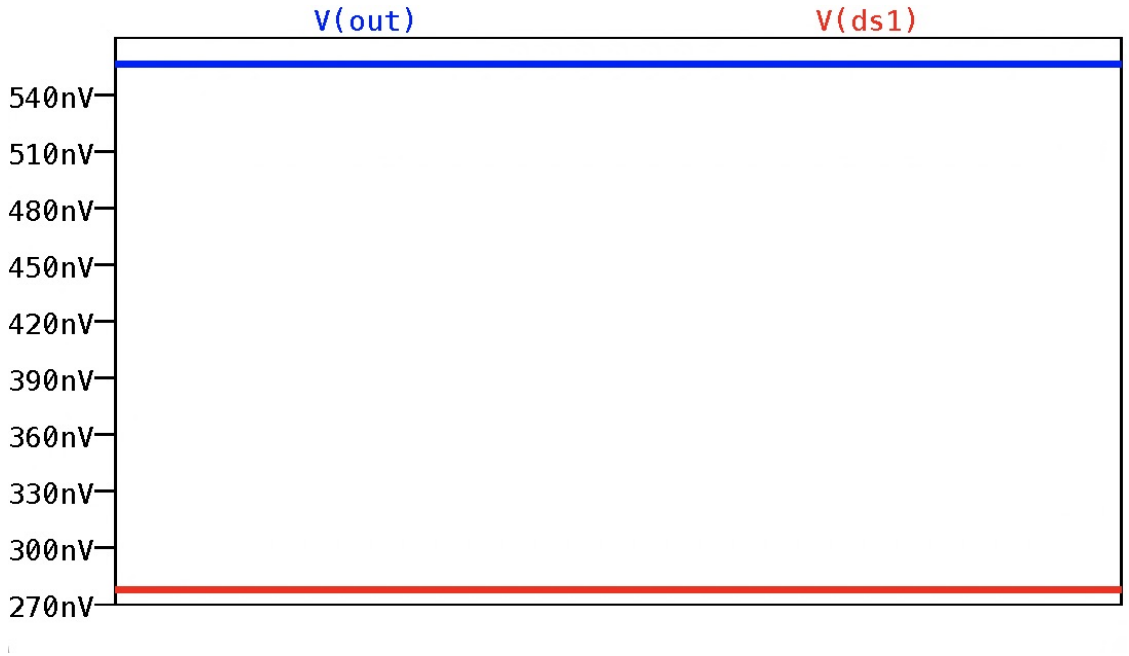
$V_{SG_4} = 0 \longrightarrow i_{D_4} = 0$

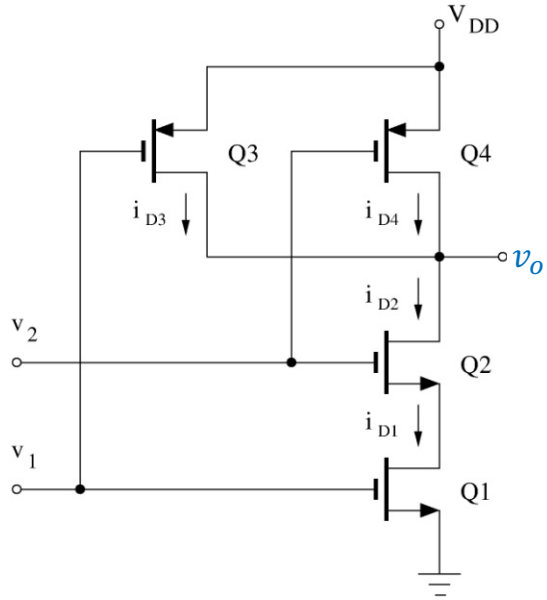
$i_{D_1} = i_{D_2} = i_{D_3} + i_{D_4} = 0 \longrightarrow i_{D_1} = 0, \; i_{D_2} = 0$

$V_0 = V_{DS_1} + V_{DS_2} = 0 \longrightarrow \boxed{V_0 = 0}$

# Analysis of CMOS NAND Gate

**Case 4:** $v_1 = V_{DD}$ & $v_2 = V_{DD}$



# Supplementary Discussion question 1.

Sketch a three input NAND gate using CMOS technology.

# Supplementary Discussion question 2

Sketch a three input NOR gate using CMOS technology.