

Name

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UNIVERSITY OF CALIFORNIA, SAN DIEGO

Electrical and Computer Engineering Department

ECE 65 – Fall 2021

Components and Circuits lab

Final Exam *Solutions*

Closed books, five double-sided cheat sheets, and calculators are allowed

Electronic devices are not allowed.

Please put all answers in the provided sheets.

Be sure to write your name and PID on **all pages**.

Please do not begin until told.

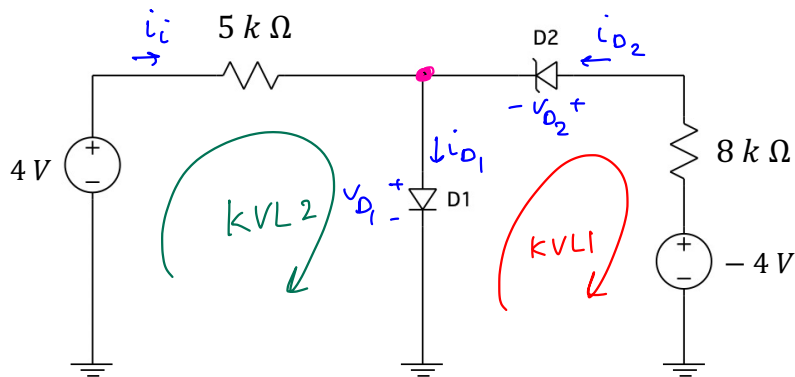
Show your work.

Good luck.

Problem 1. (5 points)

In the below circuit, can the Zener diode operate in the Zener region? The other PN junction diode can be assumed to be ON or OFF (include the analysis of both).

Assume $V_{D0} = 0.7\text{ V}$. Choose a value between 3 V and 5 V and use it as V_Z . For example, you can select and use $V_Z = 5\text{ V}$.



Show your work. *selected $V_Z = 3\text{ V}$*

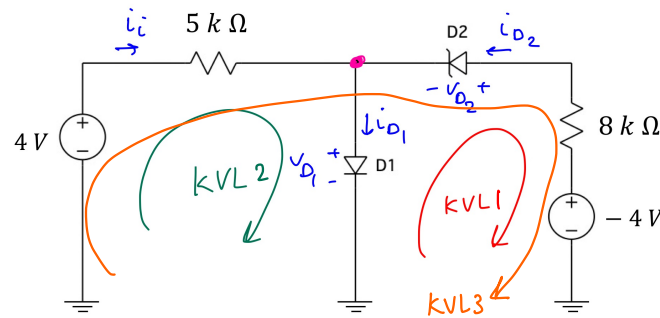
Case 1: D_2 is in Zener mode & D_1 is ON

$$i_{D1} \geq 0, \quad V_{D1} = V_{D0}, \quad i_{D2} \leq 0, \quad V_{D2} = -V_Z$$

$$\text{KVL1: } -V_{D1} - V_{D2} - 8k\Omega \times i_{D2} - 4\text{ V} = 0$$

$$8k\Omega \times i_{D2} = -0.7\text{ V} + V_Z - 4\text{ V} = -4.7 + V_Z$$

$$\rightarrow 8k\Omega \times i_{D2} = -1.7 \rightarrow i_{D2} = \frac{-1.7\text{ V}}{8k\Omega} = -0.2125\text{ mA} < 0$$



We assumed $i_{D1} \geq 0$, $V_{D1} = V_{D0}$, $i_{D2} \leq 0$, $V_{D2} = -V_Z$

$$\text{KVL2: } 4V = 5k\Omega \times i_i + V_{D1} \rightarrow i_i = \frac{4V - 0.7V}{5k\Omega} = 0.66 \text{ mA}$$

$$\text{KCL: } i_i + i_{D2} = i_{D1} \rightarrow i_{D1} = 0.66 \text{ mA} - 0.2125 \text{ mA} = 0.4475 \text{ mA} > 0$$

$$\Rightarrow i_{D1} > 0, V_{D1} = V_{D0}, i_{D2} < 0, V_{D2} = -V_Z$$

Case 2: D_1 is off and D_2 is in Zener region

$$V_{D1} < V_{D0}, i_{D1} = 0, i_{D2} \leq 0, V_{D2} = -V_Z$$

$$\text{KCL: } i_i + i_{D2} = i_{D1} \rightarrow i_i = -i_{D2}$$

$$\text{KVL3: } 4V = 5k\Omega \times i_i - V_{D2} - 8k\Omega \times i_{D2} - 4V \quad ; \quad V_Z = 3V$$

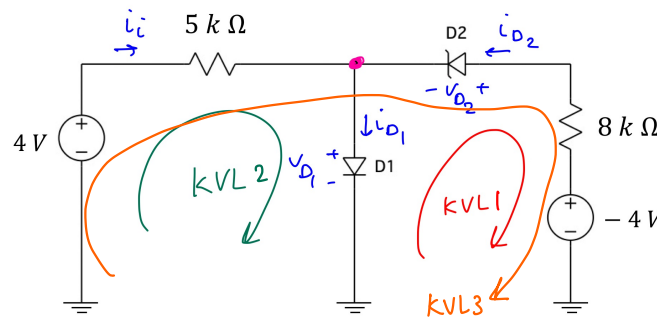
$$8V - 3V = -13k\Omega \times i_{D2} \Rightarrow i_{D2} = \frac{-5V}{13k\Omega} < 0$$

$$\text{KVL1: } V_{D1} = -V_{D2} - 8k\Omega \times i_{D2} - 4V = V_Z - 8k\Omega \times i_{D2} - 4V$$

$$V_{D1} = -1 + \frac{8}{13} \times 5 = 2.08$$

this contradicts the assumption, so case 2 cannot happen.

General solution:



Case 1: D_2 is in Zener mode & D_1 is ON, $3V \leq V_Z \leq 5V$
 $i_{D1} \geq 0$, $V_{D1} = V_{D0}$, $i_{D2} \leq 0$, $V_{D2} = -V_Z$

$$\text{KVL 2: } 4V = 5k\Omega \times i_i + V_{D1} \rightarrow i_i = \frac{4V - 0.7V}{5k\Omega} = 0.66 \text{ mA}$$

$$\text{KVL 1: } -V_{D1} - V_{D2} - 8k\Omega \times i_{D2} - 4V = 0$$

$$8k\Omega \times i_{D2} = -4.7 + V_Z \Rightarrow i_{D2} = \frac{-4.7 + V_Z}{8k\Omega}$$

To have the Zener diode operate in the Zener region, $i_{D2} \leq 0$

$$\Rightarrow i_{D2} = \frac{-4.7 + V_Z}{8k\Omega} \leq 0 \Rightarrow V_Z \leq 4.7V$$

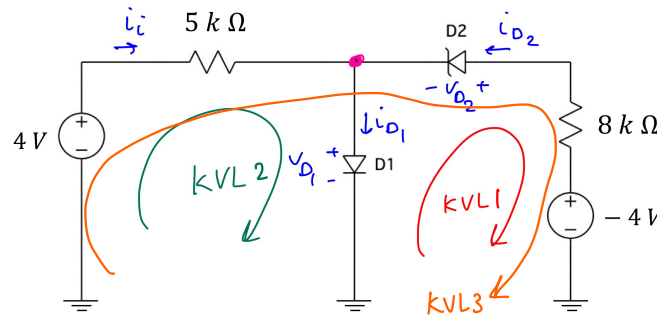
For this case to happen, i_{D1} also must be positive.

$$\text{KCL: } i_i + i_{D2} = i_{D1} \rightarrow i_{D1} = 0.66 \text{ mA} + \frac{-4.7 + V_Z}{8k\Omega} = 0.0725 \text{ mA} + \frac{V_Z}{8k\Omega}$$

$$i_{D1} = 0.0725 \text{ mA} + \frac{V_Z}{8k\Omega} \geq 0 \Rightarrow \frac{V_Z}{8k\Omega} \geq -0.0725 \text{ mA} \Rightarrow V_Z \geq -0.58$$

V_Z is positive so this condition is always satisfied.

General solution:



Case 1: D_2 is in Zener mode & D_1 is ON, $3V \leq V_Z \leq 5V$

$$i_{D1} \geq 0, V_{D1} = V_{D0}, i_{D2} \leq 0, V_{D2} = -V_Z$$

If the selected V_Z is less than $4.7V$, D_1 will be ON and D_2 will be in the Zener mode.

Case 2: D_1 is off and D_2 is in Zener region

$$V_{D1} < V_{D0}, i_{D1} = 0, i_{D2} \leq 0, V_{D2} = -V_Z$$

$$\text{KCL: } i_i + i_{D2} = i_{D1} \rightarrow i_i = -i_{D2}$$

$$\text{KVL3: } 4V = 5k\Omega \times i_i - V_{D2} - 8k\Omega \times i_{D2} - 4V \Rightarrow i_{D2} = \frac{V_Z - 8V}{13k\Omega}$$

$$\text{KVL1: } V_{D1} = -V_{D2} - 8k\Omega \times i_{D2} - 4V = V_Z - 8k\Omega \times i_{D2} - 4V = \left(1 - \frac{8}{13}\right)V_Z + \frac{8 \times 8}{13} - 4$$

$$V_{D1} = 0.38V_Z + 0.92, \text{ since } 3 \leq V_Z \leq 5 \Rightarrow 2.06 \leq V_{D1} \leq 2.82$$

this contradicts the assumption, so case 2 cannot happen.

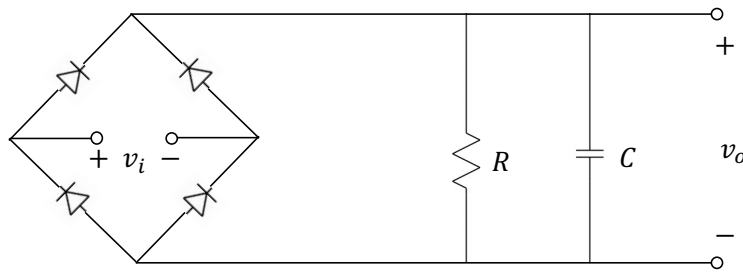
Problem 2. (5 points)

In the below circuit, sketch $v_o(t)$ for

- $V_i(t) = 10 \sin(2\pi \times f \times t)$, where $f = 1 \text{ kHz}$, $c = 1 \mu\text{F}$ and $R = 100 \text{ k}\Omega$
- $V_i(t) = 10 \sin(2\pi \times f \times t)$, where $f = 1 \text{ kHz}$, $c = 1 \mu\text{F}$ and $R = 100 \Omega$

A rough sketch for the waveform of $v_o(t)$ is enough. **Label the peak value of $v_o(t)$.** If the output waveform is different for part (i) and (ii), your sketch should be an indicator of this difference.

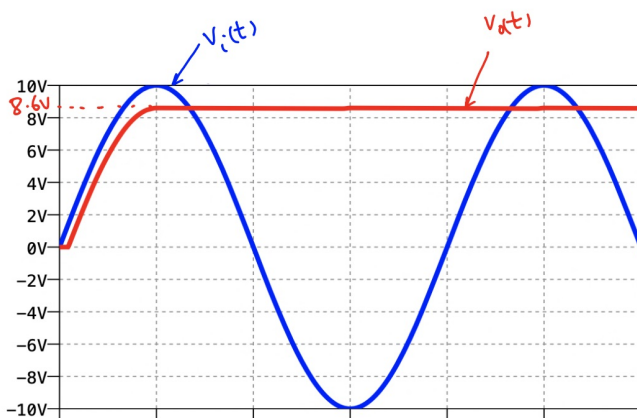
Assume $V_{D0} = 0.7 \text{ V}$.



Show your work.

$$i. \quad RC = 100 \text{ k}\Omega \times 1 \mu\text{F} = 10^5 \Omega \times 10^{-6} \text{ F} = 10^{-1} \text{ s}$$

$$T = \frac{1}{f} = 10^{-3} \quad \rightarrow \quad \frac{RC}{T} = \frac{10^{-1}}{10^{-3}} = 100 \rightarrow RC \gg T$$



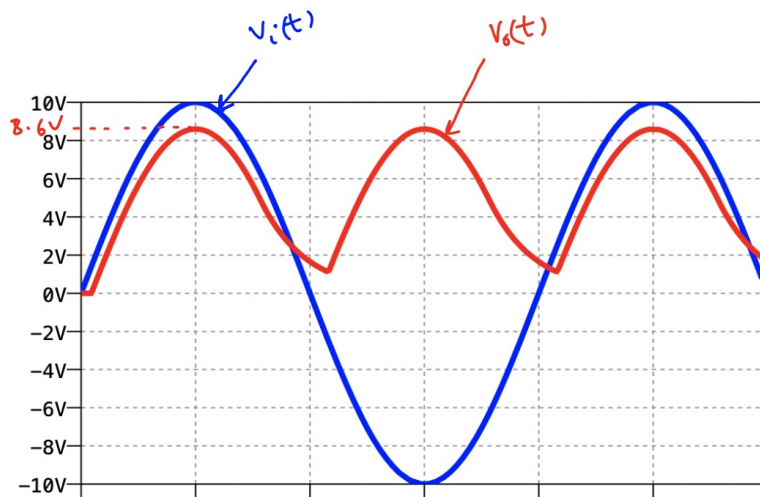
$$v_{o \text{ peak}} = 10 \text{ V} - 2 \times V_{D0} = 8.6 \text{ V}$$

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$$ii. \quad RC = 100 \, \Omega \times 1 \, \mu F = 10^2 \, \Omega \times 10^{-6} \, F = 10^{-4} \, s$$

$$T = \frac{1}{f} = 10^{-3} \quad \longrightarrow \quad \frac{RC}{T} = \frac{10^{-4}}{10^{-3}} = 0.1$$

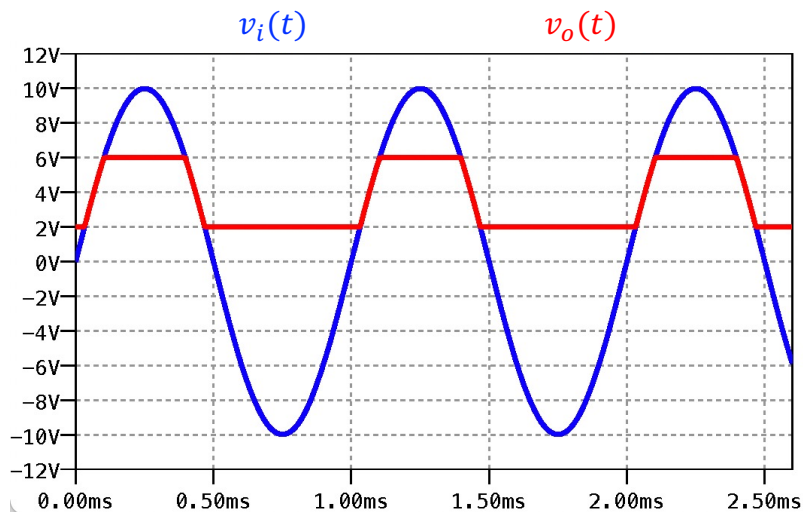


$$V_{o \text{ peak}} = 10 \, V - 2 \times V_{D_0} = 8.6 \, V$$

Problem 3. (10 points)

- a) Design a diode circuit that would generate the output waveform, $v_o(t)$, shown in the below graph when the input signal $v_i(t) = 10 \sin(\omega t)$ is applied to the circuit.

You can use regular PN junction diodes ($V_{D0} = 0.7 V$), Zener diodes (any desired V_Z), and resistor(s) in your design. Make sure to label v_i and v_o on your circuit diagram.



- b) Parametrically solve your designed circuit to find the transfer function and draw the transfer function graph. (find the relationship between v_o and v_i for different ranges of v_i and plot v_o vs v_i)

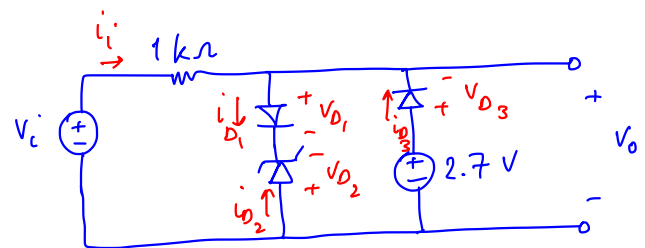
Show your work.

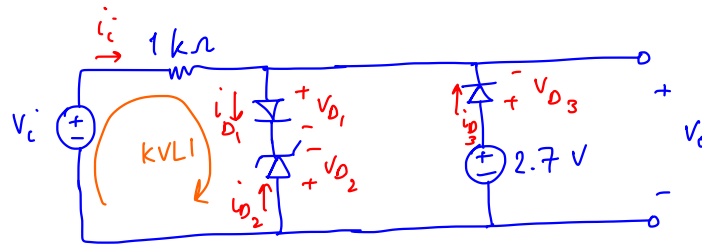
a)

$$\text{if } v_i \geq 6V \rightarrow v_o = 6V$$

$$\text{if } v_i \leq 2V \rightarrow v_o = 2V$$

$$\text{select } V_Z = 5.3V$$





$$V_2 = 5.3 \text{ V}$$

b) Case 1: D_1 is ON, D_2 is in Zener mode, D_3 is off

Case 2: D_1 & D_2 are off, D_3 is ON

Case 3: D_1, D_2, D_3 are off

Case 1: D_1 is ON, D_2 is in Zener mode, D_3 is off

$$i_{D_1} \geq 0, V_{D_1} = V_{D_0}, i_{D_2} \leq 0, V_{D_2} = -V_Z = -5.3 \text{ V}, i_{D_3} = 0, V_{D_3} < V_{D_0}$$

$$\text{KVL 1: } V_i = 1 \text{ k}\Omega \times i_i + V_{D_1} - V_{D_2} = 1 \text{ k}\Omega \times i_i + 0.7 + 5.3 \text{ V}$$

$$\Rightarrow V_i - 6 = 1 \text{ k}\Omega \times i_i \Rightarrow i_i = \frac{V_i - 6}{1 \text{ k}\Omega}$$

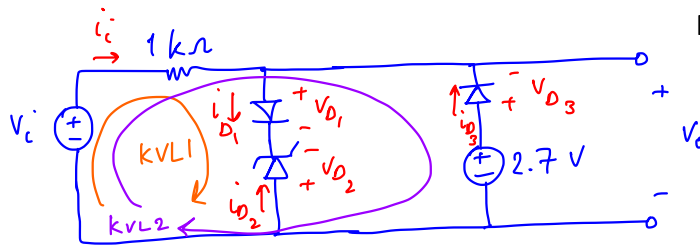
$$\text{KCL: } i_i + i_{D_3} = i_{D_1}, \quad i_{D_3} = 0 \Rightarrow i_i = i_{D_1}$$

$$i_{D_1} \geq 0 \Rightarrow \frac{V_i - 6}{1 \text{ k}\Omega} \geq 0 \Rightarrow V_i \geq 6 \text{ V}$$

$$V_o = V_{D_1} - V_{D_2} = 6 \text{ V} \rightarrow V_o = 6 \text{ V}$$

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Case 2: D_1 & D_2 are off, D_3 is ON

$$i_{D1} = i_{D2} = 0, \quad v_{D1} < V_{D0}, \quad -V_Z < v_{D2} < V_{D0}, \quad i_{D3} \geq 0, \quad v_{D3} = V_{D0}$$

KVL 2:

$$v_i = 1k\Omega \times i_i - v_{D3} + 2.7$$

$$i_i = -i_{D3}, \quad v_{D3} = 0.7V \quad \rightarrow \quad v_i = -1k\Omega \times i_{D3} + 2V$$

$$\rightarrow i_{D3} = \frac{-v_i + 2V}{1k\Omega}$$

$$i_{D3} \geq 0 \Rightarrow v_i \leq 2V$$

$$v_o = -v_{D3} + 2.7V = -0.7V + 2.7V = 2V \Rightarrow v_o = 2V$$

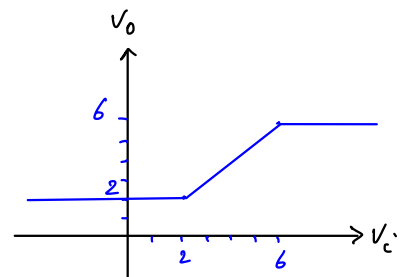
Case 3: D_1, D_2, D_3 are off

$$i_{D1} = i_{D2} = i_{D3} = 0, \quad v_{D1} < V_{D0}, \quad -V_Z < v_{D2} < V_{D0}, \quad v_{D3} < V_{D0}$$

$$i_i + i_{D3} = i_{D2} \Rightarrow i_i = 0$$

$$v_o = -i_i \times 1k\Omega \times v_i \Rightarrow v_o = v_i$$

The range of v_i will be: $2V < v_i < 6V$

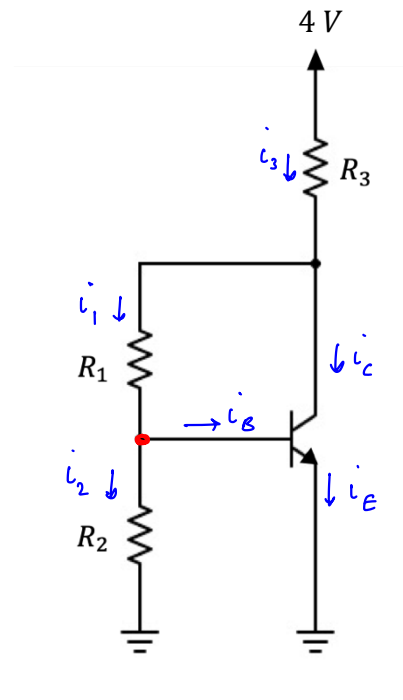


Problem 4 (10 points)

Design the following circuit to have $I_C = 2 \text{ mA}$ and $V_C = 1 \text{ V}$.

Assume $\beta = 100$, $V_D = 0.7 \text{ V}$, and $V_{sat} = 0.2 \text{ V}$.

The resistors must have finite non-zero values.



Show your work.

$$V_C = V_{CE} = 1 \text{ V} > V_{D_0} \Rightarrow \text{BJT is in the active mode.}$$

$$i_C = \beta i_B \Rightarrow i_B = \frac{2 \text{ mA}}{100} = 20 \mu\text{A}$$

$$\text{The BJT is ON} \Rightarrow V_{BE} = V_{D_0} = 0.7 \text{ V} \Rightarrow V_B - V_E = 0.7 \text{ V}$$

$$V_E = 0 \Rightarrow V_B = 0.7 \text{ V}$$

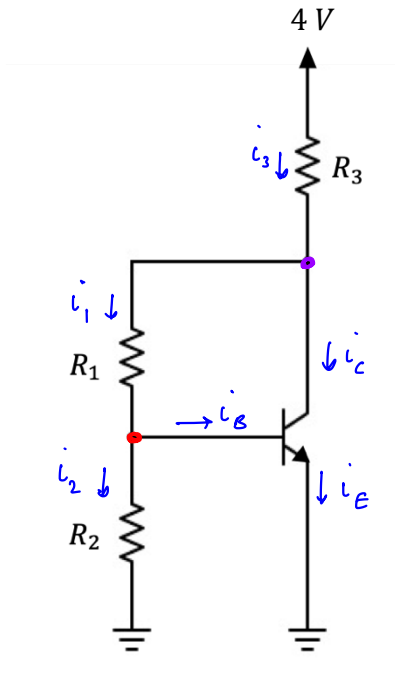
$$V_B = R_2 i_2, \text{ select } R_2 = 1 \text{ k}\Omega \rightarrow i_2 = \frac{0.7 \text{ V}}{1 \text{ k}\Omega} = 0.7 \text{ mA}$$

Problem 4 (10 points)

Design the following circuit to have $I_C = 2 \text{ mA}$ and $V_C = 1 \text{ V}$.

Assume $\beta = 100$, $V_D = 0.7 \text{ V}$, and $V_{sat} = 0.2 \text{ V}$.

The resistors must have finite non-zero values.



Show your work.

KCL at the Base : $i_1 = i_2 + i_B$

$$\Rightarrow i_1 = 0.7 \text{ mA} + 0.02 \text{ mA} = 0.72 \text{ mA}$$

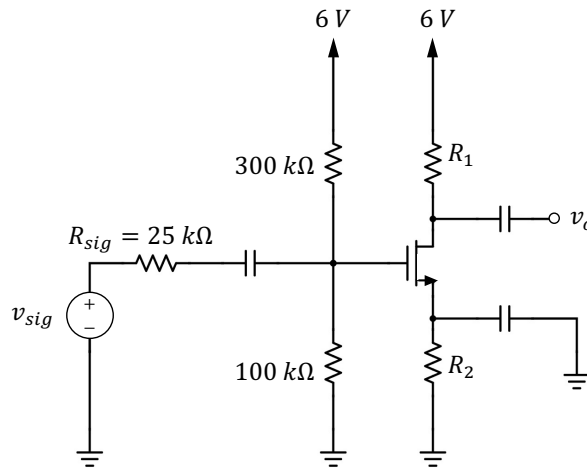
$$i_1 = \frac{V_C - V_B}{R_1} = \frac{1 - 0.7}{R_1} \Rightarrow R_1 = \frac{0.3 \text{ V}}{0.72 \text{ mA}} \approx 417 \Omega \rightarrow R_1 = 417 \Omega$$

KCL at the Collector : $i_3 = i_1 + i_C \Rightarrow i_3 = 0.72 \text{ mA} + 2 \text{ mA} = 2.72 \text{ mA}$

$$R_3 = \frac{4 \text{ V} - 1 \text{ V}}{i_3} \approx 1.103 \text{ k}\Omega \rightarrow R_3 = 1.103 \text{ k}\Omega$$

Problem 5 (15 points)

For this problem, neglect the early effect in the bias and signal circuits, assume the capacitors are short for the signal circuit and $V_t = 0.5 \text{ V}$.

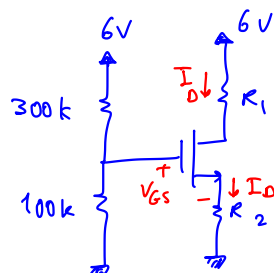


- Design the above amplifier circuit such that
 - The transistor is biased at $I_D = 0.5 \text{ mA}$ and $V_{OV} = 0.5 \text{ V}$.
 - The open-loop voltage gain is -10 V/V .
- Draw the small signal equivalent circuit.
- If v_{sig} is a sinusoidal signal with peak amplitude \hat{v}_{sig} , find the maximum allowable value of \hat{v}_{sig} for which the transistor remains in saturation. What is the corresponding amplitude of the output signal voltage?
- If we limit \hat{v}_{sig} to 40 mV , what value can R_D be increased to while maintaining saturation region operation? (I_D and V_{OV} will not change.)

Show your work.

a)

Bias circuit:



$$V_{OV} = V_{GS} - V_t \Rightarrow V_{GS} = 0.5 \text{ V} + 0.5 \text{ V} = 1 \text{ V}$$

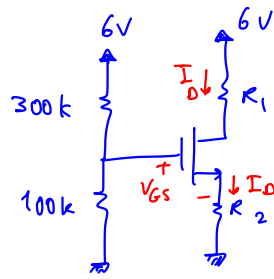
$$V_G = \frac{100 \text{ k}}{100 \text{ k} + 300 \text{ k}} \times 6 \text{ V} = 1.5 \text{ V}$$

$$V_{GS} = V_G - V_S = 1 \text{ V} \Rightarrow V_S = 0.5 \text{ V}$$

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Bias circuit:



$$V_s = I_D \times R_2 \Rightarrow R_2 = \frac{0.5 \text{ V}}{0.5 \text{ mA}} = 1 \text{ k}\Omega$$

$$R_2 = 1 \text{ k}\Omega$$

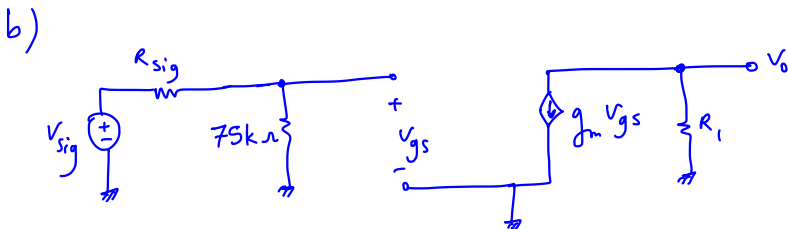
This is a common-source amplifier: $A_{V_o} = -g_m(R_1 \parallel r_o)$

Neglect the early effect: $r_o = \infty \Rightarrow A_{V_o} = -g_m R_1 = -10 \text{ V/V}$

$$g_m = \frac{2 I_D}{V_{ov}} = \frac{1 \text{ mA}}{0.5 \text{ V}} = 2 \text{ mA/V} \Rightarrow R_1 = \frac{10}{2 \text{ mA/V}} = 5 \text{ k}\Omega$$

$$R_1 = 5 \text{ k}\Omega$$

$$\rightarrow V_D = 6 \text{ V} - R_1 I_D = 3.5 \text{ V}$$



c) To stay in saturation: $V_{DS} \geq V_{ov} \rightarrow V_{DS} - \hat{v}_{ds} \geq V_{GS} + \hat{v}_{gs} - V_t$

$$V_{DS} - A \hat{v}_{gs} \geq V_{GS} + \hat{v}_{gs} - V_t \rightarrow (1 + A) \hat{v}_{gs} \leq V_{DS} - V_{GS} + V_t$$

$$\rightarrow (1 + A) \hat{v}_{gs} \leq V_D - V_G + V_t$$

$$\rightarrow 11 \hat{v}_{gs} \leq 2.5 \text{ V}$$

$$\rightarrow \hat{v}_{gs} \leq 227 \text{ mV}$$

checking the minimum amplitude of the instantaneous v_{GS} to transistor does not go to cut off:

$$v_{GS_{min}} = V_{GS} - \hat{v}_{gs_{max}} = 1V - 0.227V = 0.773 > V_t \Rightarrow \text{NMOS will not go to cut off.}$$

Finding the maximum of \hat{v}_{sig} and \hat{v}_{ds} :

$$\hat{v}_{gs} \leq 227 \text{ mV}$$

$$\hat{v}_{ds} = |A| \hat{v}_{gs} = 10 \times \hat{v}_{gs} \Rightarrow \hat{v}_{ds} \leq 2.27 \text{ V}$$

$$\hat{v}_{gs} = \frac{75 \text{ k}\Omega}{R_{sig} + 75 \text{ k}\Omega} \times \hat{v}_{sig} \rightarrow \hat{v}_{gs} = 0.75 \hat{v}_{sig}$$

$$\hat{v}_{sig} \leq \frac{227 \text{ mV}}{0.75} \rightarrow \hat{v}_{sig} \leq 303 \text{ mV}$$

$$d) \quad \hat{v}_{sig} = 40 \text{ mV} \Rightarrow \hat{v}_{gs} = 30 \text{ mV}$$

$$\text{from part b: } (1+A) \hat{v}_{gs} \leq V_D - V_G + V_t$$

$$(1+A) \hat{v}_{gs} \leq 6V - R_D \times 0.5 \text{ mA} - V_G + V_t$$

$$(1+A) \hat{v}_{gs} \leq 6V - R_D \times 0.5 \text{ mA} - 1.5 + 0.5$$

$$1+A \leq \frac{5 - R_D \times 0.5 \text{ mA}}{0.03}$$

$$A \leq \frac{5 - R_D \times 0.5 \text{ mA} - 0.03}{0.03}$$

$$A \leq \frac{4.97 - R_D \times 0.5 \text{ mA}}{0.03}$$

$$\begin{cases} A \leq \frac{4.97 - R_D \times 0.5 \text{mA}}{0.03} \\ |A| = g_m R_D = 2 \text{mA/V} \times R_D \end{cases}$$

$$\Rightarrow 2 \text{mA/V} \times R_D \leq \frac{4.97 - R_D \times 0.5 \text{mA}}{0.03}$$

$$\rightarrow 0.06 R_D + 0.5 R_D \leq 4.97$$

$$0.56 R_D \leq 4.97$$

$$\rightarrow R_D \leq 8.875 \text{ k}\Omega$$

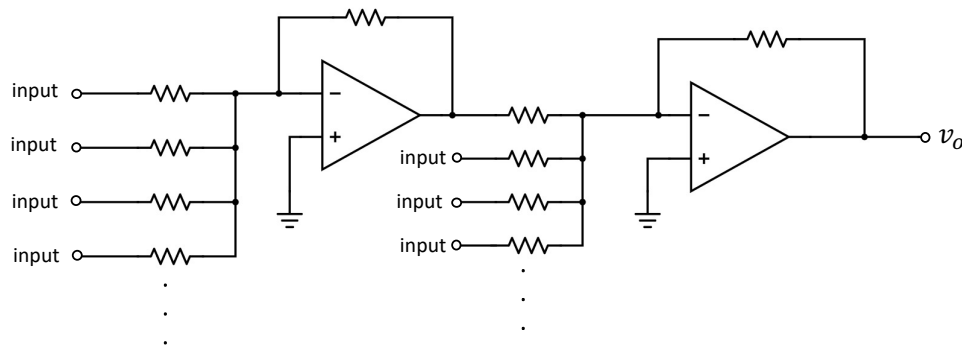
$$R_{D_{\max}} = 8.875 \text{ k}\Omega$$

Problem 6 (5 points)

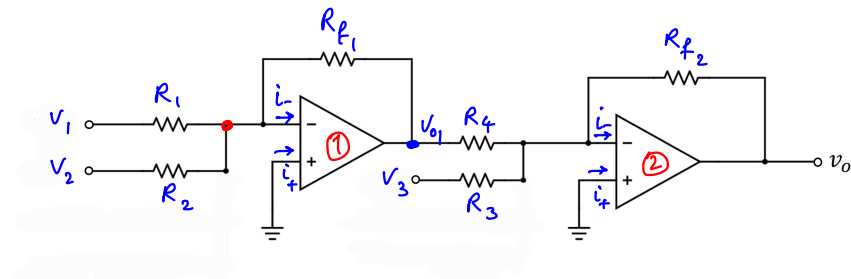
Using the general weighted summer op-amp circuit provided below, design an op-amp circuit that provides

$$v_o = 2v_1 + v_2 - 4v_3$$

where, v_1 , v_2 , and v_3 are the inputs.



Show your work.



Assume ideal op-amps: $i_+ = i_- = 0$

Negative feedback in both op-amps: $v_- = v_+$ in both op-amps

KCL at the inverting input terminal of op-amp 1:

$$\frac{V_1 - V_-}{R_1} + \frac{V_2 - V_-}{R_2} = \frac{V_- - V_{o1}}{R_{f1}}$$

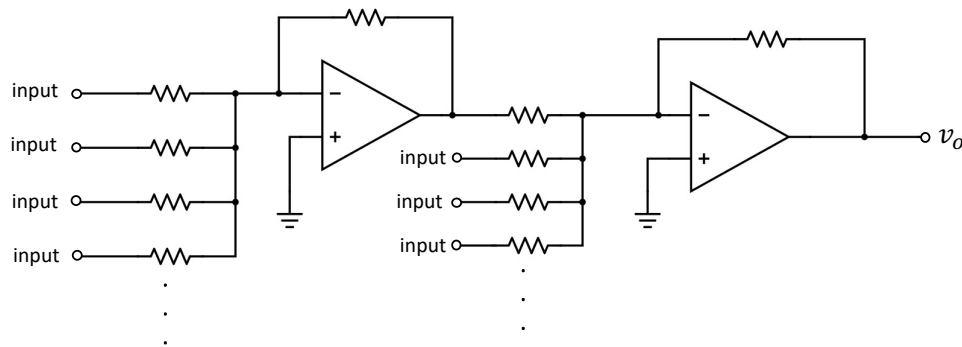
$$V_- = V_+ = 0 \rightarrow \frac{V_1}{R_1} + \frac{V_2}{R_2} = \frac{-V_{o1}}{R_{f1}} \Rightarrow V_{o1} = -\frac{R_{f1}}{R_1} V_1 + \frac{-R_{f1}}{R_2} V_2$$

Problem 6 (5 points)

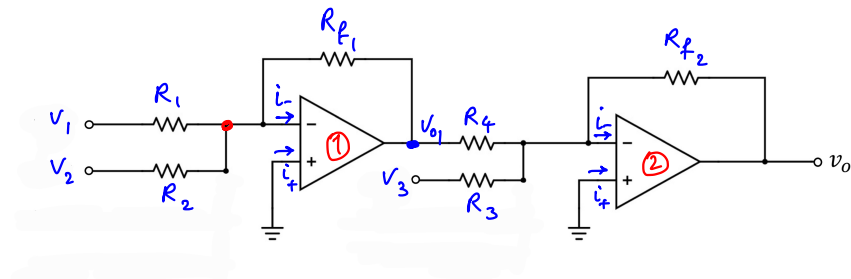
Using the general weighted summer op-amp circuit provided below, design an op-amp circuit that provides

$$v_o = 2v_1 + v_2 - 4v_3$$

where, v_1 , v_2 , and v_3 are the inputs.



Show your work.



KCL at the inverting input terminal of op-amp 2:

$$\frac{V_{o1} - V_-}{R_4} + \frac{V_3 - V_-}{R_3} = \frac{V_- - V_o}{R_{f2}}$$

$$V_- = V_+ = 0 \rightarrow \frac{V_{o1}}{R_4} + \frac{V_3}{R_3} = \frac{-V_o}{R_{f2}} \Rightarrow V_o = -\frac{R_{f2}}{R_4} V_{o1} + \frac{-R_{f2}}{R_3} V_3$$

$$V_{o1} = -\frac{R_{f1}}{R_1} V_1 + \frac{-R_{f1}}{R_2} V_2$$

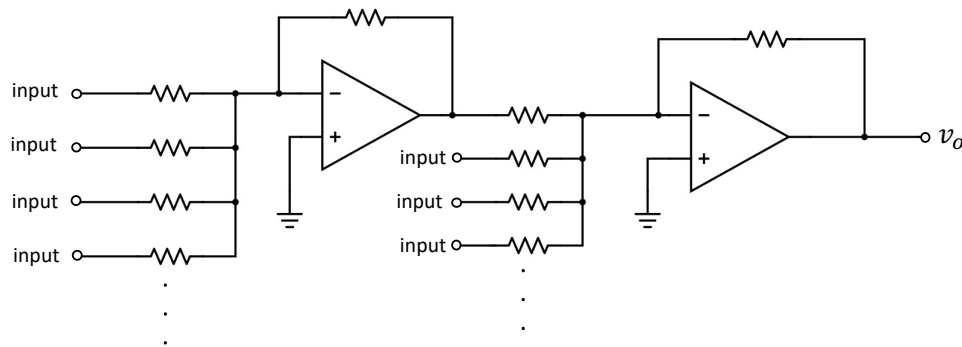
$$\Rightarrow V_o = \left(\frac{R_{f2}}{R_4}\right) \left(\frac{R_{f1}}{R_1}\right) V_1 + \left(\frac{R_{f2}}{R_4}\right) \left(\frac{R_{f1}}{R_2}\right) V_2 - \frac{R_{f2}}{R_3} V_3$$

Problem 6 (5 points)

Using the general weighted summer op-amp circuit provided below, design an op-amp circuit that provides

$$v_o = 2v_1 + v_2 - 4v_3$$

where, v_1 , v_2 , and v_3 are the inputs.



Show your work.

$$V_o = \left(\frac{R_{f2}}{R_4} \right) \left(\frac{R_{f1}}{R_1} \right) V_1 + \left(\frac{R_{f2}}{R_4} \right) \left(\frac{R_{f1}}{R_2} \right) V_2 - \frac{R_{f2}}{R_3} V_3$$

$$V_o = 2V_1 + 1 \times V_2 - 4V_3$$

$$\frac{R_{f2}}{R_3} = 4, \quad \text{select } R_3 = 1 \text{ k}\Omega, \quad R_{f2} = 4 \text{ k}\Omega$$

$$\left(\frac{R_{f2}}{R_4} \right) \left(\frac{R_{f1}}{R_2} \right) = 1, \quad \text{select } R_4 = 4 \text{ k}\Omega, \quad R_{f1} = 1 \text{ k}\Omega, \quad R_2 = 1 \text{ k}\Omega$$

$$\left(\frac{R_{f2}}{R_4} \right) \left(\frac{R_{f1}}{R_1} \right) = 2 \quad \rightarrow \quad R_1 = 0.5 \text{ k}\Omega$$