Name PID

UNIVERSITY OF CALIFORNIA, SAN DIEGO

Electrical and Computer Engineering Department

ECE 65 – Fall 2020

Components and Circuits lab

Final Exam **Solutions**

You should submit your handwritten solutions in a PDF format to Gradescope by Wednesday, 12/16, at 11:00 am (Pacific Time).

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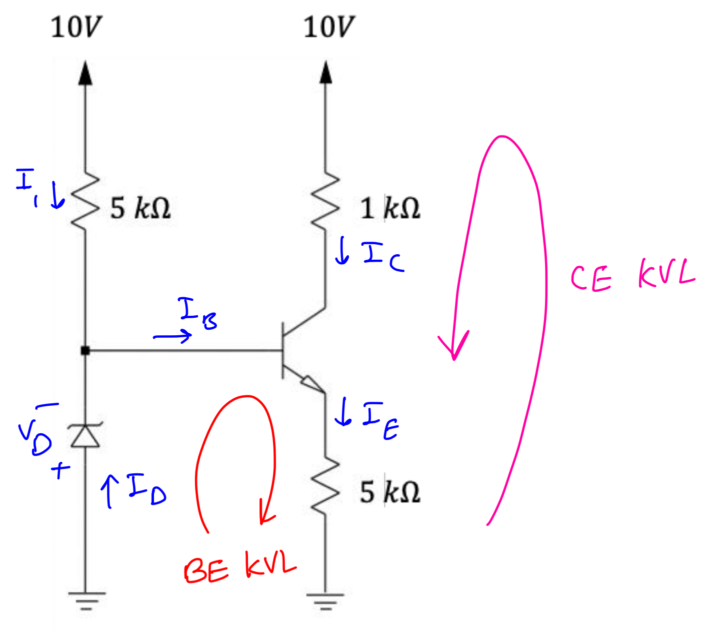
Problem 1. (5 points)

Find the node voltages and the currents in all branches in the following circuit.

Assume $V_{D0} = 0.7\ V,\ V_{sat} = 0.2\ V,\ V_z = 6.2\ V, \beta = 100$



Show your work.

Assume the Zener diode is in the Zener region and the BJT is ON and in active region.

$V_D = -V_Z = -6.2V$, $I_D \leq 0$, $V_{BE} = V_{D_0} = 0.7V$

$I_C = \beta I_B = \frac{\beta}{1+\beta} I_E$, $V_{CE} \geq V_{D_0}$

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Problem 1. (5 points)

KCL at the base: $I_B = I_1 + I_D$

Ohm's law: $I_1 = \frac{10V - V_Z}{5k\Omega} = \frac{10 - 6.2V}{5k\Omega} = 0.76\ mA$

BE KVL: $V_D + V_{BE} + 5k\Omega \times I_E = 0 \rightarrow -6.2V + 0.7 + 5k\Omega \times I_E = 0$

$\rightarrow I_E = 1.1\ mA$

$I_C = \frac{100}{101} \times 1.1\ mA \simeq 1.09\ mA$

CE KVL: $10V = 1k\Omega \times I_C + 5k\Omega \times I_E + V_{CE}$

$\rightarrow V_{CE} = 10 - 1.09 - 5.5 = 3.41\ V \geqslant V_{D_0}$

$I_B = \frac{I_C}{100} \simeq 0.0109\ mA \simeq 11\ \mu A$

KCL at the base: $I_D = I_B - I_1$

$= 0.0109\ mA - 0.76\ mA \simeq -0.749\ mA \leqslant 0$

$V_{CE} \geqslant V_{D_0}$ and $I_D \leqslant 0$, the assumption was correct.

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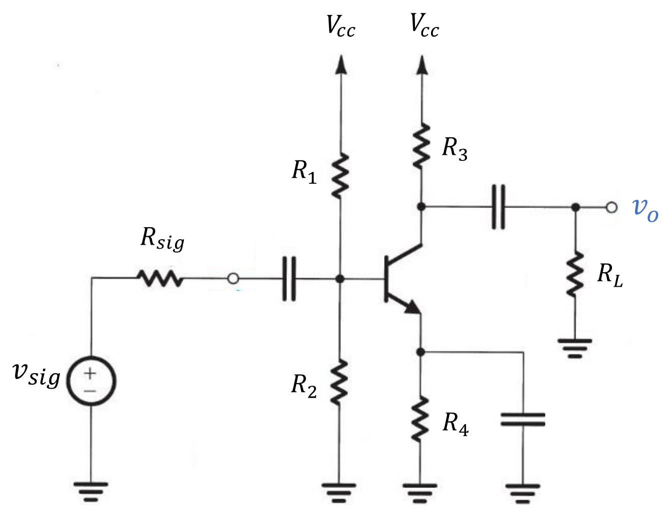
Problem 2. (10 points)

Assume

- $V_{D0} = 0.7\ V,\ V_{sat} = 0.2\ V$, and $\beta = 100\ , V_T = 26\ mV$
- The power supply available is $15\ V$.
- The output resistance of the signal source is $1\ k\Omega$ ($R_{sig} = 1\ k\Omega$) and the load resistance is $1\ k\Omega$.
- Capacitors are short in the signal circuit.
- Ignore the early effect in bias and signal circuit calculations.



Design the above amplifier circuit such that

i. The collector current is $2\ mA$.

ii. The Thevenin equivalent resistance at the base is about one tenth of R_E.

iii. The absolute value of the total gain of the amplifier ($A = \frac{v_o}{v_{sig}}$) is at least 10 V/V.

In your answers, make sure to include

a) All the resistor values.

b) All the DC node voltages.

c) The total gain of the amplifier.

d) Choose a sinusoidal signal with f = 1 kHz (choose the peak amplitude of the signal yourself), and sketch both v_{sig} and v_o.

Show your work. This is a design problem, so there are multiple answers for this problem.

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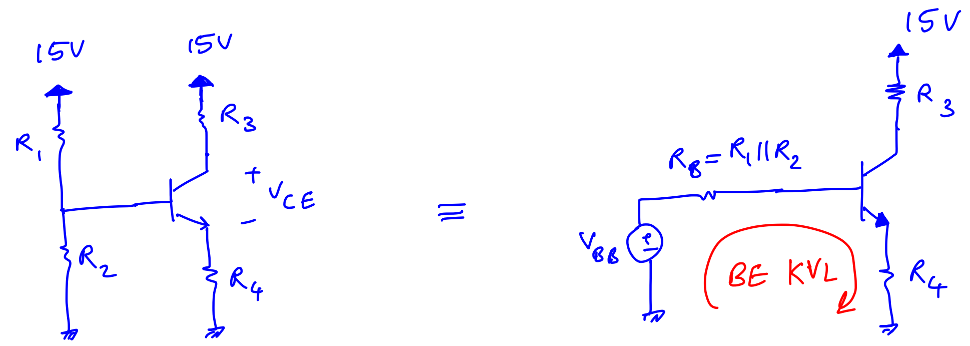
Problem 2. (5 points)

Bias circuit:



$R_B = 0.1\ R_E$, $I_C = 2\,mA$, $\beta = 100$

BJT is in active mode $\Rightarrow$ $I_E = \frac{1+\beta}{\beta} I_C = 2.02\ mA$

There are multiple ways design this circuit.

I chose $\boxed{R_E = 4\,k\Omega}$ and $\boxed{R_B = 0.4\,k\Omega}$.

$$V_E = R_E \times I_E = 4k\Omega \times 2.02\,mA = 8.08\ V$$

BE KVL: $V_{BB} = R_B I_B + V_{BE} + V_E = 0.4\,k\Omega \times \frac{2.02\,mA}{101} + 0.7 + 8.08$

$$V_{BB} = 8.79\ V$$

$R_B = \frac{R_1 R_2}{R_1 + R_2} = 0.4\,k\Omega$, $\frac{R_2}{R_1+R_2} \times 15\,V = V_{BB} = 8.79\ V$

$\boxed{R_1 = 680\ \Omega}$, $\boxed{R_2 = 971\ \Omega}$

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Problem 2. (10 points)

$$A = \frac{v_o}{v_{sig}} = \frac{R_i}{R_i + R_{sig}} \times A_{v_o} \times \frac{R_L}{R_L + R_o}$$

$R_i = R_B \parallel r_\pi$, $A_{v_o} = -g_m (R_C \parallel r_o) = -g_m R_C$, $R_o = R_C \parallel r_o = R_C$

$$g_m = \frac{I_C}{V_T} = \frac{2\,mA}{26\,mV} = 76.9\ (mA/V)$$

$$r_\pi = \frac{\beta}{g_m} = 1.3\ k\Omega$$

$$R_i = 0.4\,k\Omega \parallel 1.3\,k\Omega = 0.31\ k\Omega$$

I chose $\boxed{A = -10\ V/V}$

$$A = \frac{v_o}{v_{sig}} = \frac{0.31\,k\Omega}{0.31\,k\Omega + 1\,k\Omega} \times (-76.9\,(mA/V)\,R_C) \times \frac{1\,k\Omega}{1\,k\Omega + R_C} = -10\ V/V$$

$$\rightarrow \boxed{R_C = 1.18\ k\Omega}$$

The bias node voltages: $V_C = V_{CC} - R_C I_C = 15\,V - 1.18\,k\Omega \times 2\,mA = 12.64\,V$

$V_B = V_E + V_{BE} = 8.78\ V$

$\boxed{V_C = 12.64\ V}$, $\boxed{V_E = 8.08\ V}$, $\boxed{V_B = 8.78\ V}$

$V_{CE} = 4.56\,V > V_{D_0}$ $\longrightarrow$ BJT is in active region

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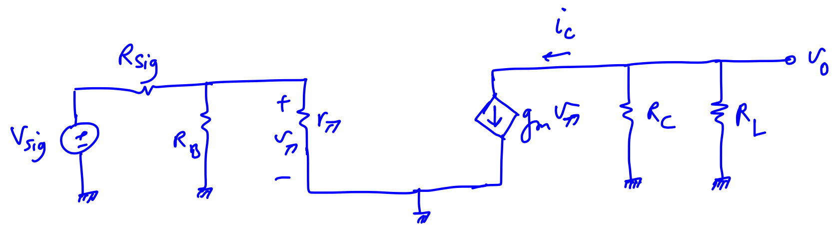
Problem 2. (10 points)

at DC, $V_C = 12.64\,V$ and $V_{CC} = 15\,V$



$$v_\pi = \frac{r_\pi \parallel R_B}{(r_\pi \parallel R_B) + R_{sig}} v_{sig} \longrightarrow v_\pi = 0.24\, v_{sig}$$

I chose $\hat{V}_{sig} = 10\ mV \longrightarrow \hat{v}_\pi = 2.4\ mV < 5\,mV$

$v_{sig} = 10 \sin(\omega t)\ (mV)$, $\omega = 2\pi \times 1\ kHz$

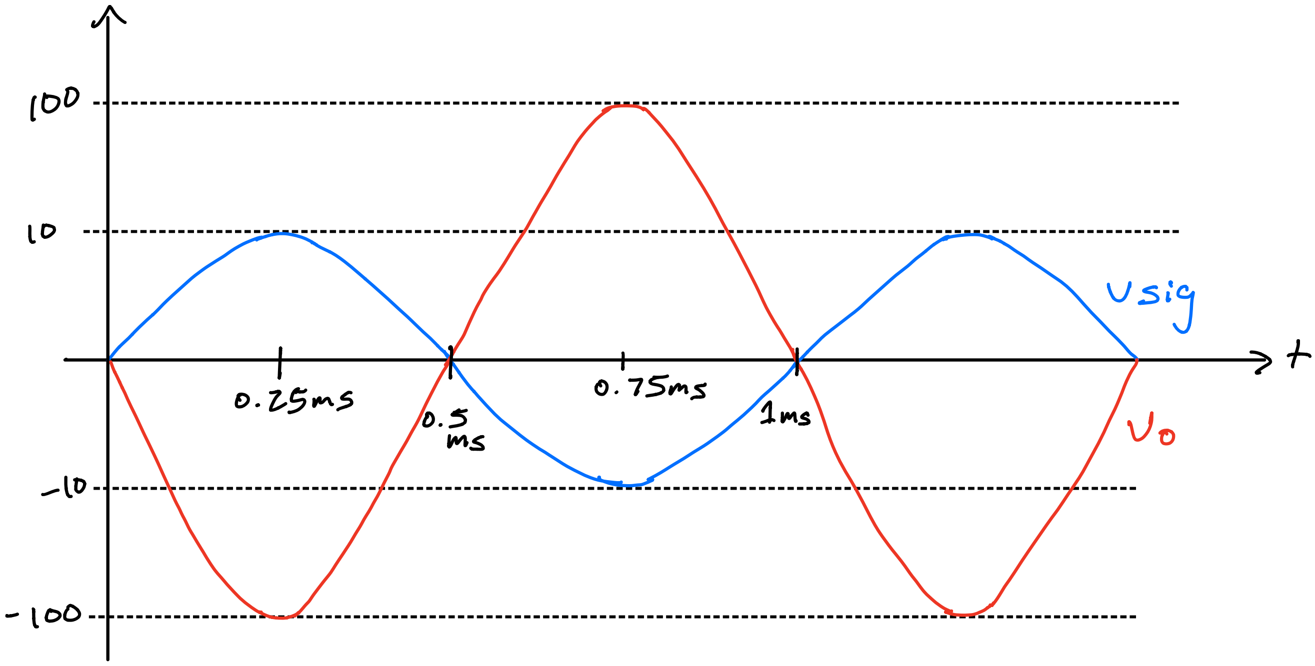
$v_o = -10\ v_{sig} \longrightarrow |\hat{v}_o| = 100\ mV \longrightarrow v_o = -100 \sin(\omega t)_{(mV)}$, $\omega = 2\pi \times 1\ kHz$

$v_o = v_c$, the signal part of the collector node voltage and v_o are the same.

$v_C = V_C + v_c = 12.64\ V - 0.1\ (V) \sin(\omega t)$

$v_E = V_E + v_e = V_E + 0 = 8.08$

$v_{CE} = v_C - v_E = 4.56\ (V) - 0.1\ (V)\ \sin(\omega t) > 0.7$ at all times



100
10
-10
-100
0.25ms
0.5 ms
0.75ms
1ms
t
vsig
vo