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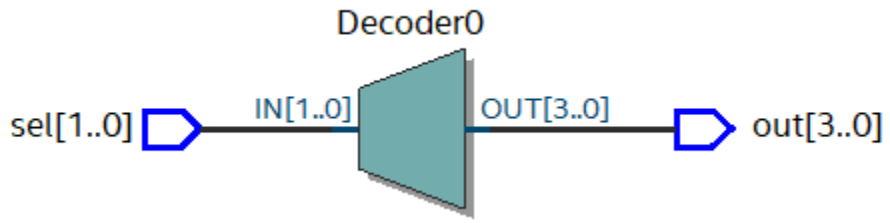
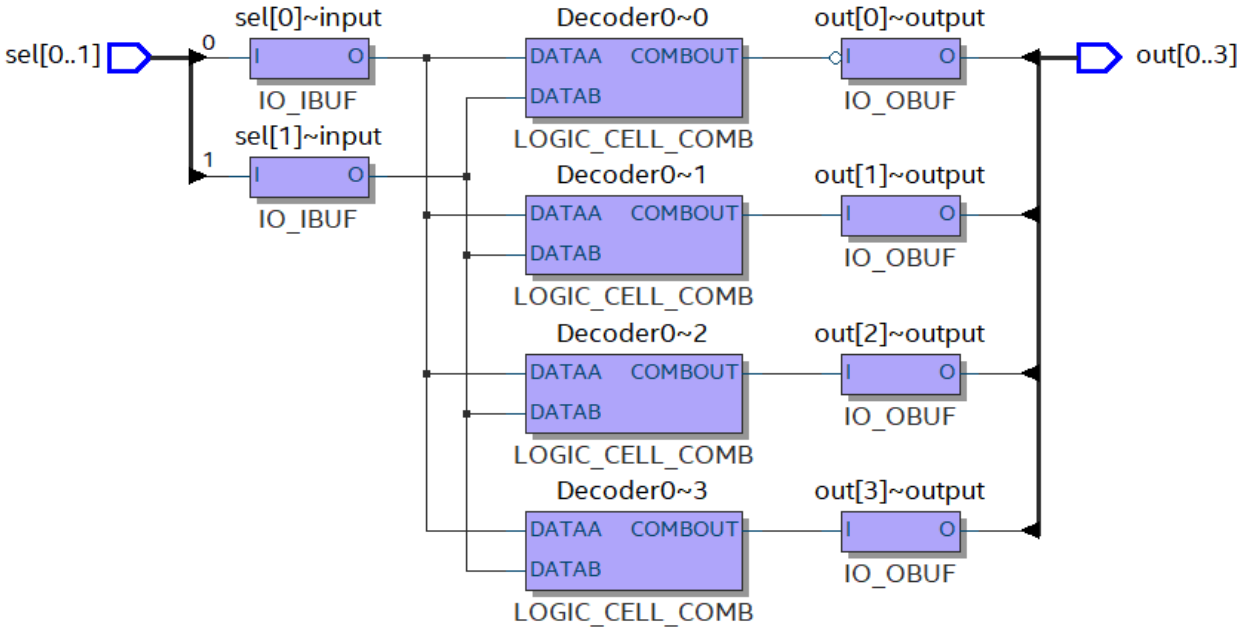
I chose option one, making the behavioral and dataflow match the gate-level implementation, thus the observable waveforms are the same.

decoder_2to4_behavioral.sv

```
// 2to4 Decoder behavioral level code
module decoder(
 input  logic[1:0] sel,
 output logic[3:0] out
);
 always @(sel)
  begin
   case (sel)
    2'b00  : out = 4'b0001; // Output for sel = 00
    2'b01  : out = 4'b0010; // Output for sel = 01
    2'b10  : out = 4'b0100; // Output for sel = 10
    2'b11  : out = 4'b1000; // Output for sel = 11
    default: out = 4'b0000; // Default case
   endcase
  end
endmodule
```





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ucsd > ece111 > HW > HW1 > decoder-Resource Usage Summary.rpt

```
+-----------------------------------------------------------------+
; Analysis & Synthesis Resource Usage Summary                     ;
+-------------------------------------------------+---------------+
; Resource                                        ; Usage         ;
+-------------------------------------------------+---------------+
; Estimated ALUTs Used                            ; 4             ;
;     -- Combinational ALUTs                      ; 4             ;
;     -- Memory ALUTs                            ; 0             ;
;     -- LUT_REGs                                ; 0             ;
; Dedicated logic registers                       ; 0             ;
;                                                 ;               ;
; Estimated ALUTs Unavailable                     ; 0             ;
;     -- Due to unpartnered combinational logic   ; 0             ;
;     -- Due to Memory ALUTs                      ; 0             ;
;                                                 ;               ;
; Total combinational functions                   ; 4             ;
; Combinational ALUT usage by number of inputs    ;               ;
;     -- 7 input functions                        ; 0             ;
;     -- 6 input functions                        ; 0             ;
;     -- 5 input functions                        ; 0             ;
;     -- 4 input functions                        ; 0             ;
;     -- <=3 input functions                      ; 4             ;
;                                                 ;               ;
; Combinational ALUTs by mode                     ;               ;
;     -- normal mode                             ; 4             ;
;     -- extended LUT mode                       ; 0             ;
;     -- arithmetic mode                         ; 0             ;
;     -- shared arithmetic mode                  ; 0             ;
;                                                 ;               ;
; Estimated ALUT/register pairs used              ; 4             ;
;                                                 ;               ;
; Total registers                                 ; 0             ;
;     -- Dedicated logic registers                ; 0             ;
;     -- I/O registers                            ; 0             ;
;     -- LUT_REGs                                 ; 0             ;
;                                                 ;               ;
;                                                 ;               ;
; I/O pins                                        ; 6             ;
;                                                 ;               ;
; DSP block 18-bit elements                       ; 0             ;
;                                                 ;               ;
; Maximum fan-out node                            ; sel[0]~input  ;
; Maximum fan-out                                 ; 4             ;
; Total fan-out                                   ; 18            ;
; Average fan-out                                 ; 1.13          ;
+-------------------------------------------------+---------------+
```

Number of ALUTs: 4 (6 I/O pins)
The 2-to-4 decoder requires 4 ALUTs, with each ALUT implementing one of the four output functions. Each output function depends on the two inputs (sel[1:0]), and each ALUT handles a 2-input Boolean function to determine when an output is active.

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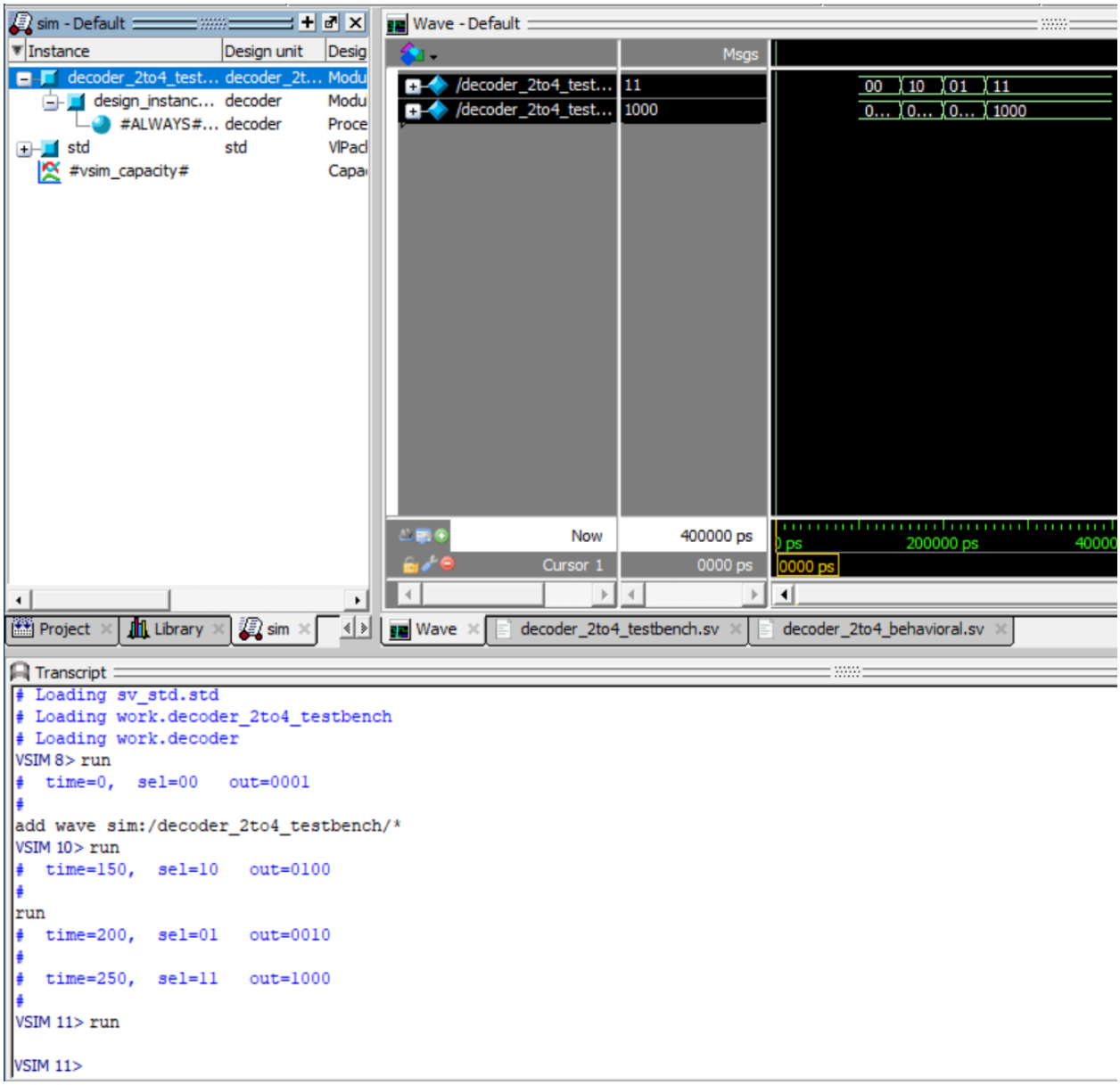

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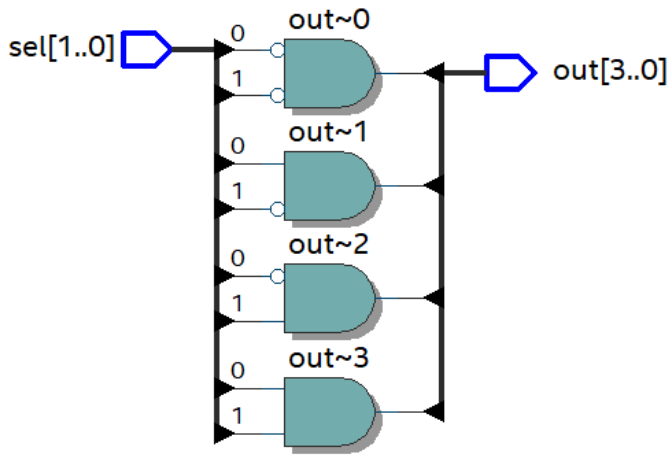
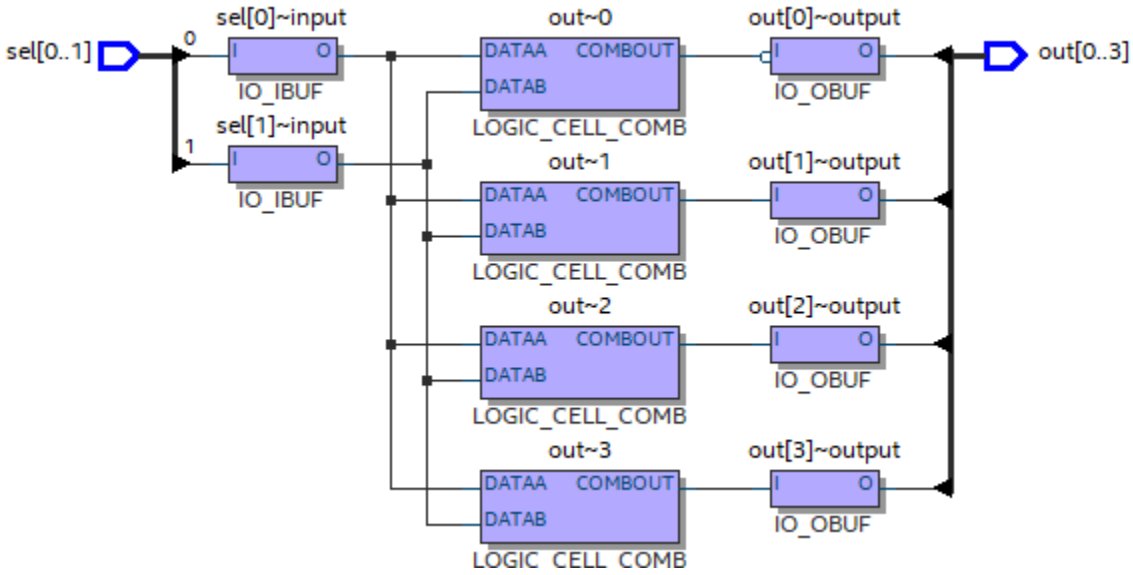
decoder_2to4_dataflow.sv

```
// 2to4 Decoder dataflow level code
module decoder(
 input  logic[1:0] sel,
 output logic[3:0] out
);
 assign out[0] = (!sel[0]) && (!sel[1]); // When sel = 00, out[0] is 1
 assign out[1] = (sel[0]) && (!sel[1]);  // When sel = 01, out[1] is 1
 assign out[2] = (!sel[0]) && (sel[1]);  // When sel = 10, out[2] is 1
 assign out[3] = (sel[0]) && (sel[1]);   // When sel = 11,

endmodule
```





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Analysis & Synthesis Resource Usage Summary	
Resource	Usage
Estimated ALUTs Used	4
-- Combinational ALUTs	4
-- Memory ALUTs	0
-- LUT_REGs	0
Dedicated logic registers	0
Estimated ALUTs Unavailable	0
-- Due to unpartnered combinational logic	0
-- Due to Memory ALUTs	0
Total combinational functions	4
Combinational ALUT usage by number of inputs	
-- 7 input functions	0
-- 6 input functions	0
-- 5 input functions	0
-- 4 input functions	0
-- <=3 input functions	4
Combinational ALUTs by mode	
-- normal mode	4
-- extended LUT mode	0
-- arithmetic mode	0
-- shared arithmetic mode	0
Estimated ALUT/register pairs used	4
Total registers	0
-- Dedicated logic registers	0
-- I/O registers	0
-- LUT_REGs	0
I/O pins	6
DSP block 18-bit elements	0
Maximum fan-out node	sel[0]~input
Maximum fan-out	4
Total fan-out	18
Average fan-out	1.13

Number of ALUTs: 4 (6 I/O pins)
The dataflow model of the 2-to-4 decoder requires 4 ALUTs. Each output (out[0] to out[3]) is a distinct Boolean function based on the two input bits (sel[1:0]). Each ALUT implements one of these 2-input Boolean functions, leading to a total of 4 ALUTs for the design.

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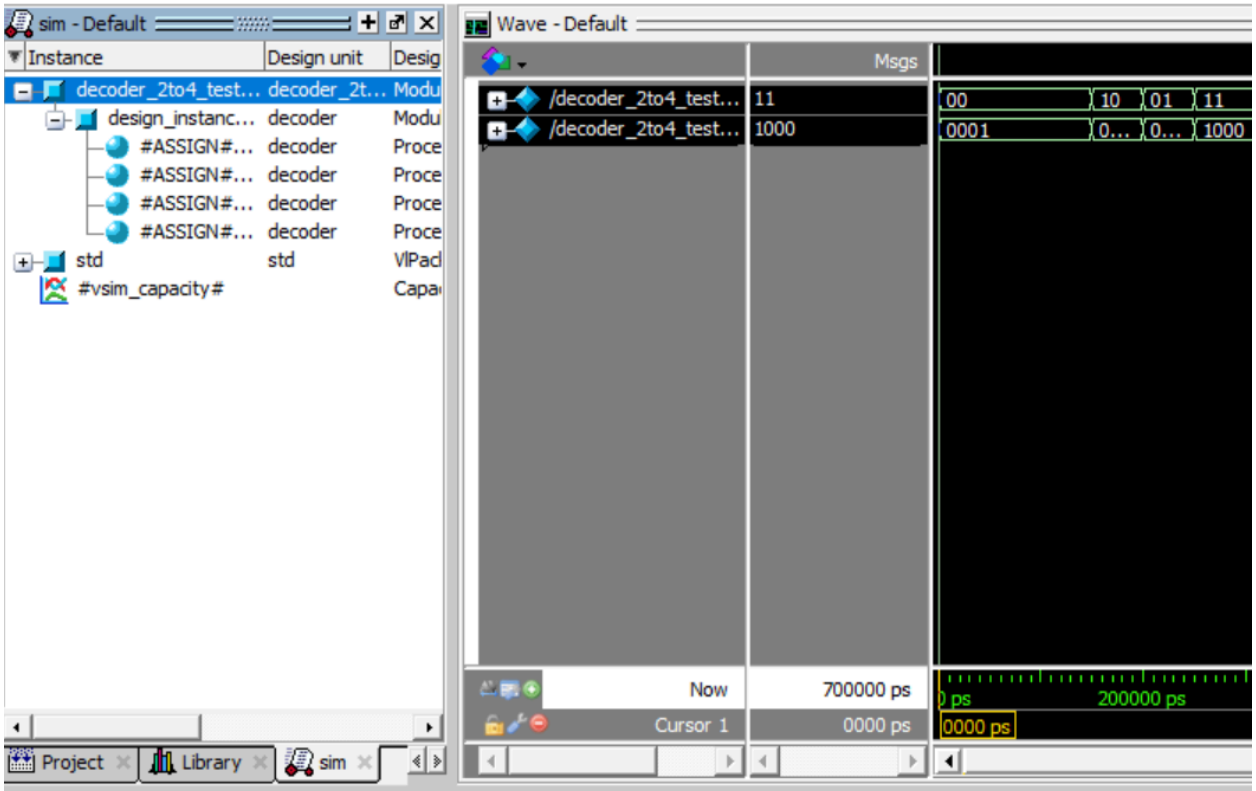

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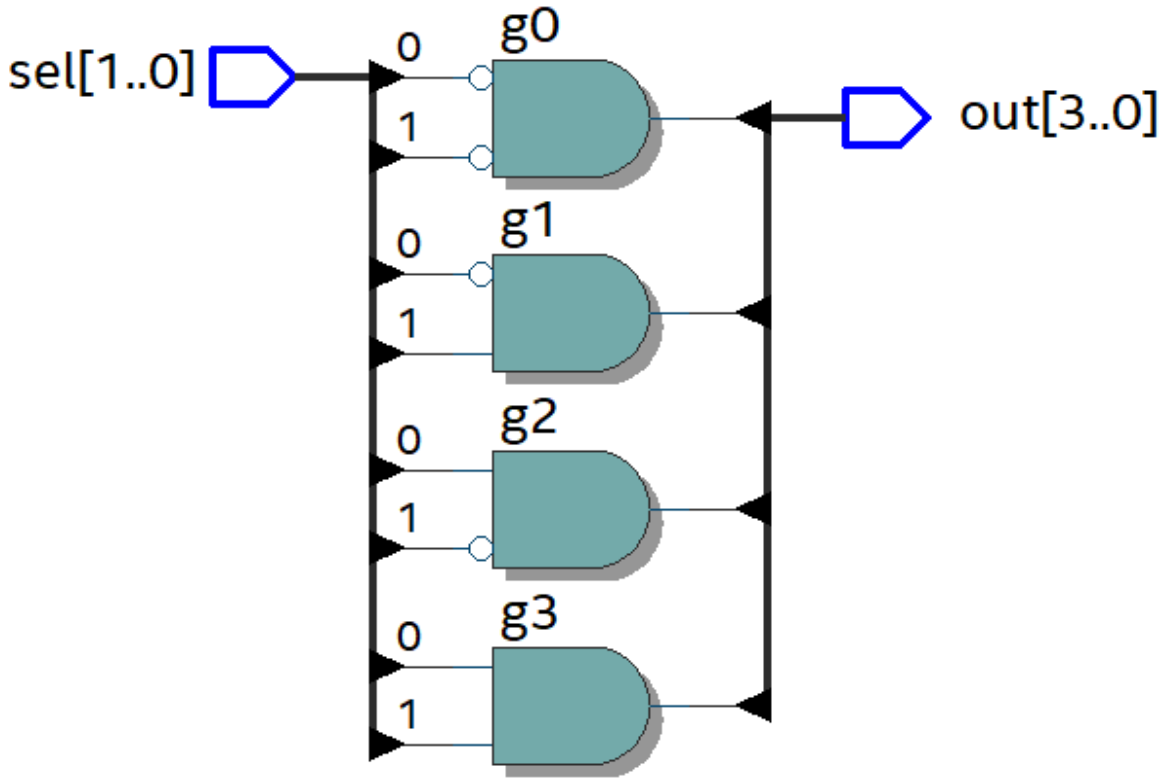
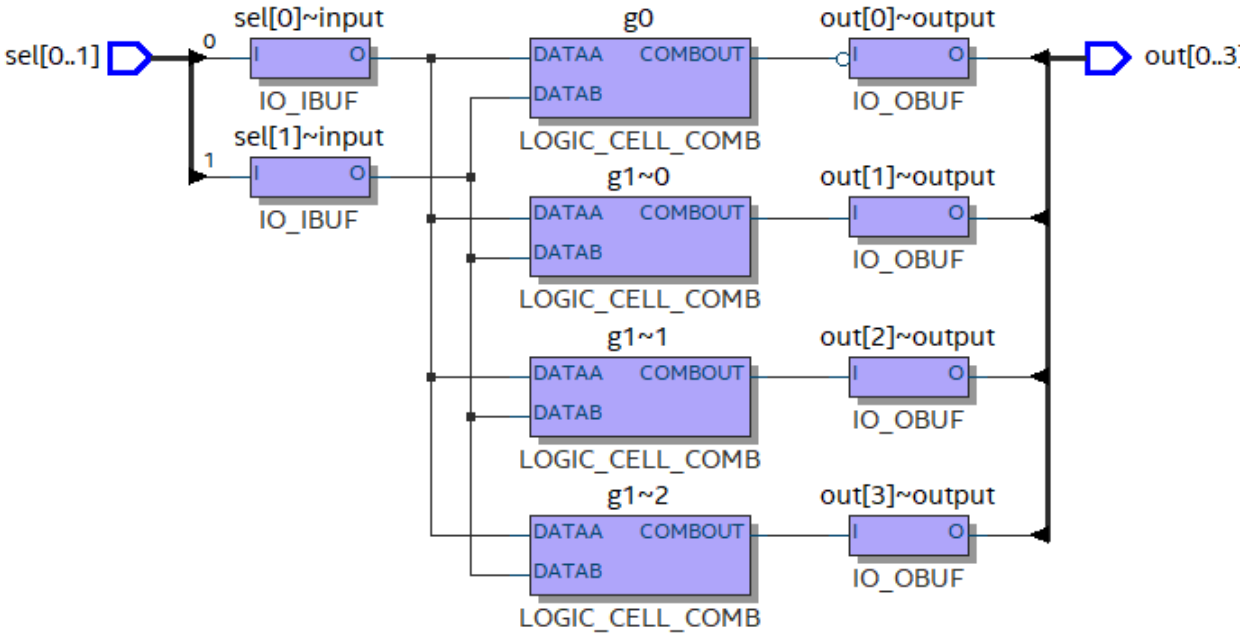
decoder_2to4_gate.sv





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Analysis & Synthesis Resource Usage Summary	
Resource	Usage
Estimated ALUTs Used	4
-- Combinational ALUTs	4
-- Memory ALUTs	0
-- LUT_REGs	0
Dedicated logic registers	0
Estimated ALUTs Unavailable	0
-- Due to unpartnered combinational logic	0
-- Due to Memory ALUTs	0
Total combinational functions	4
Combinational ALUT usage by number of inputs	
-- 7 input functions	0
-- 6 input functions	0
-- 5 input functions	0
-- 4 input functions	0
-- <=3 input functions	4
Combinational ALUTs by mode	
-- normal mode	4
-- extended LUT mode	0
-- arithmetic mode	0
-- shared arithmetic mode	0
Estimated ALUT/register pairs used	4
Total registers	0
-- Dedicated logic registers	0
-- I/O registers	0
-- LUT_REGs	0
I/O pins	6
DSP block 18-bit elements	0
Maximum fan-out node	sel[0]~input
Maximum fan-out	4
Total fan-out	18
Average fan-out	1.13

Number of ALUTs: 4 (6 I/O pins)
In the gate-level model, each output (out[0] to out[3]) is implemented using AND and NOT gates. Each output corresponds to a 2-input Boolean function that requires one ALUT to map the logic. Since there are 4 outputs, the design uses 4 ALUTs - one for each of the four AND gate combinations.

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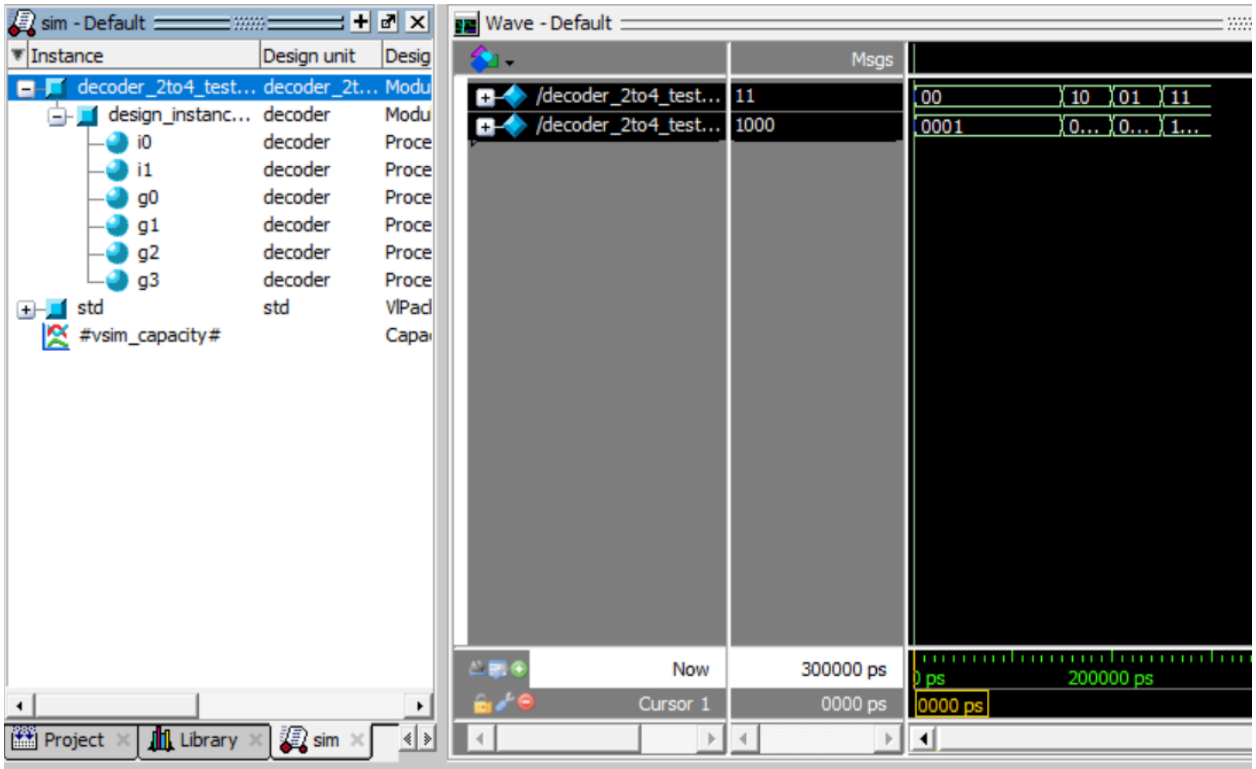

Transcript

```
# Start time: 22:35:15 on Oct 11,2024
# Loading sv_std.std
# Loading work.decoder_2to4_testbench
# Loading work.decoder
add wave sim:/decoder_2to4_testbench/*
VSIM 6> run
#  time=0,  sel=00   out=0001
#
run
#  time=150,  sel=10   out=0010
#
VSIM 7> run
#  time=200,  sel=01   out=0100
#
#  time=250,  sel=11   out=1000
```

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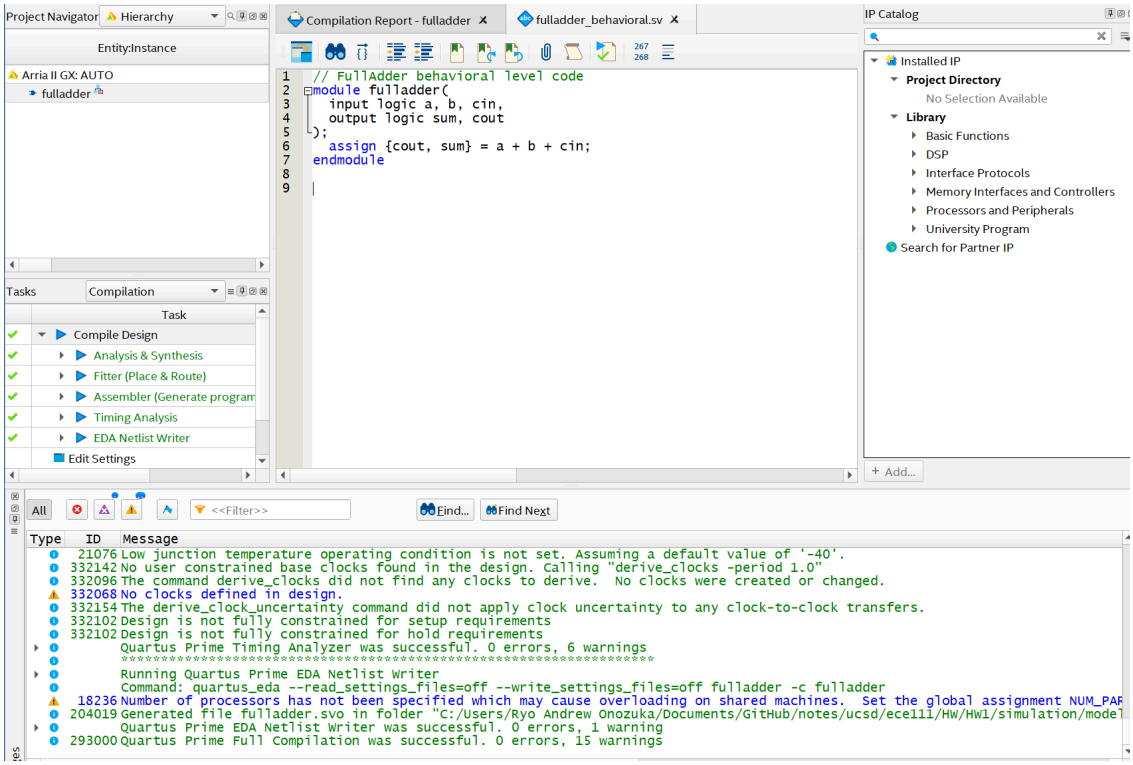
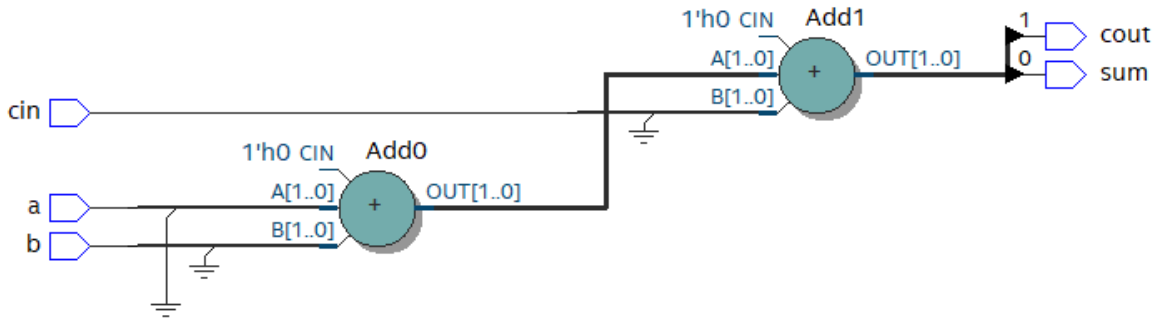
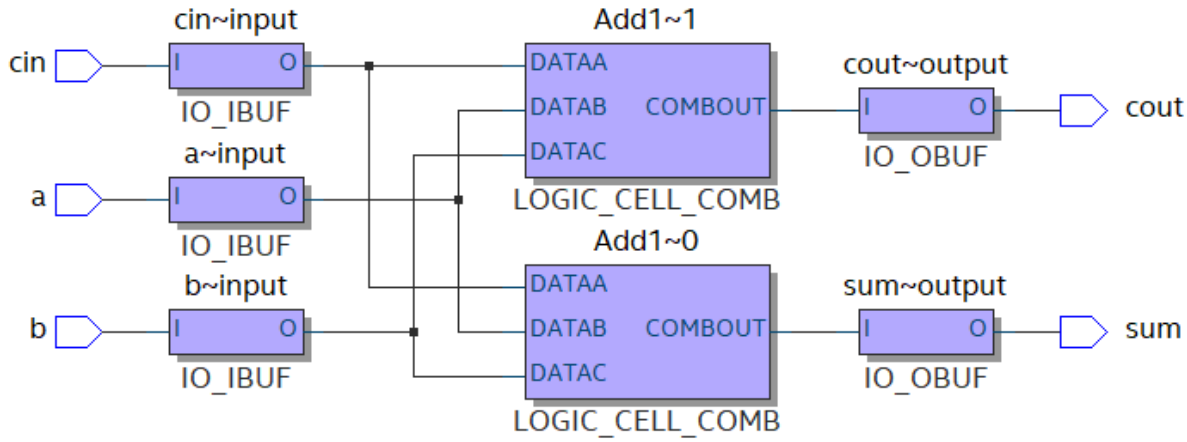
fulladder_behavioral.sv







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Analysis & Synthesis Resource Usage Summary	
Resource	Usage
Estimated ALUTs Used	2
-- Combinational ALUTs	2
-- Memory ALUTs	0
-- LUT_REGs	0
Dedicated logic registers	0
Estimated ALUTs Unavailable	0
-- Due to unpartnered combinational logic	0
-- Due to Memory ALUTs	0
Total combinational functions	2
Combinational ALUT usage by number of inputs	
-- 7 input functions	0
-- 6 input functions	0
-- 5 input functions	0
-- 4 input functions	0
-- <=3 input functions	2
Combinational ALUTs by mode	
-- normal mode	2
-- extended LUT mode	0
-- arithmetic mode	0
-- shared arithmetic mode	0
Estimated ALUT/register pairs used	2
Total registers	0
-- Dedicated logic registers	0
-- I/O registers	0
-- LUT_REGs	0
I/O pins	5
DSP block 18-bit elements	0
Maximum fan-out node	cin~input
Maximum fan-out	2
Total fan-out	13
Average fan-out	1.08

Number of ALUTs: 2 (5 I/O pins)
The full adder uses 2 combinational ALUTs to implement the sum and carry outputs. Both outputs are derived from 3-input Boolean functions (a, b, and cin), with each function requiring one ALUT. The design has no memory elements or registers, and the I/O pins correspond to the 3 inputs (a, b, cin) and 2 outputs (sum, carry).

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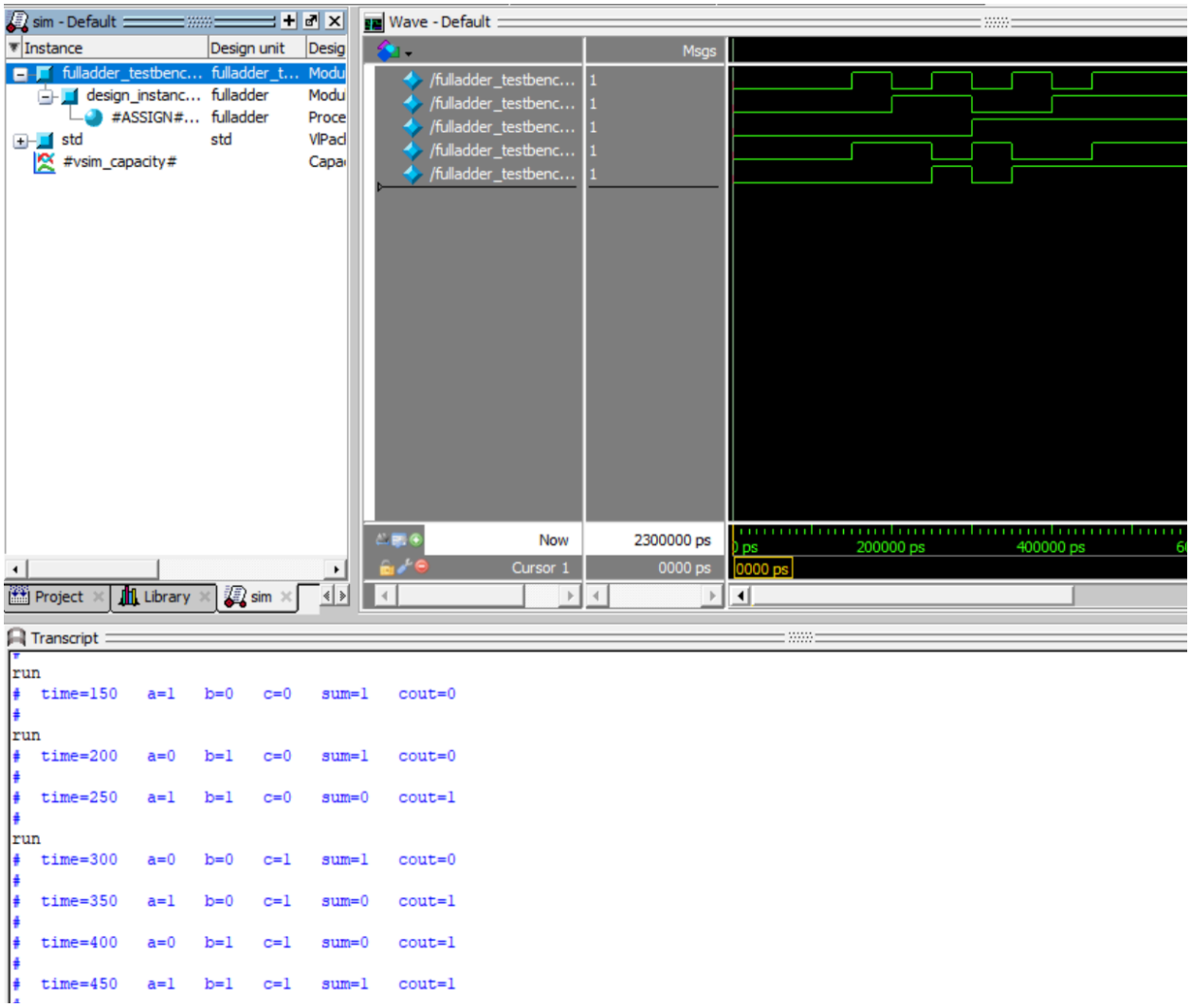

simulation same for fulladder_behavioral.sv, fulladder_dataflow.sv, fulladder_gate.sv

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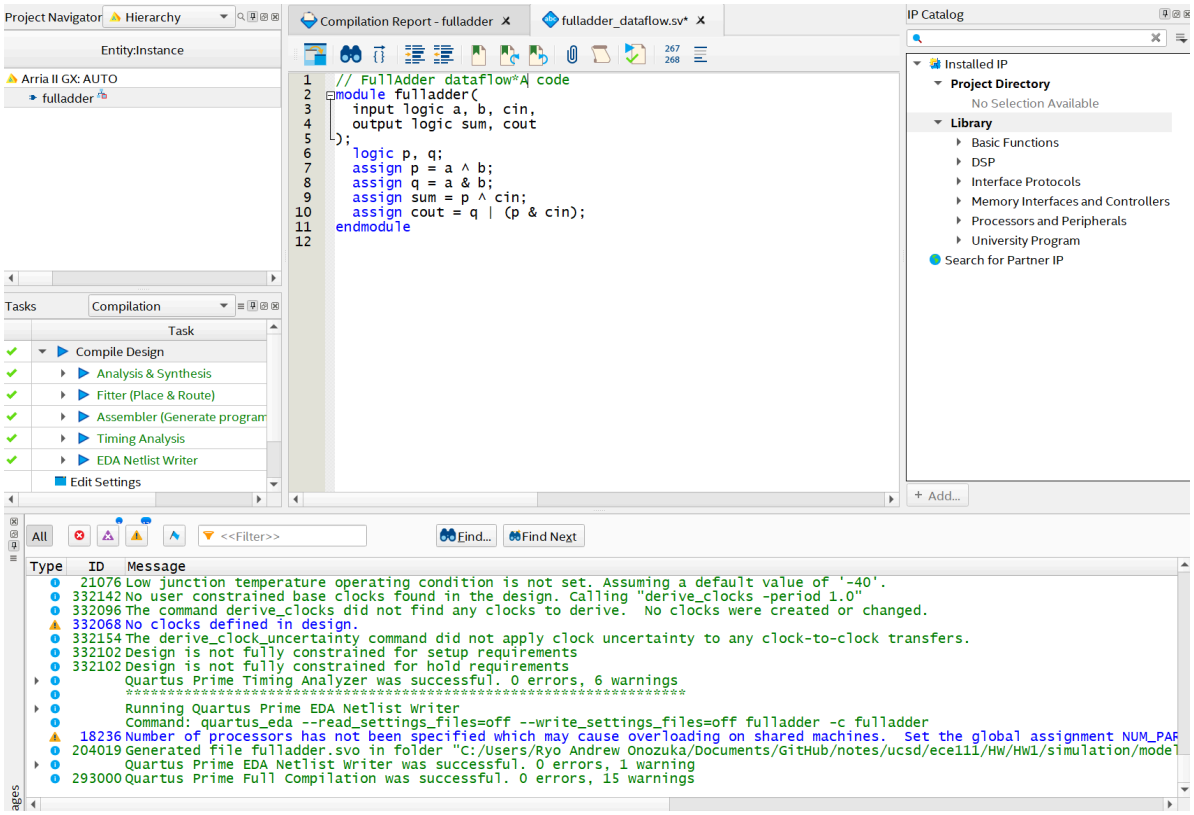
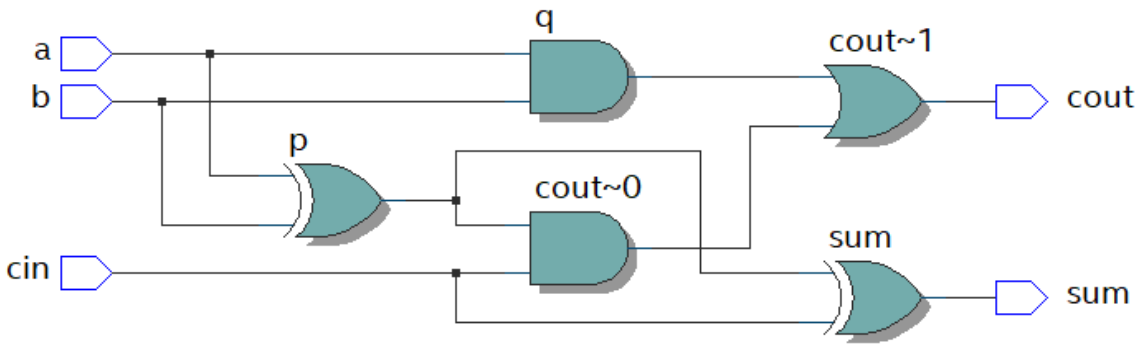
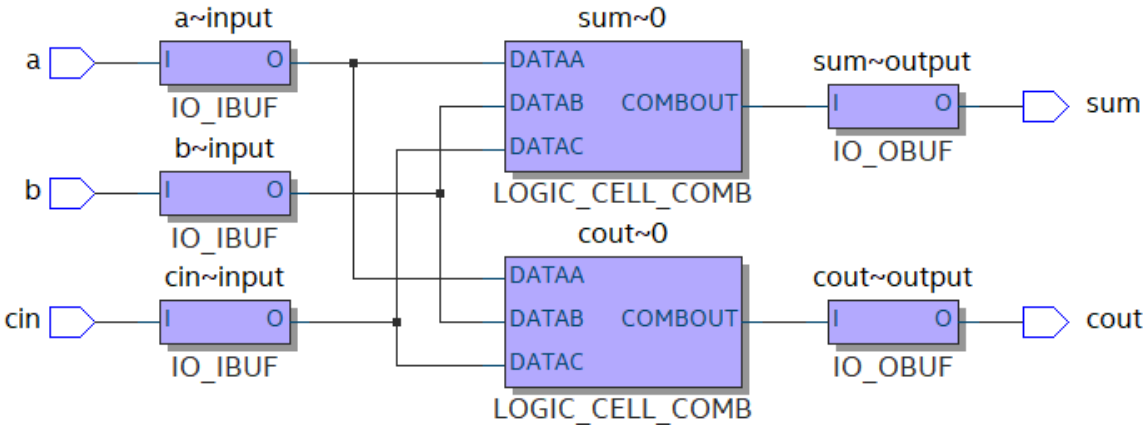
fulladder_dataflow.sv







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Analysis & Synthesis Resource Usage Summary	
Resource	Usage
Estimated ALUTs Used	2
-- Combinational ALUTs	2
-- Memory ALUTs	0
-- LUT_REGs	0
Dedicated logic registers	0
Estimated ALUTs Unavailable	0
-- Due to unpartnered combinational logic	0
-- Due to Memory ALUTs	0
Total combinational functions	2
Combinational ALUT usage by number of inputs	
-- 7 input functions	0
-- 6 input functions	0
-- 5 input functions	0
-- 4 input functions	0
-- <=3 input functions	2
Combinational ALUTs by mode	
-- normal mode	2
-- extended LUT mode	0
-- arithmetic mode	0
-- shared arithmetic mode	0
Estimated ALUT/register pairs used	2
Total registers	0
-- Dedicated logic registers	0
-- I/O registers	0
-- LUT_REGs	0
I/O pins	5
DSP block 18-bit elements	0
Maximum fan-out node	a~input
Maximum fan-out	2
Total fan-out	13
Average fan-out	1.08

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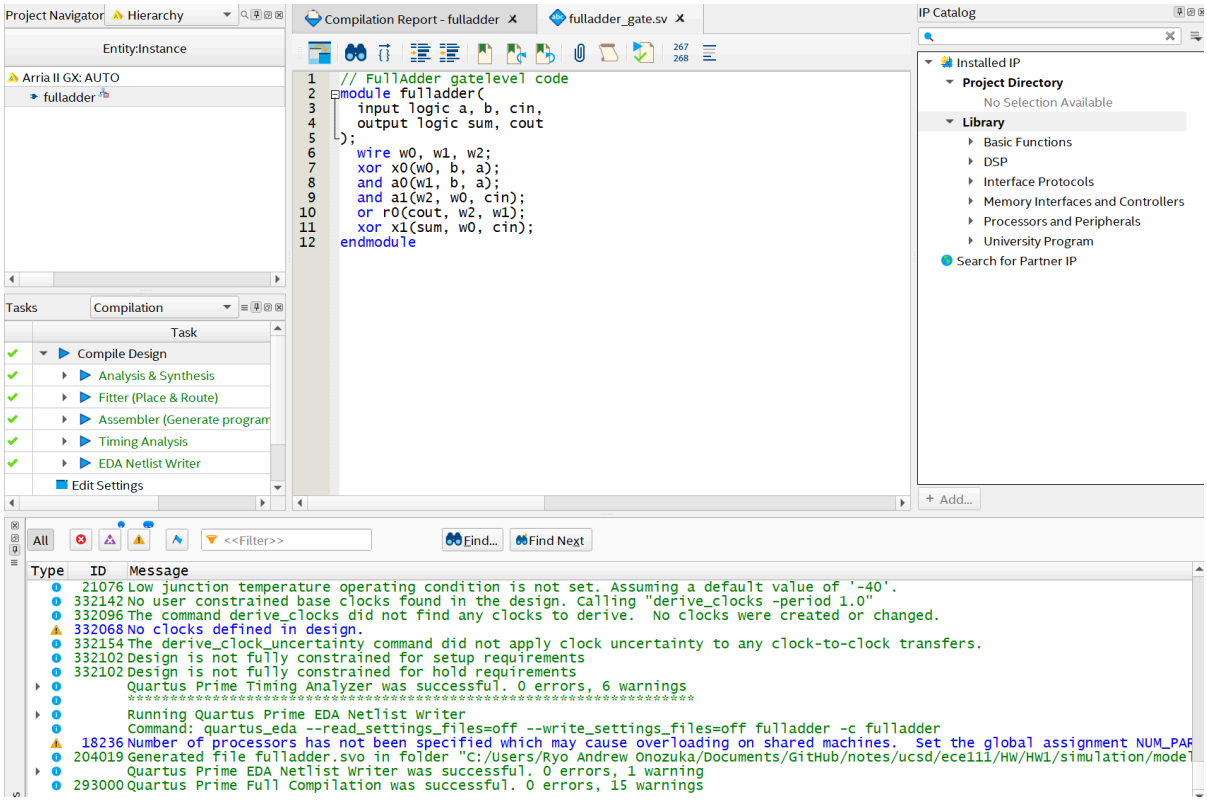
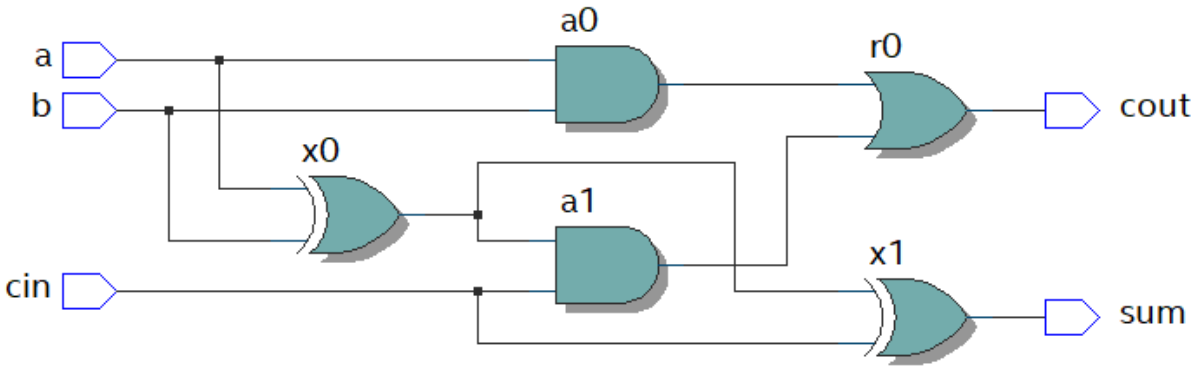
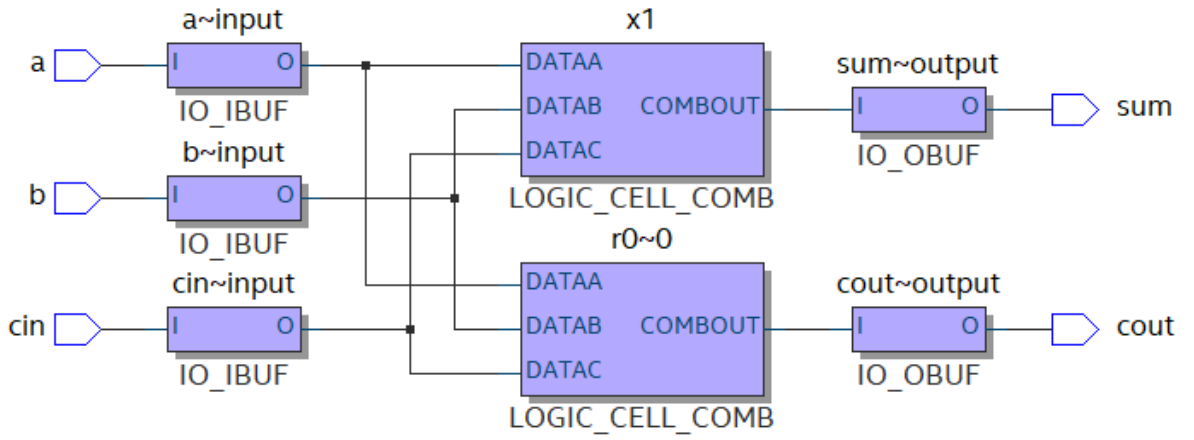
fulladder_gate.sv







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Analysis & Synthesis Resource Usage Summary	
Resource	Usage
Estimated ALUTs Used	2
-- Combinational ALUTs	2
-- Memory ALUTs	0
-- LUT_REGs	0
Dedicated logic registers	0
Estimated ALUTs Unavailable	0
-- Due to unpartnered combinational logic	0
-- Due to Memory ALUTs	0
Total combinational functions	2
Combinational ALUT usage by number of inputs	
-- 7 input functions	0
-- 6 input functions	0
-- 5 input functions	0
-- 4 input functions	0
-- <=3 input functions	2
Combinational ALUTs by mode	
-- normal mode	2
-- extended LUT mode	0
-- arithmetic mode	0
-- shared arithmetic mode	0
Estimated ALUT/register pairs used	2
Total registers	0
-- Dedicated logic registers	0
-- I/O registers	0
-- LUT_REGs	0
I/O pins	5
DSP block 18-bit elements	0
Maximum fan-out node	a~input
Maximum fan-out	2
Total fan-out	13
Average fan-out	1.08

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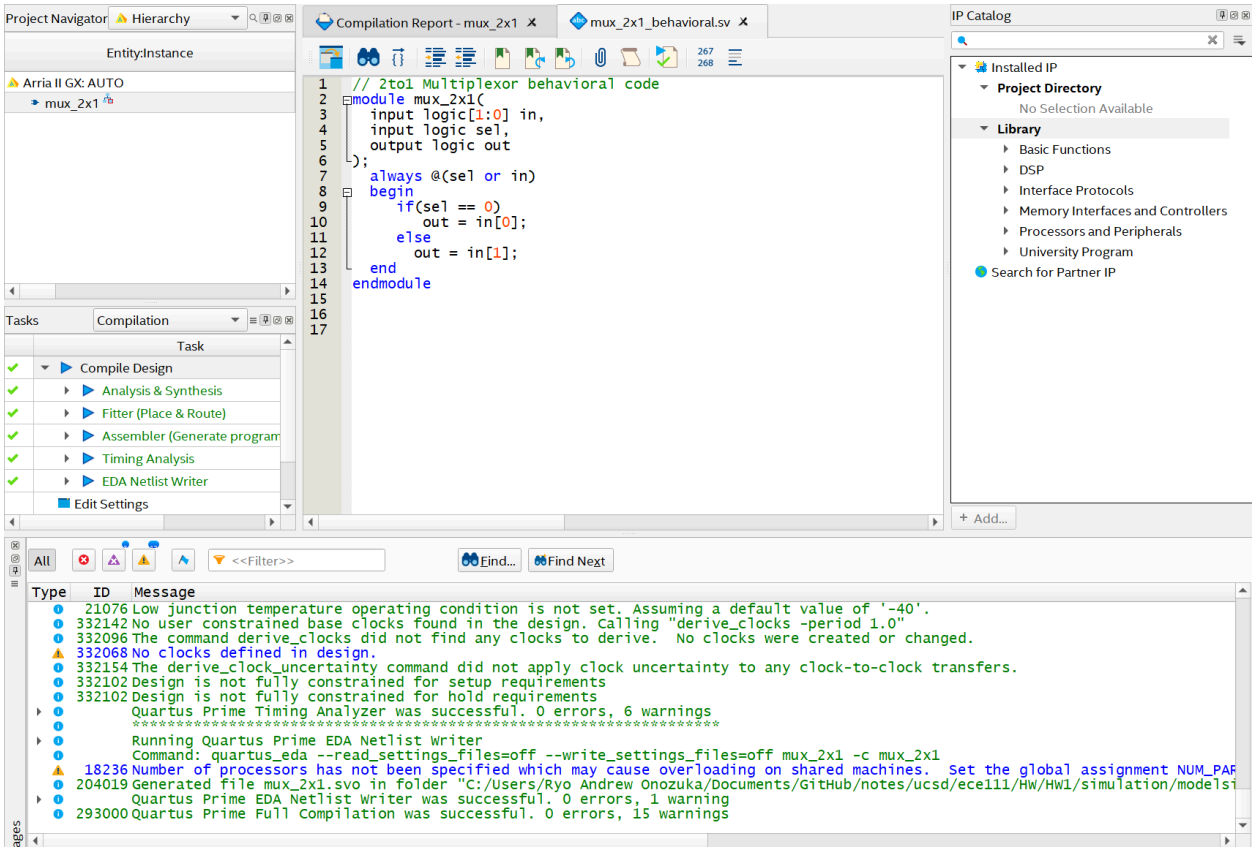
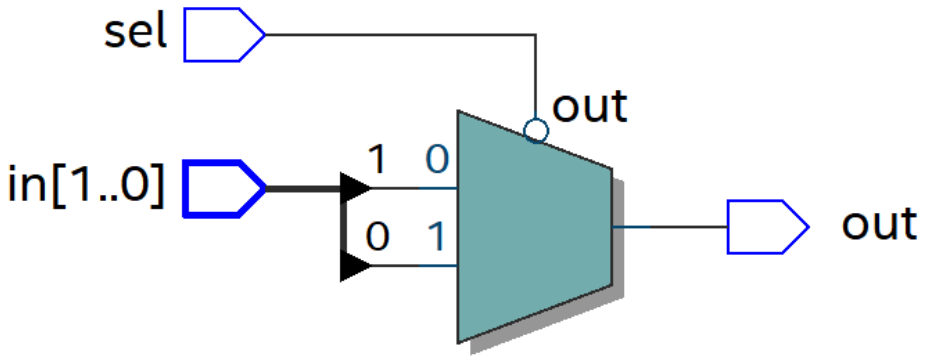
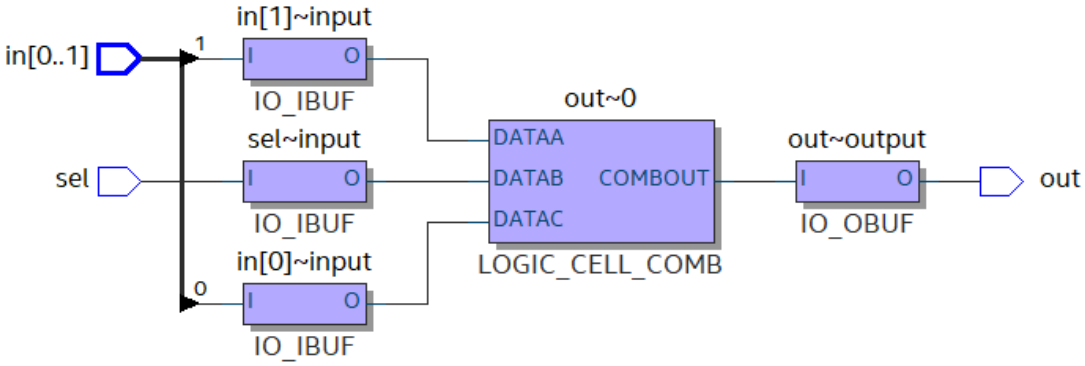
mux_2x1_behavioral.sv







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Analysis & Synthesis Resource Usage Summary	
Resource	Usage
Estimated ALUTs Used	1
-- Combinational ALUTs	1
-- Memory ALUTs	0
-- LUT_REGs	0
Dedicated logic registers	0
Estimated ALUTs Unavailable	0
-- Due to unpartnered combinational logic	0
-- Due to Memory ALUTs	0
Total combinational functions	1
Combinational ALUT usage by number of inputs	
-- 7 input functions	0
-- 6 input functions	0
-- 5 input functions	0
-- 4 input functions	0
-- <=3 input functions	1
Combinational ALUTs by mode	
-- normal mode	1
-- extended LUT mode	0
-- arithmetic mode	0
-- shared arithmetic mode	0
Estimated ALUT/register pairs used	1
Total registers	0
-- Dedicated logic registers	0
-- I/O registers	0
-- LUT_REGs	0
I/O pins	4
DSP block 18-bit elements	0
Maximum fan-out node	out~0
Maximum fan-out	1
Total fan-out	8
Average fan-out	0.89

Number of ALUTs: 1 (4 I/O pins)
The 2-to-1 MUX uses 1 ALUT to implement the Boolean function out = (sel & b) | (!sel & a), which maps the selection logic between inputs a and b based on sel. Since it is a simple 3-input function, only one ALUT is required to perform the logic operation.

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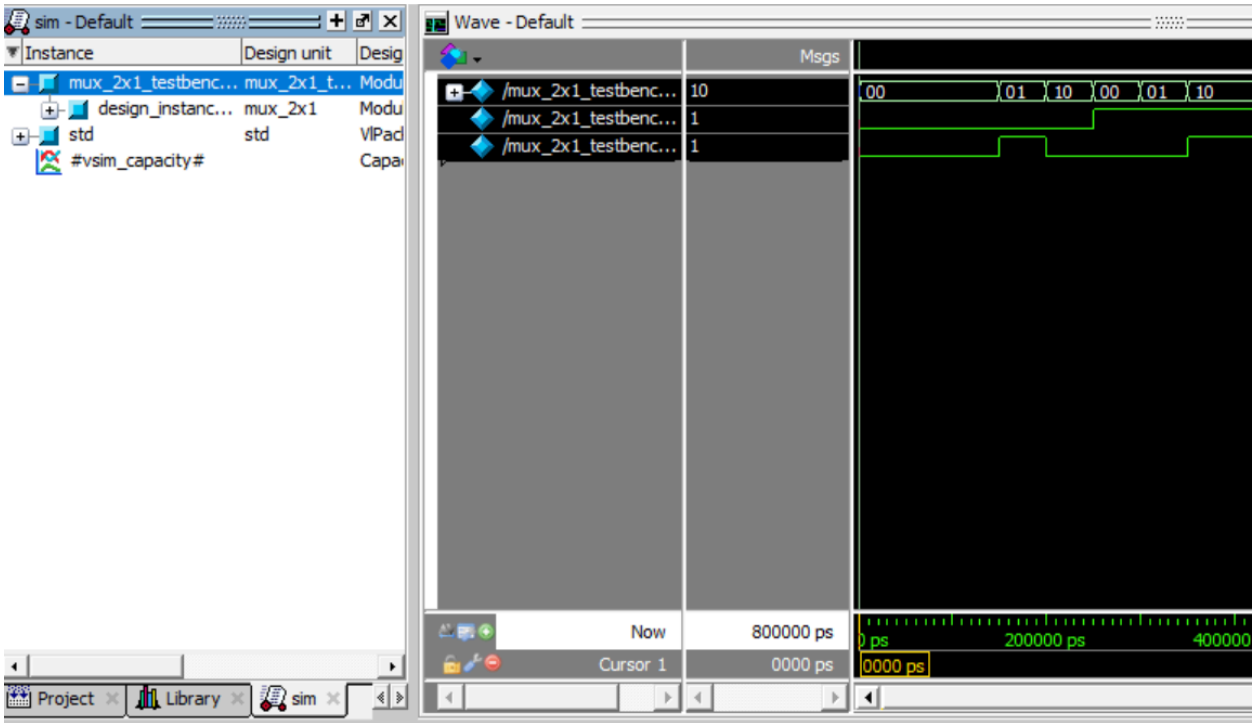

simulation same for mux_2x1_behavioral.sv, mux_2x1_dataflow.sv, mux_2x1_gate.sv

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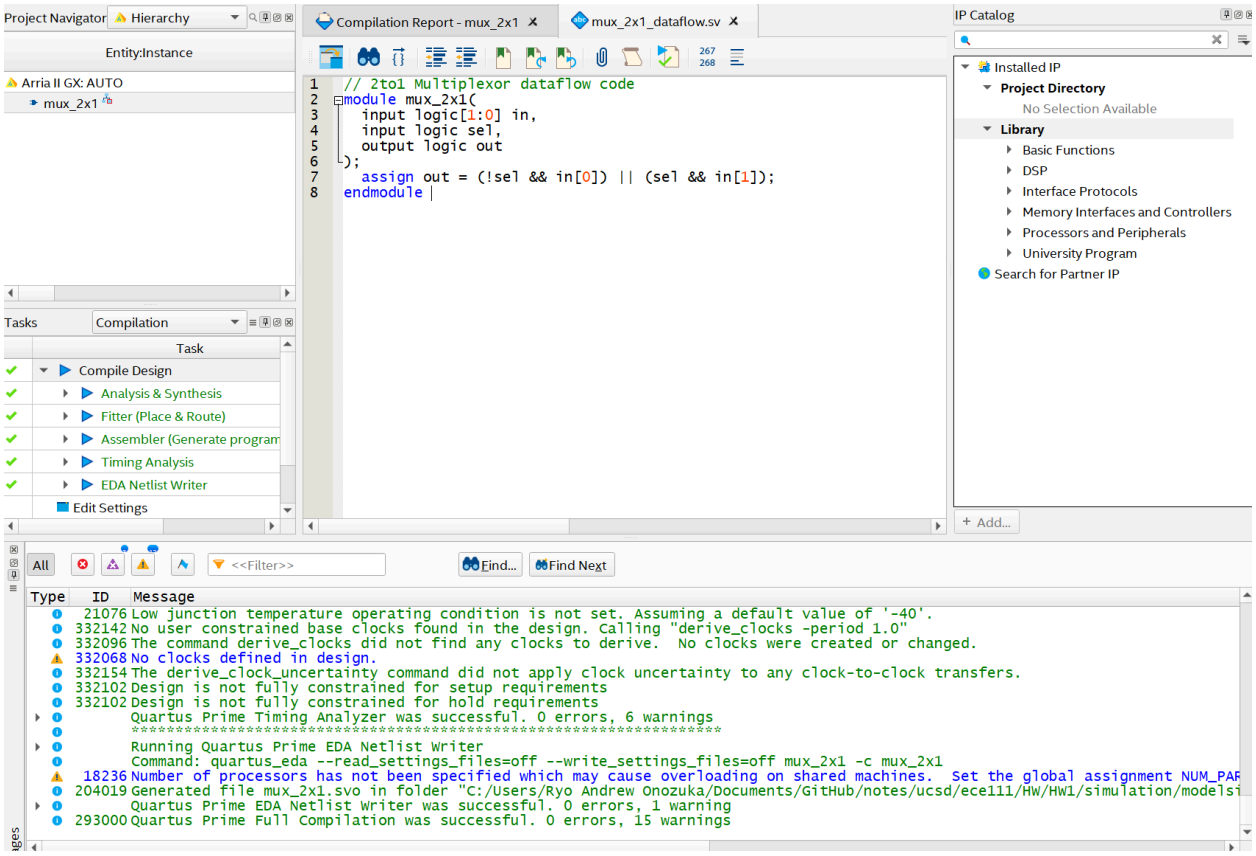
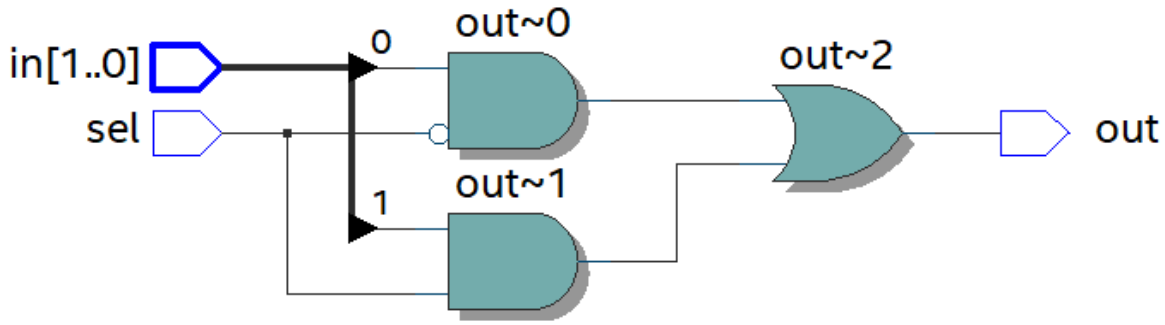
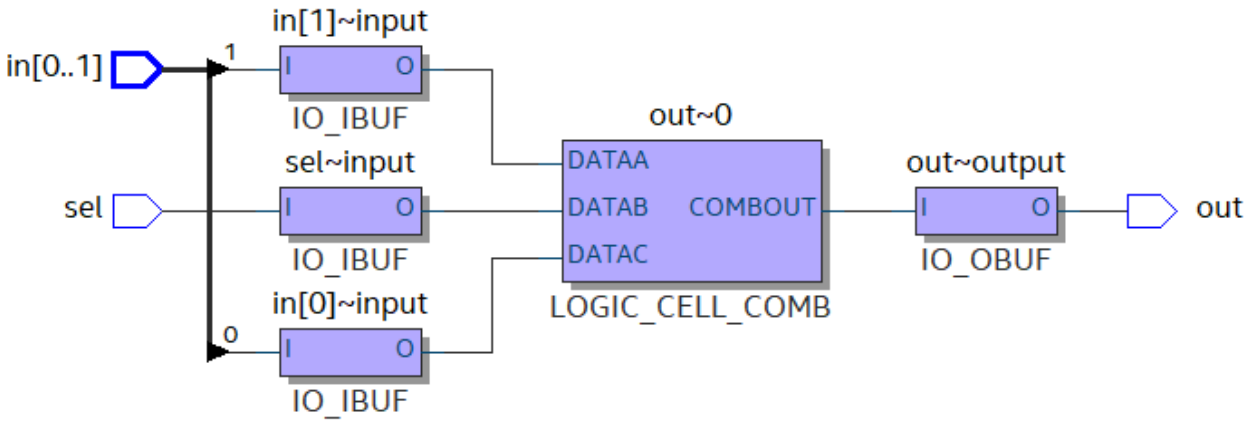
mux_2x1_dataflow.sv







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Analysis & Synthesis Resource Usage Summary	
Resource	Usage
Estimated ALUTs Used	1
-- Combinational ALUTs	1
-- Memory ALUTs	0
-- LUT_REGs	0
Dedicated logic registers	0
Estimated ALUTs Unavailable	0
-- Due to unpartnered combinational logic	0
-- Due to Memory ALUTs	0
Total combinational functions	1
Combinational ALUT usage by number of inputs	
-- 7 input functions	0
-- 6 input functions	0
-- 5 input functions	0
-- 4 input functions	0
-- <=3 input functions	1
Combinational ALUTs by mode	
-- normal mode	1
-- extended LUT mode	0
-- arithmetic mode	0
-- shared arithmetic mode	0
Estimated ALUT/register pairs used	1
Total registers	0
-- Dedicated logic registers	0
-- I/O registers	0
-- LUT_REGs	0
I/O pins	4
DSP block 18-bit elements	0
Maximum fan-out node	out~0
Maximum fan-out	1
Total fan-out	8
Average fan-out	0.89

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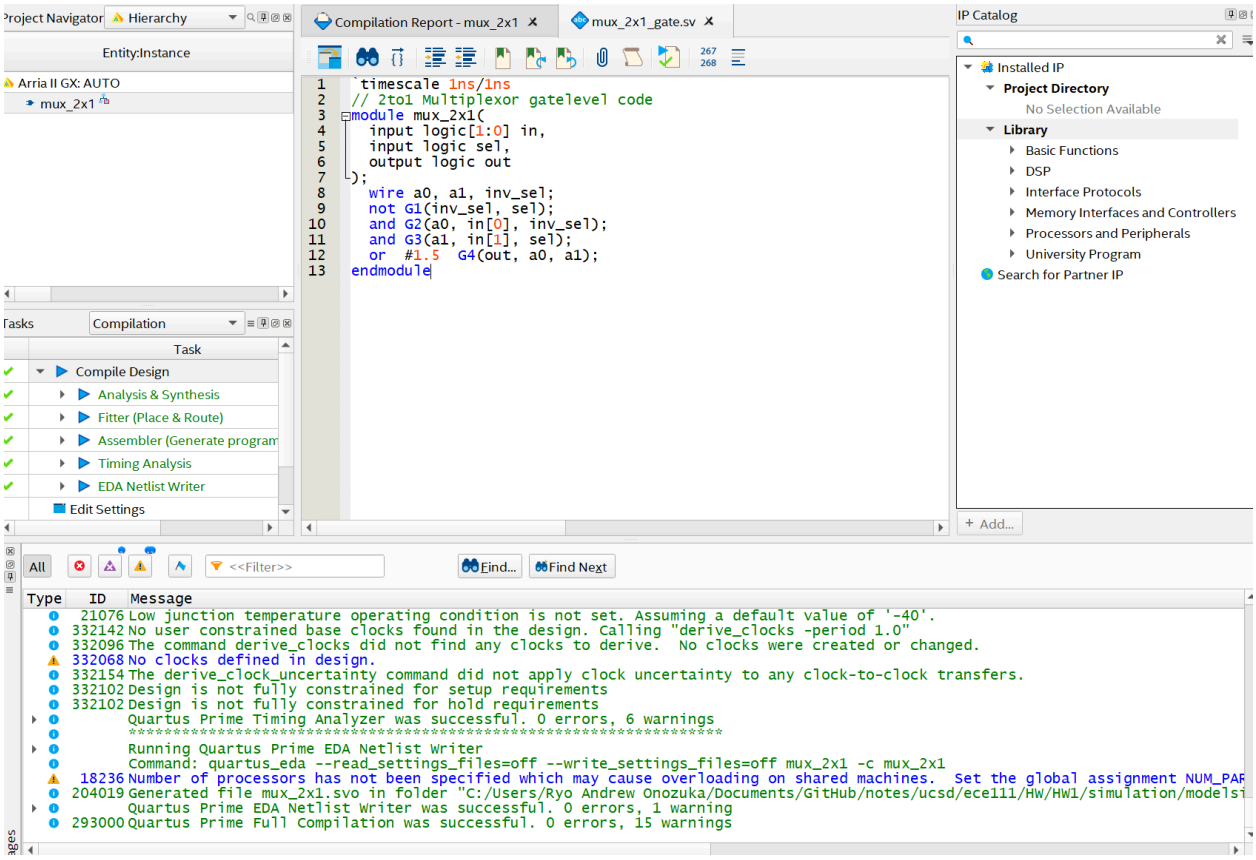
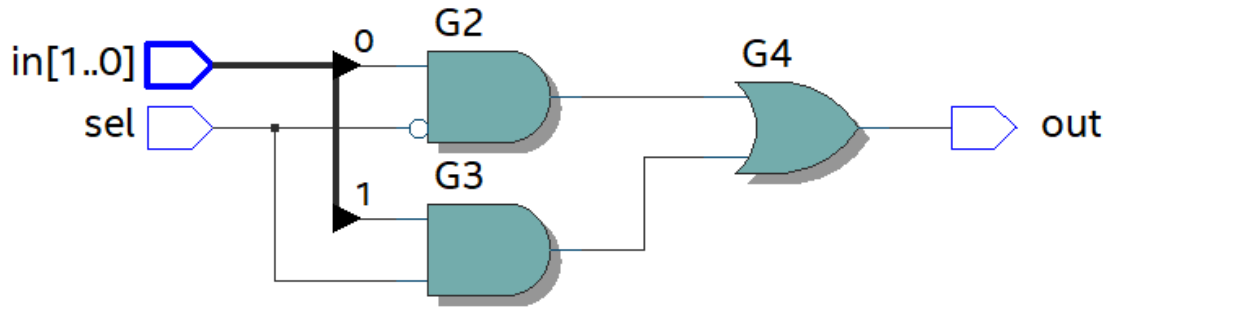
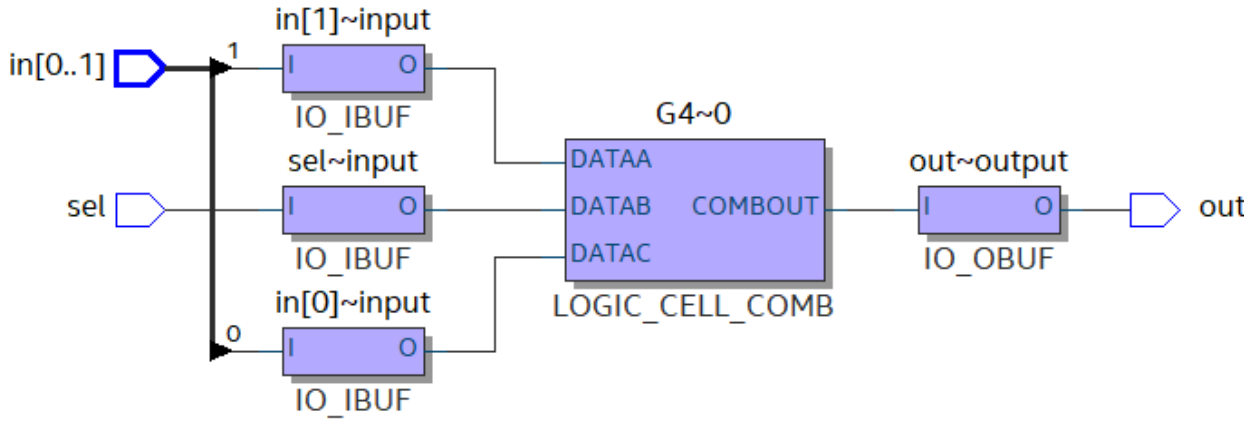
mux_2x1_gate.sv







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Analysis & Synthesis Resource Usage Summary	
Resource	Usage
Estimated ALUTs Used	1
-- Combinational ALUTs	1
-- Memory ALUTs	0
-- LUT_REGs	0
Dedicated logic registers	0
Estimated ALUTs Unavailable	0
-- Due to unpartnered combinational logic	0
-- Due to Memory ALUTs	0
Total combinational functions	1
Combinational ALUT usage by number of inputs	
-- 7 input functions	0
-- 6 input functions	0
-- 5 input functions	0
-- 4 input functions	0
-- <=3 input functions	1
Combinational ALUTs by mode	
-- normal mode	1
-- extended LUT mode	0
-- arithmetic mode	0
-- shared arithmetic mode	0
Estimated ALUT/register pairs used	1
Total registers	0
-- Dedicated logic registers	0
-- I/O registers	0
-- LUT_REGs	0
I/O pins	4
DSP block 18-bit elements	0
Maximum fan-out node	G4~0
Maximum fan-out	1
Total fan-out	8
Average fan-out	0.89