

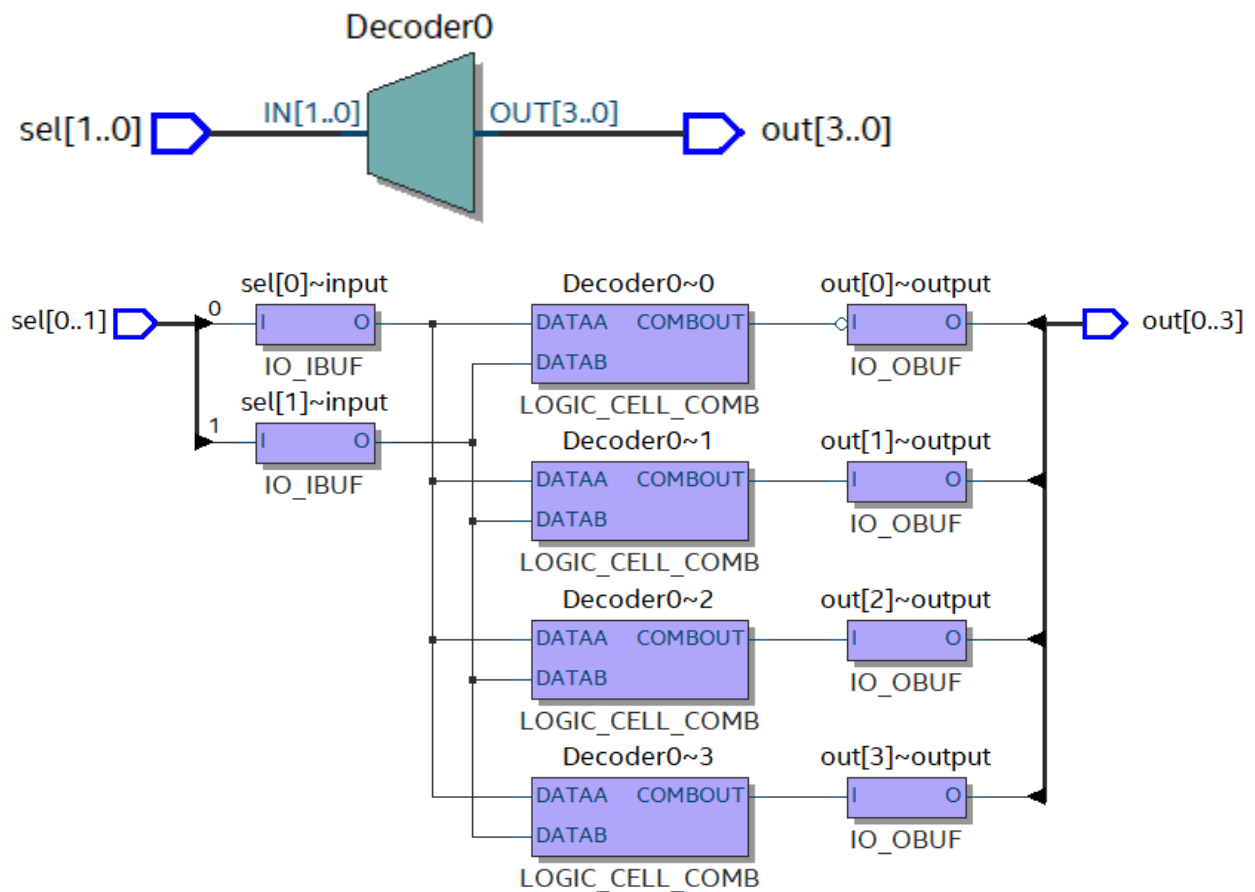
I chose option one, making the behavioral and dataflow match the gate-level implementation, thus the observable waveforms are the same.

decoder_2to4_behavioral.sv

```

1  // 2to4 Decoder behavioral level code
2  module decoder(
3      input  logic[1:0] sel,
4      output logic[3:0] out
5  );
6      always @(sel)
7          begin
8              case (sel)
9                  2'b00 : out = 4'b0001; // Output for sel = 00
10                 2'b01 : out = 4'b0010; // Output for sel = 01
11                 2'b10 : out = 4'b0100; // Output for sel = 10
12                 2'b11 : out = 4'b1000; // Output for sel = 11
13                 default: out = 4'b0000; // Default case
14             endcase
15         end
16     endmodule

```



```

ucsd > ece111 > HW > HW1 > ≡ decoder-Resource Usage Summary.rpt
33  +-----+
34  ; Analysis & Synthesis Resource Usage Summary ;
35  +-----+-----+
36  ; Resource ; Usage ;
37  +-----+-----+
38  ; Estimated ALUTs Used ; 4 ;
39  ; -- Combinational ALUTs ; 4 ;
40  ; -- Memory ALUTs ; 0 ;
41  ; -- LUT_REGS ; 0 ;
42  ; Dedicated logic registers ; 0 ;
43  ; ; ;
44  ; Estimated ALUTs Unavailable ; 0 ;
45  ; -- Due to unpartnered combinational logic ; 0 ;
46  ; -- Due to Memory ALUTs ; 0 ;
47  ; ; ;
48  ; Total combinational functions ; 4 ;
49  ; Combinational ALUT usage by number of inputs ; ;
50  ; -- 7 input functions ; 0 ;
51  ; -- 6 input functions ; 0 ;
52  ; -- 5 input functions ; 0 ;
53  ; -- 4 input functions ; 0 ;
54  ; -- <=3 input functions ; 4 ;
55  ; ; ;
56  ; Combinational ALUTs by mode ; ;
57  ; -- normal mode ; 4 ;
58  ; -- extended LUT mode ; 0 ;
59  ; -- arithmetic mode ; 0 ;
60  ; -- shared arithmetic mode ; 0 ;
61  ; ; ;
62  ; Estimated ALUT/register pairs used ; 4 ;
63  ; ; ;
64  ; Total registers ; 0 ;
65  ; -- Dedicated logic registers ; 0 ;
66  ; -- I/O registers ; 0 ;
67  ; -- LUT_REGS ; 0 ;
68  ; ; ;
69  ; ; ;
70  ; I/O pins ; 6 ;
71  ; ; ;
72  ; DSP block 18-bit elements ; 0 ;
73  ; ; ;
74  ; Maximum fan-out node ; sel[0]~input ;
75  ; Maximum fan-out ; 4 ;
76  ; Total fan-out ; 18 ;
77  ; Average fan-out ; 1.13 ;
78  +-----+-----+

```

Number of ALUTs: 4 (6 I/O pins)

The 2-to-4 decoder requires 4 ALUTs, with each ALUT implementing one of the four output functions. Each output function depends on the two inputs (sel[1:0]), and each ALUT handles a 2-input Boolean function to determine when an output is active.

The screenshot displays a Verilog simulation environment with the following components:

- Instance Panel:** Shows the hierarchy of the simulation, including `decoder_2to4_test...`, `design_instanc...`, `#ALWAYS#...`, `std`, and `#vsim_capacity#`.
- Wave Panel:** Displays the simulation results for `/decoder_2to4_test...`. The waveforms show the output `out` for different select inputs `sel`. The output values are: `00` for `sel=00`, `01` for `sel=01`, `10` for `sel=10`, and `11` for `sel=11`. The time scale is 40000 ps.
- Transcript Panel:** Shows the simulation log, including the loading of `sv_std.std`, `work.decoder_2to4_testbench`, and `work.decoder`. The log also shows the results of the simulation runs, such as `time=0, sel=00 out=0001` and `time=250, sel=11 out=1000`.

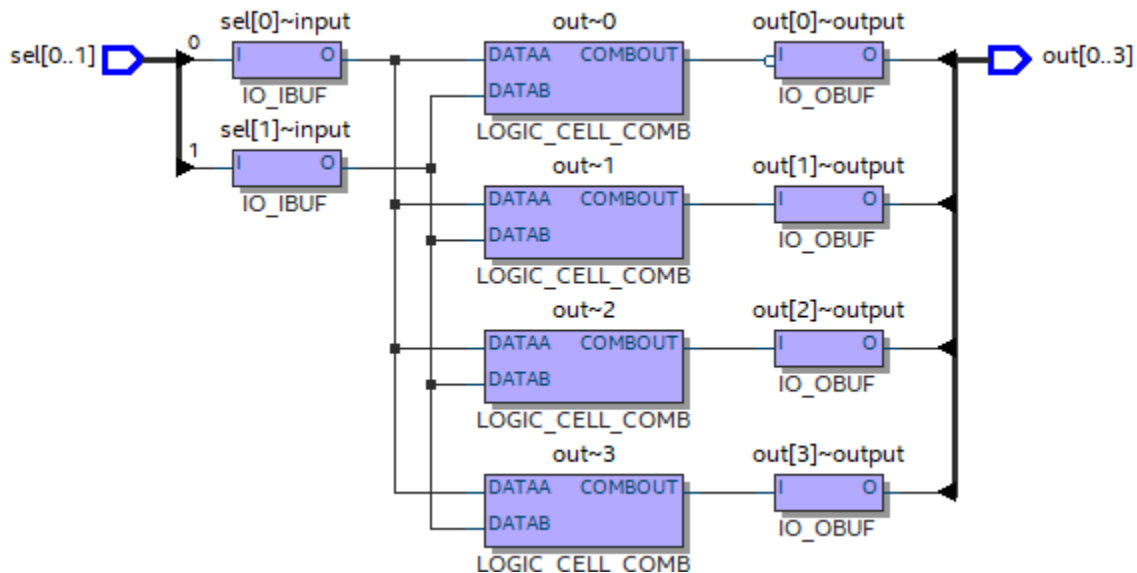
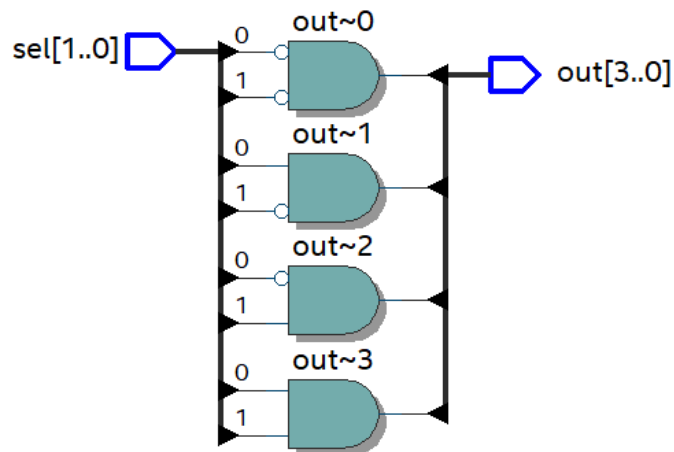
```
# Loading sv_std.std
# Loading work.decoder_2to4_testbench
# Loading work.decoder
VSIM 8> run
# time=0, sel=00 out=0001
#
add wave sim:/decoder_2to4_testbench/*
VSIM 10> run
# time=150, sel=10 out=0100
#
run
# time=200, sel=01 out=0010
#
# time=250, sel=11 out=1000
#
VSIM 11> run
VSIM 11>
```

decoder_2to4_dataflow.sv

```

1  // 2to4 Decoder dataflow level code
2  module decoder(
3      input  logic[1:0] sel,
4      output logic[3:0] out
5  );
6      assign out[0] = (!sel[0]) && (!sel[1]); // When sel = 00, out[0] is 1
7      assign out[1] = (sel[0]) && (!sel[1]); // When sel = 01, out[1] is 1
8      assign out[2] = (!sel[0]) && (sel[1]); // When sel = 10, out[2] is 1
9      assign out[3] = (sel[0]) && (sel[1]); // When sel = 11,
10
11  endmodule

```



```

+-----+
; Analysis & Synthesis Resource Usage Summary ;
+-----+
; Resource ; Usage ;
+-----+
; Estimated ALUTs Used ; 4 ;
; -- Combinational ALUTs ; 4 ;
; -- Memory ALUTs ; 0 ;
; -- LUT_REGS ; 0 ;
; Dedicated logic registers ; 0 ;
; ; ;
; Estimated ALUTs Unavailable ; 0 ;
; -- Due to unpartnered combinational logic ; 0 ;
; -- Due to Memory ALUTs ; 0 ;
; ; ;
; Total combinational functions ; 4 ;
; Combinational ALUT usage by number of inputs ; ;
; -- 7 input functions ; 0 ;
; -- 6 input functions ; 0 ;
; -- 5 input functions ; 0 ;
; -- 4 input functions ; 0 ;
; -- <=3 input functions ; 4 ;
; ; ;
; Combinational ALUTs by mode ; ;
; -- normal mode ; 4 ;
; -- extended LUT mode ; 0 ;
; -- arithmetic mode ; 0 ;
; -- shared arithmetic mode ; 0 ;
; ; ;
; Estimated ALUT/register pairs used ; 4 ;
; ; ;
; Total registers ; 0 ;
; -- Dedicated logic registers ; 0 ;
; -- I/O registers ; 0 ;
; -- LUT_REGS ; 0 ;
; ; ;
; ; ;
; I/O pins ; 6 ;
; ; ;
; DSP block 18-bit elements ; 0 ;
; ; ;
; Maximum fan-out node ; sel[0]~input ;
; Maximum fan-out ; 4 ;
; Total fan-out ; 18 ;
; Average fan-out ; 1.13 ;
+-----+

```

Number of ALUTs: 4 (6 I/O pins)

The dataflow model of the 2-to-4 decoder requires 4 ALUTs. Each output (out[0] to out[3]) is a distinct Boolean function based on the two input bits (sel[1:0]). Each ALUT implements one of these 2-input Boolean functions, leading to a total of 4 ALUTs for the design.

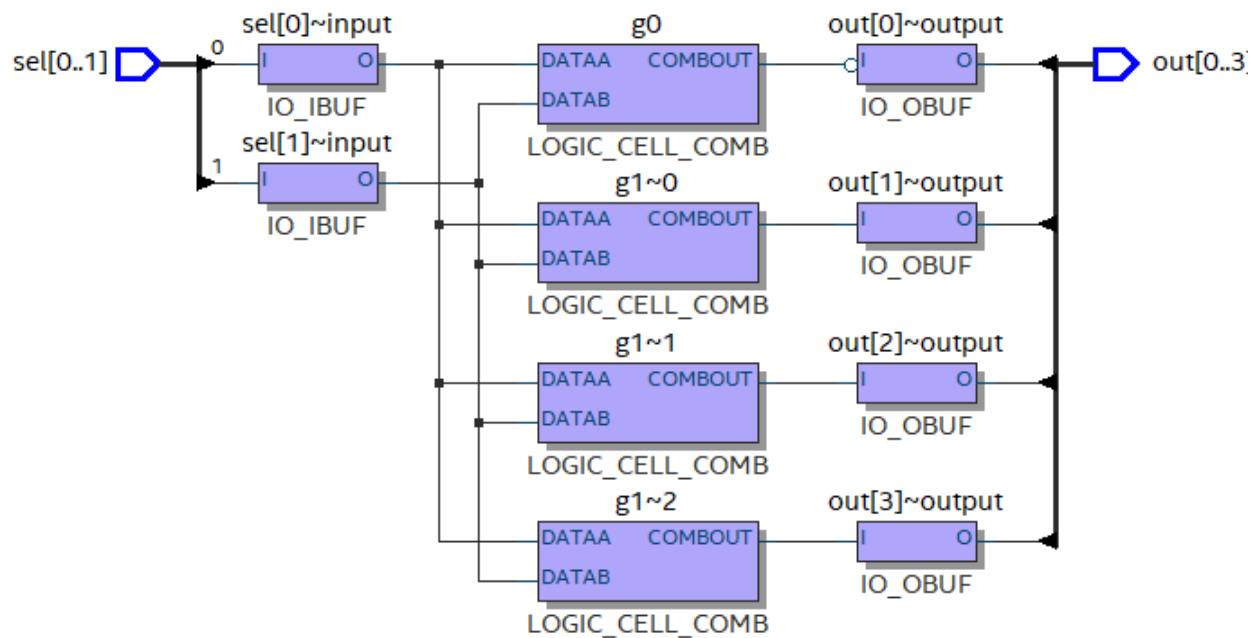
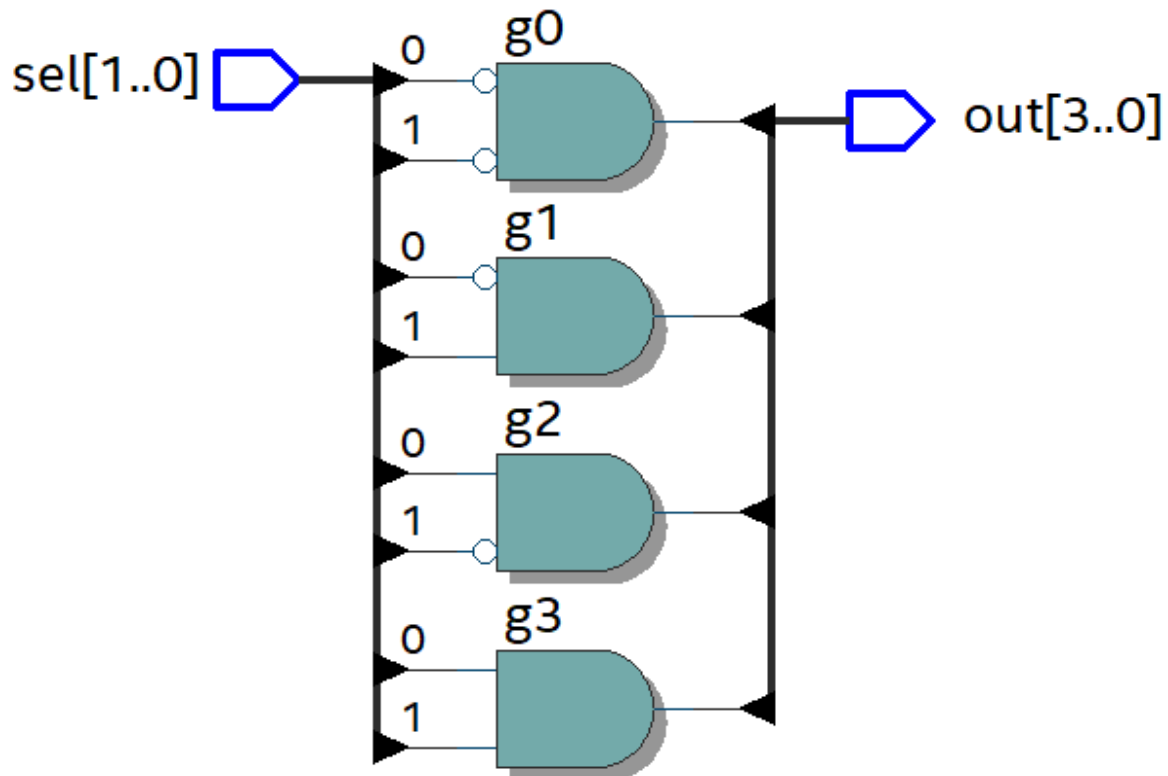
The screenshot displays a Verilog simulation environment with three main panels:

- Project Tree (Left):** Shows a hierarchy starting with 'decoder_2to4_test...' under 'Instance'. It includes a 'design_instanc...' entry and four '#ASSIGN#...' entries, all associated with 'decoder' design units. A 'std' entry is associated with 'std' design units, and a '#vsim_capacity#' entry is associated with 'Capa' design units.
- Wave - Default (Top Right):** A table showing simulation results for two instances of '/decoder_2to4_test...'. The first instance has a value of 11, and the second has a value of 1000. The table also shows a time range from 00 to 1000 ps.
- Transcript (Bottom):** A log of simulation commands and results. It starts with 'Loading sv_std.v' and 'Loading work.decoder_2to4_testbench'. It then shows 'add wave sim:/decoder_2to4_testbench/*' and 'VSIM 6> run'. The transcript lists several simulation steps with time, select, and output values: 'time=0, sel=00 out=0001', 'time=150, sel=10 out=0100', 'time=200, sel=01 out=0010', and 'time=250, sel=11 out=1000'.

Instance	Design unit	Design
decoder_2to4_test...	decoder_2t...	Modu
design_instanc...	decoder	Modu
#ASSIGN#...	decoder	Proce
#ASSIGN#...	decoder	Proce
#ASSIGN#...	decoder	Proce
#ASSIGN#...	decoder	Proce
std	std	VIPad
#vsim_capacity#		Capa

Msgs
/decoder_2to4_test... 11
/decoder_2to4_test... 1000

```
# Loading sv_std.v
# Loading work.decoder_2to4_testbench
# Loading work.decoder
add wave sim:/decoder_2to4_testbench/*
VSIM 6> run
# time=0, sel=00 out=0001
#
run
# time=150, sel=10 out=0100
#
run
# time=200, sel=01 out=0010
#
# time=250, sel=11 out=1000
#
```



```

+-----+
; Analysis & Synthesis Resource Usage Summary ;
+-----+
; Resource ; Usage ;
+-----+
; Estimated ALUTs Used ; 4 ;
; -- Combinational ALUTs ; 4 ;
; -- Memory ALUTs ; 0 ;
; -- LUT_REGS ; 0 ;
; Dedicated logic registers ; 0 ;
; ; ;
; Estimated ALUTs Unavailable ; 0 ;
; -- Due to unpartnered combinational logic ; 0 ;
; -- Due to Memory ALUTs ; 0 ;
; ; ;
; Total combinational functions ; 4 ;
; Combinational ALUT usage by number of inputs ; ;
; -- 7 input functions ; 0 ;
; -- 6 input functions ; 0 ;
; -- 5 input functions ; 0 ;
; -- 4 input functions ; 0 ;
; -- <=3 input functions ; 4 ;
; ; ;
; Combinational ALUTs by mode ; ;
; -- normal mode ; 4 ;
; -- extended LUT mode ; 0 ;
; -- arithmetic mode ; 0 ;
; -- shared arithmetic mode ; 0 ;
; ; ;
; Estimated ALUT/register pairs used ; 4 ;
; ; ;
; Total registers ; 0 ;
; -- Dedicated logic registers ; 0 ;
; -- I/O registers ; 0 ;
; -- LUT_REGS ; 0 ;
; ; ;
; ; ;
; I/O pins ; 6 ;
; ; ;
; DSP block 18-bit elements ; 0 ;
; ; ;
; Maximum fan-out node ; sel[0]~input ;
; Maximum fan-out ; 4 ;
; Total fan-out ; 18 ;
; Average fan-out ; 1.13 ;
+-----+

```

Number of ALUTs: 4 (6 I/O pins)

In the gate-level model, each output (out[0] to out[3]) is implemented using AND and NOT gates. Each output corresponds to a 2-input Boolean function that requires one ALUT to map the logic. Since there are 4 outputs, the design uses 4 ALUTs - one for each of the four AND gate combinations.

The screenshot displays a Verilog simulation environment with three main panels:

- Project Tree (Left):** Shows a hierarchy starting with 'decoder_2to4_test...' containing a 'design_instanc...' which includes components 'i0', 'i1', 'g0', 'g1', 'g2', 'g3', 'std', and '#vsm_capacity#'. Each component is associated with a 'decoder' or 'std' design unit and a 'Proce' or 'VIPad' design.
- Wave - Default (Top Right):** A table showing simulation results for two instances of '/decoder_2to4_test...'. The first instance has a value of '11' at 'Now' and '300000 ps'. The second instance has a value of '1000' at 'Cursor 1' and '0000 ps'. The table also shows a sequence of values: '00', '10', '01', '11' and '0001', '0...', '0...', '1...'.
- Transcript (Bottom):** A log of simulation commands and results. It starts with a timestamp '22:35:15 on Oct 11, 2024' and lists loaded files: 'sv_std.std', 'work.decoder_2to4_testbench', and 'work.decoder'. It then shows the command 'add wave sim:/decoder_2to4_testbench/*' and 'VSIM 6> run'. The results show a sequence of values: 'time=0, sel=00 out=0001', 'time=150, sel=10 out=0010', 'time=200, sel=01 out=0100', and 'time=250, sel=11 out=1000'.

```
# Start time: 22:35:15 on Oct 11, 2024
# Loading sv_std.std
# Loading work.decoder_2to4_testbench
# Loading work.decoder
add wave sim:/decoder_2to4_testbench/*
VSIM 6> run
# time=0, sel=00 out=0001
#
run
# time=150, sel=10 out=0010
#
VSIM 7> run
# time=200, sel=01 out=0100
#
# time=250, sel=11 out=1000
```

fulladder_behavioral.sv

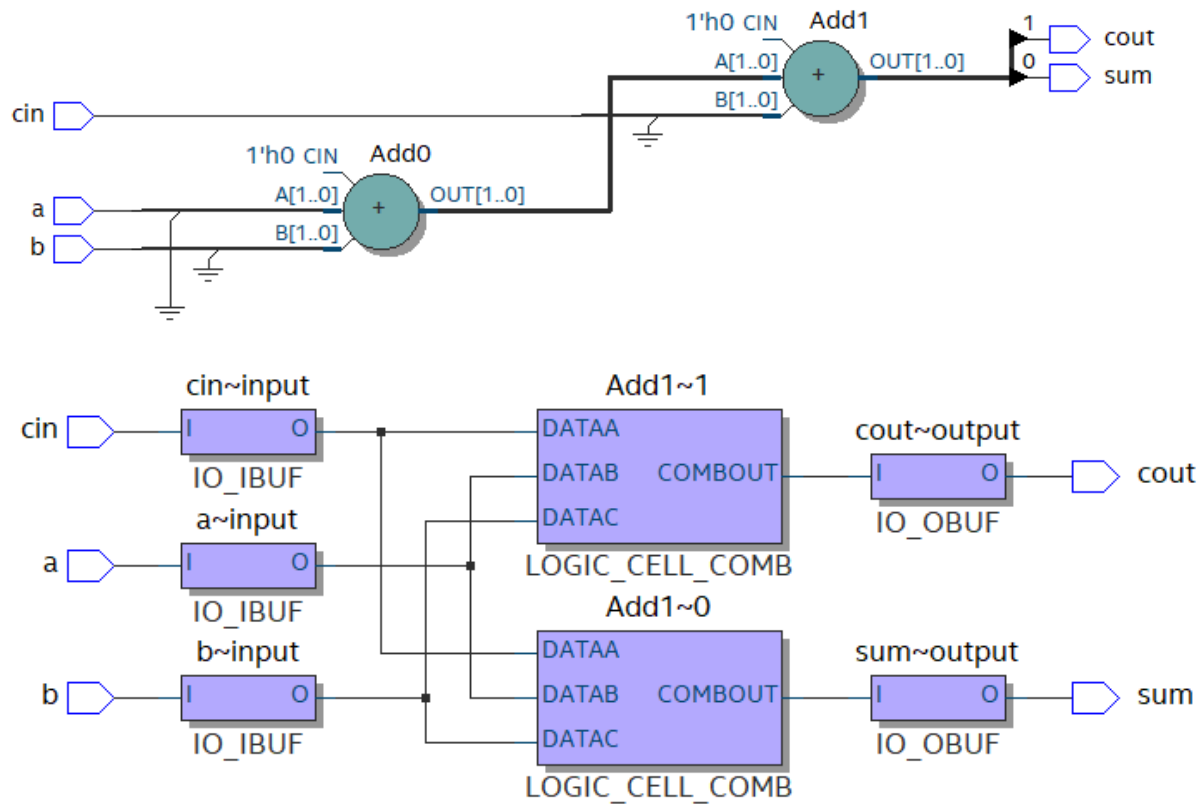
The screenshot shows the Quartus Prime IDE with the behavioral code for a full adder in the main editor. The code is as follows:

```

1 // FullAdder behavioral level code
2 module fulladder(
3     input logic a, b, cin,
4     output logic sum, cout
5 );
6     assign {cout, sum} = a + b + cin;
7 endmodule
8
9

```

The left pane shows the Project Navigator with the hierarchy: Arria II GX: AUTO > fulladder. The bottom pane shows the compilation messages, including warnings about clock constraints and a successful compilation result.



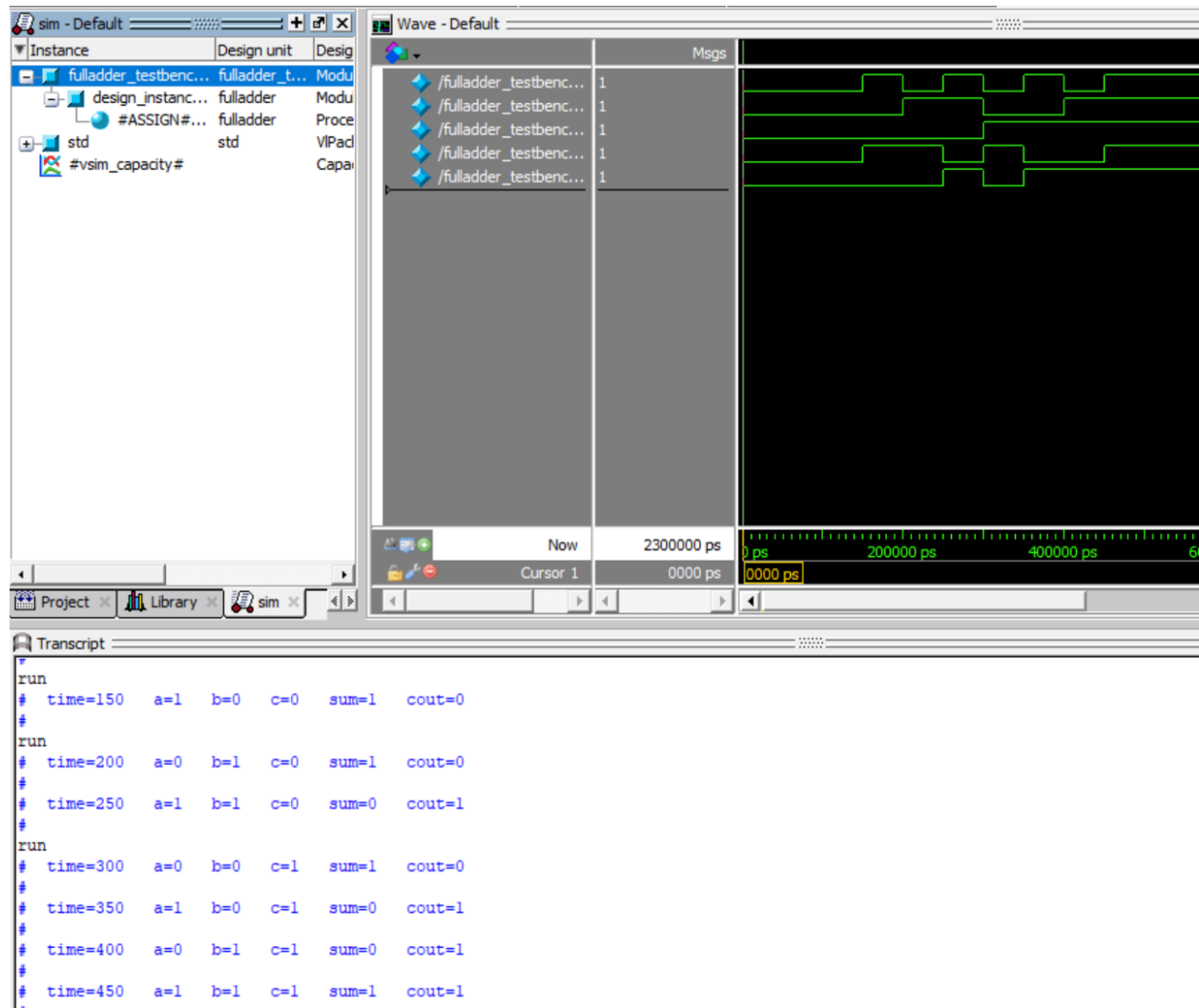
```

+-----+
; Analysis & Synthesis Resource Usage Summary
+-----+
; Resource                                ; Usage    ;
+-----+
; Estimated ALUTs Used                    ; 2        ;
;   -- Combinational ALUTs               ; 2        ;
;   -- Memory ALUTs                     ; 0        ;
;   -- LUT_REGS                          ; 0        ;
; Dedicated logic registers               ; 0        ;
;                                         ;          ;
; Estimated ALUTs Unavailable             ; 0        ;
;   -- Due to unpartnered combinational logic ; 0        ;
;   -- Due to Memory ALUTs              ; 0        ;
;                                         ;          ;
; Total combinational functions           ; 2        ;
; Combinational ALUT usage by number of inputs ;          ;
;   -- 7 input functions                  ; 0        ;
;   -- 6 input functions                  ; 0        ;
;   -- 5 input functions                  ; 0        ;
;   -- 4 input functions                  ; 0        ;
;   -- <=3 input functions                ; 2        ;
;                                         ;          ;
; Combinational ALUTs by mode             ;          ;
;   -- normal mode                       ; 2        ;
;   -- extended LUT mode                 ; 0        ;
;   -- arithmetic mode                   ; 0        ;
;   -- shared arithmetic mode             ; 0        ;
;                                         ;          ;
; Estimated ALUT/register pairs used      ; 2        ;
;                                         ;          ;
; Total registers                        ; 0        ;
;   -- Dedicated logic registers          ; 0        ;
;   -- I/O registers                     ; 0        ;
;   -- LUT_REGS                          ; 0        ;
;                                         ;          ;
;                                         ;          ;
; I/O pins                               ; 5        ;
;                                         ;          ;
; DSP block 18-bit elements               ; 0        ;
;                                         ;          ;
; Maximum fan-out node                   ; cin~input ;
; Maximum fan-out                         ; 2        ;
; Total fan-out                           ; 13       ;
; Average fan-out                         ; 1.08     ;
+-----+

```

Number of ALUTs: 2 (5 I/O pins)

The full adder uses 2 combinational ALUTs to implement the sum and carry outputs. Both outputs are derived from 3-input Boolean functions (a, b, and cin), with each function requiring one ALUT. The design has no memory elements or registers, and the I/O pins correspond to the 3 inputs (a, b, cin) and 2 outputs (sum, carry).



simulation same for fulladder_behavioral.sv, fulladder_dataflow.sv, fulladder_gate.sv

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fulladder_dataflow.v

The screenshot shows the Quartus Prime IDE interface. The top-left pane displays the Project Navigator with the 'fulladder' entity selected. The top-right pane shows the IP Catalog. The main editor displays the Verilog code for the fulladder module. The bottom pane shows the compilation report with various messages and warnings.

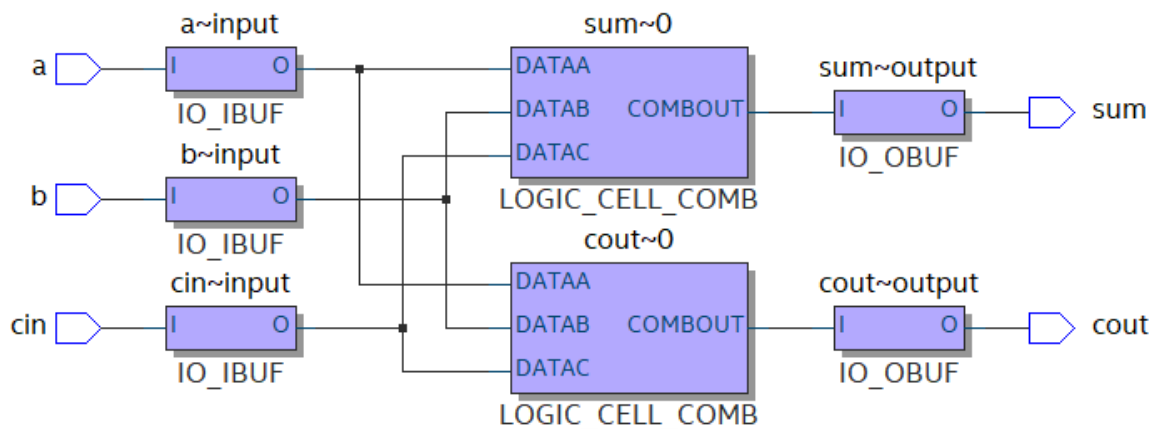
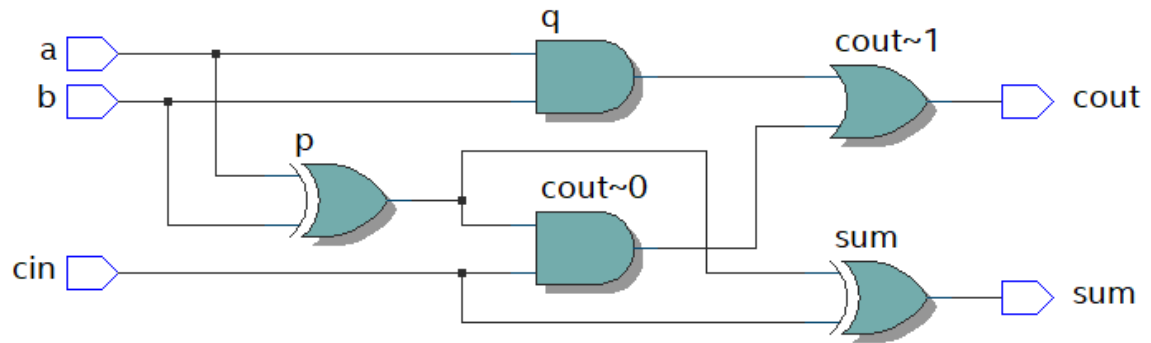
```
1 // Fulladder dataflow code
2 module fulladder(
3     input logic a, b, cin,
4     output logic sum, cout
5 );
6     logic p, q;
7     assign p = a ^ b;
8     assign q = a & b;
9     assign sum = p ^ cin;
10    assign cout = q | (p & cin);
11 endmodule
12
```

Compilation Report - fulladder

Task: Compilation

Messages:

- 21076 Low junction temperature operating condition is not set. Assuming a default value of '-40'.
- 332142 No user constrained base clocks found in the design. Calling "derive_clocks -period 1.0"
- 332096 The command derive_clocks did not find any clocks to derive. No clocks were created or changed.
- 332068 No clocks defined in design.
- 332154 The derive_clock_uncertainty command did not apply clock uncertainty to any clock-to-clock transfers.
- 332102 Design is not fully constrained for setup requirements
- 332102 Design is not fully constrained for hold requirements
- Quartus Prime Timing Analyzer was successful. 0 errors, 6 warnings
- Running Quartus Prime EDA Netlist Writer
- Command: quartus_eda --read_settings_files=off --write_settings_files=off fulladder -c fulladder
- 18236 Number of processors has not been specified which may cause overloading on shared machines. Set the global assignment NUM_PAR
- 204019 Generated file fulladder.svo in folder "C:/Users/Ryo Andrew Onozuka/Documents/GitHub/notes/ucsd/ece111/HW/HW1/simulation/model
- Quartus Prime EDA Netlist Writer was successful. 0 errors, 1 warning
- 293000 Quartus Prime Full Compilation was successful. 0 errors, 15 warnings



```

+-----+
; Analysis & Synthesis Resource Usage Summary ;
+-----+
; Resource ; Usage ;
+-----+
; Estimated ALUTs Used ; 2 ;
; -- Combinational ALUTs ; 2 ;
; -- Memory ALUTs ; 0 ;
; -- LUT_REGS ; 0 ;
; Dedicated logic registers ; 0 ;
; ; ;
; Estimated ALUTs Unavailable ; 0 ;
; -- Due to unpartnered combinational logic ; 0 ;
; -- Due to Memory ALUTs ; 0 ;
; ; ;
; Total combinational functions ; 2 ;
; Combinational ALUT usage by number of inputs ; ;
; -- 7 input functions ; 0 ;
; -- 6 input functions ; 0 ;
; -- 5 input functions ; 0 ;
; -- 4 input functions ; 0 ;
; -- <=3 input functions ; 2 ;
; ; ;
; Combinational ALUTs by mode ; ;
; -- normal mode ; 2 ;
; -- extended LUT mode ; 0 ;
; -- arithmetic mode ; 0 ;
; -- shared arithmetic mode ; 0 ;
; ; ;
; Estimated ALUT/register pairs used ; 2 ;
; ; ;
; Total registers ; 0 ;
; -- Dedicated logic registers ; 0 ;
; -- I/O registers ; 0 ;
; -- LUT_REGS ; 0 ;
; ; ;
; ; ;
; I/O pins ; 5 ;
; ; ;
; DSP block 18-bit elements ; 0 ;
; ; ;
; Maximum fan-out node ; a~input ;
; Maximum fan-out ; 2 ;
; Total fan-out ; 13 ;
; Average fan-out ; 1.08 ;
+-----+

```

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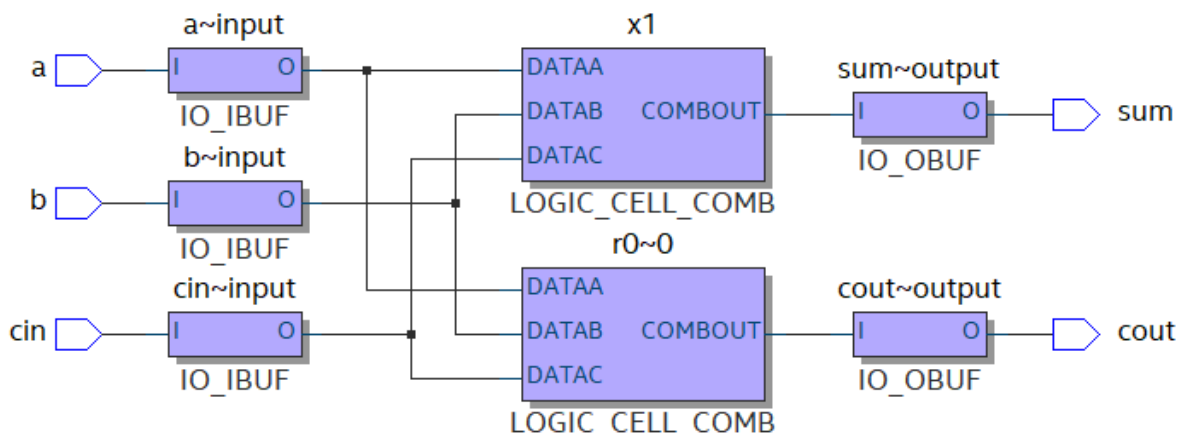
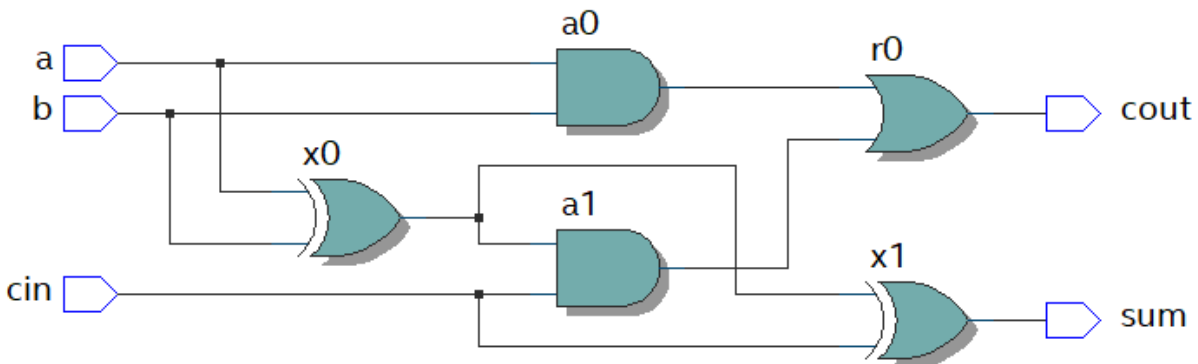
fulladder_gate.v

The screenshot shows the Quartus II IDE interface. The top pane displays the source code for `fulladder_gate.v`:

```
1 // Fulladder gatelevel code
2 module fulladder(
3     input logic a, b, cin,
4     output logic sum, cout
5 );
6
7     wire w0, w1, w2;
8     xor x0(w0, b, a);
9     and a0(w1, b, a);
10    and a1(w2, w0, cin);
11    or r0(cout, w2, w1);
12    xor x1(sum, w0, cin);
13 endmodule
```

The bottom pane shows the compilation report with the following messages:

- 21076 Low junction temperature operating condition is not set. Assuming a default value of '-40'.
- 332142 No user constrained base clocks found in the design. Calling "derive_clocks -period 1.0"
- 332096 The command derive_clocks did not find any clocks to derive. No clocks were created or changed.
- 332068 No clocks defined in design.
- 332154 The derive_clock_uncertainty command did not apply clock uncertainty to any clock-to-clock transfers.
- 332102 Design is not fully constrained for setup requirements
- 332102 Design is not fully constrained for hold requirements
- Quartus Prime Timing Analyzer was successful. 0 errors, 6 warnings
- Running Quartus Prime EDA Netlist Writer
- Command: quartus_eda --read_settings_files=off --write_settings_files=off fulladder -c fulladder
- 18236 Number of processors has not been specified which may cause overloading on shared machines. Set the global assignment NUM_PARALLEL_PROCESSORS to the number of processors to use.
- 204019 Generated file fulladder.svo in folder "C:/Users/Ryo Andrew Onozuka/Documents/GitHub/notes/ucsd/ece111/HW/HW1/simulation/model"
- Quartus Prime EDA Netlist Writer was successful. 0 errors, 1 warning
- 293000 Quartus Prime Full Compilation was successful. 0 errors, 15 warnings



```

+-----+
; Analysis & Synthesis Resource Usage Summary ;
+-----+-----+
; Resource ; Usage ;
+-----+-----+
; Estimated ALUTs Used ; 2 ;
; -- Combinational ALUTs ; 2 ;
; -- Memory ALUTs ; 0 ;
; -- LUT_REGS ; 0 ;
; Dedicated logic registers ; 0 ;
; ; ;
; Estimated ALUTs Unavailable ; 0 ;
; -- Due to unpartnered combinational logic ; 0 ;
; -- Due to Memory ALUTs ; 0 ;
; ; ;
; Total combinational functions ; 2 ;
; Combinational ALUT usage by number of inputs ; ;
; -- 7 input functions ; 0 ;
; -- 6 input functions ; 0 ;
; -- 5 input functions ; 0 ;
; -- 4 input functions ; 0 ;
; -- <=3 input functions ; 2 ;
; ; ;
; Combinational ALUTs by mode ; ;
; -- normal mode ; 2 ;
; -- extended LUT mode ; 0 ;
; -- arithmetic mode ; 0 ;
; -- shared arithmetic mode ; 0 ;
; ; ;
; Estimated ALUT/register pairs used ; 2 ;
; ; ;
; Total registers ; 0 ;
; -- Dedicated logic registers ; 0 ;
; -- I/O registers ; 0 ;
; -- LUT_REGS ; 0 ;
; ; ;
; ; ;
; I/O pins ; 5 ;
; ; ;
; DSP block 18-bit elements ; 0 ;
; ; ;
; Maximum fan-out node ; a~input ;
; Maximum fan-out ; 2 ;
; Total fan-out ; 13 ;
; Average fan-out ; 1.08 ;
+-----+-----+

```


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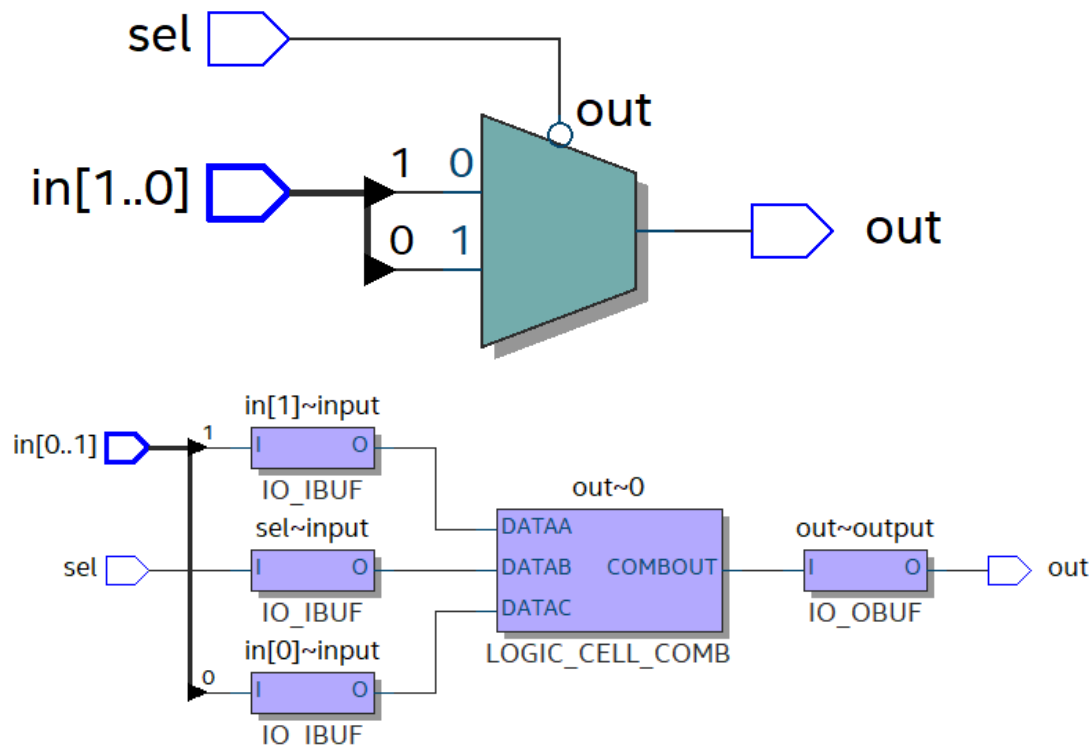
mux_2x1_behavioral.sv

The screenshot shows the Quartus II IDE with the behavioral code for a 2-to-1 multiplexer. The code is as follows:

```
1 // 2to1 Multiplexor behavioral code
2 module mux_2x1(
3     input logic[1:0] in,
4     input logic sel,
5     output logic out
6 );
7 always @(sel or in)
8 begin
9     if(sel == 0)
10        out = in[0];
11    else
12        out = in[1];
13    end
14 endmodule
```

The compilation messages at the bottom indicate that the compilation was successful with 0 errors and 15 warnings. The warnings include:

- 21076 Low junction temperature operating condition is not set. Assuming a default value of '-40'.
- 332142 No user constrained base clocks found in the design. Calling "derive_clocks -period 1.0"
- 332096 The command derive_clocks did not find any clocks to derive. No clocks were created or changed.
- 332068 No clocks defined in design.
- 332154 The derive_clock_uncertainty command did not apply clock uncertainty to any clock-to-clock transfers.
- 332102 Design is not fully constrained for setup requirements
- 332102 Design is not fully constrained for hold requirements
- Quartus Prime Timing Analyzer was successful. 0 errors, 6 warnings
- Running Quartus Prime EDA Netlist writer
- Command: quartus_eda --read_settings_files=off --write_settings_files=off mux_2x1 -c mux_2x1
- 18236 Number of processors has not been specified which may cause overloading on shared machines. Set the global assignment NUM_PARALLEL_PROCESSORS to the number of processors to use.
- 204019 Generated File mux_2x1.svo in folder "C:/Users/Ryo Andrew Onozuka/Documents/GitHub/notes/ucsd/ece111/HW/HW1/simulation/modelsim"
- Quartus Prime EDA Netlist Writer was successful. 0 errors, 1 warning
- 293000 Quartus Prime Full Compilation was successful. 0 errors, 15 warnings



```

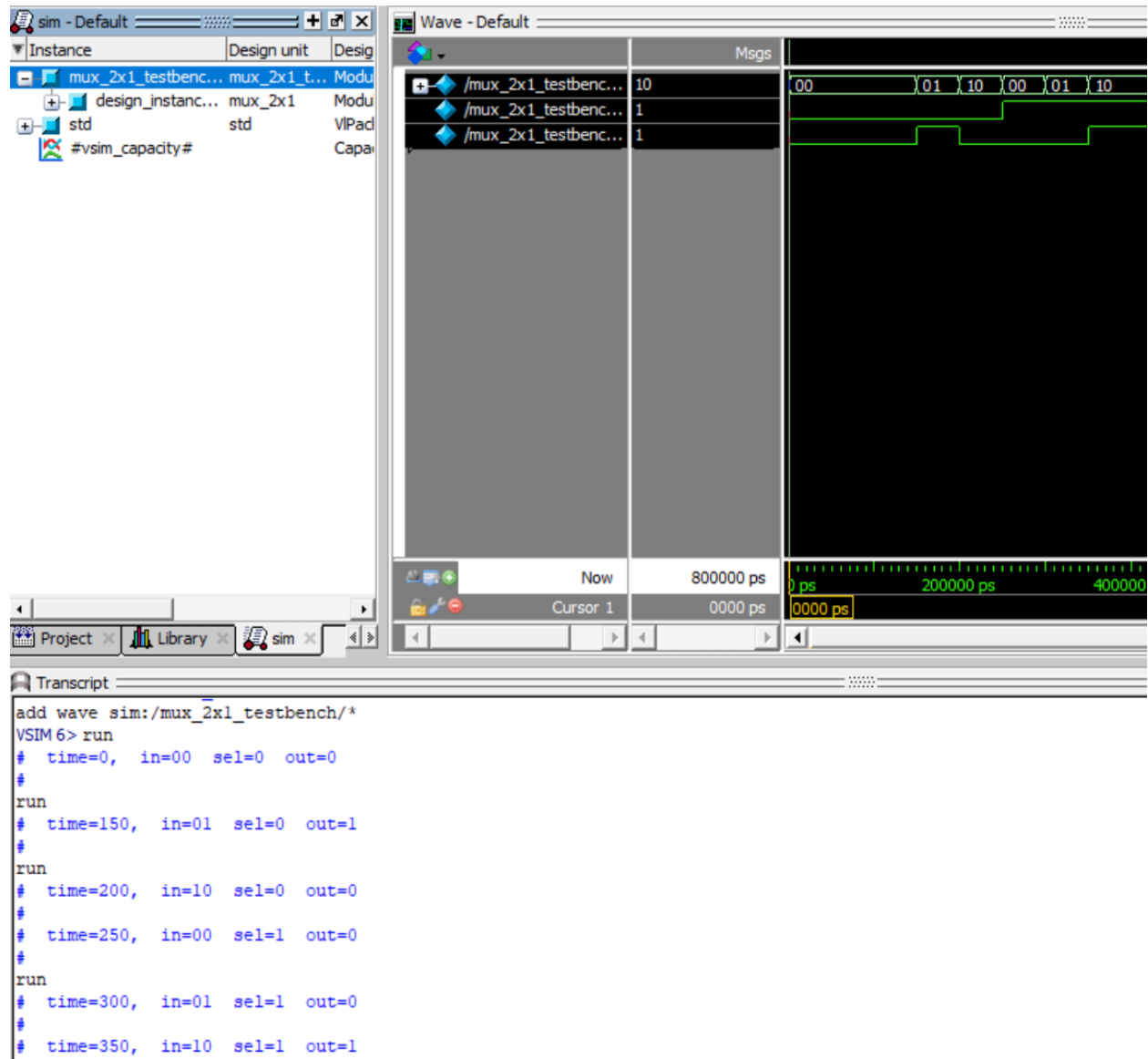
+-----+
; Analysis & Synthesis Resource Usage Summary ;
+-----+
; Resource ; Usage ;
+-----+
; Estimated ALUTs Used ; 1 ;
; -- Combinational ALUTs ; 1 ;
; -- Memory ALUTs ; 0 ;
; -- LUT_REGS ; 0 ;
; Dedicated logic registers ; 0 ;
; ; ;
; Estimated ALUTs Unavailable ; 0 ;
; -- Due to unpartnered combinational logic ; 0 ;
; -- Due to Memory ALUTs ; 0 ;
; ; ;
; Total combinational functions ; 1 ;
; Combinational ALUT usage by number of inputs ; ;
; -- 7 input functions ; 0 ;
; -- 6 input functions ; 0 ;
; -- 5 input functions ; 0 ;
; -- 4 input functions ; 0 ;
; -- <=3 input functions ; 1 ;
; ; ;
; Combinational ALUTs by mode ; ;
; -- normal mode ; 1 ;
; -- extended LUT mode ; 0 ;
; -- arithmetic mode ; 0 ;
; -- shared arithmetic mode ; 0 ;
; ; ;
; Estimated ALUT/register pairs used ; 1 ;
; ; ;
; Total registers ; 0 ;
; -- Dedicated logic registers ; 0 ;
; -- I/O registers ; 0 ;
; -- LUT_REGS ; 0 ;
; ; ;
; ; ;
; I/O pins ; 4 ;
; ; ;
; DSP block 18-bit elements ; 0 ;
; ; ;
; Maximum fan-out node ; out~0 ;
; Maximum fan-out ; 1 ;
; Total fan-out ; 8 ;
; Average fan-out ; 0.89 ;
+-----+

```

Number of ALUTs: 1 (4 I/O pins)

The 2-to-1 MUX uses 1 ALUT to implement the Boolean function $out = (sel \& b) \mid (!sel \& a)$, which maps the selection logic between inputs a and b based on sel. Since it is a simple 3-input function, only one ALUT is required to perform the logic operation.

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simulation same for mux_2x1_behavioral.sv, mux_2x1_dataflow.sv, mux_2x1_gate.sv

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mux_2x1_dataflow.v

Project Navigator: Hierarchy

Entity:Instance

Arria II GX: AUTO

mux_2x1

Compilation Report - mux_2x1

```
1 // 2to1 Multiplexor dataflow code
2 module mux_2x1(
3     input logic[1:0] in,
4     input logic sel,
5     output logic out
6 );
7     assign out = (!sel && in[0]) || (sel && in[1]);
8 endmodule
```

Tasks: Compilation

Task

- Compile Design
- Analysis & Synthesis
- Fitter (Place & Route)
- Assembler (Generate program)
- Timing Analysis
- EDA Netlist Writer
- Edit Settings

IP Catalog

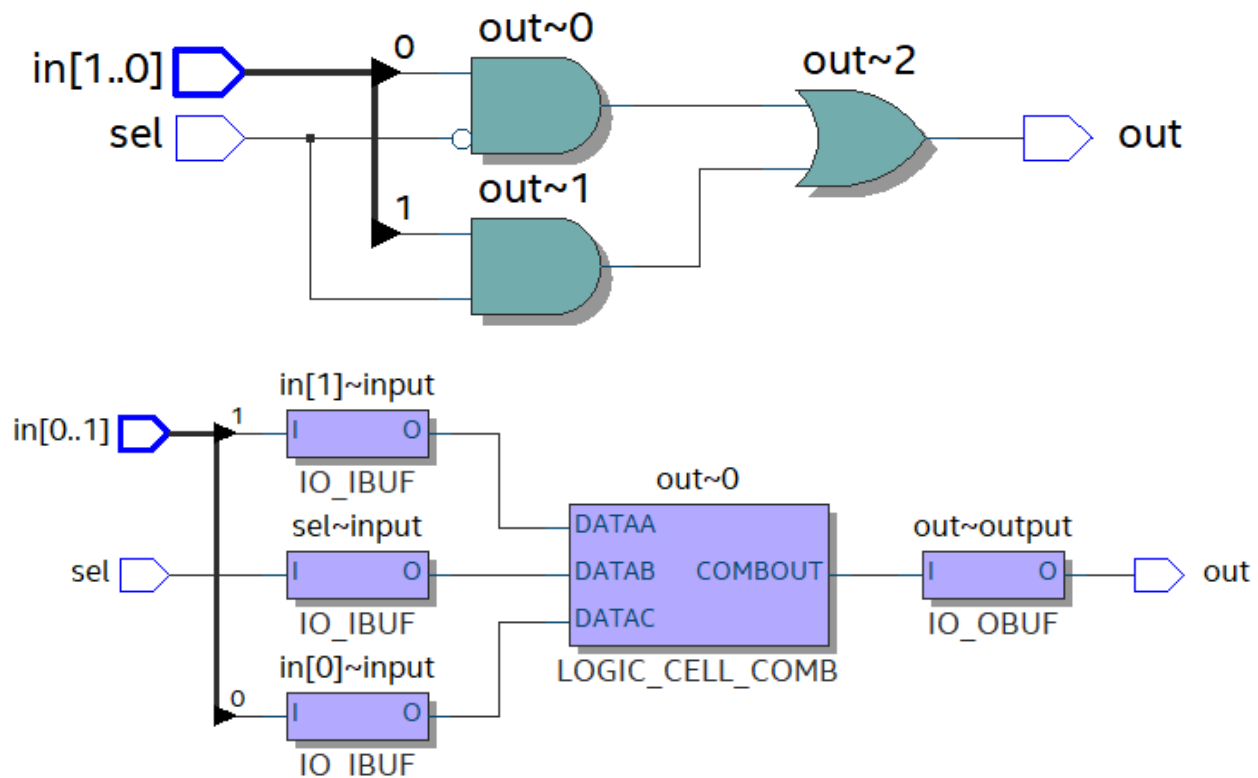
Installed IP

- Project Directory
- Library
- Basic Functions
- DSP
- Interface Protocols
- Memory Interfaces and Controllers
- Processors and Peripherals
- University Program
- Search for Partner IP

Find... Find Next

Type ID Message

- 21076 Low junction temperature operating condition is not set. Assuming a default value of '-40'.
- 332142 No user constrained base clocks found in the design. Calling "derive_clocks -period 1.0"
- 332096 The command derive_clocks did not find any clocks to derive. No clocks were created or changed.
- 332068 No clocks defined in design.
- 332154 The derive_clock_uncertainty command did not apply clock uncertainty to any clock-to-clock transfers.
- 332102 Design is not fully constrained for setup requirements
- 332102 Design is not fully constrained for hold requirements
- Quartus Prime Timing Analyzer was successful. 0 errors, 6 warnings
- Running Quartus Prime EDA Netlist Writer
- Command: quartus_eda --read_settings_files=off --write_settings_files=off mux_2x1 -c mux_2x1
- 18236 Number of processors has not been specified which may cause overloading on shared machines. Set the global assignment NUM_PARALLEL_PROCESSORS to the number of processors available on your machine.
- 204019 Generated file mux_2x1.svo in folder "C:/Users/Ryo Andrew Onozuka/Documents/Github/notes/ucsd/ece111/HW/HW1/simulation/modelsim"
- Quartus Prime EDA Netlist Writer was successful. 0 errors, 1 warning
- 293000 Quartus Prime Full Compilation was successful. 0 errors, 15 warnings



```

+-----+
; Analysis & Synthesis Resource Usage Summary ;
+-----+
; Resource ; Usage ;
+-----+
; Estimated ALUTs Used ; 1 ;
; -- Combinational ALUTs ; 1 ;
; -- Memory ALUTs ; 0 ;
; -- LUT_REGS ; 0 ;
; Dedicated logic registers ; 0 ;
; ; ;
; Estimated ALUTs Unavailable ; 0 ;
; -- Due to unpartnered combinational logic ; 0 ;
; -- Due to Memory ALUTs ; 0 ;
; ; ;
; Total combinational functions ; 1 ;
; Combinational ALUT usage by number of inputs ; ;
; -- 7 input functions ; 0 ;
; -- 6 input functions ; 0 ;
; -- 5 input functions ; 0 ;
; -- 4 input functions ; 0 ;
; -- <=3 input functions ; 1 ;
; ; ;
; Combinational ALUTs by mode ; ;
; -- normal mode ; 1 ;
; -- extended LUT mode ; 0 ;
; -- arithmetic mode ; 0 ;
; -- shared arithmetic mode ; 0 ;
; ; ;
; Estimated ALUT/register pairs used ; 1 ;
; ; ;
; Total registers ; 0 ;
; -- Dedicated logic registers ; 0 ;
; -- I/O registers ; 0 ;
; -- LUT_REGS ; 0 ;
; ; ;
; ; ;
; I/O pins ; 4 ;
; ; ;
; DSP block 18-bit elements ; 0 ;
; ; ;
; Maximum fan-out node ; out~0 ;
; Maximum fan-out ; 1 ;
; Total fan-out ; 8 ;
; Average fan-out ; 0.89 ;
+-----+

```

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mux_2x1_gate.v

Project Navigator: Entity: Instance

Arria II GX: AUTO

mux_2x1

Compilation Report - mux_2x1

```
1 timescale 1ns/1ns
2 // 2to1 Multiplexor gatelevel code
3 module mux_2x1(
4     input logic[1:0] in,
5     input logic sel,
6     output logic out
7 );
8     wire a0, a1, inv_sel;
9     not G1(inv_sel, sel);
10    and G2(a0, in[0], inv_sel);
11    and G3(a1, in[1], sel);
12    or #1.5 G4(out, a0, a1);
13 endmodule
```

Tasks: Compilation

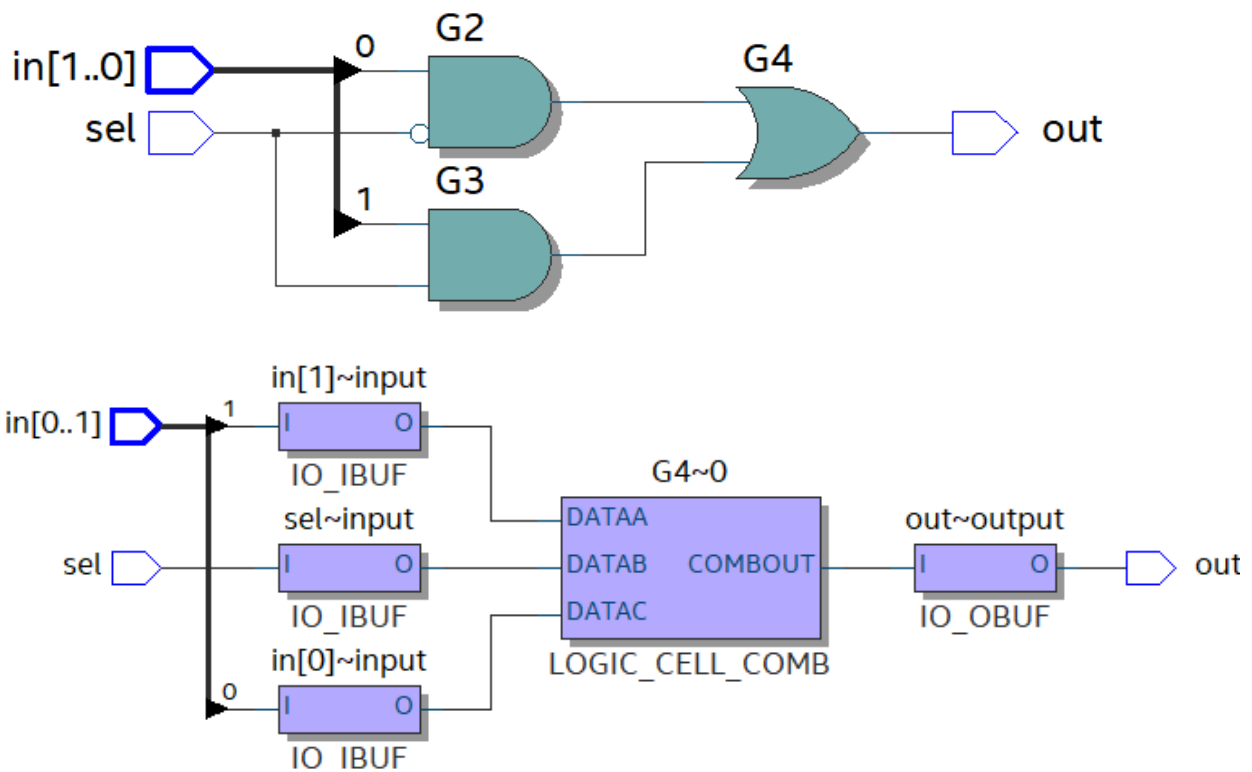
Task

- Compile Design
- Analysis & Synthesis
- Fitter (Place & Route)
- Assembler (Generate program)
- Timing Analysis
- EDA Netlist Writer
- Edit Settings

Messages

Type ID Message

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```

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; Analysis & Synthesis Resource Usage Summary ;
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; Resource ; Usage ;
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; Dedicated logic registers ; 0 ;
; ; ;
; Estimated ALUTs Unavailable ; 0 ;
; -- Due to unpartnered combinational logic ; 0 ;
; -- Due to Memory ALUTs ; 0 ;
; ; ;
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; Combinational ALUT usage by number of inputs ; ;
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; -- 5 input functions ; 0 ;
; -- 4 input functions ; 0 ;
; -- <=3 input functions ; 1 ;
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; Combinational ALUTs by mode ; ;
; -- normal mode ; 1 ;
; -- extended LUT mode ; 0 ;
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; -- shared arithmetic mode ; 0 ;
; ; ;
; Estimated ALUT/register pairs used ; 1 ;
; ; ;
; Total registers ; 0 ;
; -- Dedicated logic registers ; 0 ;
; -- I/O registers ; 0 ;
; -- LUT_REGS ; 0 ;
; ; ;
; ; ;
; I/O pins ; 4 ;
; ; ;
; DSP block 18-bit elements ; 0 ;
; ; ;
; Maximum fan-out node ; G4~0 ;
; Maximum fan-out ; 1 ;
; Total fan-out ; 8 ;
; Average fan-out ; 0.89 ;
+-----+

```