ECE 65 – Components and Circuits Lab

Lab 1 Report – Circuit Simulations

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Abstract

The purpose of this lab is to analyze and verify the behavior of basic circuits through theoretical calculations and simulations.

We performed Thevenin equivalent analysis of a voltage divider circuit, transient response analysis of an RC circuit with square wave inputs, and time-domain analysis of an operational amplifier as a voltage amplifier using LTspice.

We concluded that the simulations matched our predictions and learned how to use the appropriate software tools to help us in circuit analysis techniques..

Experimental Procedures and Results

Problem 1: Voltage Divider (Bias Point, DC Sweep, Parametric sweep, plotting)

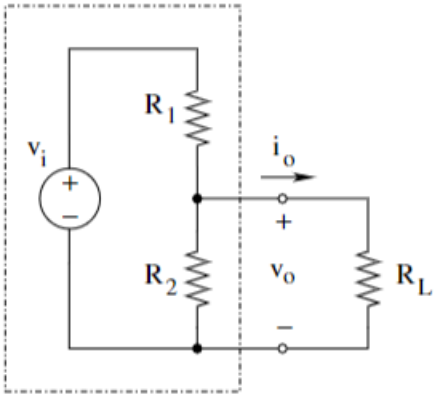


Figure 1: Circuit of Voltage Divider

Include your explanations, circuit analysis, plots, etc. here.

1. Calculate the Thevenin equivalent circuit of the voltage divider (the ”box”). Use the Thevenin equivalent circuit to find v_o and i_o in terms of v_T , R_T and R_L. Prove that for $R_L >> R_T$, $v_o = v_T$.

v_o and i_o in terms of v_T , R_T and R_L:

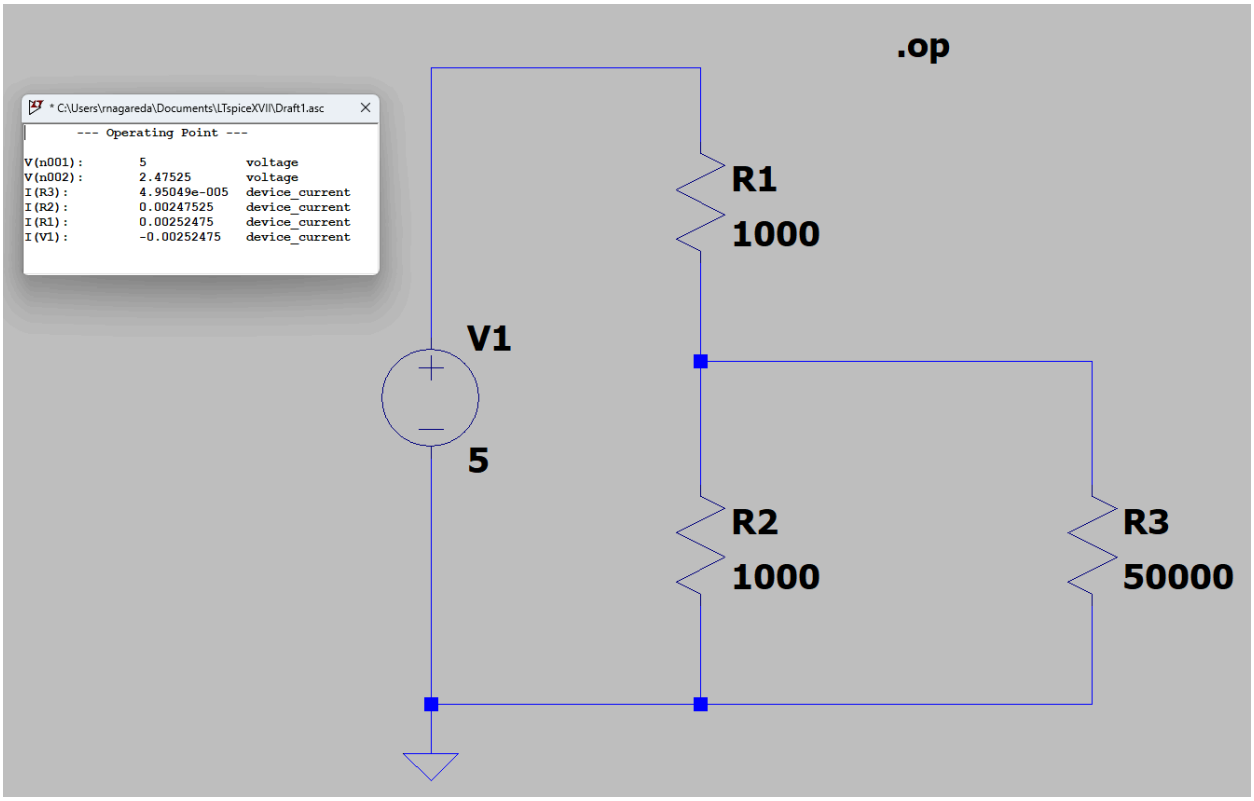
$$R_T = R_1 \,||\, R_2 = \frac{R_1 * R_2}{R_1 + R_2} \qquad v_o = v_T = v_i * \frac{R_2}{R_1 + R_2} \qquad i_o = i_T = \frac{v_T}{R_T}$$

When $R_L >> R_T$, R_{eq} becomes $R_T + R_L = R_L$

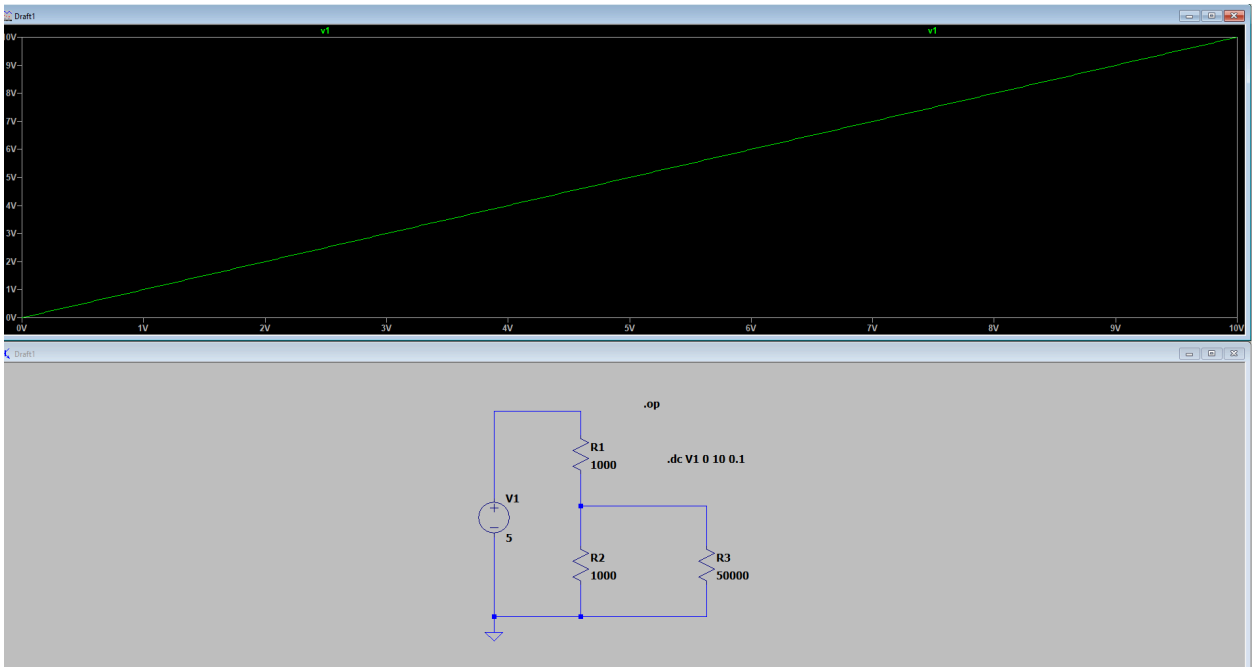
$$v_o = v_T = v_i * \frac{R_L}{R_T + R_L} \approx v_T * \frac{R_L}{R_L} = R_L$$

As $R_L >> R_T$, v_o approaches v_T, as the load resistance dominates and the voltage drop across R_T becomes negligible.

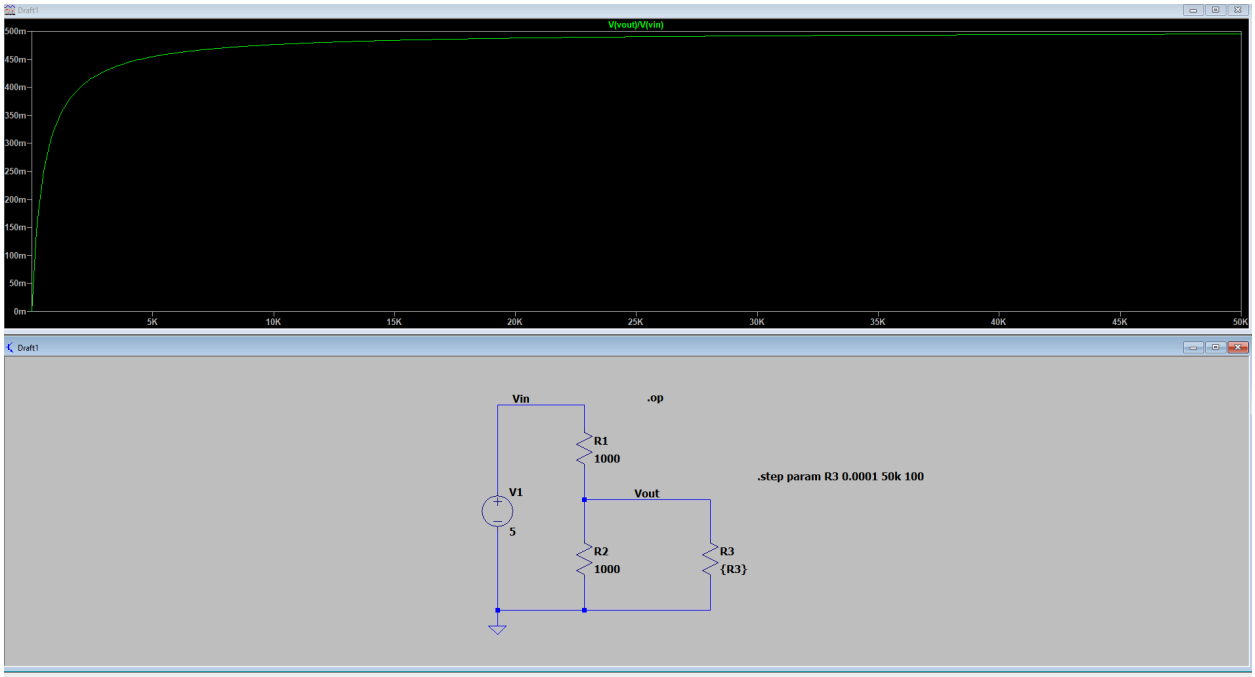
2. Use a circuit simulator to simulate the above circuit with R_1 = 1 kΩ, R_2 = 1 kΩ, R_L = 50 kΩ, and v_i = 5 V. Use ”Bias Point Details” option to find the value of v_o and i_o (attach the circuit with bias-point details).



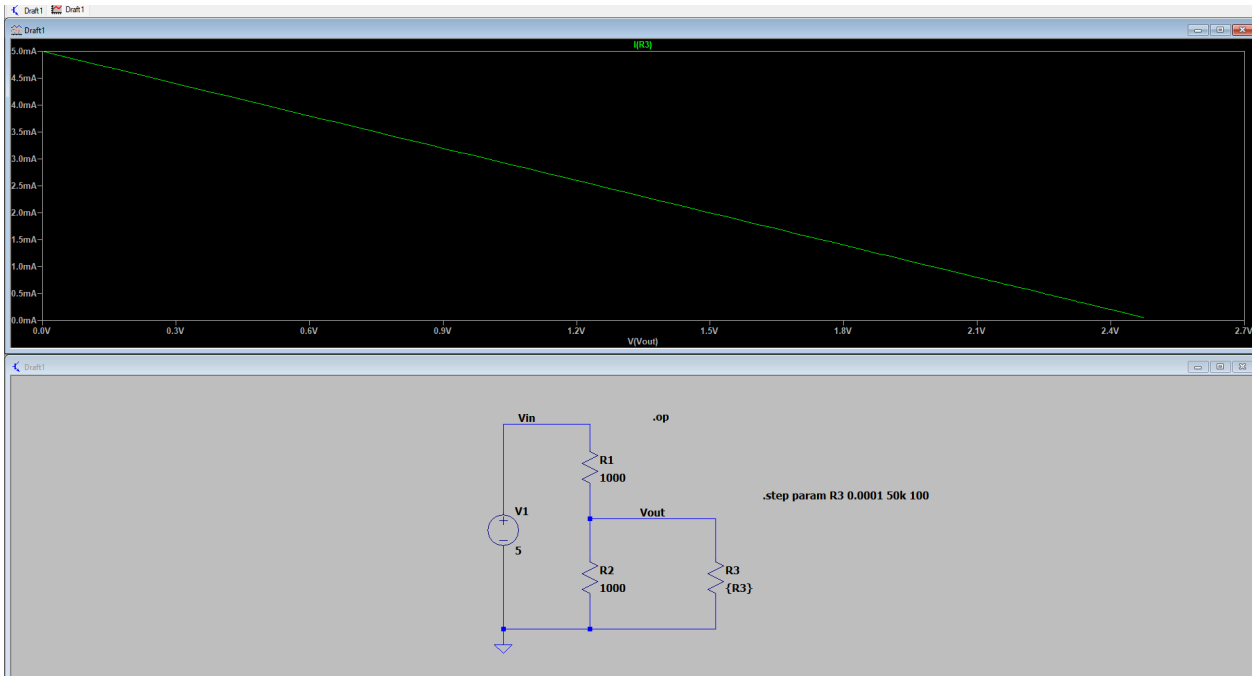
3. Simulate the above circuit with R_1 = 1 kΩ, R_2 = 1 kΩ, R_L = 50 kΩ. Use DC SWEEP to generate a plot of v_o as a function of v_i for v_i ranging from 0 to +10 V. Does it match the expression from part 1? Hint: Note that $R_L >> R_T$.



4. Simulate the above circuit with R_1 = 1 kΩ, R_2 = 1 kΩ, and v_i = 5 V. Use parametric SWEEP to generate a plot of v_o / v_i as a function of R_L for R_L ranging from 0 to 50 kΩ (choose the increment in R_L such that you have a meaningful plot, i.e., the curve looks nice and smooth). Does it match your expectations (consider cases of $R_L \rightarrow 0$, $R_L \rightarrow \infty$, and $R_L = R_T$)?



5. Without changing the simulation settings in the previous part, plot i_o (current in RL) versus v_o. Does it match your expectations? (consider cases of $R_L \to 0$, $R_L \to \infty$, and $R_L = R_T$)?



Problem 2: RC Circuit (VPULSE function, time-domain analysis, plotting)

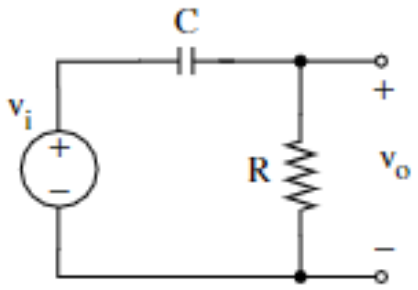
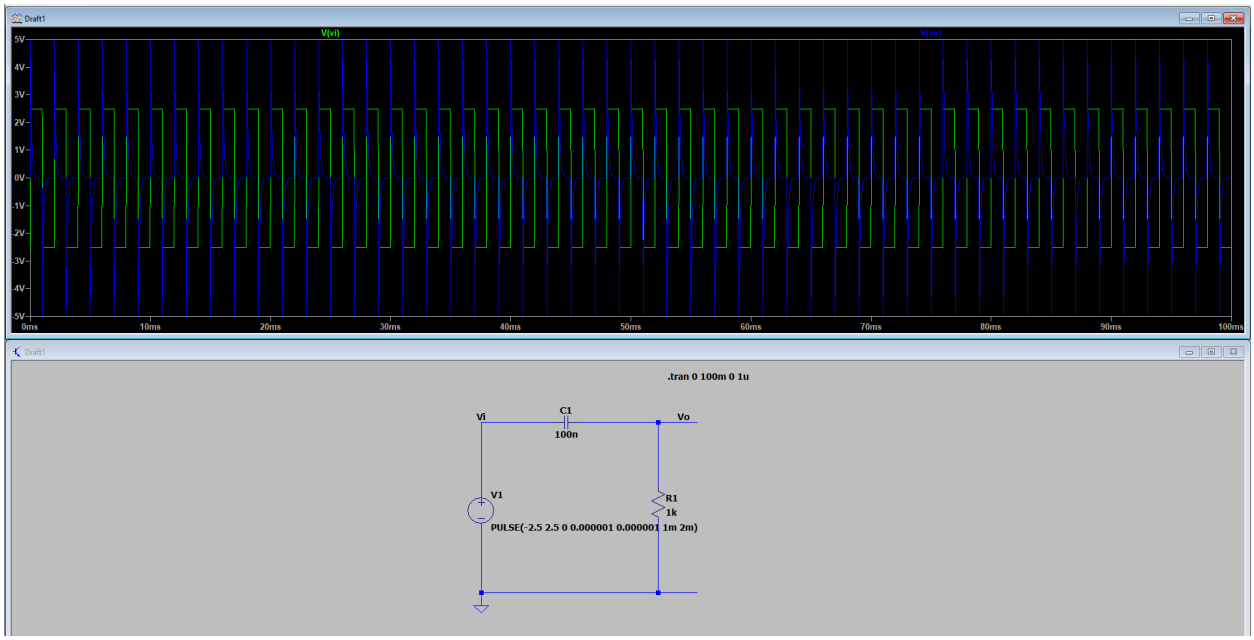


Figure 2: Circuit of RC Circuit

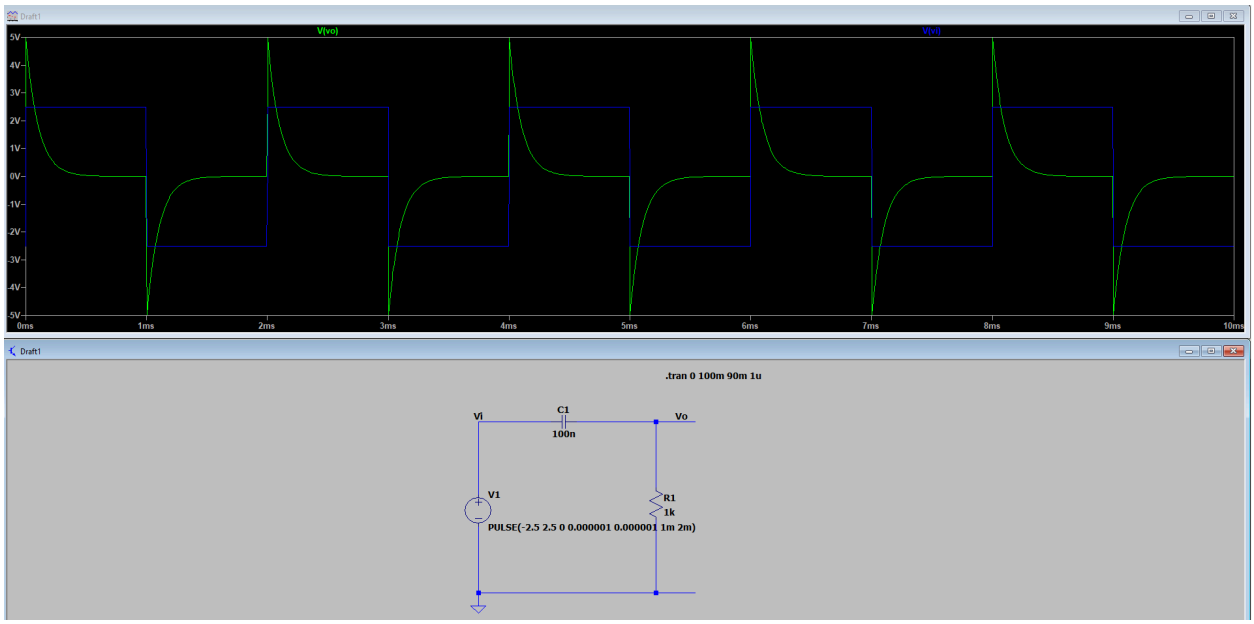
Include your explanations, circuit analysis, plots, etc. here.

Simulate the circuit above with R = 1 kΩ and vi being a square wave function with a frequency of 500 Hz, a peak to peak amplitude of 5 V, and zero DC bias (i.e., vi switches between−2.5 and 2.5 V).

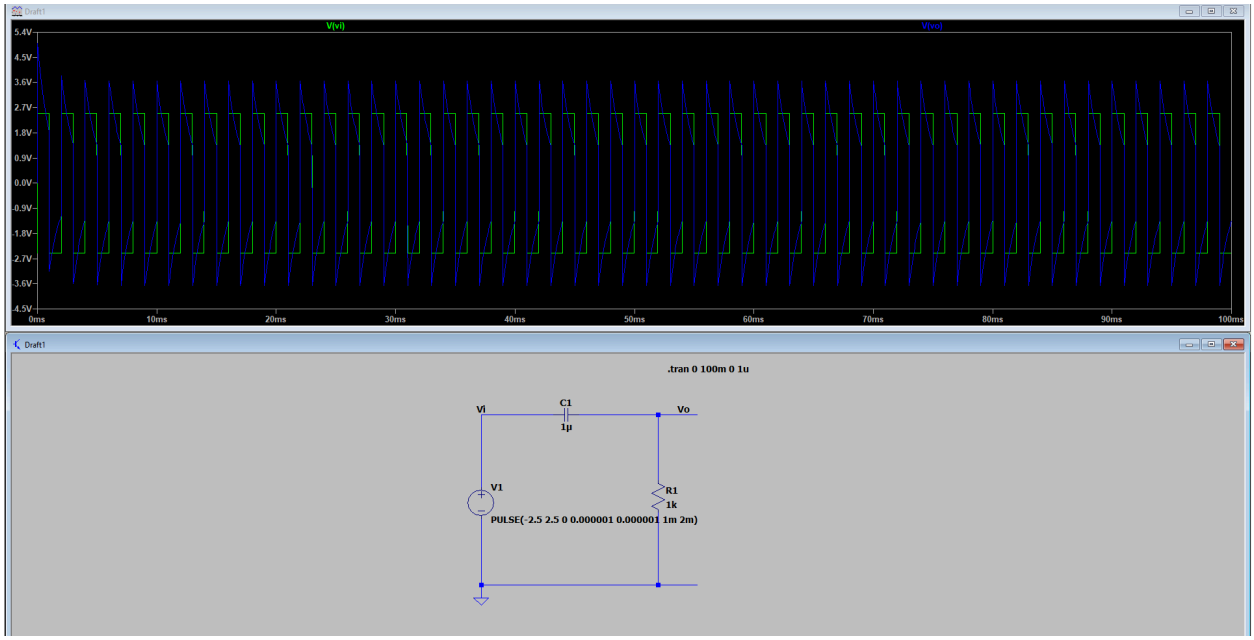
1. Plot v_o and v_i as a function of time for two periods for C = 100 nF, 1 μF, and 10 μF.
    - Make sure both traces are on the same plot.
    - For each case, simulate the circuit for 100 ms and plot the waveforms.
    - For each case, simulate the circuit from 90 ms to 100 ms and plot the waveforms.



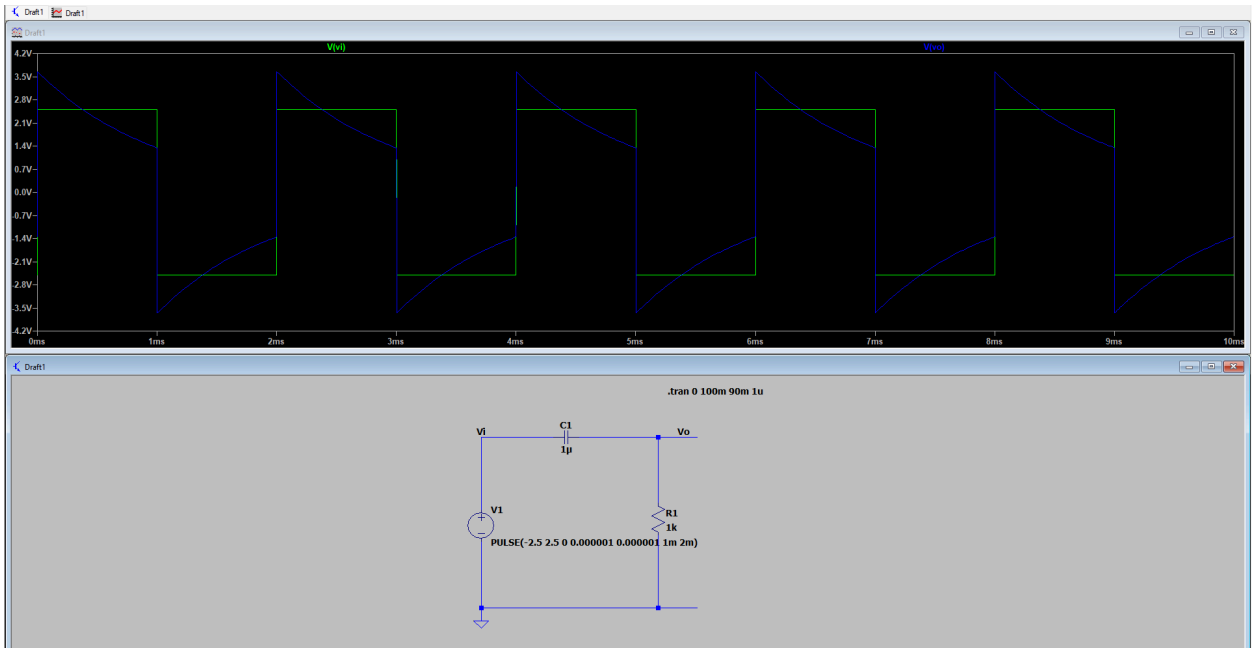
|5V|, zero DC bias, C=100nF, 100ms



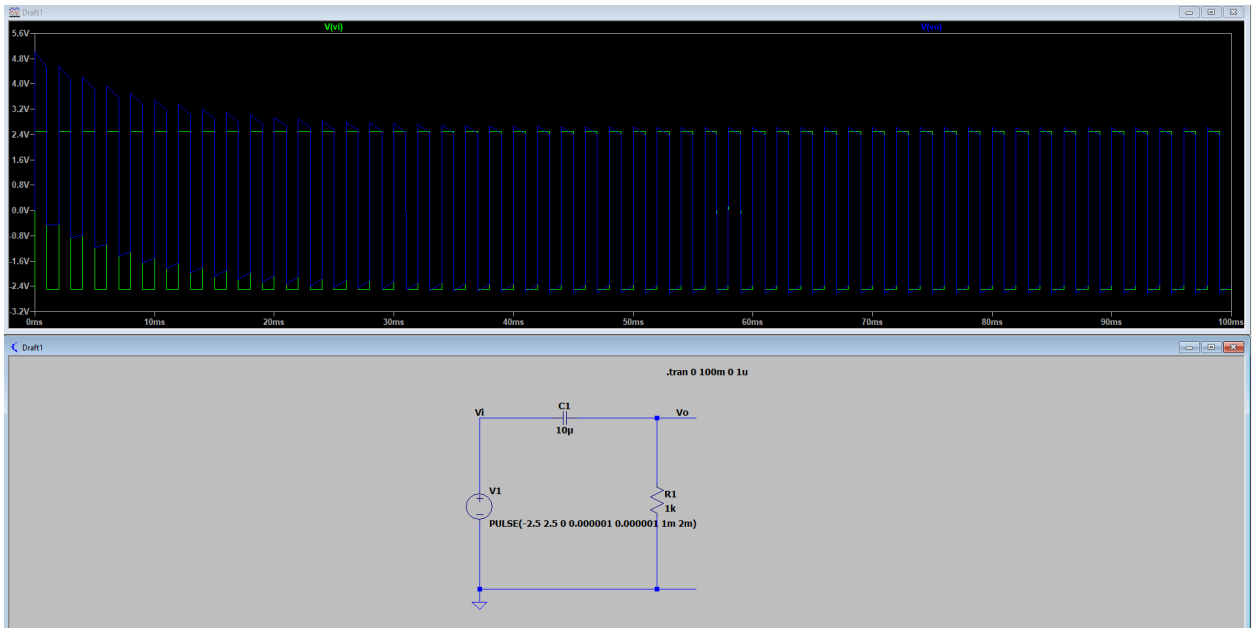
|5V|, zero DC bias, C=100nF, 90-100ms



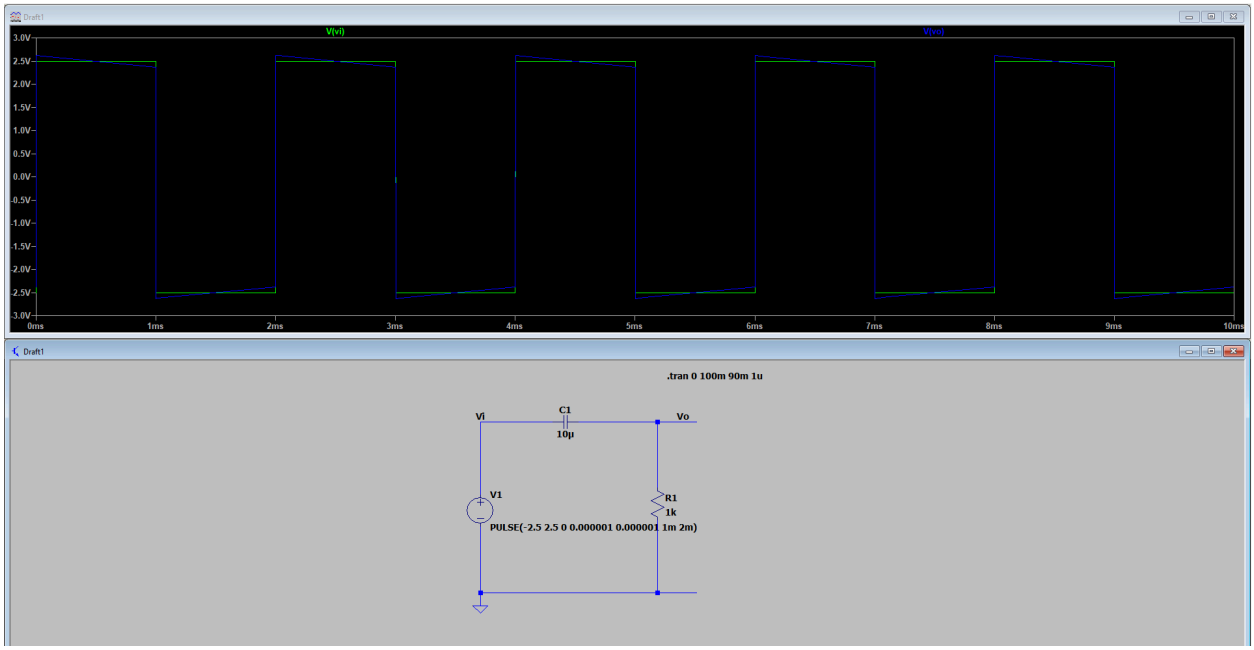
|5V|, zero DC bias, C=1µF, 100ms



|5V|, zero DC bias, C=1µF, 90-100ms

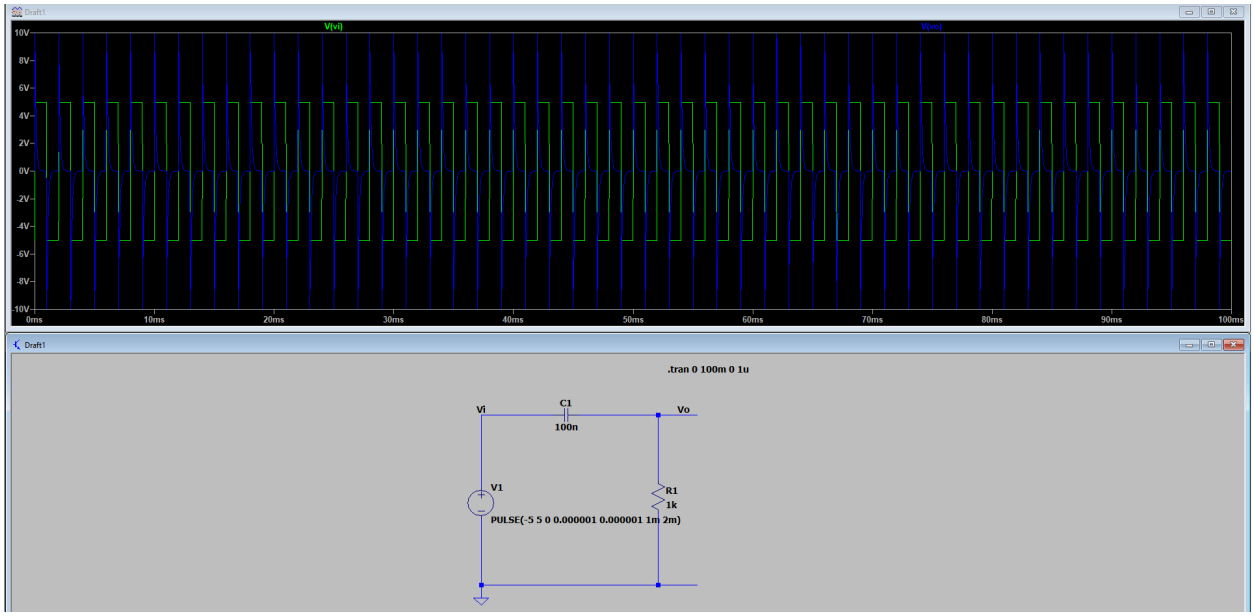


|5V|, zero DC bias, C=10µF, 100ms

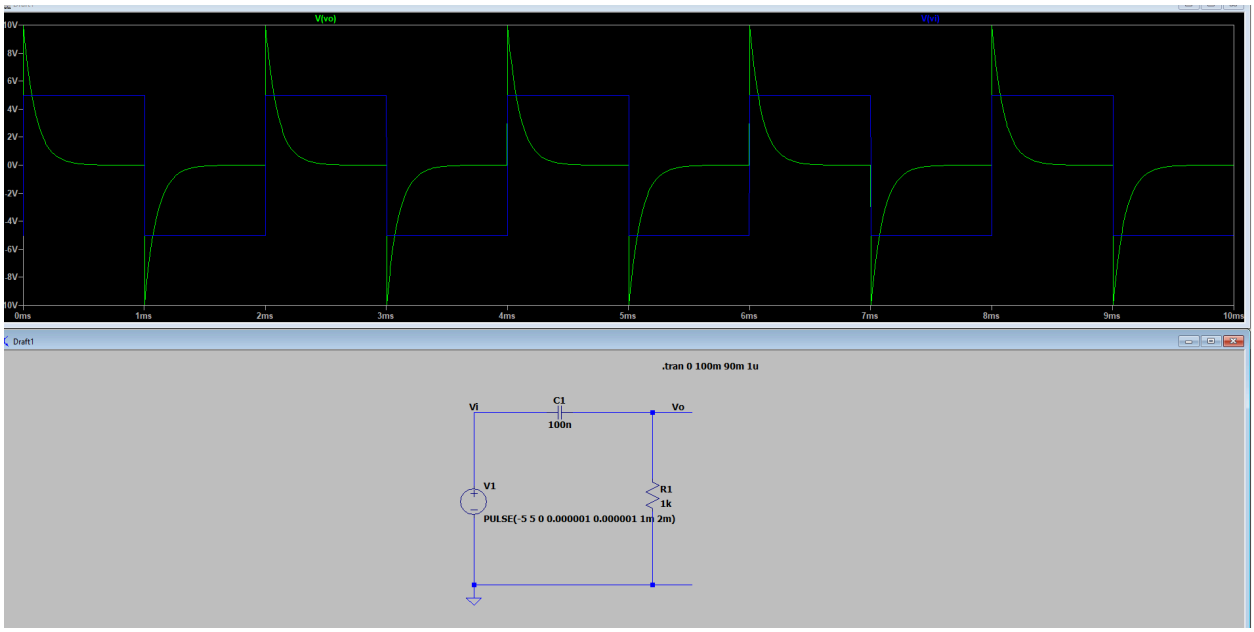


|5V|, zero DC bias, C=10µF, 90-100ms

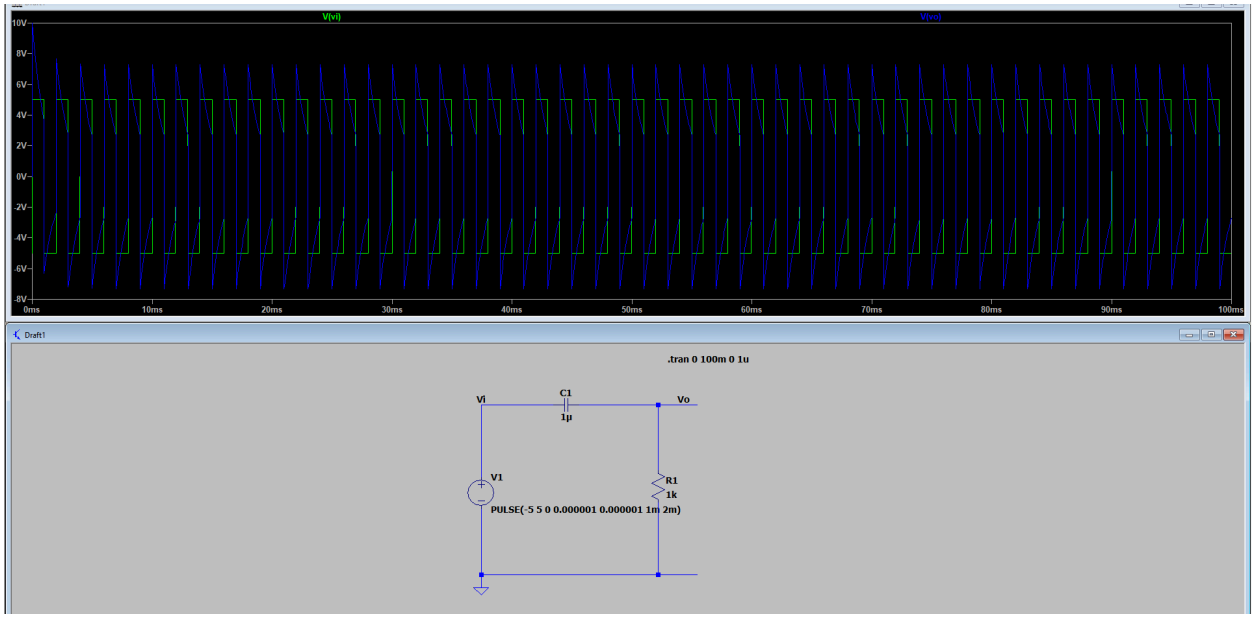
2. Repeat part 1 for vi having a peak to peak amplitude of 10 V, and zero DC bias.



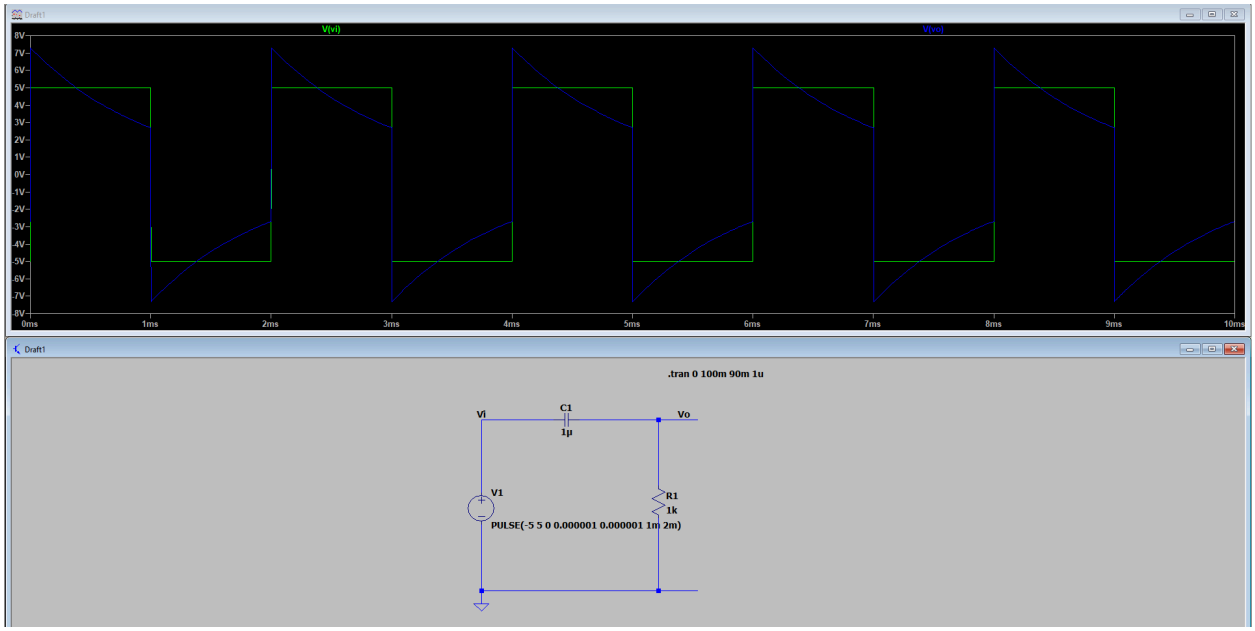
|10V|, zero DC bias, C=100nF, 100ms



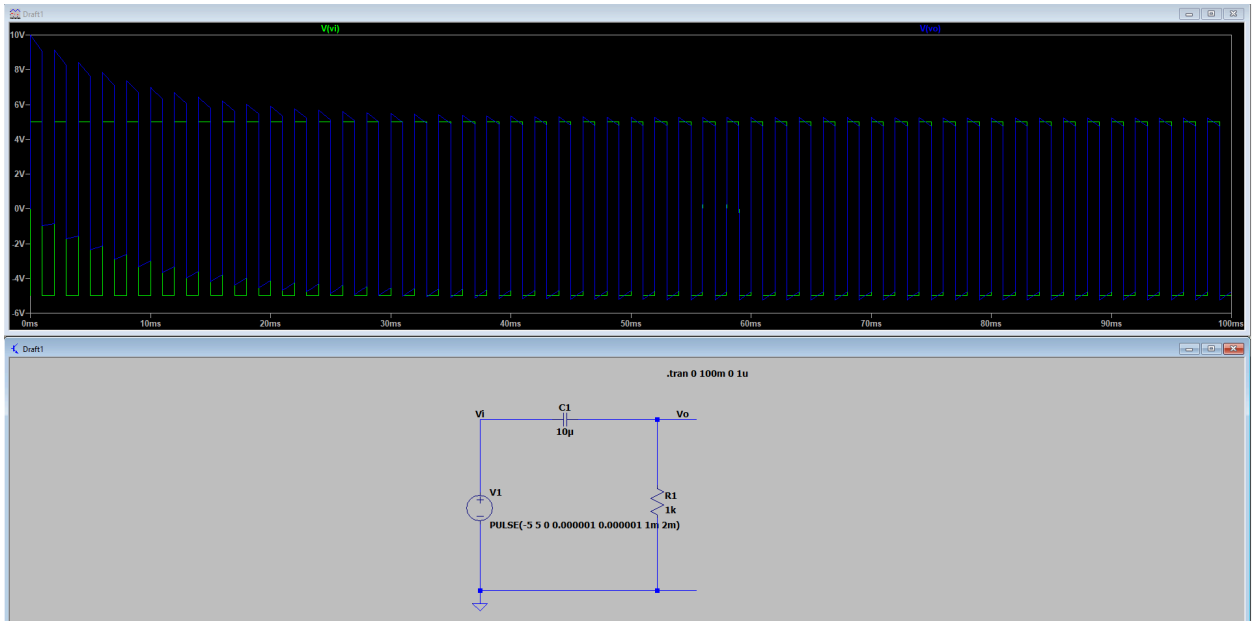
|10V|, zero DC bias, C=100nF, 90-100ms



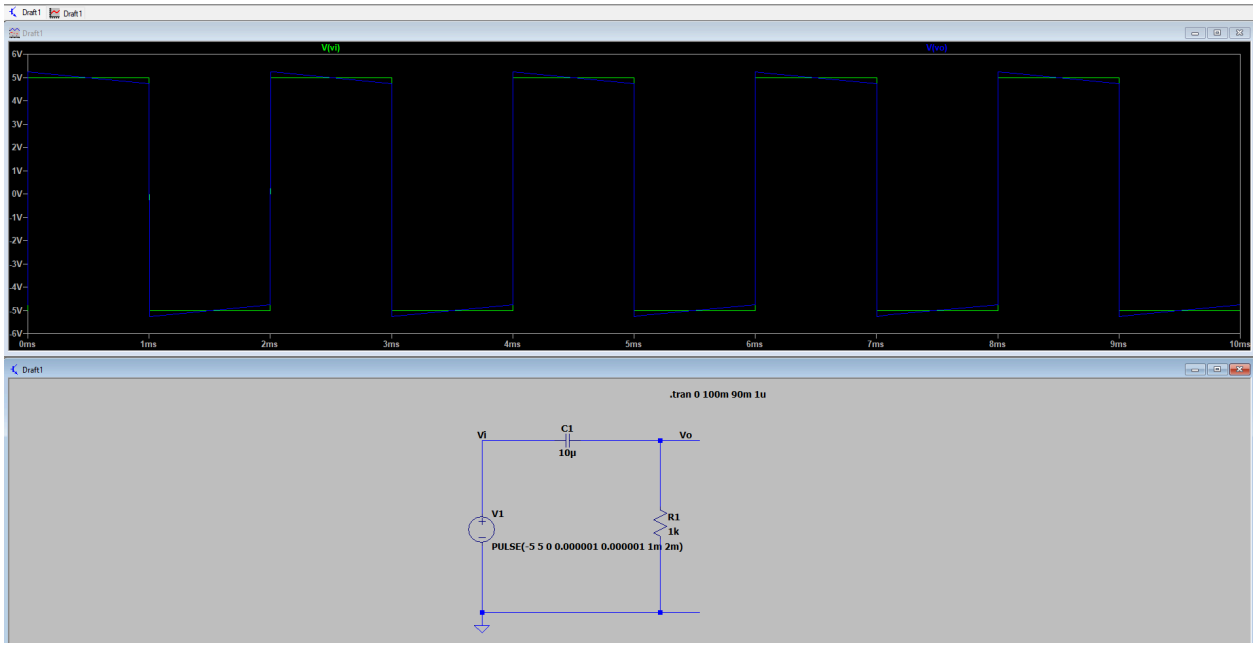
|10V|, zero DC bias, C=1µF, 100ms



|10V|, zero DC bias, C=1µF, 90-100ms



|10V|, zero DC bias, C=10µF, 100ms



|10V|, zero DC bias, C=10µF, 90-100ms

3. Compute the time constant, τ = RC, of the three circuits (i.e., 3 different values of capacitor) and compare them to the half-period of the input voltage. What do you conclude from the above two simulations?

$\tau = RC \qquad \tau = 1000 * 100n = 0.1ms$

$\tau = RC \qquad \tau = 1000 * 1u = 1\,ms$

$\tau = RC \qquad \tau = 1000 * 10u = 10ms$

We can see through our simulations that the 100nF capacitor is able to discharge fully because it has a lower time constant as calculated above. The same cannot be said for the other two capacitors, as we can see that they begin to discharge slightly, but because of the determined period size by the AC source, it never fully discharges.

Problem 3: Op-amp as a Voltage Amplifier (Sine function, time-domain analysis, plotting)

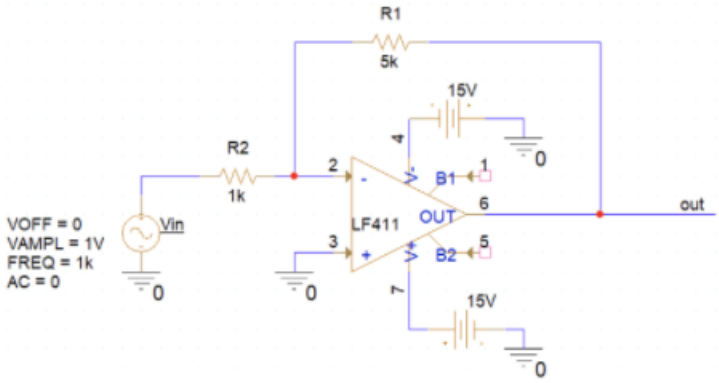
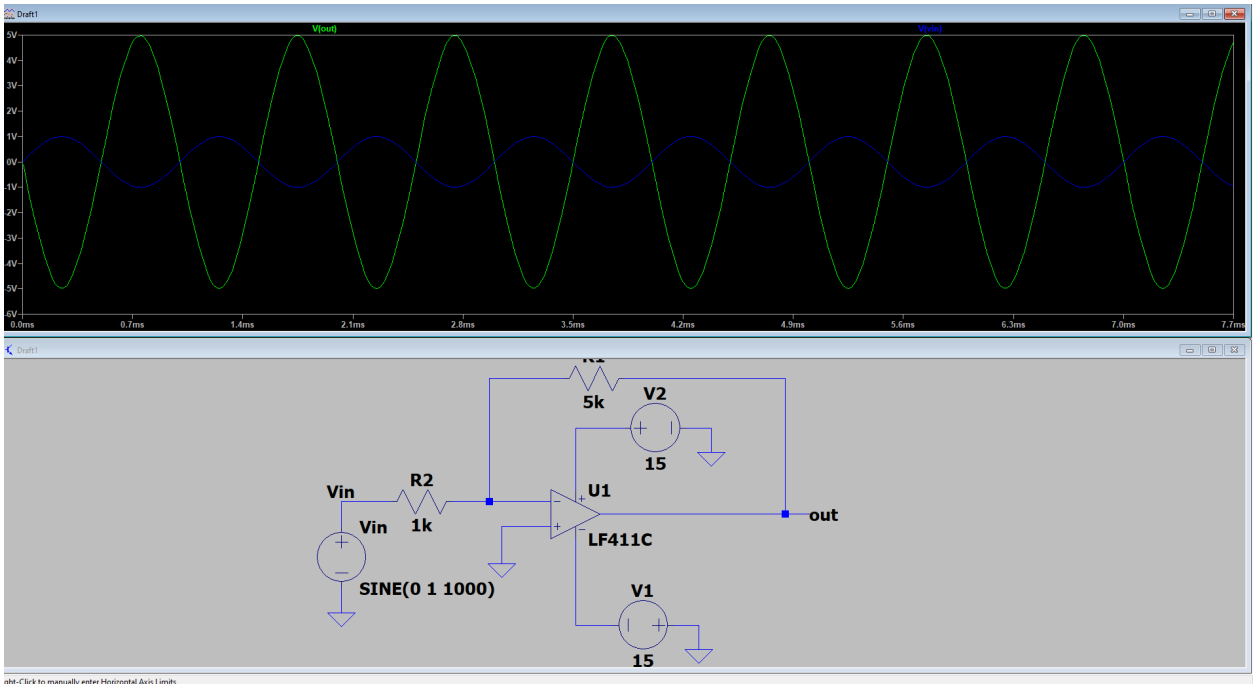


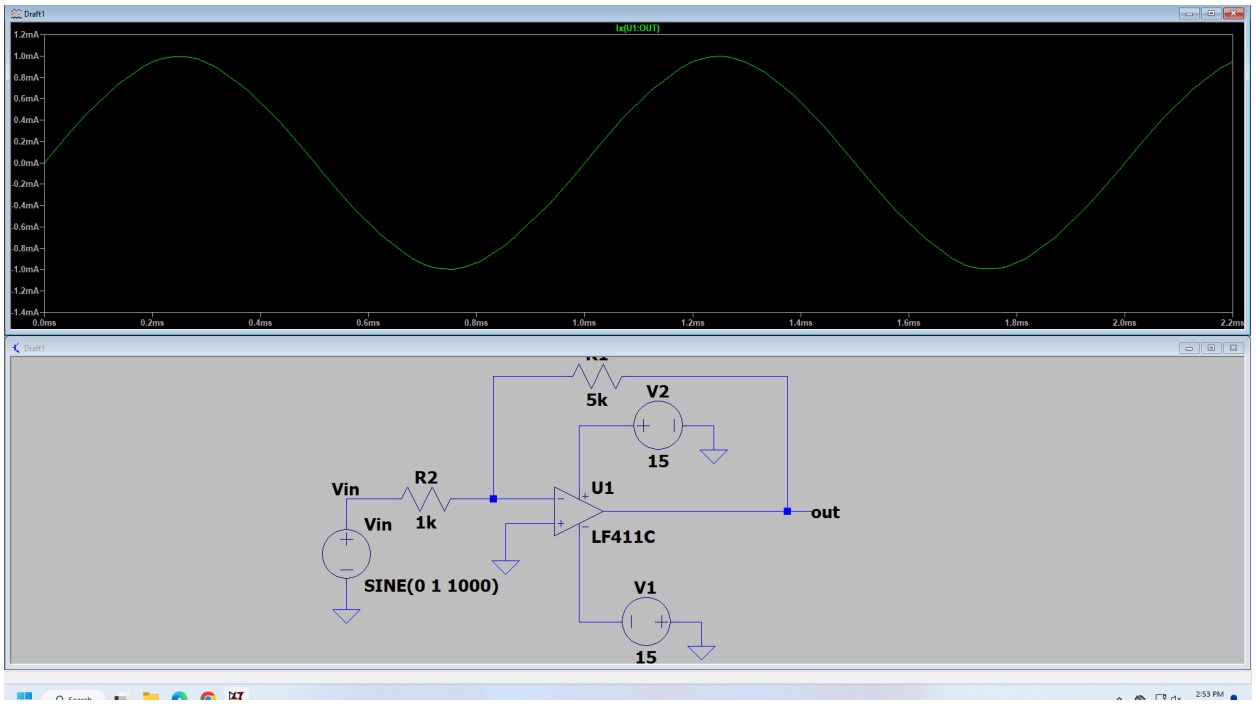
Figure 3: Circuit of Voltage Amplifier

Include your explanations, circuit analysis, plots, etc. here.

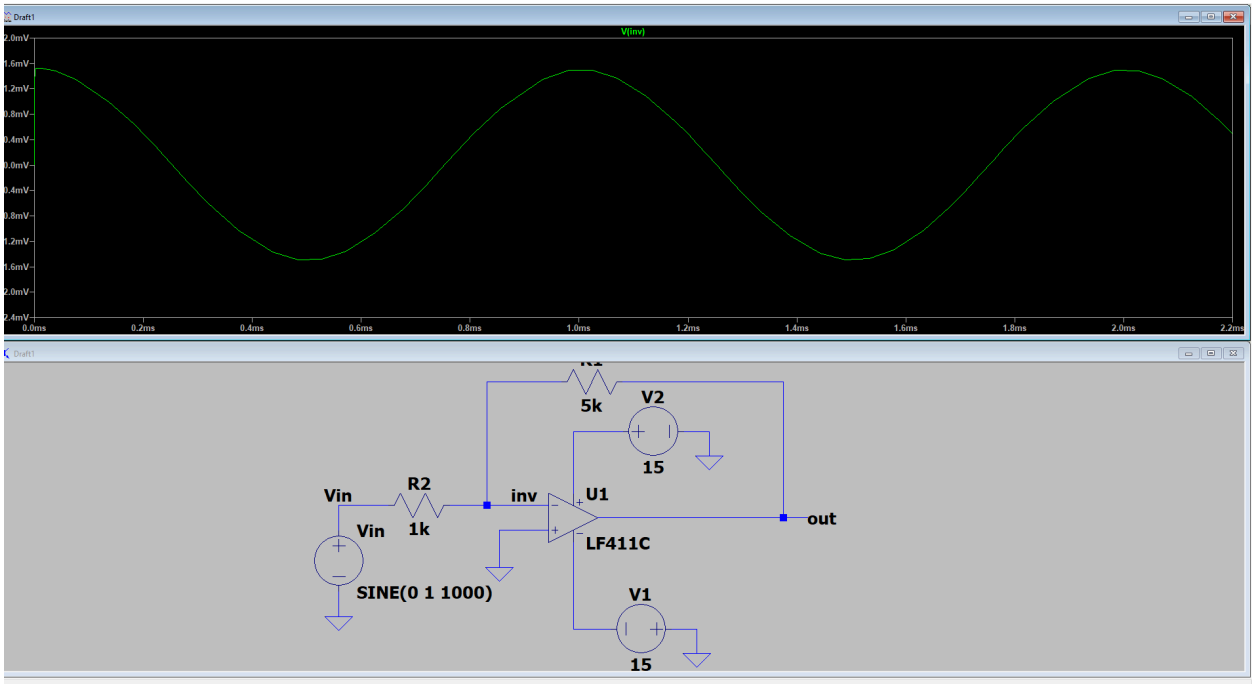
1. Plot v_o and v_{in} as a function of time for two periods (both traces on the same plot.) Is there a linear relationship between v_o and v_{in}?

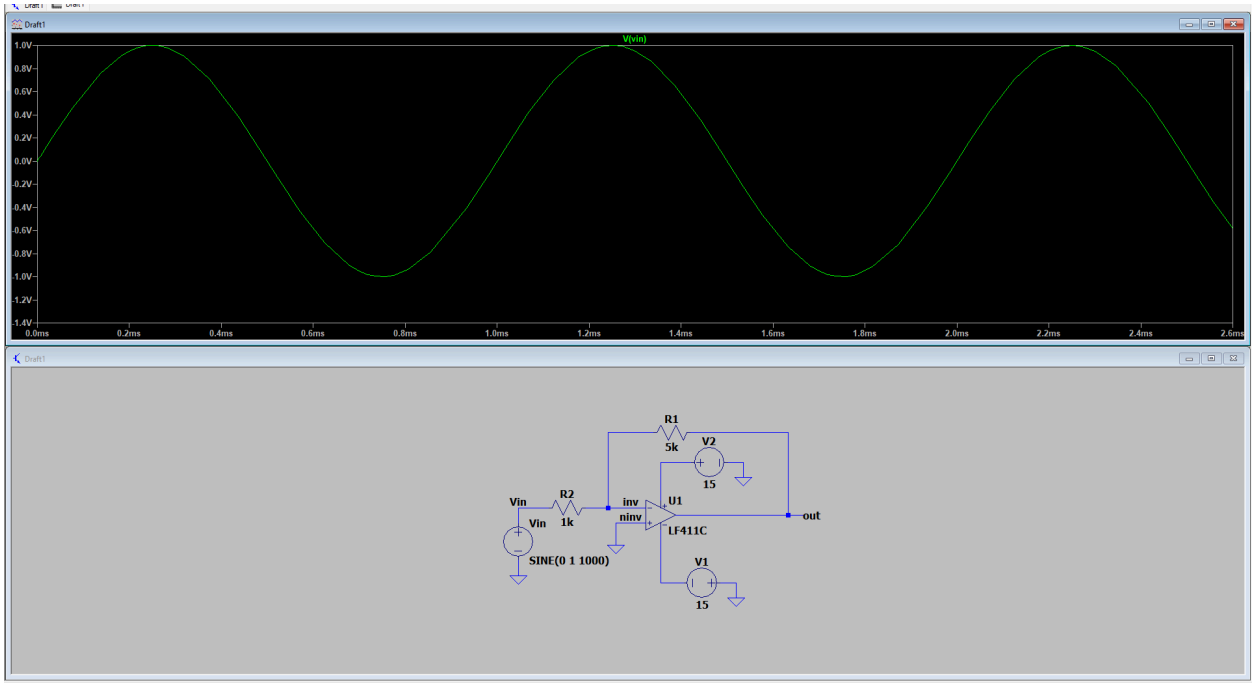


2. Plot the output current of the op-amp as a function of time for two periods.



3. Plot the node voltage at the input inverting terminal as a function of time for two periods. How does the amplitude of this node voltage compare to the amplitude of vin and the node voltage at the input non-inverting terminal?


Draft1
V(inv)
2.0mV
1.6mV
1.2mV
0.8mV
0.4mV
0.0mV
0.4mV
0.8mV
1.2mV
1.6mV
2.0mV
2.4mV
0.0ms
0.2ms
0.4ms
0.6ms
0.8ms
1.0ms
1.2ms
1.4ms
1.6ms
1.8ms
2.0ms
2.2ms
5k
V2
15
Vin
R2
inv
U1
Vin
1k
LF411C
out
SINE(0 1 1000)
V1
15


Draft1
V(vin)
1.0V
0.8V
0.6V
0.4V
0.2V
0.0V
0.2V
0.4V
0.6V
0.8V
1.0V
1.2V
1.4V
0.0ms
0.2ms
0.4ms
0.6ms
0.8ms
1.0ms
1.2ms
1.4ms
1.6ms
1.8ms
2.0ms
2.2ms
2.4ms
2.6ms
R1
5k
V2
15
Vin
R2
inv
U1
ninv
Vin
1k
LF411C
out
SINE(0 1 1000)
V1
15

Conclusion

Three circuits, including a voltage divider, an RC circuit, and an operational amplifier voltage amplifier, were analyzed in this lab. For the voltage divider network, the Thevenin equivalent circuit was calculated and analyzed. It was observed that when the load resistor (R_L) was much larger than the Thevenin equivalent resistance (R_T), the voltage drop across R_T was negligible compared to R_L , resulting in v_o being approximately equal to v_T . Simulations confirmed these theoretical findings. A parametric sweep of R_L demonstrated that for $R_L << R_T$, the voltage across the load approached zero, validating the expected behavior.

In the second experiment, the effect of the RC time constant ($\tau = RC$) on circuit response was investigated. Simulations showed that when τ was large compared to the half-period of the square wave input, the capacitor could only partially charge and discharge, resulting in minimal voltage change across the capacitor. Conversely, when τ was small compared to the half-period, the capacitor charged and discharged quickly, closely following the input waveform. This behavior was consistent with theoretical predictions.

In the third experiment, the behavior of an operational amplifier as a voltage amplifier was explored. Negative feedback was applied using a resistor network to stabilize the gain. The simulations verified that the output voltage was an amplified and inverted version of the input signal, confirming the expected phase shift of π . The inverting terminal voltage remained near zero, as expected due to the op-amp's high open-loop gain and negative feedback. The output current was proportional to the output voltage and in-phase with it, consistent with theoretical analysis.