Name: PID:

UNIVERSITY OF CALIFORNIA, SAN DIEGO

Electrical and Computer Engineering Department

ECE 65 – Winter 2019

Components and Circuits lab

Final Exam

Closed books, seven double-sided cheat sheets, and calculators are allowed

Electronic devices are not allowed.

Please put all answers in the answer sheets.

Write your name and PID on all pages.

Please do not begin until told. Show your work. Good luck.

All electronic devices including cell phones must be turned off and stored away in a backpack or a purse. Anyone caught with such a device on their person during the exam will be charged with academic dishonesty.

You can use the back of every page as a **scratch** paper. **These pages will not be graded.**

The main pages are numbered. If you remove the staple, you should order the pages from page 1 to 16 and staple them before submitting your exam.

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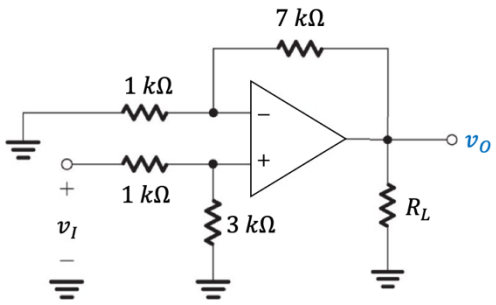
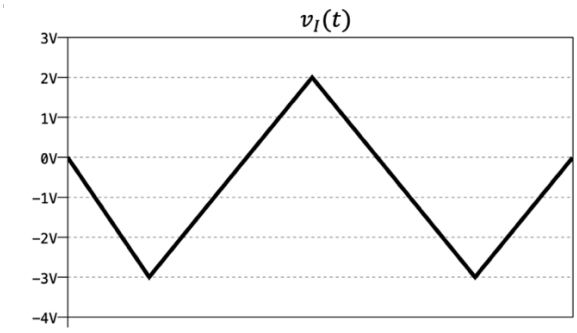
Problem 1. (12 points)

Assuming an ideal op-amp with $V_{sat} = \pm 16V$ and $I_{out_{max}} = \pm 25\ mA$ in the below circuit, answer the following questions.



a) **Find** (derive) an expression for the voltage gain. Assume $R_L = \infty$.

b) The input signal, $v_I(t)$ as shown below, is applied to the circuit. If $R_L = 1\ k\Omega$, **find** the output voltage and **sketch** it.



c) Assume a positive DC shift of 0.5 V is added to the above signal before applying it to the op-amp circuit.

i. Sketch the resulting input signal.

ii. With this new signal applied to the circuit, what is the lowest value of R_L that can be used to have an undistorted output voltage waveform?

iii. Design a diode waveform shaping circuit that can add the + 0.5 V DC shift to the signal given in part (b).

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Problem 1.

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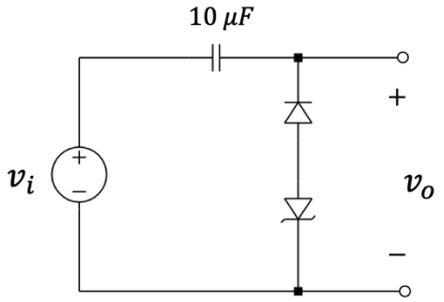
Problem 2. (10 points)

In the circuit below, $v_i(t) = 5\ sin\ (\omega t)$ where $\omega = 1000$ rad/s, $v_o(0) = 0$.

Use $V_{D0} = 0.7\ V$, $V_Z = 2.3\ V$.



a) What is the value of $v_o(t)$ at t = 2 ms?

b) What is the value of $v_o(t)$ at t = 4 ms?

c) What is the value of $v_o(t)$ at t = 6 ms?

d) Sketch the graph of $v_o(t)$ for $0 \leq t \leq 3 \times 3.14\ ms$.

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Problem 2.

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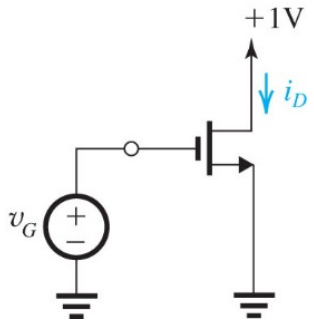
Problem 3. (6 points)

The NMOS in the below circuit has $V_t = 0.5\ V$ and $k_n = \mu_n C_{ox} \frac{W}{L} = 1\ mA/V$.



a) Sketch (approximately) the graph of i_D vs v_G with v_G varying in the range of 0 to 2 V. Clearly label your graph.

b) Write i_D equation(s) for the various portions of the resulting graph.

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Problem 3.

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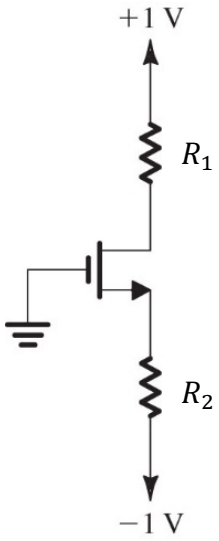
Problem 4. (10 points)

Design the following circuit (find R_D and R_s) for a drain voltage of $+0.3\ V$ and drain current of $0.1\ mA$. Assume $V_t = 0.5\ V$, k_n= $5\ mA/V^2$ and $\lambda = 0$.



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Problem 4.

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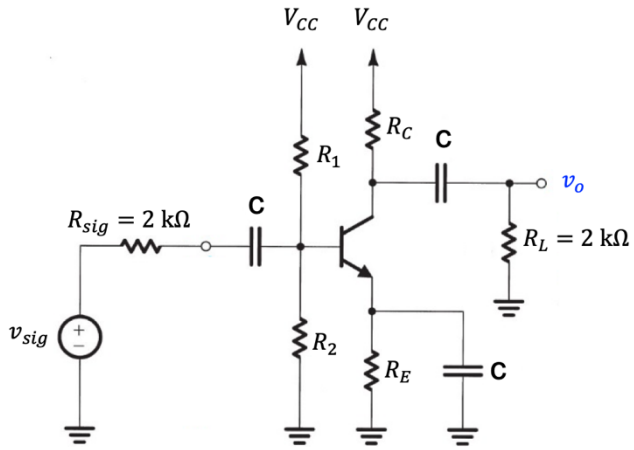
Problem 5. (12 points)

Design the following amplifier circuit, to achieve a voltage gain of $v_0/v_{sig} = -40\ V/V$.

- You have a 15 V power supply available.
- An emitter current of 2 mA is desired.
- The current through R_2 is to be one-tenth of I_E.
- The DC voltage at the base should be equal to one-third of the power supply.
- The available transistor has $\beta = 100$ and $V_{D0} = 0.7\ V$.
- Draw the signal circuit and calculate the signal parameters.

Ignore the early effect in bias and signal circuits. Assume Capacitors are short in the signal circuit. Use $V_T = 25\ mV$.



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Problem 5.

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