UNIVERSITY OF CALIFORNIA, SAN DIEGO

Electrical and Computer Engineering Department ECE 65 – Spring 2022

Components and Circuits lab

Final Exam

- Closed books, four double-sided cheat sheets, and calculators are allowed
- Electronic devices are not allowed.
- Please put all answers in the provided sheets.
- You can use the back of every page as a scratch paper.
- Please submit your handwritten solutions to Gradescope by 2:40 pm.

Please do not begin until you are told to do so.

Show your work and good luck!

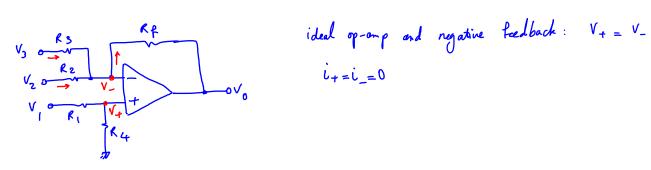
PID

Problem 1.

Design an op-amp circuit using only one op-amp and assuming ideal op-amps to implement the function of

$$v_0 = 2v_1 - 2v_2 - 4v_3$$

in which v_1 , v_2 , and v_3 are three input voltages and v_o is the output voltage.



$$V_{+} = \frac{R_{4}}{R_{14}R_{4}}V_{1}$$

$$\begin{aligned} & \text{KCL} \quad \textcircled{0} \quad V_{-} \quad : \quad \frac{V_{2} - V_{-}}{R_{2}} \, + \, \frac{V_{3} - V_{-}}{R_{3}} \, = \, \frac{V_{-} - V_{0}}{R_{p}} \\ & \quad - \frac{1}{R_{2}} \, V_{2} - \frac{1}{R_{3}} \, V_{3} \, + \left(\frac{1}{R_{2}} \, + \frac{1}{R_{3}} \, + \, \frac{1}{R_{p}} \right) \, V_{-} \, = \, \frac{1}{R_{p}} \, V_{0} \\ & \quad - \frac{1}{R_{2}} \, V_{2} - \frac{1}{R_{3}} \, V_{3} \, + \left(\frac{R_{3} \, R_{4} \, + \, R_{2} \, R_{4} + R_{2} \, R_{3}}{R_{2} \, R_{3} \, R_{p}} \right) \, V_{-} \, = \, \frac{1}{R_{p}} \, V_{0} \\ & \quad V_{0} \, = \, \frac{-R_{p}}{R_{2}} \, V_{2} \, - \, \frac{R_{p}}{R_{3}} \, V_{3} \, + \, \left(\frac{R_{3} \, R_{4} \, + \, R_{2} \, R_{4} + R_{2} \, R_{4} + R_{2} \, R_{4}}{R_{2} \, R_{3}} \right) \, V_{-} \end{aligned}$$

$$\begin{cases} V_{0} = -\frac{R f}{R_{2}} V_{2} - \frac{R f}{R_{3}} V_{3} + \left(\frac{R_{3} R f + R_{2} R f + R_{2} R_{3}}{R_{2} R_{3}} \right) V_{-} \\ V_{+} = \frac{R f}{R_{1} f R_{1}} V_{1} & \text{and} & V_{-} = V_{+} \end{cases}$$

$$\begin{cases} V_{0} = -\frac{R \rho}{R_{2}} V_{2} - \frac{R \rho}{R_{3}} V_{3} + \left(\frac{R_{3} R \rho + R_{2} R \rho + R_{2} R_{3}}{R_{2} R_{3}} \right) \left(\frac{R \rho}{R_{1} + R_{2} R \rho} \right) V_{1} \\ V_{0} = 2 V_{1} - 2 V_{2} - 4 V_{3} \end{cases}$$

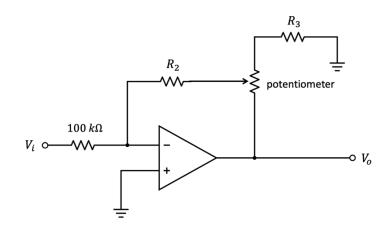
$$\frac{-R_{f}}{R_{2}} = -2 , \frac{-R_{f}}{R_{3}} = -4 , R_{f} = 4 \text{ k.r.}, R_{2} = 2 \text{ k.r.}$$

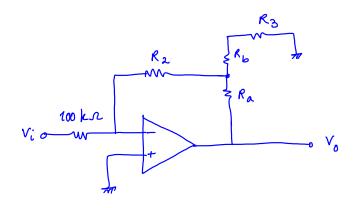
$$\frac{4+8+2}{2} \times \frac{R_4}{R_{1+}R_4} = 2 \longrightarrow \frac{R_4}{R_{1+}R_4} = \frac{4}{14}$$

$$R_{4} = 4 \text{ k.r.}, R_{1} = 10 \text{ k.r.}$$

Problem 2.

Design the following circuit (find R_2 and R_3) such that the voltage gain can be varied between -1 V/V and -100 V/V. Assume that the op-amp is ideal, and you have a $100 k\Omega$ potentiometer.

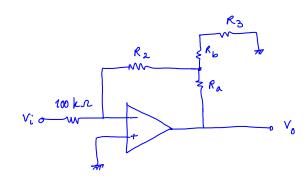




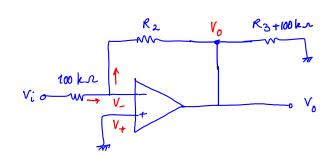
$$R_{a+}R_{b} = 100 \text{ km}$$

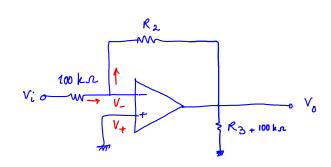
Two cases for the -1
$$\frac{1}{y}$$
 and -100 $\frac{1}{y}$ gain:
$$R_{a} = 0, R_{b} = 100 \text{ k.s.}, R_{b} = 0$$

Ra = 0 , Rb = 100ks









0p-amp is ideal and there is negotive feedback: $i_{+}=i_{-}=0$ $V_{+}=V_{-}$

 $V_{+}=0$ \longrightarrow $V_{-}=0$

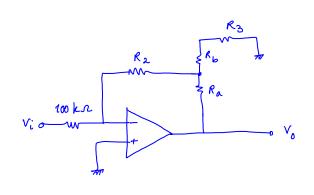
 $KCL @ V_{-} : \frac{V_{.}^{-} - V_{-}}{100 \text{ kg}} = \frac{V_{-} V_{0}}{R_{2}}$

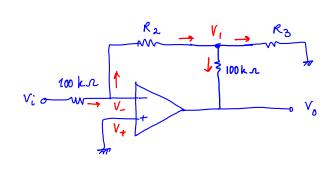
$$\frac{V_{i}-0}{100 \,\mathrm{kg}} = \frac{-V_{0}}{R_{2}} \qquad \Rightarrow \frac{V_{0}}{V_{i}} = -\frac{R_{2}}{100 \,\mathrm{kg}}$$

$$R_2 = 100 \text{ kg} \longrightarrow \frac{V_0}{V_i} = -1 \text{ } \frac{V_V}{V_i}$$

PID

 $R_a = 100 \text{ ks}$, $R_b = 0$





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 $V_{+}=0$ \longrightarrow $V_{-}=0$

$$KCL @ V_{-} : \frac{V_{.}^{-} - V_{-}}{100 \text{ kg}} = \frac{V_{-} V_{i}}{R_{2}}$$

$$\frac{V_{i-0}}{100\,\mathrm{kr}} = \frac{-V_{i}}{R_{2}}$$

$$\frac{V_{i}-0}{100 \,\mathrm{kr}} = \frac{-V_{i}}{R_{2}} \qquad \Longrightarrow \qquad V_{i} = -\frac{100 \,\mathrm{kr}}{R_{2}} \,V_{i}$$

KCL @ V2:

$$\frac{V_{-}-V_{1}}{R_{2}}=\frac{V_{1}-V_{0}}{100\,\mathrm{kn}}+\frac{V_{1}}{R_{3}}$$

$$\frac{0 - \frac{1}{2}}{R_2} = \frac{\frac{1}{2} - \frac{1}{2}}{100 \, \text{km}} + \frac{\frac{1}{2}}{R_3}$$

$$\frac{0 - \frac{V_1}{R_2}}{R_2} = \frac{V_1 - \frac{V_0}{R_3}}{100 \, \text{km}} + \frac{V_1}{R_3}$$

$$\frac{1}{100 \, \text{kn}} \, V_0 = \left(\frac{1}{R_2} + \frac{1}{R_3} + \frac{1}{100 \, \text{kn}} \right) \, V_1 = \left(\frac{100 \, R_3 + 100 R_2 + R_2 R_3}{R_2 R_3 \times 100} \right) \, V_1$$

$$\frac{100R_3 + 100R_2 + R_2R_3}{100R_3 + 100R_2 + R_2R_3} \quad V_0$$

from last page:

$$V_{i} = -\frac{100 \, \text{kn}^{R} \, 3}{100 \, R_{3} + 100 \, R_{2} + R_{2} \, R_{3}} \, V_{0}$$

$$\frac{V_0}{V_i} = -\left(1 + \frac{R_2 + \frac{R_2 R_3}{100}}{R_3}\right) = -100 \text{ } \frac{V_V}{V_i}$$

PID

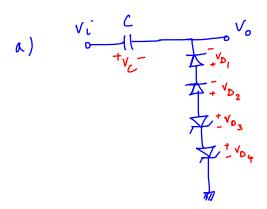
Problem 3.

- a) Design a diode circuit to add +2 V DC shift to a sinusoidal input voltage with peak amplitude of 10 V and frequency of 2 kHz. You should use regular PN junction diode(s) and Zener diode(s) in your design. Assume $V_{D0} = 0.7 V$ and $V_Z = 3.3 V$.
 - Drawing the circuit is enough for this part.
- b) Find the output at

i.
$$t = 100 \, \mu s$$

ii.
$$t = 450 \, \mu s$$

- You need to show your work on how you found the output voltage at these two time points.
- c) Draw the output waveform for $0 \le t \le 1 \, ms$.

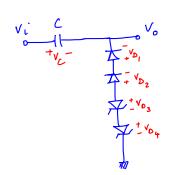


b)
$$V_{c} = V_{i} - (V_{D_{4}} + V_{D_{3}}) + V_{D_{1}} + V_{D_{2}}$$

when $V_i = -8 \, \text{V}$, D_i and D_2 will turn on and D_3 and D_4 will be in the Zener mode. The diodes will conduct and the capacitor will change untill V_i neaches $-10 \, \text{V}$. After that the diodes will turn off and V_c will not change.

When the diodes turn off: $V_c = -10 - (-3.3 - 3.3) + 0.7 + 0.7 = -2V$

After the negative peak of V_i : $V_0 = -(-2) + V_i' = 2 + V_i'$ +2V DC shift



$$f = \frac{1}{T} = 2000 \text{ Hz} \implies T = 0.5 \text{ ms} = 500 \text{ Ms}$$

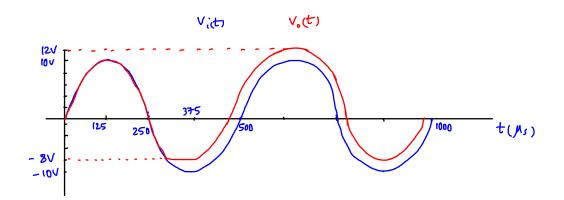
$$t = 100 \text{ /s} < \frac{T}{4} \longrightarrow \text{ Diodes are all }, V_c = 0 \longrightarrow V_o = V_c$$

$$t=450~\text{Ms}$$
 \longrightarrow ofter the negative peak: $V_0=2+V_1(t=450~\text{Ms})$

$$=2+10~\text{Sin}~(2\pi\times2k\times0.45\text{m})$$

$$=2-5.88=-3.88~\text{V}$$

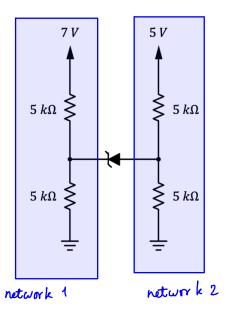
۲)



Problem 4

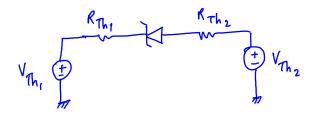
Find the current through the diode and the voltage across it in the below circuit.

Assume $V_{D0} = 0.7 V$ and $V_Z = 2 V$.



Show your work.

There nin equivalent circuit for networks 1 and 2



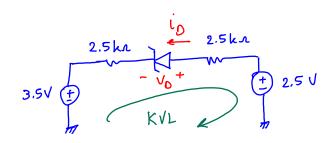
$$R_{Th_{1}} = 5 kn | | 5 kn = 2.5 kn$$

$$R_{Th_{2}} = 5 kn | | 5 kn = 2.5 kn$$

$$V_{Th_{1}} = \frac{5 kn}{5 kn + 5 kn} \times 5V = 2.5V$$

$$V_{Th_{2}} = \frac{5 kn}{5 kn + 5 kn} \times 7V = 3.5V$$

PID



Assume the zener diode is off: $-\frac{V_{Z}}{V_{O}} < V_{O}$ and $i_{O} = 0$ $-2 < \frac{V_{O}}{V_{O}} < 0.7$

 $KVL: -3.5 - 2.5 \text{ kn} \times i_0 - V_0 - 2.5 \text{ kn} \times i_0 + 2.5 = 0$ $\rightarrow V_0 = -1 - 5 \text{ kn} \times i_0$

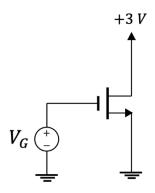
$$i_D = 0 \longrightarrow V_D = -1$$

-2 (VD = -1 < 0.7 = Assumption is correct.

$$i_{D} = 0$$
 and $V_{D} = -1 V$

Problem 5

The MOSFET in the below circuit has $V_t = 1 V$ and $\mu C_{ox} \frac{W}{L} = 1.5 \ mA/V^2$, and $\lambda = 0$.

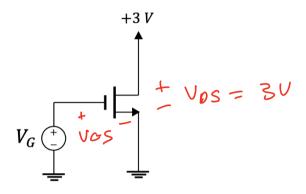


- a) Sketch (approximately) the graph of I_D vs V_G with V_G varying in the range of 0 V to 5 V. Label your graph.
- b) Write I_D equation(s) for the various portions of the resulting graph.

PID Name

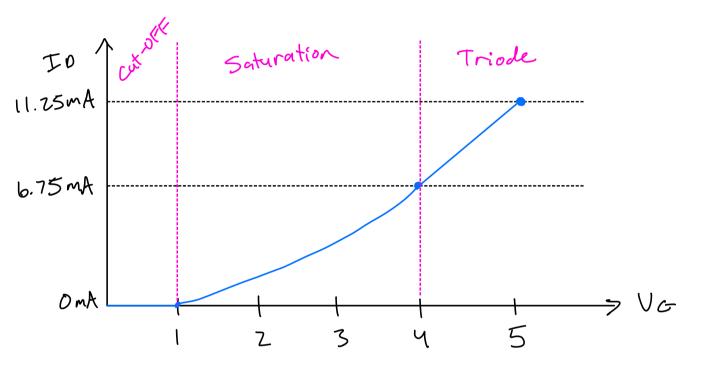
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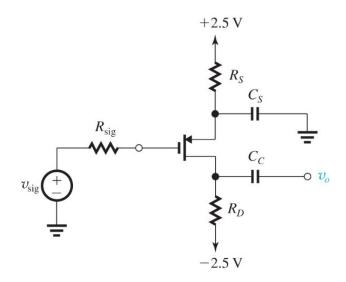
Triode: Vovzo Vos & Vov -> 3 & VG - Vt -> VGZY To = 0.5 m Cox (W/L)(2VovVos - Vos) = 0.75 m A (6(VG - 1) - 9) To = 4.5 m A · VG - [1.25 m A



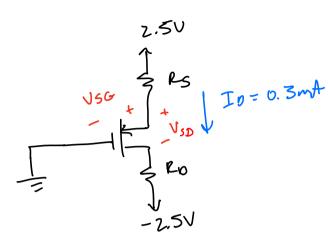
Problem 6.

The MOSFET in the following amplifier circuit has $|V_t| = 0.6 V$. Neglect the early effect in the bias and signal circuits, and assume the capacitors are short for the signal circuit.

- a) Find R_S and R_D to bias the transistor at $I_D = 0.3 \, mA$ and $V_{OV} = 0.4 \, V$ and achieve the voltage amplifier gain of $A_V = -12 \, V/V$. (Capacitors are short for the signal circuit)
- b) Find the largest \hat{v}_{sig} (\hat{v}_{sig} shows the peak amplitude of the sinusoid v_{sig}) that the amplifier can handle while remaining in the saturation region. Find the peak amplitude of the corresponding signal at the output?
- c) If \hat{v}_{sig} is limited to 10 mV, what value can R_D be increased to while maintaining saturation region operation (R_S does not change)? What is the new value of A_V ?



Bias Circuit



Signal Circuit step 1:

PID

$$PS = 2.5 - VSG$$

$$= \frac{2.5 - 1}{6.3MA}$$

$$PS = 5Kr$$

Usig (†)
Rsig

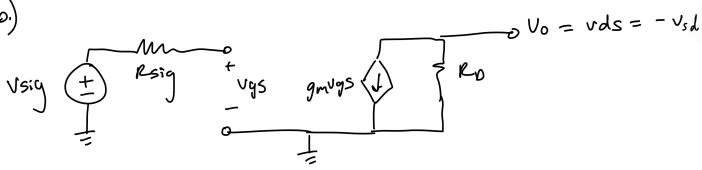
$$g_{M} = \frac{2Io}{vov}$$

$$= 1.5 \frac{mt}{vo}$$

$$= \frac{1}{3.50} = \frac{1}{0} = 20$$

Common Source Au = Auo = -gm (Ro//ro) -12 = -gmRo

5 = Io(RO+RS) + VSO -> VSD = 5 - 0.3 mA(13k) V50 = 1.1V



$$\sqrt{g}s = \sqrt{sig} = -\sqrt{sg}$$

$$V_{sd} = -g_m R_D V_{sg} = \gamma A_V = \frac{V_{sd}}{V_{sg}} = -g_m R_D$$

$$\hat{V}_{sd}$$
 is the max amplitude of the signal V_{sd} . \hat{V}_{sd} is positive.

$$V_{SO} - \hat{V}_{SA} > V_{SG} + \frac{\hat{V}_{SA}}{|A_V|} - |V_{tP}|$$

$$(1+\frac{1}{|A_{y}|})\hat{V}_{SL}$$
 (1.1 -1 + 0.6

$$\hat{V}_{sd} \leqslant \frac{0.7V}{1+\frac{1}{12}} \simeq 0.65 \text{ V}$$

max amplitude of vsd

c)
$$\hat{V}_{sig} = 10 \text{ mV}$$

From part b we know that

$$V_{SD} = V_{S} - V_{D} = 2.5 - R_{S} I_{D} - (R_{D} I_{O} - 2.5) = -5 k_{D} \times 0.3 \text{ mA} + 5 - R_{D} \times 0.3 \text{ mA}$$

$$= 3.5 - R_{D} \times 0.3 \text{ mA}$$

$$V_{SG} = V_{oV} + |V_{tP}| = 1 V$$

$$\hat{V}_{sig} = 10 \text{ m V} = 0.01 \text{ V}$$

$$0.01 + 0.01(v) \times 1.5(\frac{mA}{V}) \times R_0 \leq 3.1 - R_0 \times 0.3 \text{ mA}$$

$$(0.3 + 0.015) R_D \leq 3.09$$

$$R_D \leqslant 9.81 \text{ ks} \longrightarrow R_{0_{\text{max}}} = 9.81 \text{ ks}$$