ECE 65: Components & Circuits Lab

Lecture 16

CMOS NAND gates

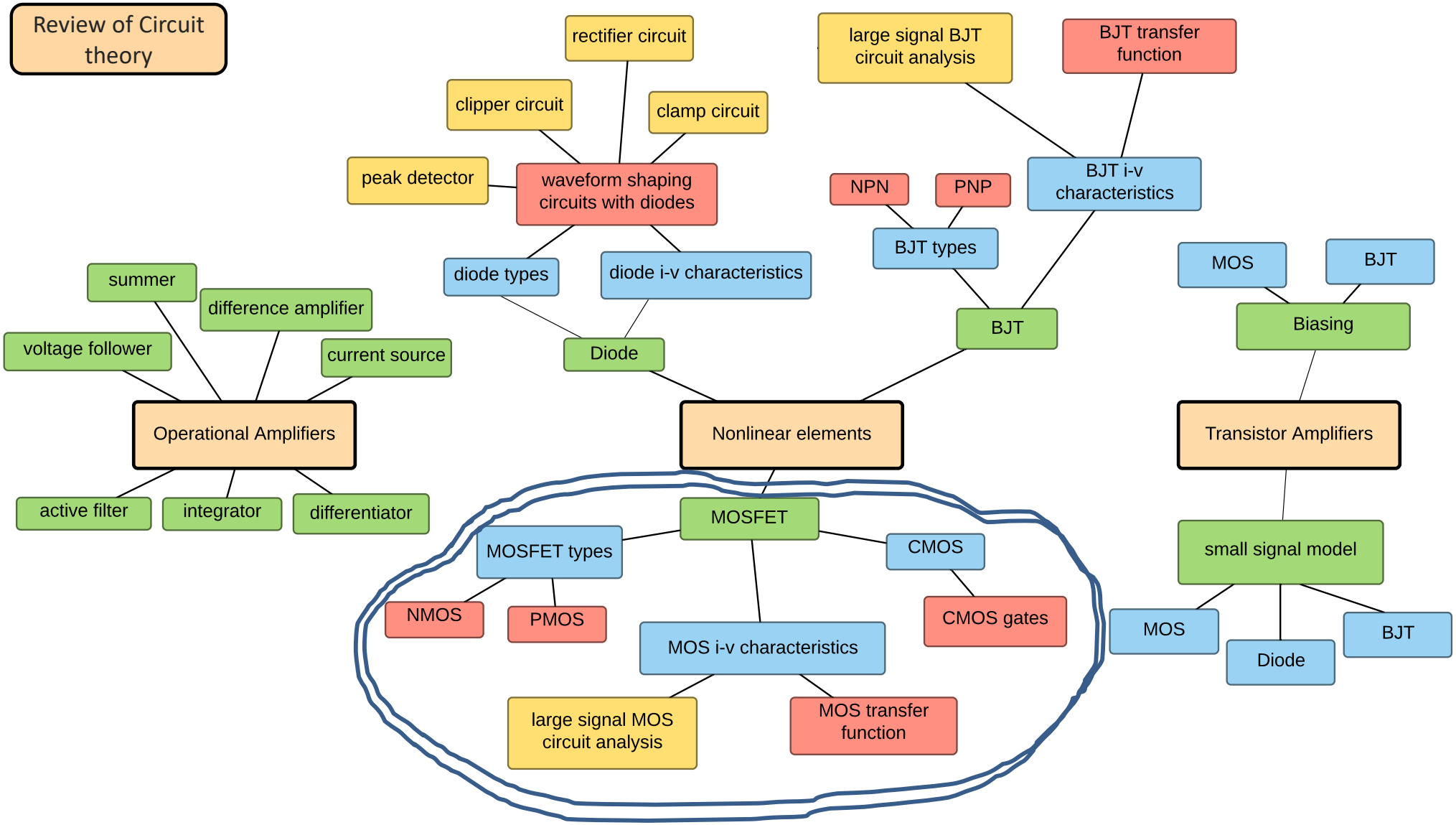
Reference notes: sections 4.4

Sedra & Smith (7th Ed): sections 5.1.8, 14.3

Saharnaz Baghdadchi

Course map

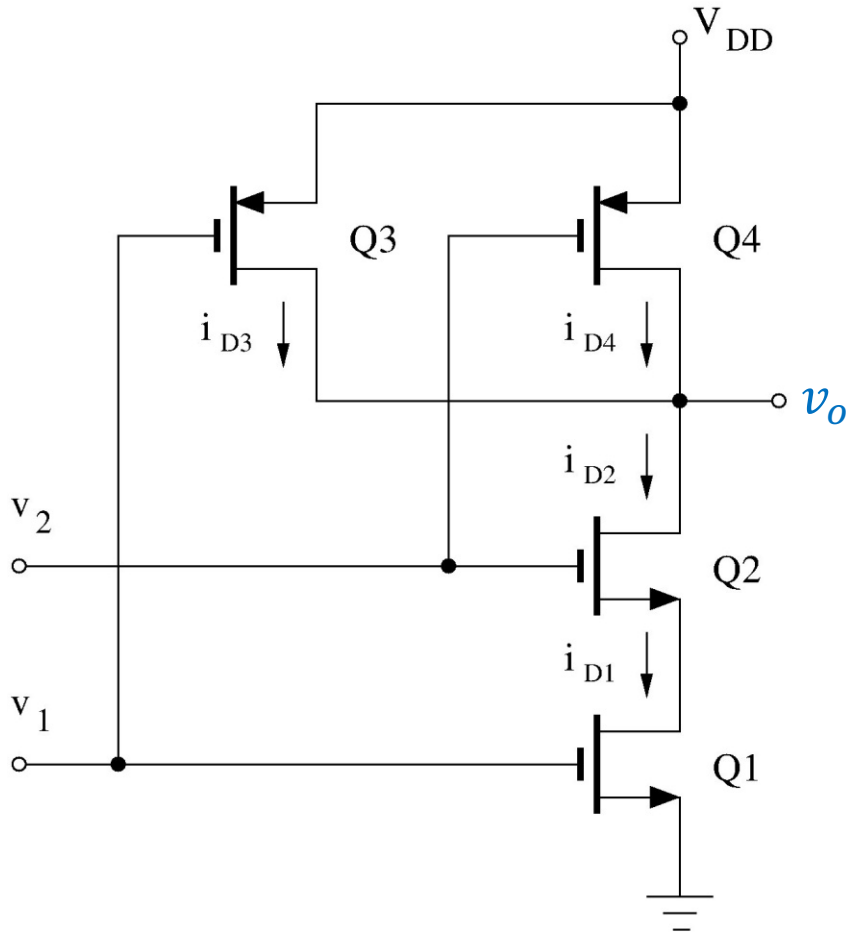
5. Metal Oxide Semiconductor Field Effect Transistor (MOSFET)



CMOS NAND Gate

Truth Table

$v_1 = 0$	$v_2 = 0$:	$v_o = V_{DD}$
$v_1 = 0$	$v_2 = V_{DD}$:	$v_o = V_{DD}$
$v_1 = V_{DD}$	$v_2 = 0$:	$v_o = V_{DD}$
$v_1 = V_{DD}$	$v_2 = V_{DD}$:	$v_o = 0$



Analysis of CMOS NAND Gate

GS1-KVL: $v_{GS1} = v_1$

GS2-KVL: $v_2 = v_{GS2} + v_{DS1}$

$\rightarrow \quad v_{GS2} = v_2 - v_{DS1}$

GS3-KVL: $V_{DD} = v_{SG3} + v_1$

$\rightarrow \quad v_{SG3} = V_{DD} - v_1$

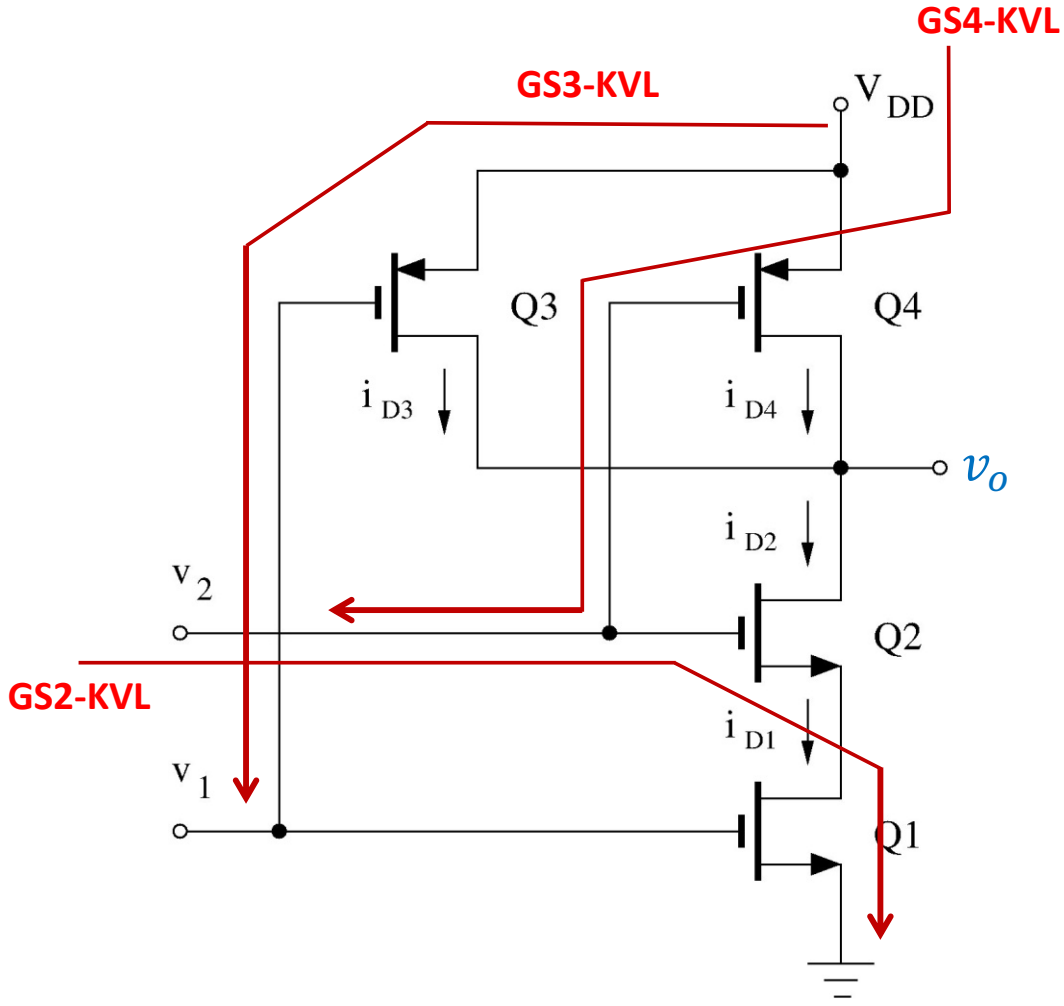
GS4-KVL: $V_{DD} = v_{SG4} + v_2$

$\rightarrow \quad v_{SG4} = V_{DD} - v_2$

DS-KVL: $V_{DD} = v_{SD4} + v_{DS2} + v_{DS1}$

$v_{SD3} = v_{SD4}$

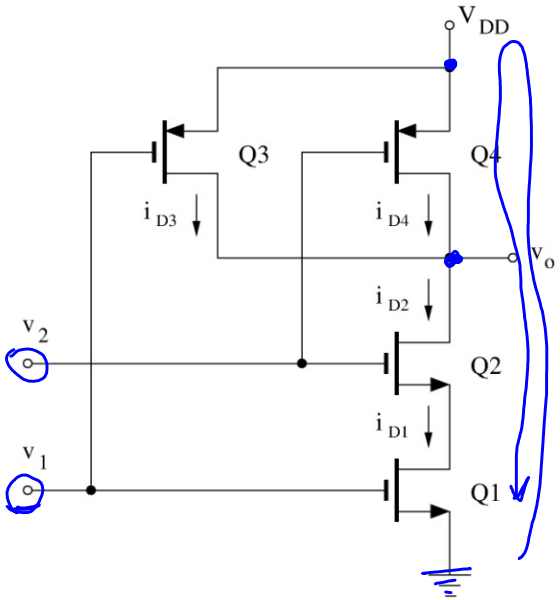
KCL: $i_{D1} = i_{D2} = i_{D3} + i_{D4}$



$v_o = v_{DS1} + v_{DS2}$

$v_o = V_{DD} - v_{SD4} = V_{DD} - v_{SD3}$

Analysis of CMOS NAND Gate



Case 1: $v_1 = V_{DD}$ & $v_2 = 0$

$V_{GS_1} = V_1 = V_{DD} > V_{tn} \longrightarrow Q_1$ is ON

$V_{GS_2} = V_2 - V_{DS_1} = -V_{DS_1} < V_{tn} \longrightarrow Q_2$ is off $\longrightarrow i_{D_2} = 0$

$i_{D_1} = i_{D_2} = 0$

$\Longrightarrow Q_1$ is ON, $i_{D_1} = 0$, $V_{DS_1} = 0$

$V_{SG_3} = V_{DD} - V_1 = 0 < |V_{tp}| \longrightarrow Q_3$ off $\longrightarrow i_{D_3} = 0$

$V_{SG_4} = V_{DD} - V_2 = V_{DD} > |V_{tp}| \longrightarrow Q_4$ is ON

$i_{D_3} + i_{D_4} = i_{D_2} \longrightarrow i_{D_4} = 0$, Q_4 is in Triode mode, $V_{SD_4} = 0$

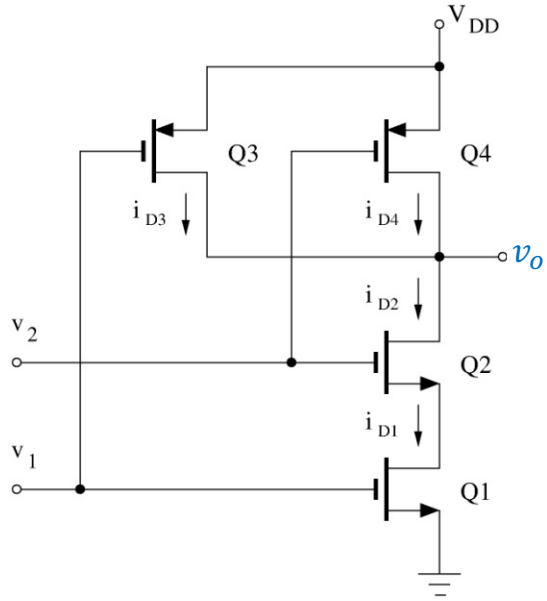
$V_0 = V_{DD} - V_{SD_4} = V_{DD}$

Lecture 16 reading quiz

In the following two-input CMOS NAND gate, find the state of Q1 and Q4 when $v_1 = 0$ & $v_2 = 0$, and when $v_1 = 0$ & $v_2 = V_{DD}$.

Analysis of CMOS NAND Gate

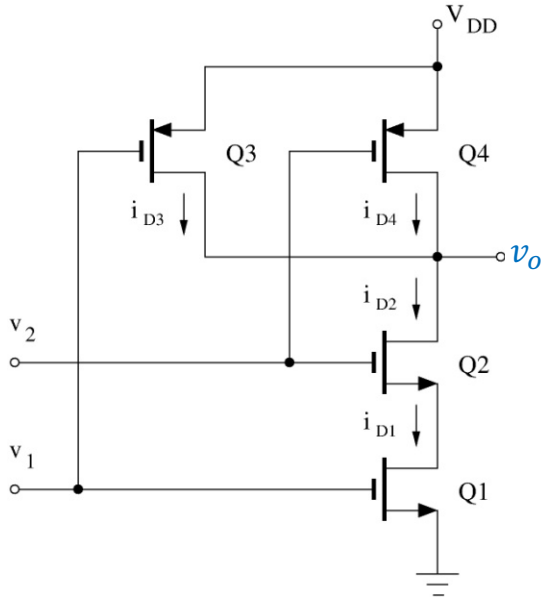
Case 2: $v_1 = 0$ & $v_2 = 0$



Hints:

Analysis of CMOS NAND Gate

Case 2: $v_1 = 0$ & $v_2 = 0$



- Label all the voltages.

- Check if the MOSFETs are in Cut-off or ON.

- If you do not have enough information to determine the mode of operation of a MOSFET, you can skip determining the mode of operation of that MOFET and move on to the next MOSFET. After you have all the unknowns, including vout, you can come back and make an assumption for the mode of operation of that MOSFET and check the assumption.

- Find the drain currents.

    - If a MOSFET is in Cut-off, i_D=0.

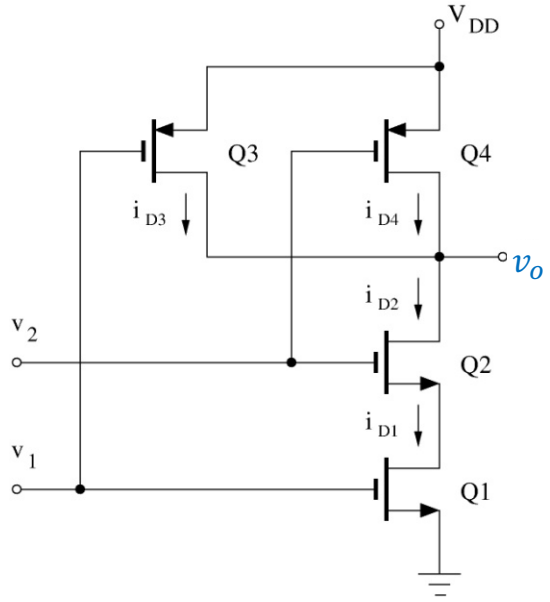
    - You can also write KCL to find the unknown currents.

    - Also, if a MOSFET is ON with i_D=0, the MOS will be in triode mode with V_{DS}=0.

- Find vout using the values of known V{DS} or V_{SD}

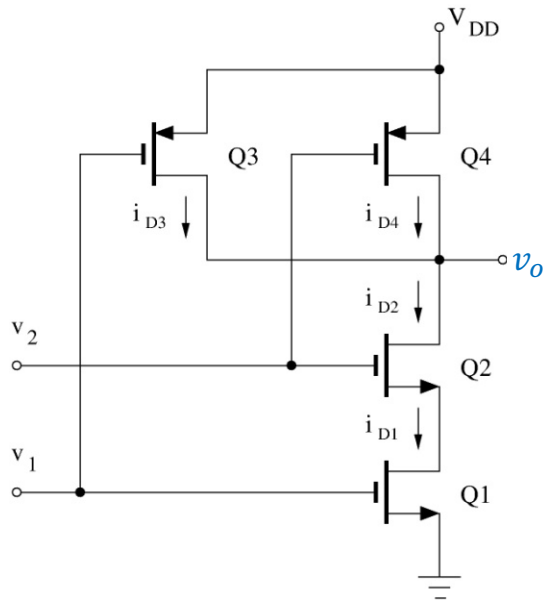
Analysis of CMOS NAND Gate

Case 2: $v_1 = 0$ & $v_2 = 0$



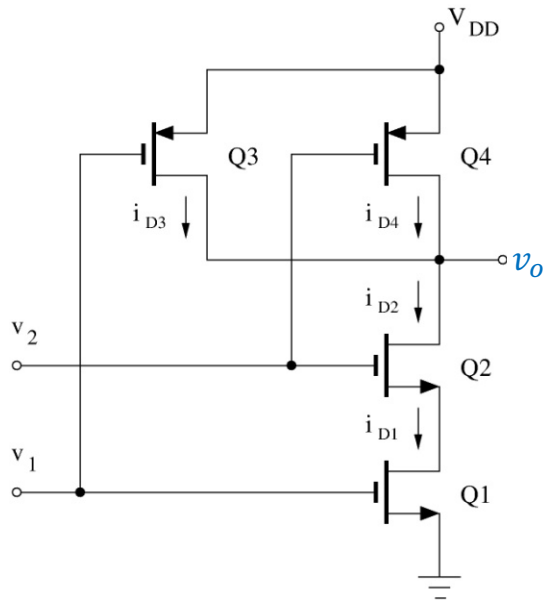
Analysis of CMOS NAND Gate

Case 3: $v_1 = 0$ & $v_2 = V_{DD}$



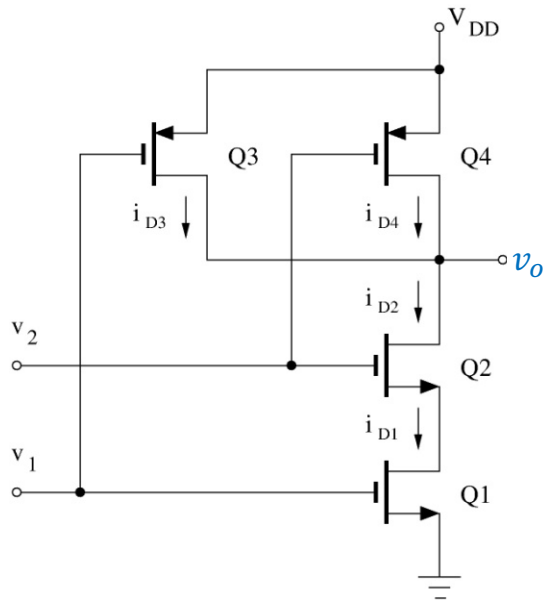
Analysis of CMOS NAND Gate

Case 3: $v_1 = 0$ & $v_2 = V_{DD}$



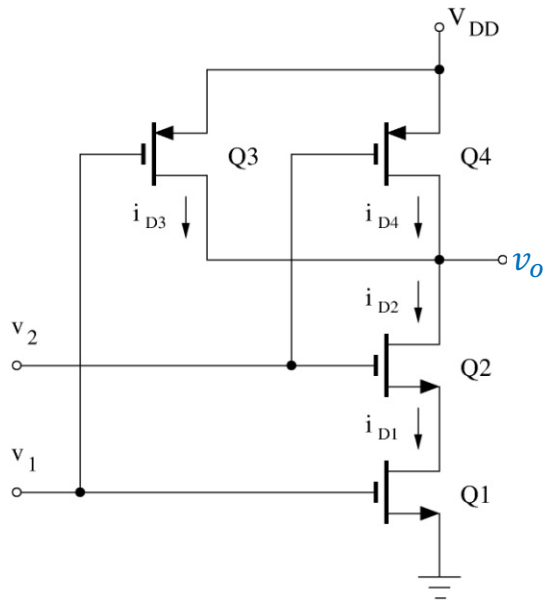
Analysis of CMOS NAND Gate

Case 4: $v_1 = V_{DD}$ & $v_2 = V_{DD}$



Analysis of CMOS NAND Gate

Case 4: $v_1 = V_{DD}$ & $v_2 = V_{DD}$



Discussion question 1.

Sketch a three input NAND gate using CMOS technology.