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ECE 111 HW2 | 10/16/2024

alu_top.sv

```
ucsd > ece111 > HW > Homework2 > Lab2 > alu_top > alu_top.sv
1 // N-bit ALU TOP RTL code
2 module alu_top // Module start declaration
3 #(parameter N=4) // Parameter declaration
4 (
5     input logic clk, reset,
6     input logic[N-1:0] operand1, operand2,
7     input logic[3:0] select,
8     output logic[(2*N)-1:0] result
9 );
10
11 // Local net declaration
12 // logic[(2*N):0] alu_out;
13 logic[(2*N)-1:0] alu_out;
14
15 // Student to Add instantiation of module alu
16 alu #(N(N)) alu_inst (
17     .operand1(operand1), // Connect operand1 from alu_top to alu
18     .operand2(operand2), // Connect operand2 from alu_top to alu
19     .operation(select), // Connect select to operation in ALU
20     .alu_out(alu_out) // Connect ALU output to local net alu_out
21 );
22
23 // Adding flipflop at the output of ALU
24 always@(posedge clk or posedge reset) begin
25     if(reset == 1) begin
26         result <= 0;
27     end
28     else begin
29         result <= alu_out;
30     end
31 end
32 endmodule: alu_top // Module alu_top end declaration
```

The screenshot displays the Quartus Prime IDE environment. The central editor shows the Verilog code for `alu_top.sv`. The left-hand pane shows the Project Navigator with the hierarchy of the project. The right-hand pane shows the IP Catalog with installed IP components. The bottom pane shows the Messages window with the following content:

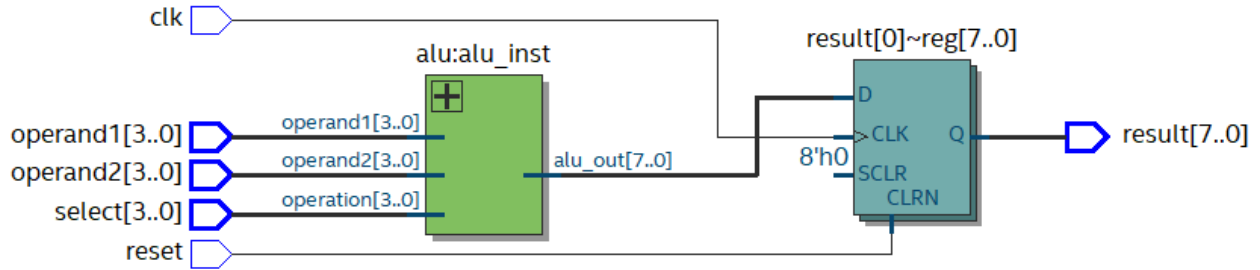
```
Type ID Message
332148 Timing requirements not met
332146 Worst-case minimum pulse width slack is -2.846
21076 High junction temperature operating condition is not set. Assuming a default value of '100'.
21076 Low junction temperature operating condition is not set. Assuming a default value of '-40'.
332154 The derive_clock_uncertainty command did not apply clock uncertainty to any clock-to-clock transfers.
332102 Design is not fully constrained for setup requirements
332102 Design is not fully constrained for hold requirements
Quartus Prime Timing Analyzer was successful. 0 errors, 5 warnings
*****
Running Quartus Prime EDA Netlist Writer
Command: quartus_eda --read_settings_files=off --write_settings_files=off alu_top -c alu_top
18236 Number of processors has not been specified which may cause overloading on shared machines. Set the global assignment NUM_PAR
204019 Generated file alu_top.svo in folder "C:/Users/Ryo Andrew Onozuka/Documents/GitHub/notes/ucsd/ece111/HW/Homework2/Lab2/alu_top
Quartus Prime EDA Netlist Writer was successful. 0 errors, 1 warning
293000 Quartus Prime Full Compilation was successful. 0 errors, 17 warnings
```

alu_top.sv Resource Usage Summary

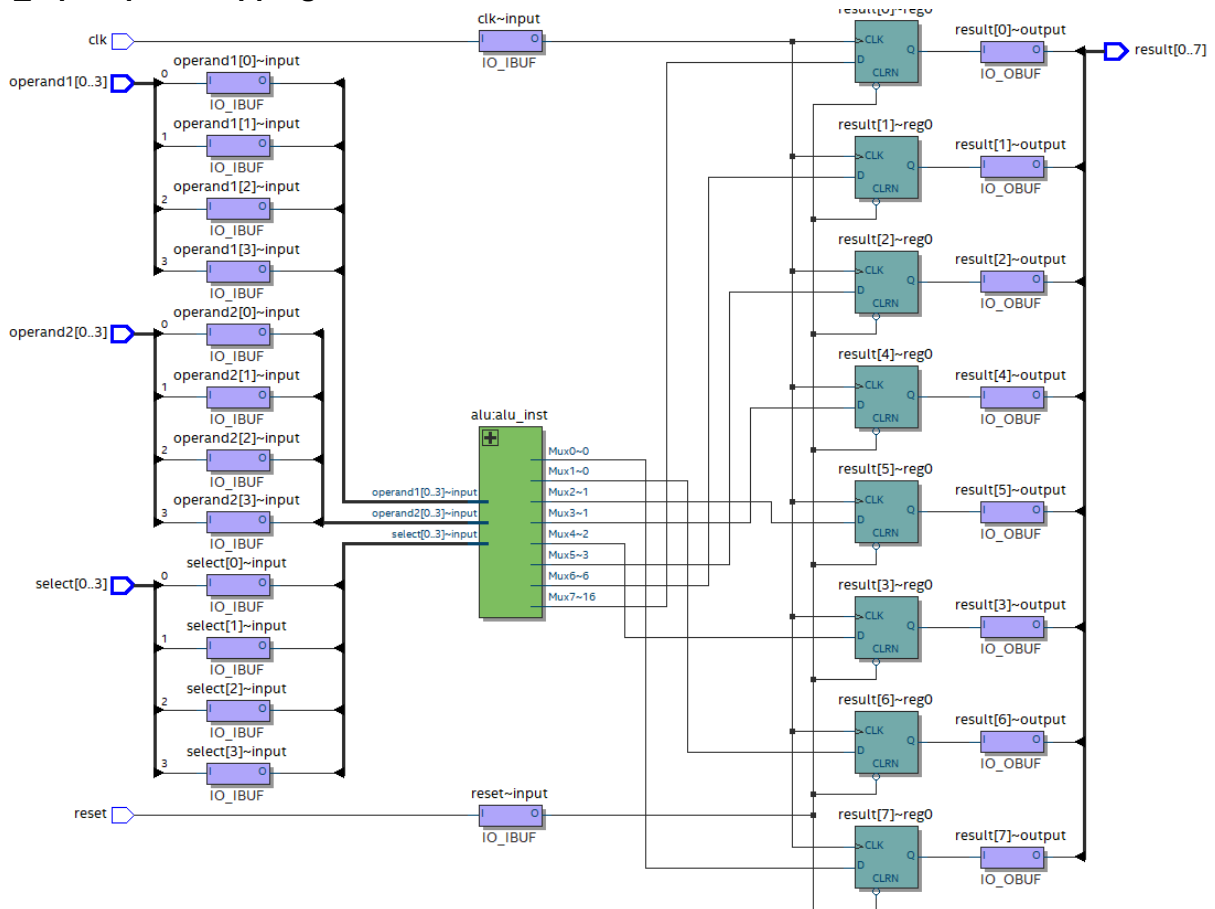
ucsd > ece111 > HW > Homework2 > Lab2 > alu_top > alu_top-Resource Usage Summary.rpt

34	+-----+-----+-----+		
35	; Analysis & Synthesis Resource Usage Summary		;
36	+-----+-----+-----+		
37	; Resource	; Usage	;
38	+-----+-----+-----+		
39	; Estimated ALUTs Used	; 113	;
40	; -- Combinational ALUTs	; 113	;
41	; -- Memory ALUTs	; 0	;
42	; -- LUT_REGS	; 0	;
43	; Dedicated logic registers	; 8	;
44	;	;	;
45	; Estimated ALUTs Unavailable	; 9	;
46	; -- Due to unpartnered combinational logic	; 9	;
47	; -- Due to Memory ALUTs	; 0	;
48	;	;	;
49	; Total combinational functions	; 113	;
50	; Combinational ALUT usage by number of inputs		;
51	; -- 7 input functions	; 3	;
52	; -- 6 input functions	; 6	;
53	; -- 5 input functions	; 21	;
54	; -- 4 input functions	; 31	;
55	; -- <=3 input functions	; 52	;
56	;	;	;
57	; Combinational ALUTs by mode		;
58	; -- normal mode	; 54	;
59	; -- extended LUT mode	; 3	;
60	; -- arithmetic mode	; 33	;
61	; -- shared arithmetic mode	; 23	;
62	;	;	;
63	; Estimated ALUT/register pairs used	; 122	;
64	;	;	;
65	; Total registers	; 8	;
66	; -- Dedicated logic registers	; 8	;
67	; -- I/O registers	; 0	;
68	; -- LUT_REGS	; 0	;
69	;	;	;
70	;	;	;
71	; I/O pins	; 22	;
72	;	;	;
73	; DSP block 18-bit elements	; 0	;
74	;	;	;
75	; Maximum fan-out node	; operand2[3]~input	;
76	; Maximum fan-out	; 31	;
77	; Total fan-out	; 466	;
78	; Average fan-out	; 2.82	;
79	+-----+-----+-----+		

alu_top.sv RTL viewer



alu_top.sv post mapping viewer



alu.sv

```

ucsd > ece111 > HW > Homework2 > Lab2 > alu_top > alu.sv
1 // 1-bit ALU behavioral code
2 module alu // Module start declaration
3 #(parameter N=4) // Parameter declaration
4 (
5     input logic[N-1:0] operand1, operand2,
6     input logic[3:0] operation,
7     output logic[(2*N)-1:0] alu_out
8 );
9
10 // always procedural block describing alu operations
11 always@(operand1 or operand2 or operation)
12 begin
13     case (operation)
14         4'b0000: alu_out = operand1 + operand2; // Addition
15         4'b0001: alu_out = operand1 - operand2; // Subtraction
16         4'b0010: alu_out = operand1 * operand2; // Multiplication
17         4'b0011: alu_out = operand1 % operand2; // Modulo
18         4'b0100: alu_out = operand1 / operand2; // Division
19         4'b0101: alu_out = operand1 & operand2; // Bitwise AND
20         4'b0110: alu_out = operand1 | operand2; // Bitwise OR
21         4'b0111: alu_out = operand1 ^ operand2; // Bitwise XOR
22         4'b1000: alu_out = operand1 && operand2; // Logical AND
23         4'b1001: alu_out = operand1 || operand2; // Logical OR
24         4'b1010: alu_out = operand1 << 1; // Left shift by 1
25         4'b1011: alu_out = operand1 >> 1; // Right shift by 1
26         4'b1100: alu_out = (operand1 == operand2) ? 1 : 0; // Logical Equality
27         4'b1101: alu_out = (operand1 != operand2) ? 1 : 0; // Logical Inequality
28         4'b1110: alu_out = (operand1 < operand2) ? 1 : 0; // Less Than Comparison
29         4'b1111: alu_out = (operand1 > operand2) ? 1 : 0; // Greater Than Comparison
30         default: alu_out = operand1 + operand2; // Default operation is addition
31     endcase
32 end
33 endmodule: alu

```

The screenshot displays the Quartus Prime IDE interface. The main editor window shows the Verilog code for the `alu.sv` module, which implements a 1-bit ALU with various operations. The code is syntax-highlighted and includes comments for each operation.

On the left, the Project Navigator shows the file structure, and the Tasks window lists compilation tasks. The Messages window at the bottom provides detailed feedback from the Quartus Prime tools:

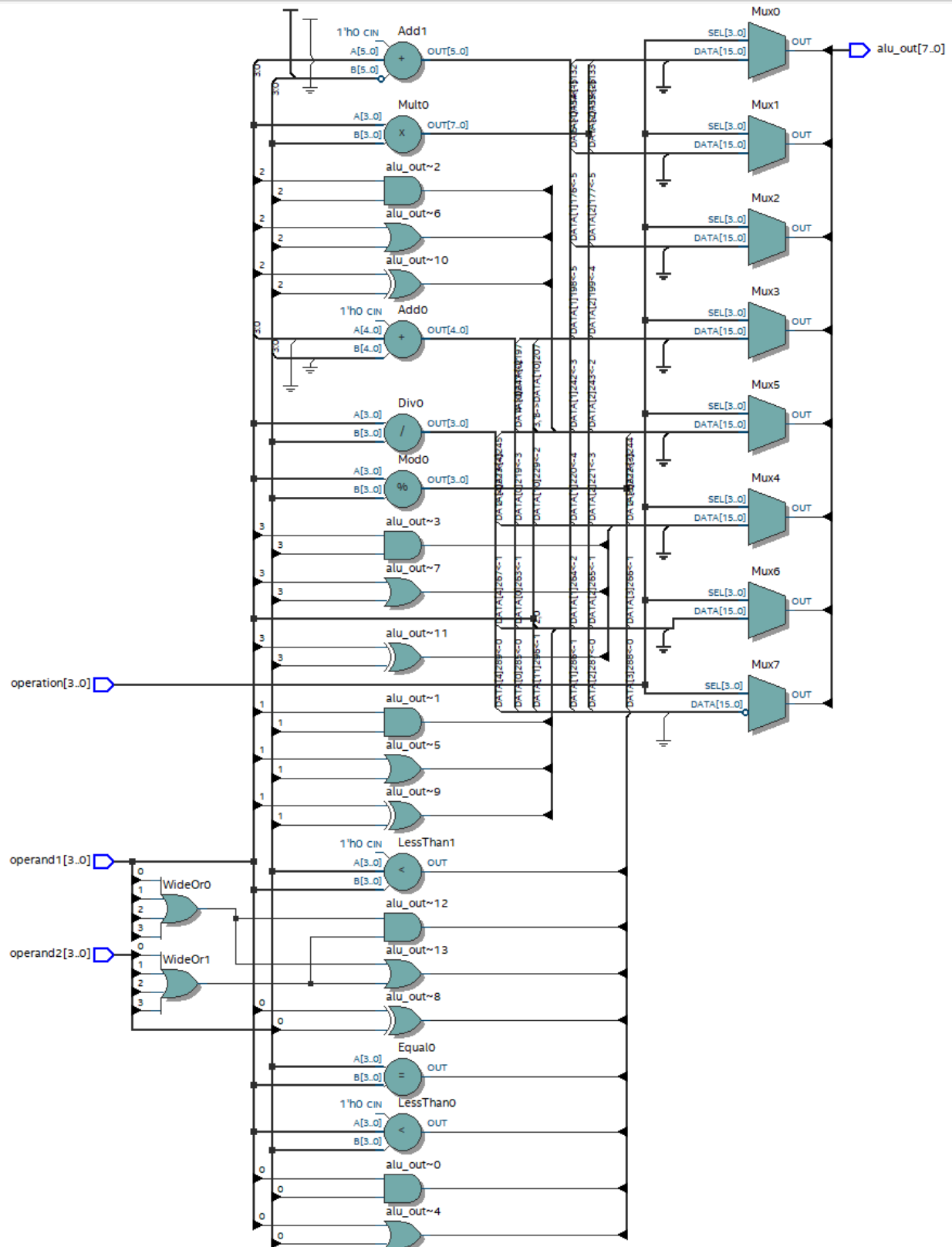
- 332068** No clocks defined in design.
- 332154** The derive_clock_uncertainty command did not apply clock uncertainty to any clock-to-clock transfers.
- 332102** Design is not fully constrained for setup requirements
- 332102** Design is not fully constrained for hold requirements
- Quartus Prime Timing Analyzer was successful. 0 errors, 6 warnings
- Running Quartus Prime EDA Netlist Writer
- Command: `quartus_eda --read_settings_files=off --write_settings_files=off alu -c alu`
- 18236** Number of processors has not been specified which may cause overloading on shared machines. Set the global assignment `NUM_PARALLEL_PROCESSORS` in the `quartus.eda` file.
- 204019** Generated file `alu.svo` in folder `"C:/Users/Ryo Andrew Onozuka/Documents/GitHub/notes/ucsd/ece111/HW/Homework2/Lab2/alu_top/simulation"`
- Quartus Prime EDA Netlist Writer was successful. 0 errors, 1 warning
- 293000** Quartus Prime Full Compilation was successful. 0 errors, 19 warnings

alu.sv Resource Usage Summary

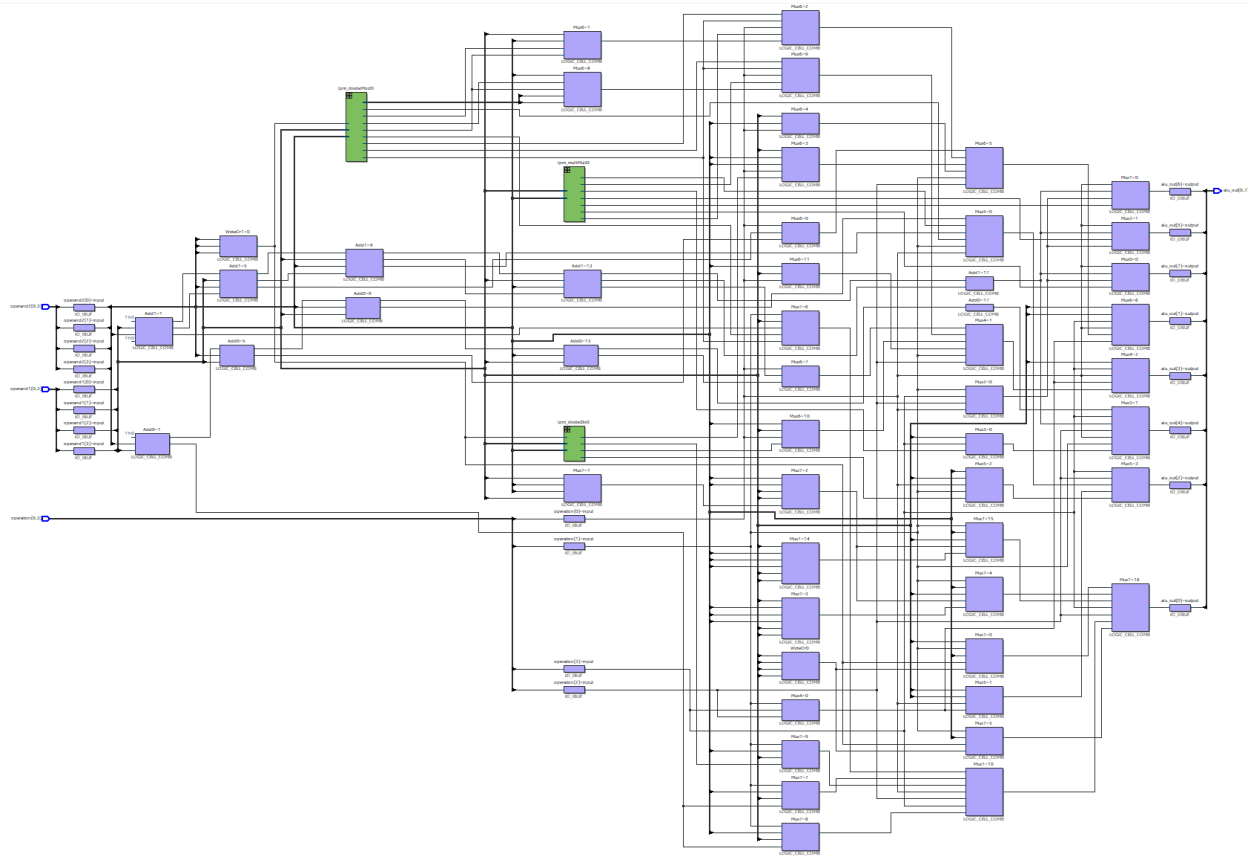
ucsd > ece111 > HW > Homework2 > Lab2 > alu_top > alu-Resource Usage Summary.rpt

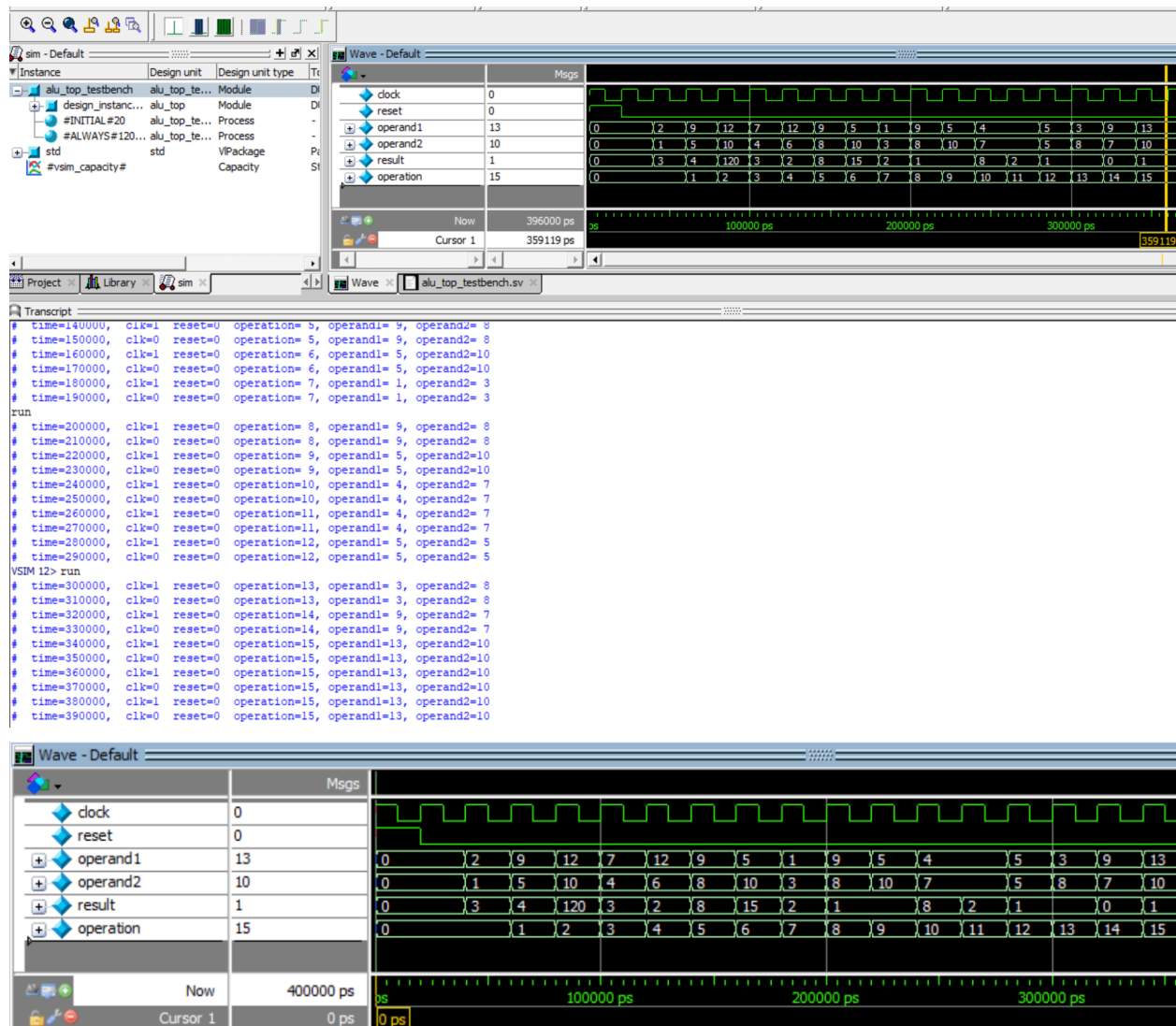
34	+-----+		
35	; Analysis & Synthesis Resource Usage Summary		;
36	+-----+		
37	; Resource	; Usage	;
38	+-----+		
39	; Estimated ALUTs Used	; 113	;
40	; -- Combinational ALUTs	; 113	;
41	; -- Memory ALUTs	; 0	;
42	; -- LUT_REGS	; 0	;
43	; Dedicated logic registers	; 0	;
44	;	;	;
45	; Estimated ALUTs Unavailable	; 9	;
46	; -- Due to unpartnered combinational logic	; 9	;
47	; -- Due to Memory ALUTs	; 0	;
48	;	;	;
49	; Total combinational functions	; 113	;
50	; Combinational ALUT usage by number of inputs	;	;
51	; -- 7 input functions	; 3	;
52	; -- 6 input functions	; 6	;
53	; -- 5 input functions	; 21	;
54	; -- 4 input functions	; 31	;
55	; -- <=3 input functions	; 52	;
56	;	;	;
57	; Combinational ALUTs by mode	;	;
58	; -- normal mode	; 54	;
59	; -- extended LUT mode	; 3	;
60	; -- arithmetic mode	; 33	;
61	; -- shared arithmetic mode	; 23	;
62	;	;	;
63	; Estimated ALUT/register pairs used	; 122	;
64	;	;	;
65	; Total registers	; 0	;
66	; -- Dedicated logic registers	; 0	;
67	; -- I/O registers	; 0	;
68	; -- LUT_REGS	; 0	;
69	;	;	;
70	;	;	;
71	; I/O pins	; 20	;
72	;	;	;
73	; DSP block 18-bit elements	; 0	;
74	;	;	;
75	; Maximum fan-out node	; operand2[3]~input	;
76	; Maximum fan-out	; 31	;
77	; Total fan-out	; 440	;
78	; Average fan-out	; 2.88	;
79	+-----+		

alu.sv RTL viewer



alu.sv post mapping viewer



simulation waveform**simulation wavelength results explanation:**

The testbench for the 4-bit ALU initializes the clock, reset, operand1, operand2, and operation signals, with the clock switching every 10ns and holding the reset high so the ALU's output can be reset every 20ns. The purpose of the testbench is to check if all of the outlined 16 operations are implemented correctly. The testbench sequentially applies different values to operand1, operand2, and the operation signal every 20ns, testing all 16 ALU operations (addition, subtraction, multiplication, etc.). A \$monitor statement continuously prints the values of the clock, reset, operation, operands, and the resulting output, allowing us to observe how the ALU responds to each operation. This is why the operations go from 0 to 15 (16 total) and the results are the outcomes of each operation given the 2 numbers. For the results to be displayed correctly, I needed to make sure the wave displays were on leaf and the radix on unsigned.

up_down_counter.sv

```

ucsd > ece111 > HW > Homework2 > Lab2 > up_down_counter > up_down_counter.sv
1 // 4-bit up and down counter RTL code
2 module up_down_counter // Module start declaration
3 // Parameter declaration, count signal width set to '4'
4 #(parameter WIDTH=4)
5 (
6     input logic clk,
7     input logic clear,
8     input logic select,
9     output logic[WIDTH-1:0] count_value
10 );
11
12 // Local variable declaration
13 logic[WIDTH-1:0] up_count_value, down_count_value;
14
15 // Instantiate up counter
16 up_counter #(WIDTH(WIDTH)) up_counter_inst (
17     .clk(clk),
18     .clear(clear),
19     .count(up_count_value)
20 );
21
22 // Instantiate down counter
23 down_counter #(WIDTH(WIDTH)) down_counter_inst (
24     .clk(clk),
25     .clear(clear),
26     .count(down_count_value)
27 );
28
29 // Instantiate 2-to-1 multiplexer
30 mux_2x1 #(WIDTH(WIDTH)) mux_inst (
31     .in0(up_count_value), // Input from up counter
32     .in1(down_count_value), // Input from down counter
33     .sel(select), // Select signal to choose between up or down counter
34     .out(count_value) // Output selected count value
35 );
36
37 endmodule: up_down_counter // Module end declaration

```

The screenshot displays the Quartus Prime IDE interface. The central editor shows the RTL code for the `up_down_counter` module. The left sidebar contains the Project Navigator and a list of tasks, including Compile Design, Analysis & Synthesis, Fitter (Place & Route), Assembler (Generate program), Timing Analysis, and EDA Netlist Writer. The bottom status bar shows a message log with the following entries:

- 332140 No Recovery paths to report
- 332140 No Removal paths to report
- 332148 Timing requirements not met
- 332146 worst-case minimum pulse width slack is -2.846
- 21076 High junction temperature operating condition is not set. Assuming a default value of '100'.
- 21076 Low junction temperature operating condition is not set. Assuming a default value of '-40'.
- 332123 Deriving Clock Uncertainty. Please refer to report_sdc in the Timing Analyzer to see clock uncertainties.
- 332102 Design is not fully constrained for setup requirements
- 332102 Design is not fully constrained for hold requirements
- Quartus Prime Timing Analyzer was successful. 0 errors, 5 warnings
- Running Quartus Prime EDA Netlist Writer
- Command: quartus_eda --read_settings_files=off --write_settings_files=off up_down_counter -c up_down_counter
- 18236 Number of processors has not been specified which may cause overloading on shared machines. Set the global assignment NUM_PA
- 204019 Generated file up_down_counter.svo in folder "C:/Users/Ryo Andrew Onozuka/Documents/GitHub/notes/ucsd/ece111/HW/Homework2/Lab
- Quartus Prime EDA Netlist Writer was successful. 0 errors, 1 warning
- 293000 Quartus Prime Full Compilation was successful. 0 errors, 18 warnings

up_down_counter.sv Resource Usage Summary

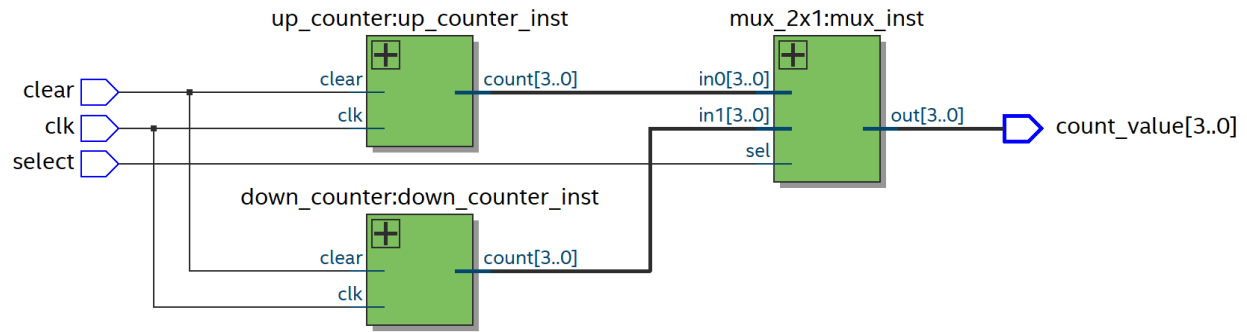
ucsd > ece111 > HW > Homework2 > Lab2 > up_down_counter > up_down_counter-Resource Usage Summary.rpt

36	+-----+-----+		
37	; Resource	; Usage	;
38	+-----+-----+		
39	; Estimated ALUTs Used	; 10	;
40	; -- Combinational ALUTs	; 10	;
41	; -- Memory ALUTs	; 0	;
42	; -- LUT_REGS	; 0	;
43	; Dedicated logic registers	; 7	;
44	;	;	;
45	; Estimated ALUTs Unavailable	; 0	;
46	; -- Due to unpartnered combinational logic	; 0	;
47	; -- Due to Memory ALUTs	; 0	;
48	;	;	;
49	; Total combinational functions	; 10	;
50	; Combinational ALUT usage by number of inputs	;	;
51	; -- 7 input functions	; 0	;
52	; -- 6 input functions	; 0	;
53	; -- 5 input functions	; 0	;
54	; -- 4 input functions	; 2	;
55	; -- <=3 input functions	; 8	;
56	;	;	;
57	; Combinational ALUTs by mode	;	;
58	; -- normal mode	; 10	;
59	; -- extended LUT mode	; 0	;
60	; -- arithmetic mode	; 0	;
61	; -- shared arithmetic mode	; 0	;
62	;	;	;
63	; Estimated ALUT/register pairs used	; 10	;
64	;	;	;
65	; Total registers	; 7	;
66	; -- Dedicated logic registers	; 7	;
67	; -- I/O registers	; 0	;
68	; -- LUT_REGS	; 0	;
69	;	;	;
70	;	;	;
71	; I/O pins	; 7	;
72	;	;	;
73	; DSP block 18-bit elements	; 0	;
74	;	;	;
75	; Maximum fan-out node	; down_counter:down_counter_inst cnt_value[0]	;
76	; Maximum fan-out	; 8	;
77	; Total fan-out	; 60	;
78	; Average fan-out	; 1.94	;
79	+-----+-----+		

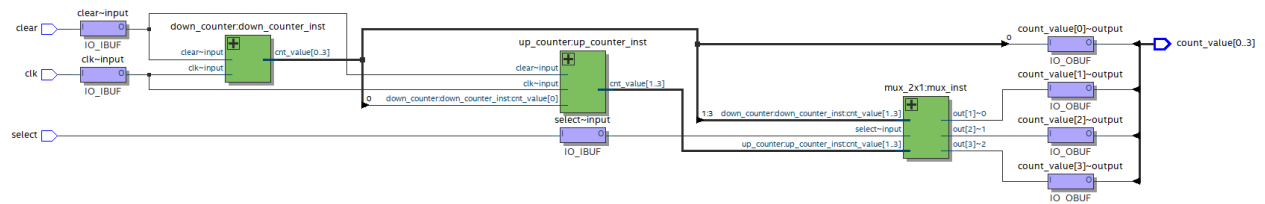
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up_down_counter.sv RTL viewer



up_down_counter.sv post mapping viewer



up_counter.v

```

ucsd > ece111 > HW > Homework2 > Lab2 > up_down_counter > up_counter.v
1 // 4-bit counter RTL behavioral code
2 module up_counter // Module start declaration
3 // Parameter declaration, count signal width set to '4'
4 #(parameter WIDTH=4)
5 (
6     input logic clk,
7     input logic clear,
8     output logic[WIDTH-1:0] count
9 );
10
11 // Local variable declaration
12 logic[WIDTH-1:0] cnt_value;
13
14 // always procedural block describing up counter behavior
15 always @(posedge clk or posedge clear)
16 begin
17     if (clear == 1)
18         cnt_value = 0;
19     else
20         cnt_value = cnt_value + 1;
21 end
22
23 // Counter value assigned to output port count
24 assign count = cnt_value;
25 endmodule: up_counter // Module end declaration

```

The screenshot displays the Quartus Prime IDE interface. The top pane shows the source code for `up_counter.v`. The middle pane shows the compilation report, which includes a list of tasks and a detailed message window.

Tasks:

- Compile Design
- Analysis & Synthesis
- Fitter (Place & Route)
- Assembler (Generate program)
- Timing Analysis
- EDA Netlist Writer

Message Window:

- 332140 No Recovery paths to report
- 332140 No Removal paths to report
- 332148 Timing requirements not met
- 332146 Worst-case minimum pulse width slack is -2.846
- 21076 High junction temperature operating condition is not set. Assuming a default value of '100'.
- 21076 Low junction temperature operating condition is not set. Assuming a default value of '-40'.
- 332123 Deriving Clock Uncertainty. Please refer to report_sdc in the Timing Analyzer to see clock uncertainties.
- 332102 Design is not fully constrained for setup requirements
- 332102 Design is not fully constrained for hold requirements
- Quartus Prime Timing Analyzer was successful. 0 errors, 5 warnings
- Running Quartus Prime EDA Netlist Writer
- Command: quartus_eda --read_settings_files=off --write_settings_files=off up_counter -c up_counter
- 18236 Number of processors has not been specified which may cause overloading on shared machines. Set the global assignment NUM_PA...
- 204019 Generated file up_counter.svo in folder "C:/Users/Ryo Andrew Onozuka/Documents/GitHub/notes/ucsd/ece111/HW/Homework2/Lab2/up_...
- Quartus Prime EDA Netlist Writer was successful. 0 errors, 1 warning
- 293000 Quartus Prime Full Compilation was successful. 0 errors, 14 warnings

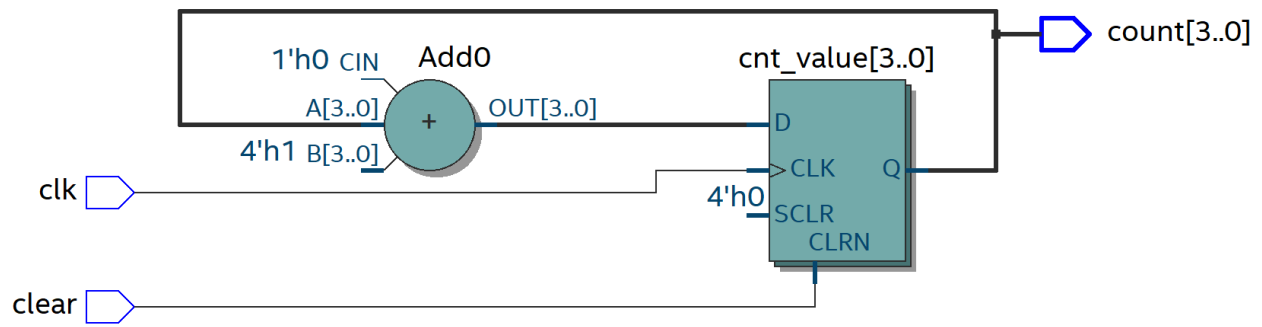
up_counter.sv Resource Usage Summary

ucsd > ece111 > HW > Homework2 > Lab2 > up_down_counter > up_counter-Resource Usage Summary.rpt			
36	+-----+-----+		
37	; Resource	; Usage	;
38	+-----+-----+		
39	; Estimated ALUTs Used	; 4	;
40	; -- Combinational ALUTs	; 4	;
41	; -- Memory ALUTs	; 0	;
42	; -- LUT_REGS	; 0	;
43	; Dedicated logic registers	; 4	;
44	;	;	;
45	; Estimated ALUTs Unavailable	; 0	;
46	; -- Due to unpartnered combinational logic	; 0	;
47	; -- Due to Memory ALUTs	; 0	;
48	;	;	;
49	; Total combinational functions	; 4	;
50	; Combinational ALUT usage by number of inputs	;	;
51	; -- 7 input functions	; 0	;
52	; -- 6 input functions	; 0	;
53	; -- 5 input functions	; 0	;
54	; -- 4 input functions	; 1	;
55	; -- <=3 input functions	; 3	;
56	;	;	;
57	; Combinational ALUTs by mode	;	;
58	; -- normal mode	; 4	;
59	; -- extended LUT mode	; 0	;
60	; -- arithmetic mode	; 0	;
61	; -- shared arithmetic mode	; 0	;
62	;	;	;
63	; Estimated ALUT/register pairs used	; 4	;
64	;	;	;
65	; Total registers	; 4	;
66	; -- Dedicated logic registers	; 4	;
67	; -- I/O registers	; 0	;
68	; -- LUT_REGS	; 0	;
69	;	;	;
70	;	;	;
71	; I/O pins	; 6	;
72	;	;	;
73	; DSP block 18-bit elements	; 0	;
74	;	;	;
75	; Maximum fan-out node	; cnt_value[0]	;
76	; Maximum fan-out	; 5	;
77	; Total fan-out	; 32	;
78	; Average fan-out	; 1.60	;
79	+-----+-----+		

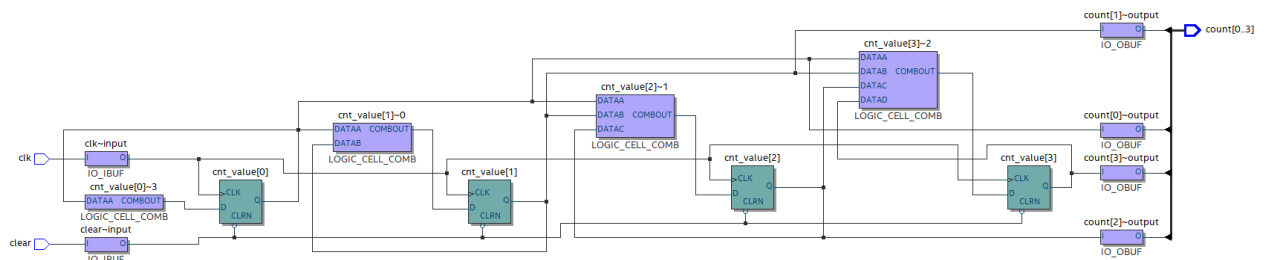
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up_counter.sv RTL viewer



up_counter.sv post mapping viewer



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ECE 111 HW2 | 10/16/2024

down_counter.sv

```
ucsd > ece111 > HW > Homework2 > Lab2 > up_down_counter > down_counter.sv
1 // 4-bit counter RTL code
2 module down_counter // Module start declaration
3 // Parameter declaration, count signal width set to '4'
4 #(parameter WIDTH=4)
5 (
6     input logic clk,
7     input logic clear,
8     output logic[WIDTH-1:0] count
9 );
10
11 // Local variable declaration
12 logic[WIDTH-1:0] cnt_value;
13
14 // always procedural block describing down counter behavior
15 always @(posedge clk or posedge clear)
16 begin
17     if (clear == 1)
18         cnt_value = 0;
19     else
20         cnt_value = cnt_value - 1;
21 end
22
23 // Counter value assigned to output port count
24 assign count = cnt_value;
25 endmodule: down_counter // Module end declaration
```

The screenshot shows the Quartus Prime IDE interface. The Project Navigator on the left displays the hierarchy of the project, including the 'down_counter' module. The main window shows the source code of the 'down_counter.sv' file, which is a 4-bit counter module. The IP Catalog on the right shows the installed IP blocks, including 'Basic Functions', 'DSP', 'Interface Protocol', 'Memory Interfaces', 'Processors and Peripherals', and 'University Program'. The bottom status bar shows the compilation progress and messages, including the command 'quartus_eda --read_settings_files=off --write_settings_files=off down_counter -c down_counter' and the message '18236 Number of processors has not been specified which may cause overloading on shared machines. Set the global assignment NUM_PA...'. The compilation was successful with 0 errors and 14 warnings.

down_counter.sv Resource Usage Summary

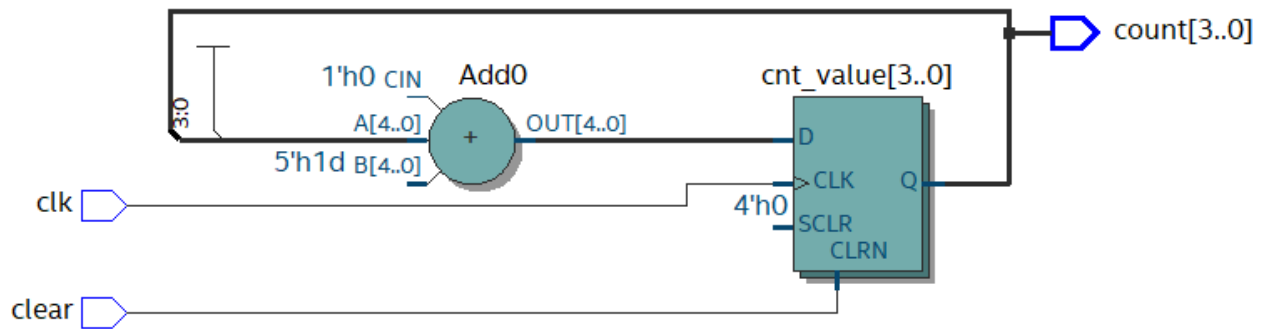
ucsd > ece111 > HW > Homework2 > Lab2 > up_down_counter > down_counter-Resource Usage Summary.rpt

```

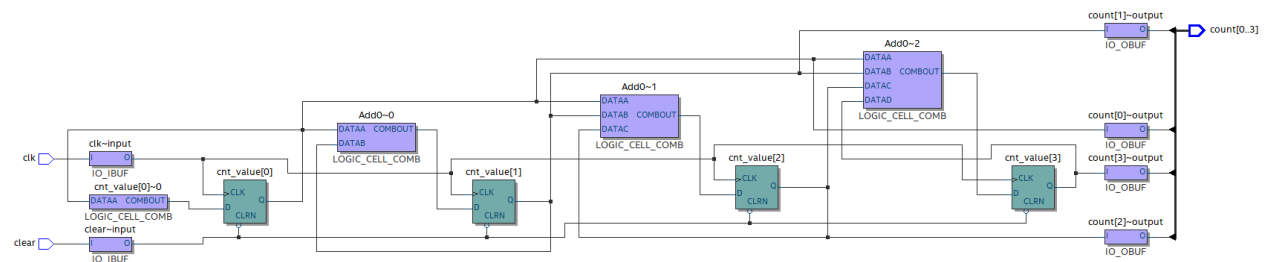
34  +-----+
35  ; Analysis & Synthesis Resource Usage Summary ;
36  +-----+
37  ; Resource ; Usage ;
38  +-----+
39  ; Estimated ALUTs Used ; 4 ;
40  ; -- Combinational ALUTs ; 4 ;
41  ; -- Memory ALUTs ; 0 ;
42  ; -- LUT_REGS ; 0 ;
43  ; Dedicated logic registers ; 4 ;
44  ; ; ;
45  ; Estimated ALUTs Unavailable ; 0 ;
46  ; -- Due to unpartnered combinational logic ; 0 ;
47  ; -- Due to Memory ALUTs ; 0 ;
48  ; ; ;
49  ; Total combinational functions ; 4 ;
50  ; Combinational ALUT usage by number of inputs ; ;
51  ; -- 7 input functions ; 0 ;
52  ; -- 6 input functions ; 0 ;
53  ; -- 5 input functions ; 0 ;
54  ; -- 4 input functions ; 1 ;
55  ; -- <=3 input functions ; 3 ;
56  ; ; ;
57  ; Combinational ALUTs by mode ; ;
58  ; -- normal mode ; 4 ;
59  ; -- extended LUT mode ; 0 ;
60  ; -- arithmetic mode ; 0 ;
61  ; -- shared arithmetic mode ; 0 ;
62  ; ; ;
63  ; Estimated ALUT/register pairs used ; 4 ;
64  ; ; ;
65  ; Total registers ; 4 ;
66  ; -- Dedicated logic registers ; 4 ;
67  ; -- I/O registers ; 0 ;
68  ; -- LUT_REGS ; 0 ;
69  ; ; ;
70  ; ; ;
71  ; I/O pins ; 6 ;
72  ; ; ;
73  ; DSP block 18-bit elements ; 0 ;
74  ; ; ;
75  ; Maximum fan-out node ; cnt_value[0] ;
76  ; Maximum fan-out ; 5 ;
77  ; Total fan-out ; 32 ;
78  ; Average fan-out ; 1.60 ;
79  +-----+

```


down_counter.sv RTL viewer



down_counter.sv post mapping viewer



mux_2x1.sv

```

ucsd > ece111 > HW > Homework2 > Lab2 > up_down_counter > mux_2x1.sv
1  // 2to1 Multiplexor RTL code
2  module mux_2x1 #(parameter WIDTH=4)
3  (
4      input logic [WIDTH-1:0] in0, // Updated in0 width to 4
5      input logic [WIDTH-1:0] in1, // Updated in1 width to 4
6      input logic sel,
7      output logic [WIDTH-1:0] out // Updated out width to 4
8  );
9
10 // always procedural block describing 2to1 Multiplexor behavior
11 always @(sel or in0 or in1)
12 begin
13     if(sel == 0)
14         out = in0;
15     else
16         out = in1;
17 end
18 endmodule

```

The screenshot shows the Quartus Prime IDE interface. The main window displays the mux_2x1.sv file with the following code:

```

1 // 2to1 Multiplexor RTL code
2 module mux_2x1 #(parameter WIDTH=4)
3 (
4     input logic [WIDTH-1:0] in0, // Updated in0 width to 4
5     input logic [WIDTH-1:0] in1, // Updated in1 width to 4
6     input logic sel,
7     output logic [WIDTH-1:0] out // Updated out width to 4
8 );
9
10 // always procedural block describing 2to1 Multiplexor behavior
11 always @(sel or in0 or in1)
12 begin
13     if(sel == 0)
14         out = in0;
15     else
16         out = in1;
17 end
18 endmodule

```

The left sidebar shows the Project Navigator with the hierarchy: Arria II GX: AUTO > mux_2x1. The bottom pane shows the Compilation Report - mux_2x1, which includes the following messages:

- 332140 No Minimum Pulse Width paths to report
- 21076 High junction temperature operating condition is not set. Assuming a default value of '100'.
- 21076 Low junction temperature operating condition is not set. Assuming a default value of '-40'.
- 332142 No user constrained base clocks found in the design. Calling "derive_clocks -period 1.0"
- 332096 The command derive_clocks did not find any clocks to derive. No clocks were created or changed.
- 332068 No clocks defined in design.
- 332154 The derive_clock_uncertainty command did not apply clock uncertainty to any clock-to-clock transfers.
- 332102 Design is not fully constrained for setup requirements
- 332102 Design is not fully constrained for hold requirements
- Quartus Prime Timing Analyzer was successful. 0 errors, 6 warnings
- Running Quartus Prime EDA Netlist Writer
- Command: quartus_eda --read_settings_files=off --write_settings_files=off mux_2x1 -c mux_2x1
- 18236 Number of processors has not been specified which may cause overloading on shared machines. Set the global assignment NUM_PA
- 204019 Generated file mux_2x1.svo in folder "C:/Users/Ryo Andrew Onozuka/Documents/GitHub/notes/ucsd/ece111/HW/Homework2/Lab2/up_down
- Quartus Prime EDA Netlist Writer was successful. 0 errors, 1 warning
- 293000 Quartus Prime Full Compilation was successful. 0 errors, 15 warnings

mux_2x1.sv Resource Usage Summary

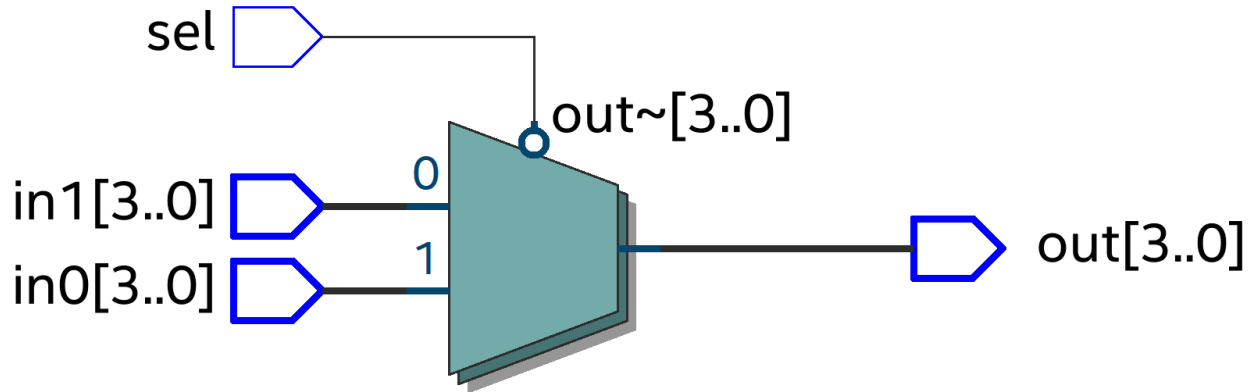
ucsd > ece111 > HW > Homework2 > Lab2 > up_down_counter > mux_2x1-Resource Usage Summary.rpt

```

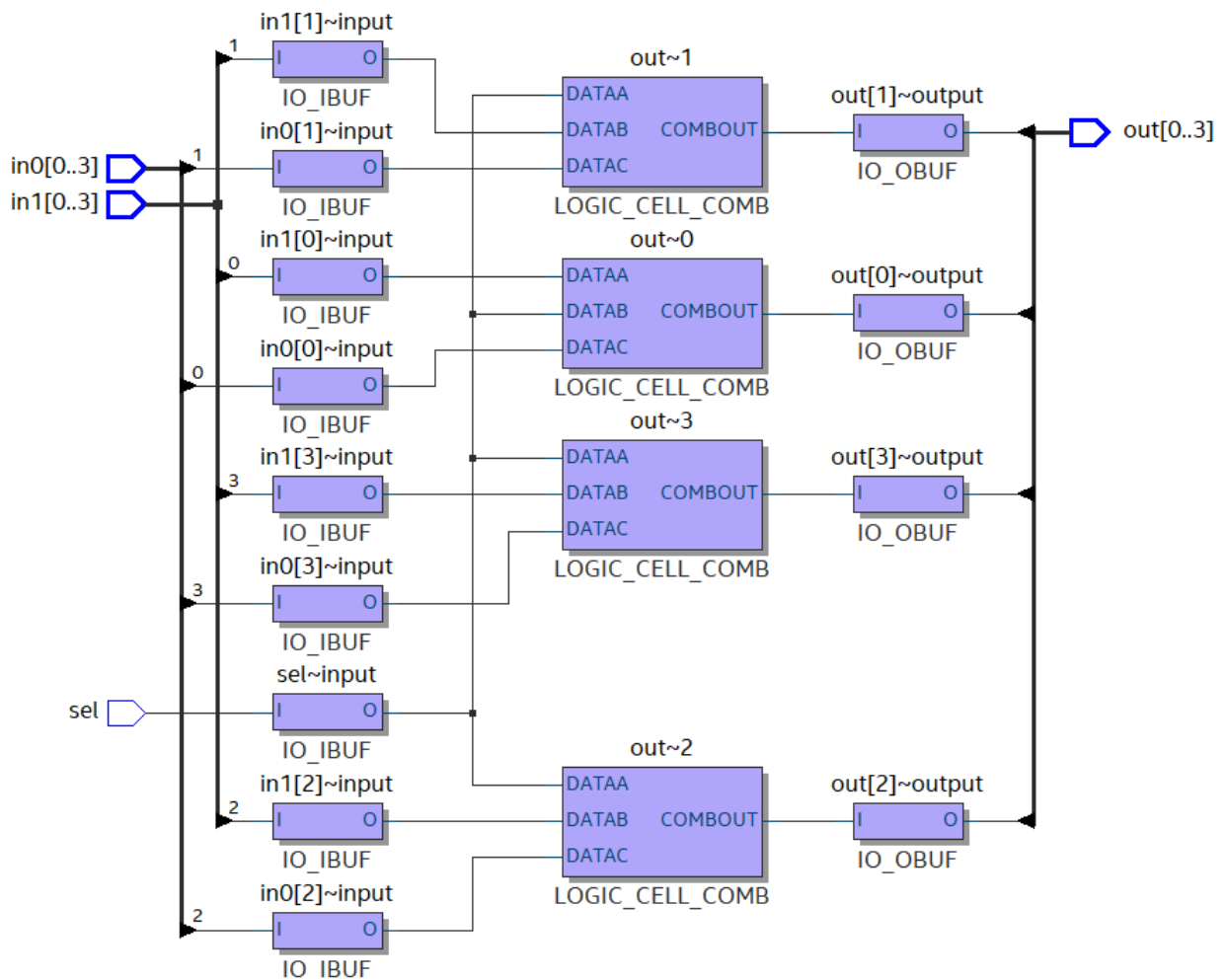
34 +-----+
35 ; Analysis & Synthesis Resource Usage Summary ;
36 +-----+
37 ; Resource ; Usage ;
38 +-----+
39 ; Estimated ALUTs Used ; 4 ;
40 ; -- Combinational ALUTs ; 4 ;
41 ; -- Memory ALUTs ; 0 ;
42 ; -- LUT_REGS ; 0 ;
43 ; Dedicated logic registers ; 0 ;
44 ; ; ;
45 ; Estimated ALUTs Unavailable ; 0 ;
46 ; -- Due to unpartnered combinational logic ; 0 ;
47 ; -- Due to Memory ALUTs ; 0 ;
48 ; ; ;
49 ; Total combinational functions ; 4 ;
50 ; Combinational ALUT usage by number of inputs ; ;
51 ; -- 7 input functions ; 0 ;
52 ; -- 6 input functions ; 0 ;
53 ; -- 5 input functions ; 0 ;
54 ; -- 4 input functions ; 0 ;
55 ; -- <=3 input functions ; 4 ;
56 ; ; ;
57 ; Combinational ALUTs by mode ; ;
58 ; -- normal mode ; 4 ;
59 ; -- extended LUT mode ; 0 ;
60 ; -- arithmetic mode ; 0 ;
61 ; -- shared arithmetic mode ; 0 ;
62 ; ; ;
63 ; Estimated ALUT/register pairs used ; 4 ;
64 ; ; ;
65 ; Total registers ; 0 ;
66 ; -- Dedicated logic registers ; 0 ;
67 ; -- I/O registers ; 0 ;
68 ; -- LUT_REGS ; 0 ;
69 ; ; ;
70 ; ; ;
71 ; I/O pins ; 13 ;
72 ; ; ;
73 ; DSP block 18-bit elements ; 0 ;
74 ; ; ;
75 ; Maximum fan-out node ; sel~input ;
76 ; Maximum fan-out ; 4 ;
77 ; Total fan-out ; 29 ;
78 ; Average fan-out ; 0.97 ;
79 +-----+

```

mux_2x1.sv RTL viewer



mux_2x1.sv post mapping viewer



simulation waveform