Name PID

UNIVERSITY OF CALIFORNIA, SAN DIEGO

Electrical and Computer Engineering Department

ECE 65 – Spring 2023

Components and Circuits lab

Midterm Exam#2 solutions

Closed books, one one-sided cheat sheet, and calculators are allowed

Electronic devices are not allowed.

Please put all answers in the provided sheets.

Be sure to write your name and PID.

Please do not begin until told.

Show your work.

Good luck.

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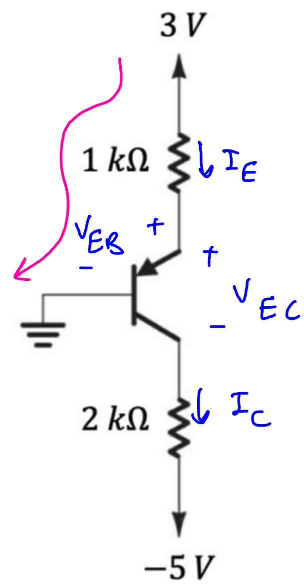
Problem 1.

In the below circuit, find all the BJT currents and node voltages.

Assume $\beta = 100, V_{D0} = 0.7\ V, V_{sat} = 0.2V$.



Show your work.

Assume BJT is off: $V_{EB} < V_{D_0}$, $I_B = 0$, $I_E = 0$

KVL: $3 = 1k\Omega \times I_E + V_{EB}$

$I_E = 0 \rightarrow V_{EB} = 3V > V_{D_0} \rightarrow$ BJT is not off

$\Rightarrow V_{EB} = V_{D_0}$

$3 = 1k\Omega \times I_E + 0.7 \rightarrow I_E = 2.3\ mA$

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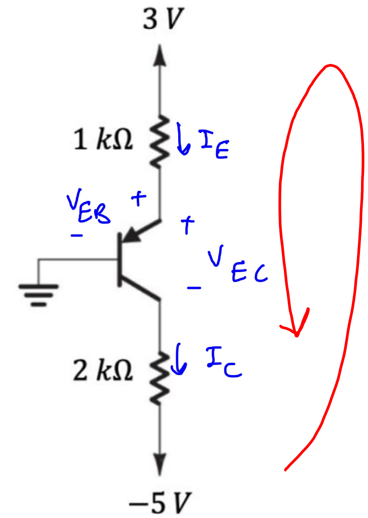
Assume active mode:

$I_C = \beta I_B$, $V_{EC} \geq V_{D_0}$



$I_E = I_C + I_B = I_C + \frac{1}{\beta} I_C = \frac{101}{100} I_C$

$I_E = 2.3 \text{ mA} \longrightarrow I_C \simeq 2.28 \text{ mA}$

$I_B = \frac{I_C}{\beta} = 0.0228 \text{ mA}$

KVL:

$3V = 1k\Omega \times I_E + V_{EC} + 2k\Omega \times I_C - 5$

$\rightarrow V_{EC} \simeq 1.14 \text{ V} > V_{D_0} \implies$ Assumption was correct.

$V_B = 0 \text{ V}$ $V_{EB} = V_E - V_B = 0.7V \implies V_E = 0.7V$

$V_{EC} = V_E - V_C = 1.14V \rightarrow V_C = -0.44V$

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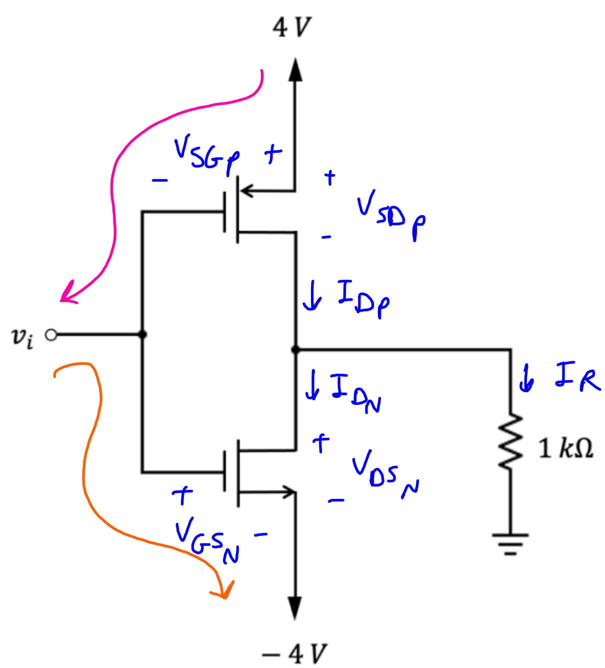
Problem 2.

In the following circuit, find the drain current and the drain node voltage for each MOSFET when $V_i = 3.5\ V$.

Assume MOSFETs have $|V_t| = 1\ V$, $\mu_n C_{ox} = \mu_p C_{ox} = 250\ \mu A/V^2$, $\lambda = 0$, $L = 1\ \mu m$, and $W = 2\ \mu m$.



Show your work.

KVL : $4 = V_{SG_p} + V_i = V_{SG_p} + 3.5 \rightarrow V_{SG_p} = 0.5 < |V_{tp}|$

PMOS is off

$I_{D_p} = 0$

KVL : $V_i = V_{GS_N} - 4 \Rightarrow V_{GS_N} = 3.5 + 4 = 7.5\ V > V_{t_n}$

NMOS is ON

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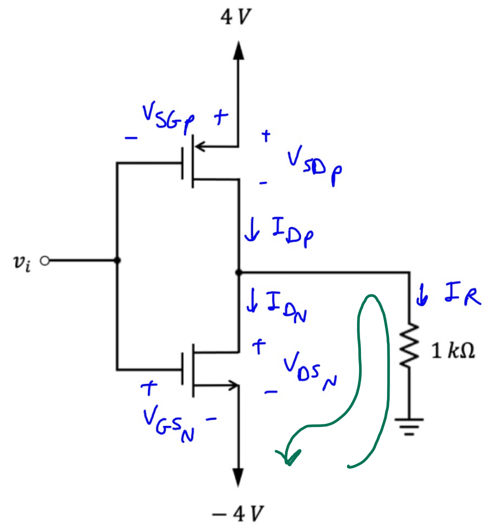
KCL: $I_{D_P} = I_{D_N} + I_R$

$I_{D_P} = 0 \longrightarrow I_R = -I_{D_N}$



Assume NMOS is in saturation:

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} V_{ov}^2$$

$$= \frac{1}{2} \times 0.25 \frac{mA}{V^2} \times \frac{2\ \mu m}{1\ \mu m} (7.5 - 1)^2 = 10.56\ mA$$

KVL:

$$1k\Omega \times (-I_R) + V_{DS_N} - 4 = 0$$

$$1k\Omega \times I_{D_N} + V_{DS_N} - 4 = 0 \longrightarrow V_{DS_N} = -6.56\ V < V_{ov_N}$$

NMOS is not in saturation.

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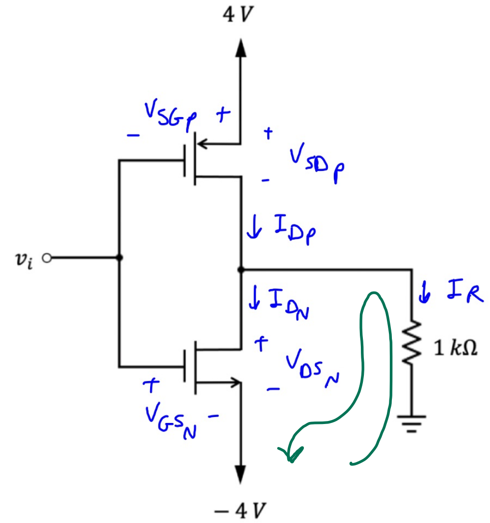

Assume NMOS is in triode:

$$I_{D_N} = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} \left(2 V_{ov_N} V_{DS_N} - V_{DS_N}^2 \right)$$

$$I_{D_N} = 0.25 \ mA/V^2 \left(2 \times 6.5 \times V_{DS_N} - V_{DS_N}^2 \right)$$

KVL:

$$1k\Omega \times I_{D_N} + V_{DS_N} - 4 = 0 \quad \longrightarrow \quad V_{DS_N} = 4 - 1k\Omega \times I_{D_N}(mA)$$

$$I_{D_N}(mA) = 0.25 \left(\frac{mA}{V^2}\right) \left(13 \left(4 - I_{D_N}(mA)\right) - \left(4 - I_{D_N}\right)^2 \right)$$

$$\Rightarrow I_{D_N} = \begin{cases} 3 \ mA \ \checkmark \\ -12 \ mA \ \times \ \text{not possible} \end{cases}$$

$I_{D_N} = 3 mA \Rightarrow V_{DS_N} = 1 \ V < V_{ov_N} \Rightarrow$ Assumption was correct.

PMOS is in cut-off, $I_{D_P} = 0$

NMOS is in triode, $I_{D_N} = 3mA$

$$V_{D_N} = V_{D_P} = -I_{D_N} \times 1k\Omega = -3 \ V$$