Name: PID:

UNIVERSITY OF CALIFORNIA, SAN DIEGO

Electrical and Computer Engineering Department

ECE 65 – Fall 2019

Components and Circuits lab

Final Exam

Closed books, twenty-five double-sided cheat sheets, and calculators are allowed

Electronic devices are not allowed.

Please put all answers in the answer sheets.

Write your name and PID on all pages.

Please do not begin until told. Show your work. Good luck.

All electronic devices including cell phones must be turned off and stored away in a backpack or a purse. Anyone caught with such a device on their person during the exam will be charged with academic dishonesty.

You can use the back of every page as a **scratch** paper.

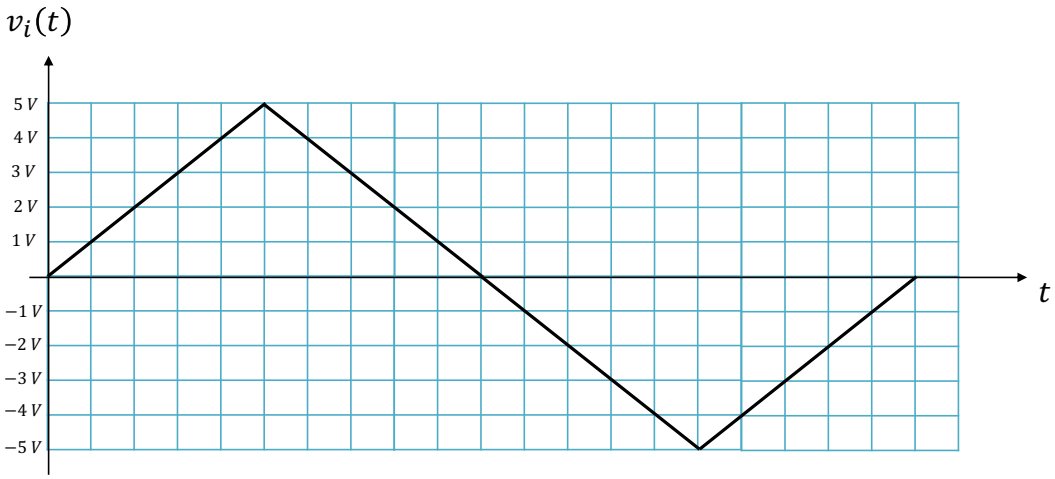
The main pages are numbered. If you remove the staple, you should order the pages and staple them before submitting your exam. **Do not remove or add any pages to your exam script.**

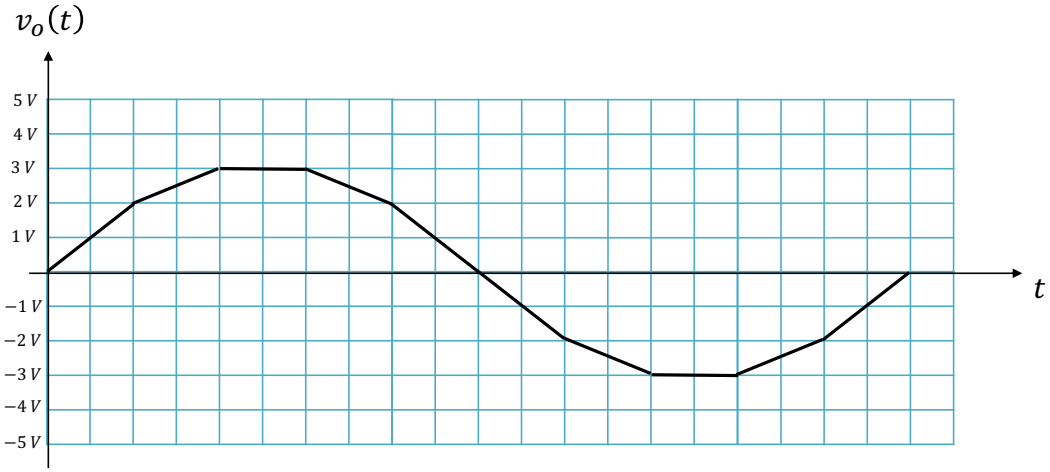
Name: PID:

Problem 1. (15 points)

a) Design a diode waveform shaping circuit that would produce the following output voltage waveform in response to the sketched input voltage waveform. You can use PN junction diodes with $V_{D0} = 0.7\ V$, DC voltage sources and resistors in your design. Make sure to include the input signal source and label the output terminals.

b) Parametrically solve your designed circuit. That means write the possible cases of the operation of the diode(s) in your designed circuit, and for each case, include the calculation of finding v_o and the range of v_i. **Write complete equations and show your work.**





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Problem 1.

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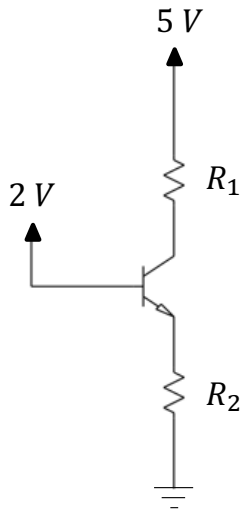
Problem 2. (6 points)

Design this BJT circuit to establish a collector current of $0.5\ mA$ and a reverse-bias voltage of 1V on the collector-base junction. Assume $\beta = 100, V_{D0} = 0.7V,\ V_{sat} = 0.2\ V$.

Show your work.



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Problem 2.

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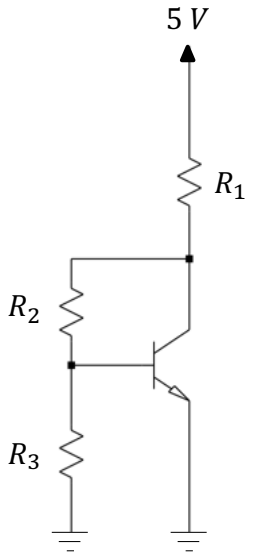
Problem 3. (8 points)

Design the following circuit to establish $I_c = 2\ mA$, $I_{R_3} = 0.02\ mA$, and $V_c = 2.5\ V$.

Assume $\beta = 100, V_{D0} = 0.7V,\ \ V_{sat} = 0.2\ V$.

Show your work.



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Problem 3.

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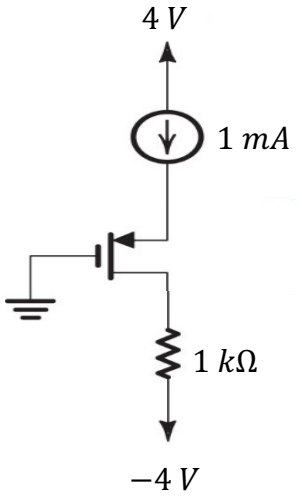
Problem 4. (8 points)

In the following circuit the transistor has $|V_t| = 1\ V$, $\mu\ C_{ox}\frac{W}{L} = 2\ mA/V^2$, and $\lambda = 0$.

a) Find the node voltages at the source and drain.

b) Replace the current source with a resistor. Calculate the value of the resistor such that the current flowing through the resistor is equal to $1\ mA$.



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Problem 4.

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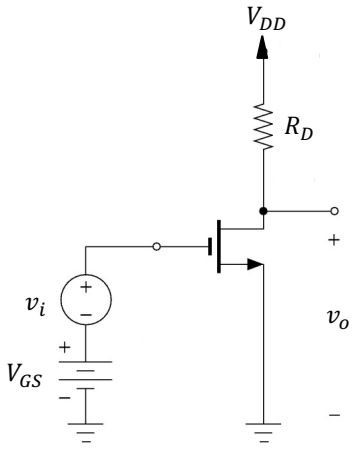
Problem 5. (8 points)

In the following circuit, $V_{DD} = 5\ V, V_{OV} = 0.5\ V, k_n = 1\ mA/V^2$, and $\lambda = 0$. Complete the table. Neglect the effect of v_i on V_{OV}.

Note: $\hat{v}_o$ represents the maximum symmetrical signal swing allowed at the drain and $\hat{v}_i$ is the maximum allowable amplitude of the input signal.

Show your work.



V_{DS}	A_v	$\hat{v}_o$	$\hat{v}_i$	I_D	R_D
$1\ V$					
$1.5\ V$					
$2\ V$					

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Problem 5.

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Problem 6. (15 points)

Answer the following questions for the below MOSFET amplifier circuit. Assume capacitors are short in the signal circuit. Use $V_A = 100\ V$, $k_n = 4\ mA/V^2$, $V_t = 1\ V$, and Ignore the early effect in the bias circuit.

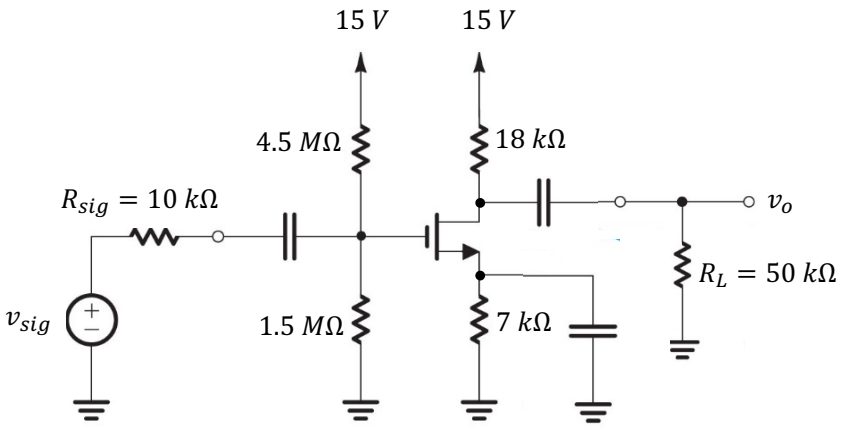
a) Find the Bias point of the amplifier circuit.

b) Find the small signal parameters of the amplifier.

c) Draw the small signal equivalent circuit.

d) Find the open loop voltage gain (A_{vo}), voltage gain (A_v), total circuit voltage gain (A), input resistance (R_i), and output resistance (R_o) of this circuit.

e) If v_{sig} is a sine wave with peak amplitude of 5 mV, sketch the instantaneous current and voltages $i_D(t)$, $v_G(t)$, $v_D(t)$, $v_L(t)$, and $v_S(t)$.



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Problem 6.

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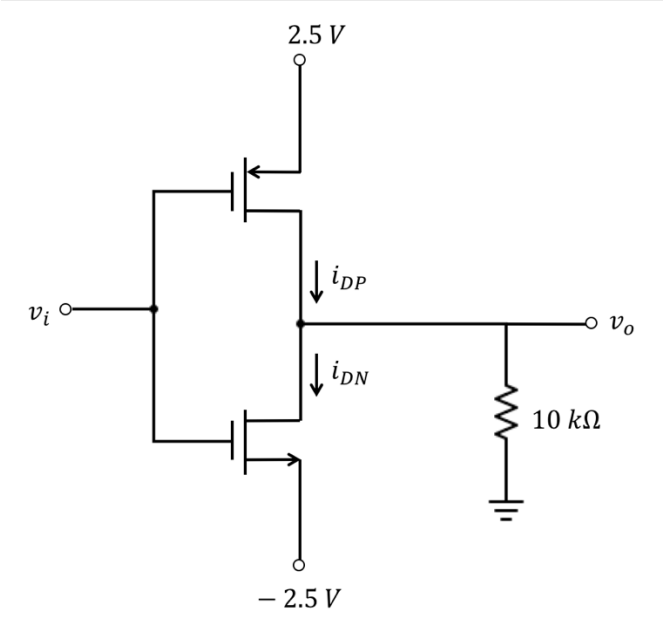
Problem 7. (6 points)

Find v_o, i_{DN} and i_{DP} in the following circuit for $v_i = 2.5\ V$. For the NMOS and PMOS, $\mu_n C_{ox}\left(\frac{W}{L}\right)_n = \mu_p C_{ox}\left(\frac{W}{L}\right)_p = 1\ mA/V^2$, $|V_{tn}| = |V_{tp}| = 1\ V$. Assume $\lambda = 0$ for both devices.



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Problem 7.

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