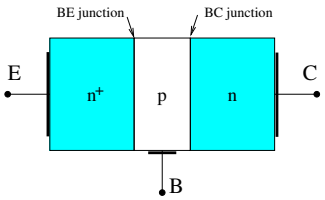
III. Introduction to Bipolar-Junction Transistors

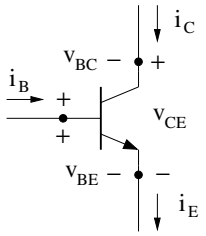
3.1 BJT iv characteristics

A bipolar junction transistor is formed by joining three sections of semiconductors with alternative different dopings. The middle section (base) is narrow and one of the other two regions (emitter) is heavily doped. The other region is called the collector.

Two variants of BJT are possible: NPN (base is made of p-type material) and PNP (base is made of n-type material). Let's first consider a NPN transistor. A simplified physical structure of a NON transistor is shown on the right.



A BJT has three terminals. Six parameters; i_C, i_B, i_E, v_{CE}, v_{BE}, and v_{BC}; define the state of the transistor. However, because a BJT has three terminals, KVL and KCL should hold for these terminals:

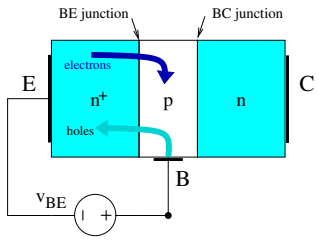


$$i_E = i_C + i_B \qquad\qquad v_{BC} = v_{BE} - v_{CE}$$

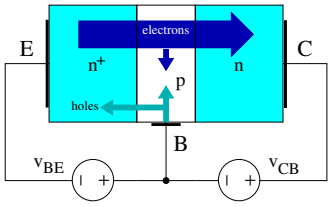
Thus, only four of these 6 parameters are independent. Two relationships among these four parameters (i_B, v_{BE}, i_C and v_{CE}) represent the "iv" characteristics of the BJT.

A BJT looks like 2 diodes placed back to back if we apply a voltage to only two of the three terminals, letting the third terminal float. We can use this feature to check if a transistor is working: use a multi-meter to ensure that both diodes are in working condition. (One should also check the resistance between C & E terminals and read a vary high resistance as one may have a burn through the base connecting collector and emitter.)

When the BE junction is forward biased, electrons from the emitter diffuse into the base and holes from the base into the emitter setting up the BE diode diffusion current. Because the emitter is heavily doped, a large number of electrons enter the base. If the base is thin enough, there would be a substantial number of electrons in the vicinity of the BC junction.



If a "negative" voltage is applied to the BC junction, the electrons from the emitter which had diffused to the vicinity of the BC junction are swept into the collector (a drift current). As a result, a substantial current flows between emitter and collector terminals. Note that the BC junction is reversed biased in this case (but the BC junction does not "act" as a diode).



This mode of operation is called the active mode: the BE junction is forward biased while the BC junction is reversed biased:

$$v_{BE} = V_{D0} \qquad \& \qquad v_{BC} < 0 \qquad \rightarrow \qquad v_{CE} = v_{CB} + v_{BE} > V_{D0}$$

Since the BE junction acts as a diode, the number of electrons which diffused into base and are near the BC junction scales as $\exp(v_{BE}/V_T)$ (for an emission coefficient, $n = 1$). As all these electrons will be swept into the collector, regardless of v_{BC} (or $v_{CE} = v_{BE} - v_{BC}$), the collector current, i_C should not depend on v_{CE}. Furthermore,

$$i_C = I_S\, e^{v_{BE}/V_T}$$

The base current, i_B, also scales as $\exp(v_{BE}/V_T)$. However, because emitter is heavily doped and base is thin, only a very small fraction of electrons that diffused into base combine with holes – majority of emitter-originated electrons are swept into the collector. As such, the ratio of $i_C/i_B = \beta$ is large and relatively constant (but changes with temperature, *etc.*). Parameter β is called the BJT common-emitter current gain (or current gain for short):

$$i_B = \frac{I_S}{\beta}\, e^{v_{BE}/V_T}$$

As can be seen, operation of a BJT requires the presence of emitter-generated electrons near the BC junction (thus, the BE junction should be forward biased). A BJT is called to be in "cut-off" if the BE junction is NOT forward biased. In this case, $i_B = 0$ and $i_C = 0$ regardless of any voltage applied to the BC junction.

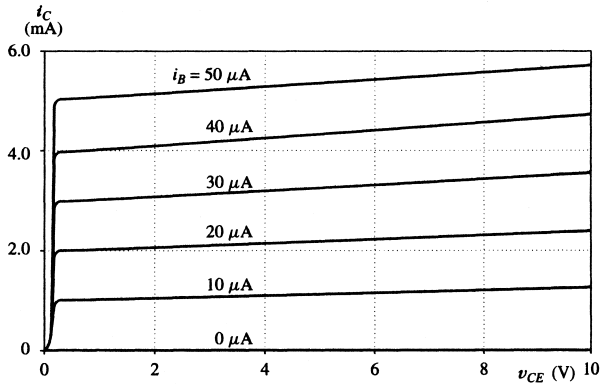
Now, let's consider the case of the BC junction being forward biased (with BE junction still forward biased), *i.e.,* $v_{CE} = v_{BE} - v_{BC} < V_{D0}$. This is called the saturation mode.

As the BC junction is forward biased, a diffusion current is set up between the collector and base regions (which is in the opposite direction to i_B and i_C). When v_{BC} is small ($v_{BC} < 0.3V$, or $v_{CE} > 0.4$V for Si), the diffusion current from the BC junction is negligible and i_C remains close to its value for the active mode. This region is usually called the "soft saturation region." Some text books include this region as part of the active mode, *i.e.,* say BJT is in active if $v_{CE} > 0.4$ V (instead of $v_{CE} \geq V_{D0} = 0.7$ V).

When v_{BC} becomes large enough ($v_{CE} \approx 0.1 - 0.3$ V for Si) a substantial diffusion current flows from the collector to the base, thereby reducing i_C below its active-mode level, *i.e.,* $i_C < \beta i_B$. This is called the "deep saturation" region.

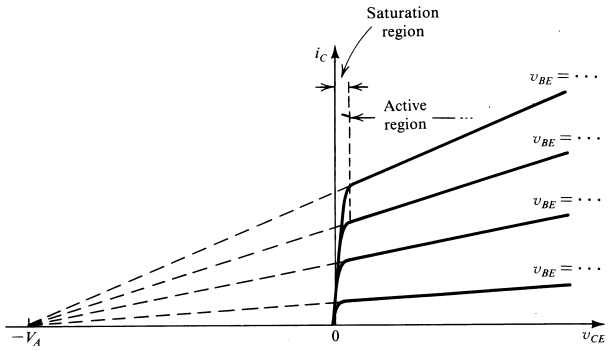
For v_{CE} close to zero ($v_{CE} < 0.1$ V for Si), the collector current rapidly goes to zero. This region is referred to as the "near cut-off" region.

BJT iv characteristics above is typically shown as plot of i_B vs v_{BE} (similar to a diode iv curve) and a "contour" plot of i_C vs v_{CE} with each contour lines representing a value of i_B. Note that $i_C = g(v_{CE}, i_B)$ is actually a "surface" plot in the 3-D space of i_C, v_{CE}, i_B. The $i_C v_{CE}$ plot shown is a projection of this 3-D surface with the i_B axis pointing into the plane. An $i_C v_{CE}$ plot of a commercial BJT is shown on the right.



A transistor can be damaged if (1) a large positive voltage is applied between the collector and emitter (breakdown region), or (2) product of $i_C v_{CE}$ exceed the power handling capability of the transistor, or (3) a large reverse voltage is applied between any two terminals.

Our rather simple description of the operation of a BJT in the active mode indicated that for a given i_B, $i_C = \beta i_B$ and is independent of v_{CE}. However, as $i_C v_{CE}$ plot above shows, i_C increases slightly with v_{CE}. The reason for this increase in i_C is that as v_{CE} is increased, the "effective" width of the base region is reduced and more electrons can reach the collector. This is called the "Early" effect.



In fact, if we extrapolate all characteristics lines of the active region, they would meet at a negative voltage of $v_{CE} = -V_A$ as is shown. The voltage V_A is particular to each BJT (depends on its manufacturing) and has a typical value of 50 to 100 V. It is called the "Early" voltage. The Early effect can be accounted for by the following addition to the i_C equation (Note that i_B equation does NOT change):

$$i_C = I_S e^{v_{BE}/V_T} \left(1 + \frac{v_{CE}}{V_A}\right)$$

The above model, reproduced in the table below, is called a "large signal" model as it applies to any size currents/voltages applied to the BJT (as opposed to a "small-signal" model discussed later). While rather simple, it is quite sufficient for analysis. Note that the explicit non-linear form is included only in the active mode equations (we will use this form later). Furthermore, only "deep" saturation mode is included as for practical reasons, BJT is only operated in deep saturation mode when it is used as a switch or a logic gate and soft

saturation is usually avoided when BJT is used in the active mode (*e.g.,* as an amplifier), in order to reduce non-linear distortion.

PSpice uses the Ebers-Moll model which includes a better treatment of transistor operation in the saturation mode. Furthermore, Ebers-Moll model provides a "smooth" transition from active to saturation to cut-off modes which is necessary for numerical calculations.

Summary of BJT Large-Signal Models (NPN):

	Large-signal model	**Linear Approximation**
Cut-off:		
BE reverse biased	$i_B = 0$	$i_B = 0, \quad v_{BE} < V_{D0}$
	$i_C = 0$	$i_C = 0$
Active:		
BE forward biased	$i_B = \dfrac{I_S}{\beta}\, e^{v_{BE}/V_T}$	$v_{BE} = V_{D0}, \quad i_B \geq 0$
CE reverse biased	$i_C = I_S\, e^{v_{BE}/V_T}\left(1 + \dfrac{v_{CE}}{V_A}\right)$	$i_c = \beta i_B, \quad v_{CE} \geq V_{D0}$
"Deep" Saturation:		
BE forward biased		$v_{BE} = V_{D0}, \quad i_B \geq 0$
CE forward biased	$v_{CE} = 0.1 - 0.3$ V, $\quad i_C < \beta i_B$	$v_{CE} = V_{sat} \quad i_C < \beta i_B$

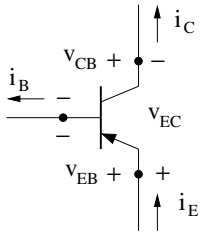
For Si, $V_{D0} = 0.7$ V, $V_{sat} = 0.2$ V.

Similar to diodes, we need to use approximate linear models for BJT iv equations for hand calculations and analysis. This can be easily achieved by using the diode constant voltage model for the BE junction. Such a piecewise linear model is also listed in the table above. Usually Early effect is ignored in such a linear approximation.

The BJT model above requires three parameters. Two (V_{D0} and V_{sat}) depend on the base semiconductor, *e.g.,* for Si, $V_{D0} = 0.7$ V, $V_{sat} = 0.2$ V. The third, β, depends on BJT structure. Also, β changes substantially with temperature, depends on on i_C, and can vary in commercial BJTs of similar type due to manufacturing inaccuracies. Typically, the manufacturer spec sheet specifies, an average value and a range for β of a BJT. The specified β_{min} (minimum value of β) is an important parameter, *i.e.,* all commercial BJTs of that type have a β larger than β_{min} (although some BJTs can have a β which is lower than the average value). This variation should be taken into account in designing BJT circuits. For example for a BJT circuit operating in deep saturation, we should set $i_C/i_B < \beta_{min}$ (instead of the average β) to ensure that it works correctly for all commercial BJTs of that particular model.

PNP transistor: A PNP transistor operates in a similar manner to a NPN BJT, expect that holes (instead of electrons) from the emitter diffuse through the base, reach the vicinity of the CB junction, and swept into the collector.

As a result, currents and voltages have opposite signs when compared to a NPN transistor *e.g.,* $v_{EB} = V_{D0}$ for the EB junction to be forward biased. The circuit symbol and conventions for currents/voltages in a PNP transistor are shown. With this convention, all currents and voltages would be positive and the NPN large signal model above directly applies to PNP transistors if we switch the subscripts for voltages, i.e., $v_{BE} \rightarrow v_{EB}$ and $v_{CE} \rightarrow v_{EC}$.



3.2 Solving BJT circuits

Similar to diode circuits, we need to assume that BJT is in a particular state, use BJT model for that state to solve the circuit, and then check the validity of our assumption.

Recipe for solving NPN BJT circuits:

1) Write down a KVL including the BE terminals (BE-KVL) and a KVL including CE terminals (CE-KVL).

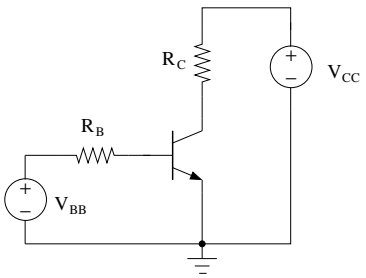
2) Assume BJT is in cut-off (this is the simplest). Set $i_B = 0$. Calculate v_{BE} from BE-KVL.
2a) If $v_{BE} < V_{D0}$, then BJT is in cut-off, $i_B = 0$ and v_{BE} is what you just calculated. Set $i_C = i_E = 0$, and calculate v_{CE} from CE-KVL. You are done.
2b) If $v_{BE} > V_{D0}$, then BJT is not in cut-off. Set $v_{BE} = V_{D0}$. Solve BE-KVL to find i_B. You should get $i_B > 0$.

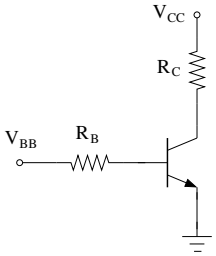
3) Assume that BJT is in the active mode. Let $i_C = \beta i_B$. Calculate v_{CE} from CE-KVL.
3a) If $v_{CE} > V_{D0}$, then BJT is in the active mode. You are done.
3b) If $v_{CE} < V_{D0}$, then BJT is not in the active mode. It is in saturation. Let $v_{CE} = V_{sat}$ and compute i_C from CE-KVL. You should find that $i_C < \beta i_B$. You are done.

For PNP transistors one should substitute, respectively, v_{EB} and v_{EC} for v_{BE} and v_{CE} in the above recipe.

Note that if there exists a resistor (or other elements) in the emitter circuit, BE-KVL and CE-KVL have to be solved simultaneously (See Example 3, page 3-7).

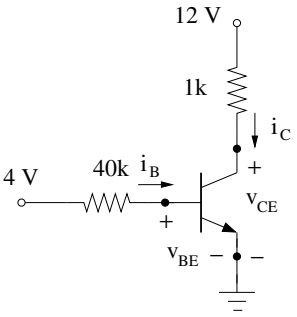
Circuit diagram conventions: For resistors attached to BJT terminals, it is customary to identify them with a subscript corresponding to that particular terminal, *i.e.,* R_B is a resistor attached to the base terminal as is shown below. The voltage sources attach to each terminal are identified with a "double subscripts" corresponding to that particular terminal, *i.e.,* V_{CC} is a voltage source attached to the collector terminal circuit. Lastly, we usually do not show the independent voltage sources on the circuit, rather we identify them with a "node" with a corresponding voltage (compare figures below).





Example 1: Compute transistor parameters (Si BJT with $\beta = 100$).

Following the procedure above (for NPN transistor):



BE-KVL: $\quad 4 = 40 \times 10^3 i_B + v_{BE}$

CE-KVL: $\quad 12 = 10^3 i_C + v_{CE},$

Assume BJT is in cut-off. Set $i_B = 0$ in BE-KVL:

$$\text{BE-KVL:} \quad 4 = 40 \times 10^3 i_B + v_{BE} \quad \rightarrow \quad v_{BE} = 4 > V_{D0} = 0.7 \text{ V}$$

So BJT is not in cut off and BJT is ON. Set $v_{BE} = 0.7\ V$ and use BE-KVL to find i_B.

$$\text{BE-KVL:} \quad 4 = 40 \times 10^3 i_B + v_{BE} \quad \rightarrow \quad i_B = \frac{4 - 0.7}{40,000} = 82.5\ \mu\text{A}$$

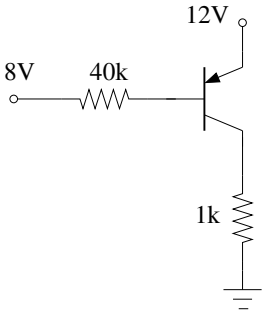
Assume BJT is in active, Find $i_C = \beta i_B$ and use CE-KVL to find v_{CE}:

$$i_C = \beta i_B = 100 i_B = 8.25 \text{ mA}$$

$$\text{CE-KVL:} \quad 12 = 1,000 i_C + v_{CE}, \quad \rightarrow \quad v_{CE} = 12 - 8.25 = 3.75 \text{ V}$$

As $v_{CE} = 3.75 > V_{D0}$, the BJT is indeed in active and we have: $v_{BE} = 0.7$ V, $i_B = 82.5\ \mu$A, $i_E = (\beta + 1) i_C = 8.33$ mA, and $v_{CE} = 3.75$ V.

Example 2: Compute transistor parameters (Si BJT with $\beta = 100$).



Following the procedure above (Note PNP transistor):

BE-KVL: $\quad 12 = v_{EB} + 40 \times 10^3 i_B + 8 \quad \rightarrow \quad 4 = v_{EB} + 40 \times 10^3 i_B$

CE-KVL: $\quad 12 = v_{EC} + 10^3 i_C$

Assume BJT is in cut-off. Set $i_B = 0$ in BE-KVL:

BE-KVL: $\quad 4 = v_{EB} + 40 \times 10^3 i_B \quad \rightarrow \quad v_{EB} = 4 > V_{D0} = 0.7$ V

So BJT is not in cut off and BJT is ON. Set $v_{EB} = 0.7\ V$ and use BE-KVL to find i_B.

BE-KVL: $\quad 4 = v_{EB} + 40 \times 10^3 i_B \quad \rightarrow \quad i_B = \dfrac{4 - 0.7}{40,000} = 82.5\ \mu$A

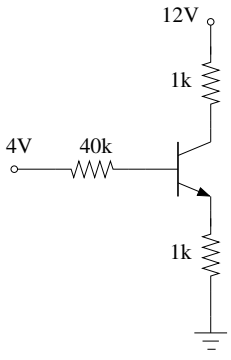
Assume BJT is in active mode. Find $i_C = \beta i_B$ and use CE-KVL to find v_{EC}:

$$i_C = \beta i_B = 100 i_B = 8.25 \text{ mA}$$

CE-KVL: $\quad 12 = v_{EC} + 10^3 i_C, \quad \rightarrow \quad v_{EC} = 12 - 8.25 = 3.75$ V

As $v_{EC} = 3.75 > V_{D0}$, the BJT is indeed in active mode and we have: $v_{EB} = 0.7$ V, $i_B = 82.5\ \mu$A, $i_E = (\beta + 1) i_B = 8.33$ mA, and $v_{EC} = 3.75$ V.

Example 3: Compute transistor parameters (Si BJT with $\beta = 100$).



BE-KVL: $\quad 4 = 40 \times 10^3 i_B + v_{BE} + 10^3 i_E$

CE-KVL: $\quad 12 = 1,000 i_C + v_{CE} + 1,000 i_E$

Assume BJT is in cut-off. Set $i_B = 0$ and $i_E = i_C = 0$ in BE-KVL:

BE-KVL: $\quad 4 = 40 \times 10^3 i_B + v_{BE} + 10^3 i_E \quad \rightarrow \quad v_{BE} = 4 > 0.7$ V

So BJT is not in cut off and $v_{BE} = 0.7$ V and $i_B > 0$.

In this circuit, there is a resistor in the emitter circuit and BE-KVL include i_E. Therefore, we need to solve BE-KVL and CE-KVL simultaneously.

Assume BJT is in active, $i_E = (\beta + 1)i_B$:

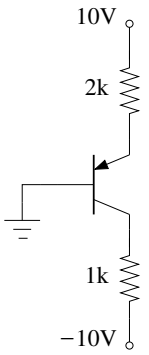
$$\text{BE-KVL:} \quad 4 = 40 \times 10^3 i_B + v_{BE} + 10^3(\beta+1)i_B = 0.7 + (40 \times 10^3 + 10^3 \times 101)i_B$$

$$i_B = 23.4\ \mu\text{A} \quad \rightarrow \quad i_C = \beta i_B = 2.34\ \text{mA}, \qquad i_E = (\beta+1)i_B = 2.36\ \text{mA}$$

$$\text{CE-KVL:} \quad 12 = 1,000 i_C + v_{CE} + 1,000 i_E, \quad \rightarrow \quad v_{CE} = 7.30\ \text{V}$$

As $v_{CE} = 7.30 > V_{D0}$, the BJT is indeed in active and we have: $v_{BE} = 0.7$ V, $i_B = 23.4\ \mu$A, $i_E \approx i_C = 2.34$ mA, and $v_{CE} = 7.30$ V.

Example 4: Compute transistor parameters (Si BJT with $\beta = 100$).



Since there is a 10 V supply in the EB-loop, it is a good starting assumption that BJT is ON (PNP: $v_{EB} = V_{D0} = 0.7$ V and $i_B > 0$)

$$\text{BE-KVL:} \quad 10 = 2 \times 10^3 i_E + v_{EB}$$

$$i_E = \frac{10 - 0.7}{2 \times 10^3} = 4.65\ \text{mA}$$

Since $i_E > 0$, the assumption of BE ON is justified (since $i_E > 0$ requires both i_B and $i_C > 0$). Assuming BJT in active:

$$i_E = i_C + i_B = (\beta+1)i_B \quad \rightarrow \quad i_B = 4.65/101 \simeq 46.0\ \mu\text{A}$$

$$i_C = i_E - i_B \simeq 4.60\ \text{mA}$$

$$\text{CE-KVL:} \quad 10 = 2 \times 10^3 i_E + v_{EC} + 10^3 i_C - 10 \quad \rightarrow \quad v_{EC} = 6.10\ \text{V}$$

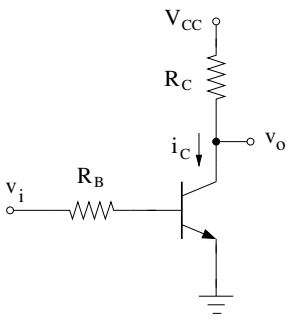
Since $v_{EC} = 6.10 > 0.7 = V_{D0}$), the assumption of BJT in active is justified and $v_{EB} = 0.7$ V, $i_B = 46.0\ \mu$A, $v_{EC} = 6.10$ V, and $i_C = 4.60$ mA.

3.3 BJT transfer function

It is essential to realize that a transistor acts as a "valve." In a BJT, i_B controls how much i_C flows through the transistor. The BJT does not "create" i_C. Rather a voltage or a current source is needed in the CE circuit which supplies i_C.

If BJT is in cut-off ($i_B = 0$), the valve is closed and no i_C flows, In the active mode, the valve is partially open and changes in i_B cause proportional changes in i_C. In saturation, the valve is open enough such that i_C has reached the maximum value that can be provided by the outside circuit. Increasing i_B would not lead to any increase in i_C (*i.e.,* i_C is "saturated").

Transistor is a three terminal element. It should be configured as a "two-port" network with two input wires and two output wires (so, one BJT terminal would be common between the input and the output). The widely used common-emitter configuration is shown (emitter is the common terminal).



It is obvious that we cannot directly apply v_i between the base and the emitter as the range of acceptable v_i would be quite limited (the BE junction is ON only for a small range of voltages around 0.7 V). As such, a resistor R_B is placed in the base circuit in order to "convert" v_i into an i_B that controls BJT operation.

As discussed, the voltage source V_{CC} is necessary to provide i_C. A resistor R_C is placed in the collector circuit. Otherwise, $v_{CE} = V_{CC}$ and no useful output is taken from the circuit.

We can compute the transfer function of this BJT circuit with a parametric method (similar to that used for diodes). We compute $v_o = v_{CE}$ in terms of v_i. Value of i_C is also computed as it provides insight into building switch circuits. We start with:

BE-KVL: $v_i = R_B i_B + v_{BE}$

CE-KVL: $V_{CC} = R_C i_C + v_{CE}$

BJT in Cut-off: $i_B = 0$, $v_{BE} < V_{D0}$, and $i_C = 0$

BE-KVL: $v_i = v_{BE}$ and $v_{BE} < V_{D0} \quad \rightarrow \quad v_i < V_{D0}$

CE-KVL: $V_{CC} = R_C i_C + v_{CE} \quad \rightarrow \quad v_o = v_{CE} = V_{CC}$

Thus, as long as $v_i < V_{D0}$, BJT will be in cut-off with $v_{CE} = V_{CC}$ and $i_C = 0$.

BJT in Active: $v_{BE} = V_{D0}$, $i_B \geq 0$, $i_C = \beta i_B$, and $v_{CE} \geq V_{D0}$

BE-KVL: $v_i = R_B i_B + V_{D0} \quad \rightarrow \quad i_B = \dfrac{v_i - V_{D0}}{R_B} \quad \rightarrow \quad i_C = \beta i_B = \beta \times \dfrac{v_i - V_{D0}}{R_B}$

CE-KVL: $V_{CC} = R_C i_C + v_{CE} \quad \rightarrow \quad v_o = v_{CE} = V_{CC} - \dfrac{\beta R_C}{R_B} \times (v_i - V_{D0})$

$$v_{CE} \geq V_{D0} \quad \rightarrow \quad v_i \leq V_{D0} + \frac{R_B}{\beta R_C} \times (V_{CC} - V_{D0}) \equiv V_{IH}$$

Thus, for $V_{D0} \leq v_i \leq V_{IH}$, BJT will be in active with v_{CE} and i_C given by the above expressions. Note that as v_i increases, i_B and i_C increase while $v_o = v_{CE}$ decreases.

BJT in saturation: $v_{BE} = V_{D0}$, $i_B \geq 0$, $v_{CE} = V_{sat}$, and $i_C < \beta i_B$.

$$\text{BE-KVL:} \quad v_i = R_B i_B + V_{D0} \quad \rightarrow \quad i_B = \frac{v_i - V_{D0}}{R_B}$$

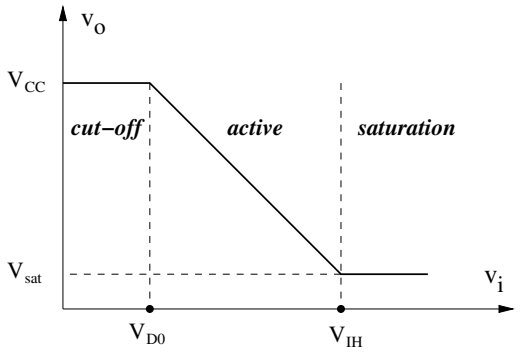
$$v_o = v_{CE} = V_{sat}$$

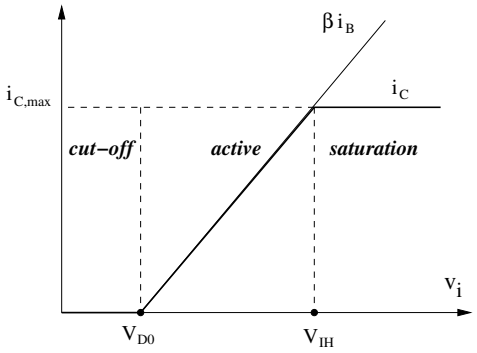
$$\text{CE-KVL:} \quad V_{CC} = R_C i_C + V_{sat} \quad \rightarrow \quad i_C = \frac{V_{CC} - V_{sat}}{R_C}$$

$$i_C < \beta i_B \quad \rightarrow \quad v_i > V_{D0} + \frac{R_B}{\beta R_C} \times (V_{CC} - V_{sat}) \equiv \hat{V}_{IH}$$

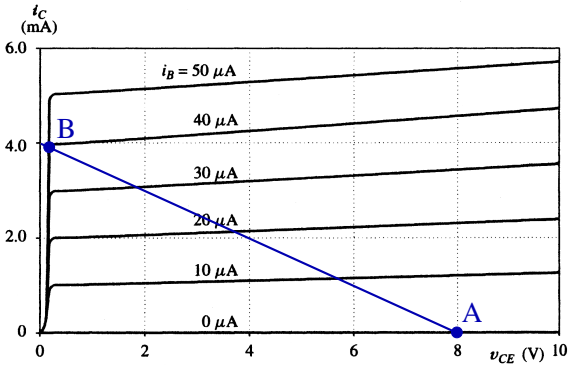
Thus, for $v_i > \hat{V}_{IH}$, BJT will be in saturation with $v_o = v_{CE} = V_{sat}$ and i_C given by the above expressions. Note that as v_i increases, i_C and $v_o = v_{CE}$ do not change, although i_B increases (i_C is "saturated!").

$\hat{V}_{IH}$ is very close to V_{IH} defined above (V_{sat} replaced with V_{DD} in the fraction). This discontinuity in v_i range is due to the use "deep" saturation model. In practice, a BJT transitions from active to saturation smoothly. Figures below show the transfer function of the BJT common-emitter configuration. Both v_o and i_C are plotted.





The behavior of the circuit can also be explored through the use of a load line. For BJTs, the load line is the relationship between i_C and v_{CE} that is imposed on BJT by the external circuit (*i.e.* through CE-KVL). Recall that $i_C v_{CE}$ plot shown is a projection of a 3D surface with the i_B axis into the plane. In this 3-D space, CE-KVL represents a plane which is parallel to i_B axis (since CE-KVL does not include i_B).



The BJT load line is the intersection of CE-KVL plane with 3-D BJT *iv* characteristics.

In our 2-D projection, the BJT operating point is at the intersection of the load line with the corresponding i_B contour of the transistor (*e.g.,* if $i_B = 20$ μA, the intersection of the load line with the BJT line labeled $i_B = 20$ μA).

In the load line plot above, BJT is at point A as long as $v_i < V_{D0}$ and BJT is in cut-off ($i_B = 0$). When v_i exceeds this value, $i_B > 0$ and operating point move along the load line toward higher i_C and lower $v_o = v_{CE}$ (compare this with the transfer function plots!). When $v_i > V_{IH}$, transistor is in the saturation region (point B). As can be seen, increasing v_i further (and increasing i_B) does not change i_C and value of i_C is saturated.

The transfer function plots above provide an insight into BJT functional circuits. If a BJT is in the active mode, i_C is proportional to i_B (and $v_o = v_{CE}$ has a linear relationship with v_i). Thus, one can utilize a BJT in the active mode to amplify signals since $i_C = \beta i_B$ and $\beta \gg 1$.

Features of the transfer function in the cut-off and the saturation regions allow one to build BJT switches and logic gates.

In electronic circuits, mechanical switches are not used. The switching action is performed by a transistor (similar to the circuit above). The input to the switch, v_i, is the output of some logic gate. When $v_i = 0$, the BJT will be in cut-off and $i_C = 0$ (open switch). When $v_i > V_{IH}$, the BJT is in saturation with a large i_C. When R_C is replaced with a load, this circuit can switch a load ON or OFF (see *e.g.,* Problems 12 & 13).

Similarly, the BJT circuit above is a NOT (or inverter) logic gate. When $v_i = 0$ (low state), BJT will be in cut-off and $v_o = V_{CC}$ (high State) When $v_i > V_{IH}$ (high state), BJT is in saturation with $v_o = v_{CE} = V_{sat} \approx 0.2$ V (low state). BJT logic gates are explored below.

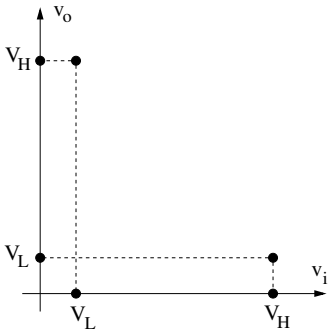
3.4 BJT Logic Gates

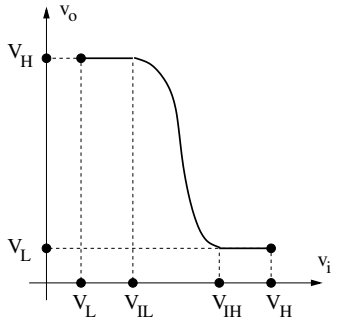
You have seen binary mathematics and logic gates in ECE25. We will explore some electronic logic gates in this course. Binary mathematics is built upon two states: 0, and 1. We need to relate these binary states to currents or voltages to build logic circuits. It is advantageous (from the point of view of power consumption) to operate circuits with a low current. Thus, we denote these the binary states with voltages V_L for state 0 or the Low state and V_H for state 1 or the High state (for example, 0 V to represent state 0 and 5 V to represent state 1). These voltages are quite arbitrary and can be chosen to have any value.

The desired transfer function of an "ideal" inverter is shown in the figure below (left): when the input is low, the output is high and the when the input is high, the output is low. We can see a difficulty right away. In a practical circuit, there would be an output voltage for any input voltage, so the output voltage has to make a "smooth" transition from v_H to v_L as

the input voltage is varied. We also need to define a range of voltages (instead of one value) to represent high and low states as it is extremely difficult to design an electronic circuit to give an exact voltage value. So, gates are designed to respond to a range of voltages, *i.e.,* the gate would think that the input is low if the input voltage is smaller than V_{IL} and would think that the input is high if the input voltage is larger than V_{IH} (see figure).

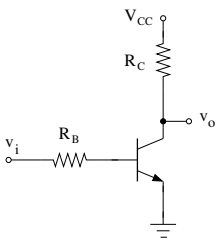
With these definitions, the transfer function of a practical inverter is shown below (right). The range of voltages, V_L to V_{IL} and V_{IH} to V_H are called the noise margin(s). The range of voltages between V_{IL} to V_{IH} is the forbidden region as in this range the output of the gate does not correspond to a binary state. The maximum speed that a logic gate can operate is set by the time it takes the circuit to traverse this forbidden region as the input voltage is varied from one state to another state.

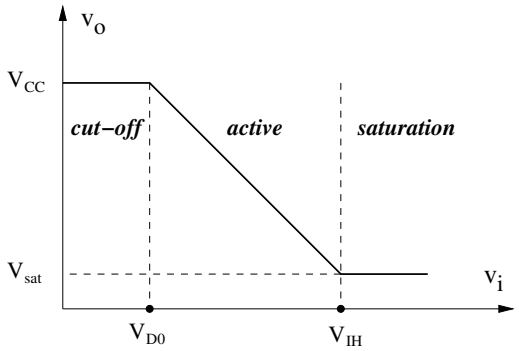




3.4.1 Resistor-Transistor Logic (RTL)

The transfer function of the common-emitter configuration is reproduced below. Comparing this transfer function with the transfer function of a NOT gate (above), we can see the circuit would acts as a NOT gate (or an inverter) with a low state of $V_L = V_{sat}$ and a high state of $V_H = V_{CC}$ with $V_{IL} = V_{D0}$ and V_{IH} defined in page 3-10.



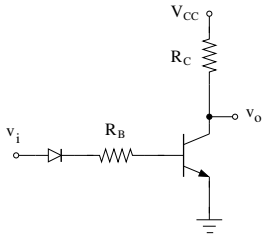


This circuit is a member of resistor-transistor (RTL) family of logic gates.

A major drawback of this RTL inverter gate is the limited input range for the "low" signal (V_{IL}). While the noise margin for the "high" state can be controlled by adjusting values of R_C and R_B, the noise margin for the "low" state is quite small and is set by $V_L = V_{sat} = 0.2$ V and $V_{IL} = V_{D0} = 0.7$ V. Moreover, we have used a constant-voltage model for the BE junction diode which assumes that BE junction turns ON at $V_{D0} = 0.7$ V. In reality, the BJT will come out of cut-off (the BE junction will conduct) at smaller voltages (~ 0.5 V), making the noise margin for "low" state even smaller. Note that this issue of noise margin equally applies to BJT switches.

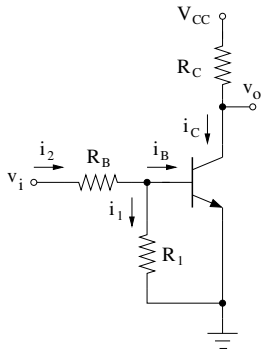
In order to build a gate with a larger noise margin for the "low" state, we examine the BE-KVL: $v_i = R_B i_B + v_{BE}$. Note that $v_i = V_{IL}$ corresponds to $v_{BE} = V_{D0}$ and $i_B > 0$ but small. Two approaches are possible. First, we can add an element in series with R_B which would have a large voltage drop for a small current, *e.g.,* a diode.

For this circuit, BE-KVL gives: $v_i = v_D + R_B i_B + v_{BE}$. Then to find V_{IL}, we substitute for $v_{BE} = V_{D0}$ and $i_B > 0$ but small to get: $V_{IL} \approx v_D + V_{D0}$. Since $i_D = i_B > 0$ but small, the diode should also be forward biased and $v_D = V_{D0}$. Thus, $V_{IL} \approx 2V_{D0} = 1.4$ V. Note that V_{IL} can be increased further in increments of V_{D0} by adding more diodes in the input.



This approach works reasonably well in ICs as the diode and the BE junction can be constructed with similar reverse saturation currents. However, for a circuit built with discrete components (*e.g.,* a BJT switch) this approach may not work well as the reverse saturation current for discrete diodes, is typically 2 to 3 orders of magnitude larger than reverse saturation current for the BE junction. As such, the small current needed to make $v_{BE} \simeq V_{D0}$ only leads to $v_D = 0.3 - 0.4$ V. (see Lab 4 for a solution to this problem).

The second way to increase the noise margin is to add a resistor between the base and ground as is shown. To see the impact of this resistor, note that V_{IL} is the input voltage when BJT is just leaving the cut-off region. At this point, $v_{BE} = V_{D0}$, and i_B is positive but very small (effectively zero). Since a voltage v_{BE} has appeared across R_1, we have:



$$i_1 = \frac{v_{BE}}{R_1} \qquad i_2 = i_B + i_1 \approx i_1 = \frac{v_{BE}}{R_1}$$

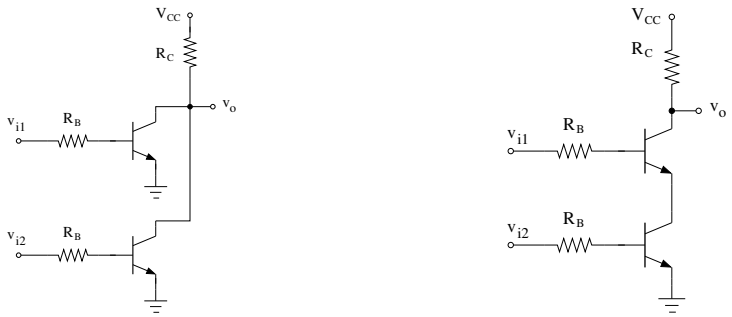
$$V_{IL} = v_i = R_B i_2 + v_{BE} = v_{BE}\frac{R_B}{R_1} + v_{BE} = V_{D0}\left(1 + \frac{R_B}{R_1}\right)$$

This value should be compared with $V_{IL} = V_{D0}$ in the absence of resistor R_1. It can be seen that for $R_B = R_1$, V_{IL} can be raised from 0.7 to 1.4 V. Moreover, arbitrary values of V_{IL} can

be achieved by proper choice of R_B and R_1. Typically, R_1 does not affect V_{IH} as i_B needed to put the BJT in saturation is typically several times larger than i_1.

RTL NOR Gate

All high-level logic gate can be constructed from "basic" logic gates like NOR or NAND. By combining two or more RTL inverters, one obtains the basic logic gate circuit of RTL family, a "NOR" gate, as is shown below left (see Problem 15). More BJTs can be added for additional input signals. A RTL NAND gate is shown below right (see Problem 16).



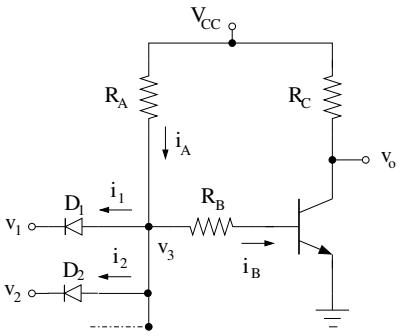
RTLs were the first digital logic circuits using transistors. They require at least one resistor and one BJT per input. They were replaced with diode-transistor logic, DTL (reduced number of resistors and BJTs) and transistor-transistor logic, TTL (which "packs" all of the didoes in a special transistor). With the advent of CMOS technology, almost digital gates are CMOS gates and BJTs are only used in high-speed emitter-coupled logic (ECL) circuits.

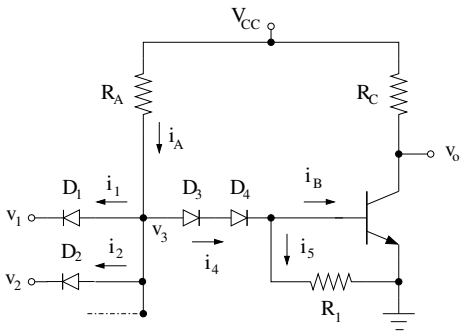
A DTL circuit is analyzed in the following section is as it provides a good example for solving BJT circuits.

3.4.2 Diode-Transistor Logic (DTL)

The basic gate of DTL logic circuits is a NAND gate which is constructed by a combination of a diode AND gate (analyzed in pages 2-12) and a BJT inverter gate as is shown below (left figure). Because R_B is large, on ICs, this resistor is usually replaced with two diodes. The combination of the two diodes and the BE junction diode leads to a voltage of 2.1 V for the inverter to switch and a $V_{IL} = 1.4$ V for the NAND gate (Why?). Resistor R_1 is necessary because without this resistor, current i_B will be too small and the voltage across D_3 and D_4 will not reach 0.7 V although they are both forward biased.

Example: Verify that the DTL circuit above (with $R_A = 5$ kΩ, $R_C = 1$ kΩ, $R_1 = 5$ kΩ, and $V_{CC} = 5$ V) is a NAND gate. Assume that "low"state is 0.2 V, "high" state is 5 V, and BJT $\beta_{min} = 40$.





Case 1: $v_1 = v_2 = 0.2$ V It appears that D_1 and D_2 will be forward biased by the 5-V supply. Assume D_1 and D_2 are ON: $v_{D1} = v_{D2} = V_{D0} = 0.7$ V and $i_1 > 0$, $i_2 > 0$.

$$v_3 = v_1 + v_{D1} = v_2 + v_{D2} = 0.2 + 0.7 = 0.9 \text{ V}$$

Voltage $v_3 = 0.9$ V is not sufficient to froward bias D_3 and D_4 as $v_3 = v_{D3} + v_{D4} + v_{BE}$ and we need at least 1.4 V to forward bias the two diodes. So both D_3 and D_4 are OFF and $i_4 = 0$. (Note that D_3 and D_4 can be forward biased without the BE junction being forward biased as long as the current i_4 is small enough such that voltage drop across the 5 kΩ resistor parallel to the BE junction is smaller than 0.7 V. In this case, $i_5 = i_4$ and $i_B = 0$.) Then:

$$i_1 + i_2 = i_A = \frac{5 - v_3}{5,000} = \frac{5 - 0.9}{5,000} = 0.82 \text{ mA}$$

And by symmetry, $i_1 = i_2 = 0.5 i_A = 0.41$ mA. Since both i_1 and i_2 are positive, our assumption of D_1 and D_2 being ON are justified. Since $i_4 = 0$, $i_B = 0$ and BJT will be in cut-off with $i_C = 0$ and $v_o = 5$ V.

So, in this case, D_1 and D_2 are ON, D_3 and D_4 are OFF, BJT is in cut-off, and $v_o = 5$ V.

Case 2: $v_1 = 0.2$ V, $v_2 = 5$ V Following arguments of case 1, assume D_1 is ON. Again, $v_3 = 0.7 + 0.2 = 0.9$ V, and D_3 and D_4 will be OFF with $i_4 = 0$. We find that voltage across D_2 is $v_{D2} = v_3 - v_2 = 0.9 - 5 = -4.1$ V and, thus, D_2 will be OFF and $i_2 = 0$. Then:

$$i_1 = i_A = \frac{5 - v_3}{5,000} = \frac{5 - 0.9}{5,000} = 0.82 \text{ mA}$$

and since $i_1 > 0$, our assumption of D_1 ON is justified. Since $i_4 = 0$, $i_B = 0$ and BJT will be in cut-off with $i_C = 0$ and $v_o = 5$ V.

So, in this case, D_1 is ON, D_2 is OFF, D_3 and D_4 are OFF, BJT is in cut-off, and $v_o = 5$ V.

Case 3: $v_1 = 5$ V, $v_2 = 0.2$ V Because of the symmetry in the circuit, this is exactly the same as case 2 with roles of D_1 and D_2 reversed.

So, in this case, D_1 is OFF, D_2 is ON, D_3 and D_4 are OFF, BJT is in cut-off, and $v_o = 5$ V.

Case 4: $v_1 = v_2 = 5$ V Examining the circuit, it appears that the 5-V supply will NOT be able to forward bias D_1 and D_2. Assume D_1 and D_2 are OFF: $i_1 = i_2 = 0$, $v_{D1} < V_{D0}$ and $v_{D2} < V_{D0}$. On the other hand, it appears that D_3 and D_4 will be forward biased. Assume D_3 and D_4 are forward biased: $v_{D3} = v_{D4} = V_{D0} = 0.7$ V and $i_4 > 0$. Further, assume the BJT is not in cut-off $v_{BE} = V_{D0} = 0.7$ V and $i_B > 0$. In this case:

$$v_3 = v_{D3} + v_{D4} + v_{BE} = 0.7 + 0.7 + 0.7 = 2.1 \text{ V}$$

$$v_{D1} = v_3 - v_1 = 2.1 - 5 = -2.9 \text{ V} < V_{D0} \qquad v_{D2} = v_3 - v_2 = 2.1 - 5 = -2.9 \text{ V} < V_{D0}$$

Thus, our assumption of D_1 and D_2 being OFF are justified. Furthermore:

$$i_4 = i_A = \frac{5 - v_3}{5,000} = \frac{5 - 2.1}{5,000} = 0.58 \text{ mA}$$

$$i_5 = \frac{v_{BE}}{5,000} = \frac{0.7}{5,000} = 0.14 \text{ mA}$$

$$i_B = i_4 - i_5 = 0.58 - 0.14 = 0.44 \text{ mA}$$

and since $i_4 > 0$ our assumption of D_3 and D_4 being ON are justified and since $i_B > 0$ our assumption of BJT not in cut-off is justified.

We still do not know if BJT is in active or saturation. Assume BJT is in saturation: $v_o = v_{CE} = V_{sat} = 0.2$ V and $i_C/i_B < \beta$. Then, assuming no gate is attached to the circuit, we have

$$i_C = \frac{5 - V_{sat}}{1,000} = \frac{5 - 0.2}{1,000} = 4.8 \text{ mA}$$

and since $i_C/i_B = 4.8/0.44 = 11 < \beta = 40$, our assumption of BJT in saturation is justified.

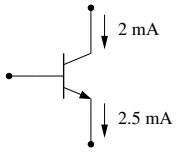
So, in this case, D_1 and D_2 are OFF, D_3 and D_4 are ON, BJT is in saturation and $v_o = 0.2$ V.

Overall, the output in "low" only if both inputs are "high", thus, this is a NAND gate.

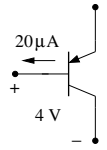
3.5 Exercise Problems

Problems 1 to 6. Find the transistor parameters (Si BJTs with $\beta = 100$).

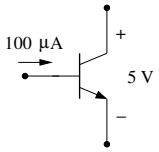
Problem 7. Find I (Si BJT with $\beta = 100$).



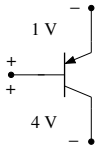
Problem 1



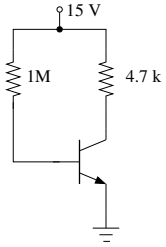
Problem 2



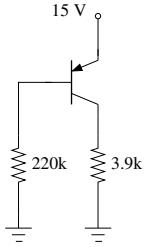
Problem 3



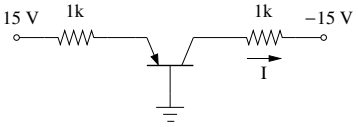
Problem 4



Problem 5



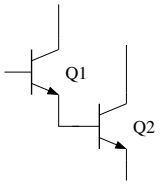
Problem 6



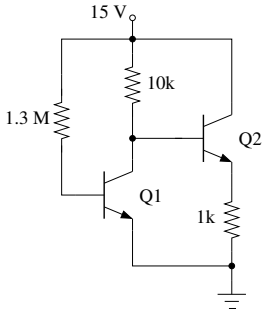
Problem 7

Problem 8. This configuration is called a Darlington Pair. A) Show that If Q1 is OFF, Q2 will be OFF and if Q1 is ON, Q2 will ON, B) Show that if both BJTs are in active, the transistor pair act like one BJT in active with $\beta = i_{C2}/i_{B1} \approx \beta_1\beta_2$.

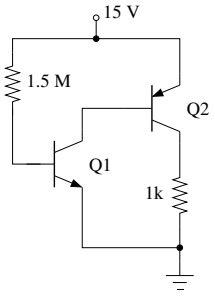
Problems 9 and 10. Find i_B, v_{BE}, i_C, v_{CE}, and state of both transistors (Si BJTs with $\beta = 100$).



Problem 8



Problem 9



Problem 10

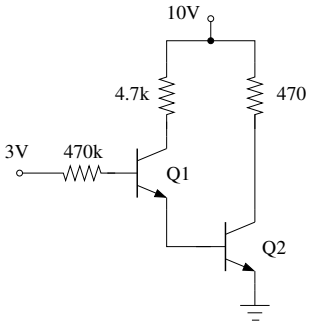
Problem 11. Find i_B, v_{BE}, i_C, v_{CE}, and state of both transistors for A) $v_i = 1$ V, B) $v_i = 3$ V, C) $v_i = 5$ V. Si BJTs with $\beta_1 = 100$ and $\beta_2 = 50$.

Problem 12. This is a switching circuit. v_i is the output of a logic gate which turns the light-emitting diode (LED) on or off depending on the state of the logic gate. The LED is made of GaAs and has a $V_{D0} = 1.7$ V. A) Show that for $v_i = 0$, LED will be OFF, B) Show that for $v_i = 5$ V, LED will be ON, and C) If we tarting from $v_i = 0$ and slowly increase v_i, at what voltage LED starts to light up? (Si BJT with $\beta = 100$.)

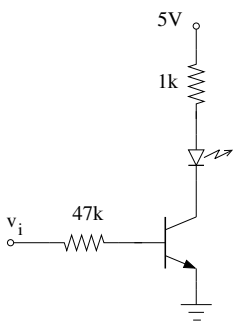
Problem 13. Design a switch circuit similar to problem 12 which turns an LED OFF and ON such that the LED is OFF for $v_i < 2.5$ V and is ON for $v_i > 2.5$ V. (Hint: See page 3-13 of lecture notes).

Problem 14. Show that this is NOR gate with a LOW state of 0.2 V and a HIGH state of 5 V (Si BJTs with $\beta = 100$).

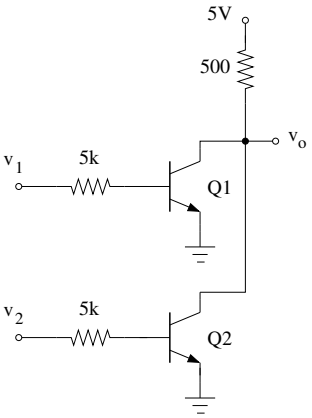
Problem 15. Show that this is NAND gate with a LOW state of 0.4 V and a HIGH state of 1.2 V (Si BJTs with $\beta = 200$).



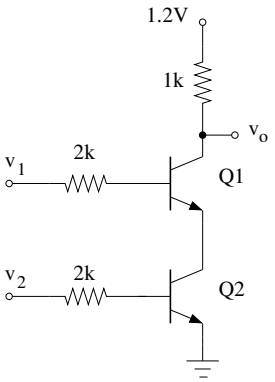
Problem 11



Problem 12



Problem 14

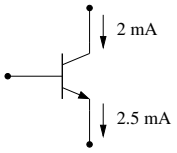


Problem 15

3.6 Solution to Selected Exercise Problems

Problem 1. Find the transistor parameters (Si BJTs with $\beta = 100$).

This is a NPN transistor with $i_C = 2$ mA and $i_E = 2.5$ mA.

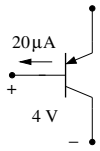


$$i_B = i_E - i_C = 0.5 \text{ mA} > 0 \quad \rightarrow \quad \text{BJT is ON} \quad \rightarrow \quad v_{BE} = 0.7 \text{ V}$$

$$\frac{i_C}{i_B} = \frac{2}{0.5} = 4 < 100 = \beta \quad \rightarrow \quad \text{BJT is in saturation} \quad \rightarrow \quad v_{CE} = 0.2 \text{ V}$$

Problem 2. Find the transistor parameters (Si BJTs with $\beta = 100$).

This is a PNP transistor with $i_B = 20$ μA and $v_{CB} = -4$ V.



Since $i_B > 0$, EB is ON and $v_{EB} = 0.7$ V.

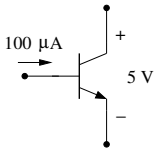
Since $v_{CB} = -4 < V_{D0} = 0.7$ V, CB is reverse biased and this transistor is in active mode:

$$v_{EC} = v_{EB} + v_{BC} = 0.7 + 4 = 4.7 \text{ V}$$

$$i_C = \beta i_B = 2 \text{ mA}$$

Problem 3. Find the transistor parameters (Si BJTs with $\beta = 100$).

This is a NPN transistor with $i_B = 100$ μA and $v_{CE} = 5$ V.

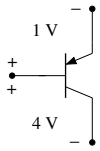


$$i_B = 100 \ \mu \text{ A} > 0 \quad \rightarrow \quad \text{BJT is ON} \quad \rightarrow \quad v_{BE} = 0.7 \text{ V}$$

$$v_{CE} = 5 \text{ V} > V_{D0} = 0.7 \text{ V} \quad \rightarrow \quad \text{BJT is in active} \quad \rightarrow \quad i_C = \beta i_B = 10 \text{ mA}$$

Problem 4. Find the transistor parameters (Si BJTs with $\beta = 100$).

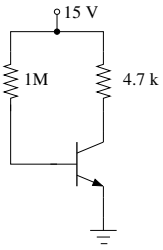
This is a PNP transistor with $v_{EB} = -1$ V and $v_{CB} = -4$ V.



$$v_{EB} = -1 \text{ V} < 0.7 = V_{D0} \quad \rightarrow \quad \text{BJT is in cut-off} \quad \rightarrow \quad i_B = 0 \quad \& \quad i_C = 0$$

$$v_{EC} = v_{EB} + v_{BC} = -1 + 4 = 3 \text{ V}$$

Problem 5. Find the transistor parameters (Si BJTs with $\beta = 100$).



BE-KVL: $\quad 15 = 10^6 i_B + v_{BE}$

CE-KVL: $\quad 15 = 4.7 \times 10^3 i_C + v_{CE}$

Assume BJT is ON, $v_{BE} = 0.7$ V, $i_B > 0$. BE-KVL gives:

BE-KVL: $\quad 15 = 10^6 i_B + 0.7 \quad \rightarrow \quad i_B = 14.3\ \mu$A

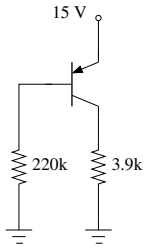
Since $i_B > 0$, our assumption of BJT is ON is justified.

Assume BJT is in active: $i_C = \beta i_B = 100 i_B = 1.43$ mA and $v_{CE} > 0.7$ V. CE-KVL gives:

CE-KVL: $\quad 15 = 4.7 \times 10^3 \times 1.43 \times 10^{-3} + v_{CE} \quad \rightarrow \quad v_{CE} = 8.28$ V

Since $v_{CE} = 8.28 > 0.7$ V our assumption of BJT in active is justified with $i_B = 14.3\ \mu$A, $i_C = 1.43$ mA, and $v_{CE} = 8.28$ V.

Problem 6. Find the transistor parameters (Si BJTs with $\beta = 100$).



BE-KVL: $\quad 15 = v_{EB} + 220 \times 10^3 i_B$

CE-KVL: $\quad 15 = v_{EC} + 3.9 \times 10^3 i_C$

Assume BJT (PNP) is ON, $v_{EB} = 0.7$ V, $i_B > 0$. BE-KVL gives:

BE-KVL: $\quad 15 = 0.7 + 220 \times 10^3 i_B \quad \rightarrow \quad i_B = 65\ \mu$A

Since $i_B > 0$, our assumption of BJT ON is justified.

Assume BJT is in active: $i_C = \beta i_B = 100 i_B = 6.5$ mA and $v_{EC} > 0.7$ V. CE-KVL gives:

CE-KVL: $\quad 15 = v_{EC} + 3.9 \times 10^3 \times 6.5 \times 10^{-3} \quad \rightarrow \quad v_{EC} = -10.4$ V

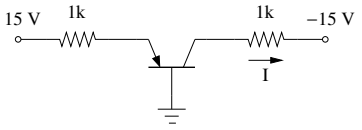
Since $v_{EC} = -10.4 < 0.7$ V our assumption of BJT in active is NOT justified.

Assume BJT in saturation, $v_{EC} = 0.2$ V, and $i_C < \beta i_B$. CE-KVL gives:

$$15 = 0.2 + 3.9 \times 10^3 i_C \quad \rightarrow \quad i_C = 3.79 \text{ mA}$$

Since $i_C / i_B = 3.79/0.065 = 58 < 100 = \beta$, our assumption of BJT in saturation is justified with $i_B = 65\ \mu$A, $i_C = 3.79$ mA, and $v_{EC} = 0.2$ V.

Problem 7. Find I (Si BJTs with $\beta = 100$).



EB-KVL: $\quad 15 = 10^3 i_E + v_{EB}$

EC-KVL: $\quad 15 = 10^3 i_E + v_{EC} + 10^3 i_C - 15$

Assume BJT (PNP) is OFF, $i_B = i_C = i_E = 0$ and $v_{EB} < 0.7$ V. EB-KVL gives:

EB-KVL: $\quad 15 = v_{EB}$

Since $v_{EB} = 15 > 0.7$ V, BJT is NOT in cut-off.

Assume BJT is ON, $v_{EB} = 0.7$ V, $i_B > 0$. EB-KVL gives:

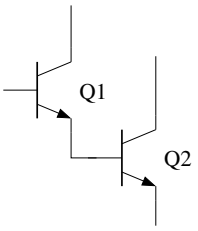
EB-KVL: $\quad 15 = 10^3 i_E + 0.7 \quad \rightarrow \quad i_E = 14.3$ mA

Assume BJT is in active: $i_E \approx i_C = \beta i_B$ and $v_{EC} > 0.7$ V. Therefore $i_C \approx i_E = 14.3$ mA and $i_B = i_C/100 = 143$ μA. EC-KVL gives

EC-KVL: $\quad 15 = 10^3 \times 14.3 \times 10^{-3} + v_{EC} + 10^3 \times 14.3 \times 10^{-3} - 15 \quad \rightarrow \quad v_{EC} = 1.4$ V

Since $v_{EC} = 1.4 > 0.7$ V, BJT is in active with $i_B = 143$ μA, $i_C = 14.3$ mA, and $v_{EC} = 1.4$V.

Problem 8. This configuration is called a Darlington Pair. A) Show that If Q1 is OFF, Q2 will be OFF and if Q1 is ON, Q2 will ON, B) Show that if both BJTs are in active, the transistor pair act like one BJT in active with $\beta = i_{C2}/i_{B1} \approx \beta_1\beta_2$.



Darlington pair are arranged such that $i_{E1} = i_{B2}$.

<u>Part A:</u>

If Q1 is OFF, $i_{B1} = i_{C1} = i_{E1} = 0$. Because of Darlington pair arrangement, $i_{B2} = i_{E1} = 0$ and Q2 would also be OFF.
If Q1 is ON, $i_{E1} > 0$. Because of Darlington pair arrangement, $i_{B2} = i_{E1} > 0$ and Q2 would also be ON.

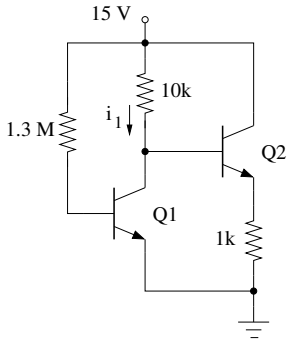
<u>Part B:</u>

If Q1 & Q2 are both in active:

$$i_{C2} = \beta_2 i_{B2} = \beta_2 i_{E1} \approx \beta_2 i_{C1} = \beta_1\beta_2 i_{B1} \quad \rightarrow \quad \frac{i_{C2}}{i_{B1}} = \beta_1\beta_2$$

So, the Darlington pair act as a super high β BJT.

Problem 9. Find i_B, v_{BE}, i_C, v_{CE}, and state of both transistors (Si BJTs with $\beta = 100$).



BE1-KVL: $15 = 1.3 \times 10^6 i_{B1} + v_{BE1}$

CE1-KVL: $15 = 10 \times 10^3 i_1 + v_{CE1}$

BE2-KVL: $v_{CE1} = v_{BE2} + 10^3 i_{E2}$

CE2-KVL: $15 = v_{CE2} + 10^3 i_{E2}$

KCL: $i_1 = i_{C1} + i_{B2}$

Assume Q1 is ON, $V_{BE1} = 0.7$ V and $i_{B1} > 0$. BE1-KVL gives:

BE1-KVL: $15 = 1.3 \times 10^6 i_{B1} + 0.7 \quad \rightarrow \quad i_{B1} = 11\ \mu$A

Since $i_{B1} > 0$, our assumption of Q1 ON is justified.

Assume Q1 is active, $i_{C1} = 100 i_{B1} = 1.1$ mA and $v_{CE1} > 0.7$ V. In principle, we should move forward and assume state of Q2 and solve the remaining three equations together. However, solution can be simplified if we assume $i_{B2} \ll i_{C1}$ and check this assumption after solution.

If $i_{B2} \ll i_{C1}$, then $i_1 \approx i_{C1}$. CE1-KVL gives:

CE1-KVL: $15 = 10 \times 10^3 i_{C1} + v_{CE1} = 10 \times 10^3 \times 1.1 \times 10^{-3} + v_{CE1} \rightarrow v_{CE1} = 3.9$ V

Since $v_{CE1} > 0.7$ V, our assumption of Q1 in active is correct. State of Q2 can be found from BE2-KVL and CE2-KVL. Assume Q2 active: $V_{BE2} = 0.7$ V, $i_{B2} > 0$, $i_{C2} = 100 i_{B2}$, and $v_{CE2} > 0.7$ V. Then $i_{E2} \approx i_{C2}$ and:

BE2-KVL: $v_{CE1} = v_{BE2} + 10^3 i_{E2}$

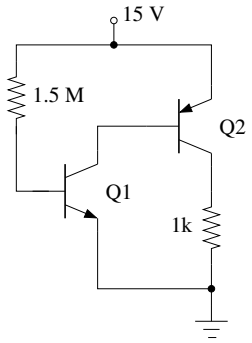
$3.9 = 0.7 + 10^3 i_{C2} \quad \rightarrow \quad i_{C2} = 3.2$ mA

CE2-KVL: $15 \approx v_{CE2} + 10^3 i_{C2} = v_{CE2} + 10^3 \times 3.2 \times 10^{-3} \quad \rightarrow \quad v_{CE2} = 11.8$ V

Since $v_{CE2} > 0.7$ V, our assumption of Q2 in active is correct. Then $i_{B2} = i_{C2}/100 = 32\ \mu$A. We note that $i_{B2} = 32\ \mu\text{A} \ll i_{C1} = 1.1$ mA. Therefore that assumption was also correct.

In sum, bot BJTs are in active and $v_{BE1} = 0.7$ V, $i_{B1} = 11\ \mu$A, $i_{C1} = 1.1$ mA, $v_{CE1} = 3.9$ V, $v_{BE2} = 0.7$ V, $i_{B2} = 32\ \mu$A, $i_{C2} = 3.2$ mA, $v_{CE2} = 11.8$ V.

Problem 10. Find i_B, v_{BE}, i_C, v_{CE}, and state of both transistors (Si BJTs with $\beta = 100$).



Note that Q2 is a PNP transistor

$$\begin{aligned} \text{BE1-KVL:} &\quad 15 = 1.5 \times 10^6 i_{B1} + v_{BE1} \\ \text{CE1-KVL \& BE2-KVL:} &\quad 15 = v_{EB2} + v_{CE1} \\ \text{CE2-KVL:} &\quad 15 = v_{EC2} + 10^3 i_{C2} \\ \text{KCL:} &\quad i_{C1} = i_{B2} \end{aligned}$$

Assume Q1 is ON, $v_{BE1} = 0.7$ V and $i_{B1} > 0$. BE1-KVL gives:

$$\text{BE1-KVL:} \quad 15 = 1.5 \times 10^6 i_{B1} + 0.7 \quad \rightarrow \quad i_{B1} = 9.5\ \mu\text{A}$$

Since $i_{B1} > 0$, our assumption of Q1 ON is correct. Also, since $i_{B2} = i_{C1} > 0$, Q2 is ON and $v_{EB2} = 0.7$ V. Then CE1-KVL gives $v_{CE1} = 14.3$ V. Since $v_{CE1} > 0.7$ V, Q1 is in active and $i_{C1} = 100 i_{B1} = 0.95$ mA.

KCL gives $i_{B2} = i_{C1} = 0.95$ mA. Assume Q2 is in active: $i_{C2} = 100 i_{B2} = 95$ mA and $v_{EC2} > 0.7$ V. CE2-KVL gives

$$\text{CE2-KVL:} \quad 15 = v_{EC2} + 10^3 i_{C2} = v_{EC2} + 10^3 \times 95 \times 10^{-3} \quad \rightarrow \quad v_{EC2} = -80\ \text{V}$$

Since $v_{EC2} = -80 < 0.7$ V, our assumption of Q2 in active is incorrect. Assume Q2 is in saturation: $v_{EC2} = 0.2$ V and $i_{C2}/i_{B2} < 100$. CE2-KVL gives:

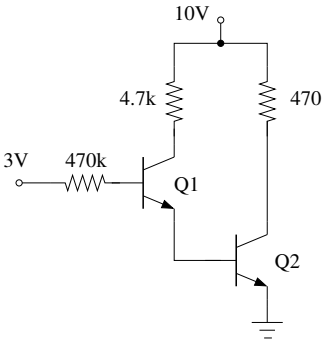
$$\text{CE2-KVL:} \quad 15 = v_{EC2} + 10^3 i_{C2} = 0.2 + 10^3 i_{C2} \quad \rightarrow \quad i_{C2} = 14.8\ \text{mA}$$

Since $i_{C2}/i_{B2} = 14.8/0.95 = 15.6 < 100$, our assumption of Q2 in saturation is correct.

In sum, Q1 is in active, Q2 is in saturation, and $v_{BE1} = 0.7$ V, $i_{B1} = 9.5\ \mu$A, $i_{C1} = 0.95$ mA, $v_{CE1} = 14.3$ V, $v_{EB2} = 0.7$ V, $i_{B2} = 0.95$ mA, $i_{C2} = 14.8.2$ mA, $v_{EC2} = 0.2$ V.

Problem 11. Find i_B, v_{BE}, i_C, v_{CE}, and state of both transistors for A) $v_i = 1$ V, B) $v_i = 3$ V, C) $v_i = 5$ V. Si BJTs with $\beta_1 = 100$ and $\beta_2 = 50$.

Note that BJTs are arranged as a Darlington pair with $i_{E1} = i_{B2}$. So they will be either both ON or both OFF.



$$\begin{aligned}
\text{BE1-KVL:} \quad & V_i = 470 \times 10^3 i_{B1} + v_{BE1} + v_{BE2} \\
\text{CE1-KVL \& BE2-KVL:} \quad & 10 = 4.7 \times 10^3 i_{C1} + v_{CE1} + v_{BE2} \\
\text{CE2-KVL:} \quad & 10 = 470 i_{C2} + v_{CE2} \\
\text{KCL:} \quad & i_{C1} = i_{B2}
\end{aligned}$$

Part A: $v_i = 1$ V.

Assume both BJTs are ON: $v_{BE1} = v_{BE2} = 0.7$ V, $i_{B1} > 0$, and $i_{B2} > 0$. BE1-KVL gives:

$$\text{BE1-KVL:} \quad 1 = 470 \times 10^3 i_{B1} + 0.7 + 0.7 \quad \rightarrow \quad i_{B1} = -0.8\ \mu\text{A}$$

Since $i_{B1} < 0$, our assumption is incorrect and both BJTs are in cut-off with $i_{B1} = i_{C1} = i_{B2} = i_{C2} = 0$. CE2-KVL gives $v_{CE2} = 10$ V. CE1-KVL gives $v_{CE1} + v_{BE2} = 10$ V. Our simple large-signal model for the BJT cannot resolve the values of v_{CE1} and v_{BE2} because any values of $v_{BE2} < 0.7$V and the corresponding value of $v_{CE1} = 10 - v_{BE2}$ will be acceptable.

The problem of not finding unique values for v_{CE1} and v_{BE2} is due to our simple diode model of the BE junction. In reality both BE junctions will be forward biased with voltages smaller than 0.7 V (so both i_B's will be very small) and BJTS will have small values of i_C's.

Part B: $v_i = 3$ V.

Assume both BJTs are ON: $v_{BE1} = v_{BE2} = 0.7$ V, $i_{B1} > 0$, and $i_{B2} > 0$. BE1-KVL gives:

$$\text{BE1-KVL:} \quad 3 = 470 \times 10^3 i_{B1} + 0.7 + 0.7 \quad \rightarrow \quad i_{B1} = 3.4\ \mu\text{A}$$

Since $i_{B1} > 0$, our assumption is correct and both BJTs are ON.

Assume Q1 in active: $i_{C1} = 100 i_{B1} = 0.34$ mA and $v_{CE1} > 0.7$ V. Then CE1-KVL gives:

$$\begin{aligned}
\text{CE1-KVL \& BE2-KVL:} \quad & 10 = 4.7 \times 10^3 i_{C1} + v_{CE1} + v_{BE2} \\
& 10 = 4.7 \times 10^3 \times 0.34 \times 10^{-3} + v_{CE1} + 0.7 \quad \rightarrow \quad v_{CE1} = 7.7\ \text{V}
\end{aligned}$$

Since $v_{CE1} = 7.7 > 0.7$ V, our assumption of Q1 in active is correct. Then, $i_{B2} = i_{E1} \approx i_{C1} = 0.34$ mA.

Assume Q2 is in active: $i_{C2} = 50 i_{B2} = 17$ mA and $v_{CE2} > 0.7$ V. Then CE2-KVL gives:

$$\text{CE2-KVL:} \quad 10 = 470 i_{C2} + v_{CE2} = 470 \times 17 \times 10^{-3} + v_{CE2} \quad \rightarrow \quad v_{CE2} = 2.01 \text{ V}$$

Since $v_{CE2} = 2.01 > 0.7$ V, our assumption of Q2 in active is correct.

Therefore, Q1 & Q2 are in active, and $v_{BE1} = v_{BE2} = 0.7$ V, $i_{B1} = 3.4$ μA, $i_{C1} = 0.34$ mA, $v_{CE1} = 7.7$ V, $i_{B2} = 0.34$ mA, $i_{C2} = 17$ mA, and $v_{CE2} = 2.01$ V.

Part C: $v_i = 5$ V.

Assume both BJTs are ON: $v_{BE1} = v_{BE2} = 0.7$ V, $i_{B1} > 0$, and $i_{B2} > 0$. BE1-KVL gives:

$$\text{BE1-KVL:} \quad 5 = 470 \times 10^3 i_{B1} + 0.7 + 0.7 \quad \rightarrow \quad i_{B1} = 7.66 \text{ } \mu\text{A}$$

Since $i_{B1} > 0$, our assumption is correct and both BJTs are ON.

Assume Q1 is in active: $i_{C1} = 100 i_{B1} = 0.77$ mA and $v_{CE1} > 0.7$ V. Then CE1-KVL gives:

$$\text{CE1-KVL \& BE2-KVL:} \quad 10 = 4.7 \times 10^3 i_{C1} + v_{CE1} + v_{BE2}$$
$$10 = 4.7 \times 10^3 \times 0.77 \times 10^{-3} + v_{CE1} + 0.7 \rightarrow v_{CE1} = 5.70 \text{ V}$$

Since $v_{CE1} = 5.70 > 0.7$ V, our assumption of Q1 in active is correct. Then, $i_{B2} = i_{E1} \approx_{C1} =$ 0.77 mA.

Assume Q2 is in active: $i_{C2} = 50 i_{B2} = 38.3$ mA and $v_{CE2} > 0.7$ V. Then CE2-KVL gives:

$$\text{CE2-KVL:} \quad 10 = 470 i_{C2} + v_{CE2} = 470 \times 38.3 \times 10^{-3} + v_{CE2} \quad \rightarrow \quad v_{CE2} = -8.0 \text{ V}$$

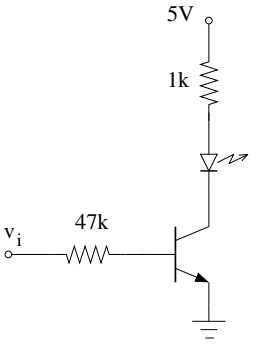
Since $v_{CE2} = -8.0 < 0.7$ V, our assumption is incorrect and Q2 is in saturation: $v_{CE2} = 0.2$ V and $i_{C2}/i_{B2} < 50$. Then CE2-KVL gives:

$$\text{CE2-KVL:} \quad 10 = 470 i_{C2} + v_{CE2} = 470 i_{C2} + 0.2 \quad \rightarrow \quad i_{C2} = 20.9 \text{ mA}$$

Since $i_{C2}/i_{B2} = 20.9/0.77 = 27 < 50$, our assumption is correct.

Therefore, Q1 is in active, Q2 is in saturation, and $v_{BE1} = v_{BE2} = 0.7$ V, $i_{B1} = 7.66$ μA, $i_{C1} = 0.77$ mA, $v_{CE1} = 5.7$ V, $i_{B2} = 0.77$ mA, $i_{C1} = 20.9$ mA, and $v_{CE2} = 0.2$ V.

Problem 12. This is a switching circuit. v_i is the output of a logic gate which turns the light-emitting diode (LED) on or off depending on the state of the logic gate. The LED is made of GaAs and has a $V_{D0} = 1.7$ V. A) Show that for $v_i = 0$, LED will be OFF, B) Show that for $v_i = 5$ V, LED will be ON, and C) If we tarting from $v_i = 0$ and slowly increase v_i, at what voltage LED starts to light up? (Si BJT with $\beta = 100$.)



BE-KVL: $v_i = 47 \times 10^5 i_B + v_{BE}$

CE-KVL: $5 = 10^3 i_C + v_D + v_{CE}$

$i_C = i_D$

Part A: $v_i = 0$:

Assume BJT is OFF, $i_B = 0$ and $v_{BE} < 0.7$ V. BE-KVL gives:

BE-KVL: $0 = 47 \times 10^3 i_B + v_{BE} = 0 + v_{BE} \quad \rightarrow \quad v_{BE} = 0$

Since $v_{BE} = 0 < 0.7$ V, our assumption of BJT in cut-off is correct and $i_C = 0$. Since $i_D = i_C = 0$, the diode will be OFF.

Part B: $v_i = 5$ V:

Assume BJT is ON, $v_{BE} = 0.7$ V, $i_B > 0$. BE-KVL gives:

BE-KVL: $5 = 47 \times 10^3 i_B + 0.7 \quad \rightarrow \quad i_B = 91.5\ \mu$A

Since $i_B > 0$ our assumption of BJT is ON is justified. When BJT is ON, $i_C > 0$ and since $i_D = i_C > 0$, the LED will be on with $v_D = 1.7$ V.

Assume BJT is in active: $i_C = \beta i_B = 100 i_B = 9.15$ mA and $v_{CE} > 0.7$ V. CE-KVL gives:

CE-KVL: $5 = 10^3 i_C + v_D + v_{CE}$

$5 = 10^3 \times 9.15 \times 10^{-3} + 1.7 + v_{CE} \quad \rightarrow \quad v_{CE} = -5.85$ V

Since $v_{CE} = -5.85 < 0.7$ V our assumption of BJT in active is NOT justified.

Assume BJT in saturation, $v_{CE} = 0.2$ V, and $i_C < \beta i_B$. CE-KVL gives:

CE-KVL: $5 = 10^3 i_C + v_D + v_{CE} = 10^3 i_C + 1.7 + 0.2 \quad \rightarrow \quad i_C = 3.1$ mA

Since $i_C / i_B = 3.1/0.0915 = 34 < 100 = \beta$, our assumption of BJT in saturation is justified.

Therefore, for $v_i = 5$ V, LED is ON, BJT is in saturation, and $v_{BE} = 0.7$ V, $v_D = 1.7$ V, $i_B = 91.5$ μA, $i_C = 3.1$ mA, and $v_{CE} = 0.2$ V.

Part C:

LED is ON when $i_D > 0$. Since $i_C = i_D > 0$, the BJT should be ON.

We found that for $v_i = 0$, BJT is in cut-off and LED is OFF. As we increase v_i and while BJT is still in cut-off, BE-KVL gives $v_{BE} = v_i$ since $i_B = 0$. So as we increase v_i, v_{BE} increases while i_B remains zero.

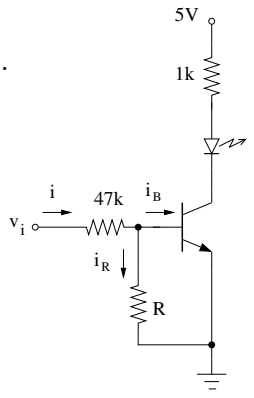
When v_i reaches 0.7 V, v_{BE} also reaches 0.7 V while i_B is still zero.

If we increase v_i beyond this point, v_{BE} cannot increase, rather i_B becomes positive and BJT will be turned ON leading to $i_C > 0$ and LED turning ON.

So, LED will light up when $v_i \geq 0.7$ V.

Problem 13. Design a switch circuit similar to problem 12 which turns an LED OFF and ON such that the LED is OFF for $v_i < 2.5$ V and is ON for $v_i > 2.5$ V. (Hint: See page 3-13 of lecture notes).

Addition of a resistor R (see circuit) will raise v_i that turns the LED ON.



In problem 12, we saw that LED will just turn ON when $v_{BE} = 0.7$ V and $i_B \approx 0$. BE-KVL gives:

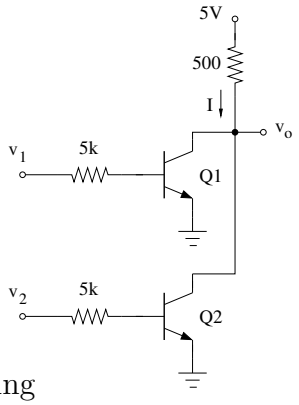
$$\text{BE-KVL:} \quad v_i = 47 \times 10^3 i + v_{BE}$$

$$2.5 = 47 \times 10^5 i + 0.7 \quad \rightarrow \quad i = 38.3 \ \mu\text{A}$$

Since $i_B = 0$, $i_R = i = 38.3$ μA. Ohm's law for the resistor R gives:

$$v_{BE} = R i_R \quad \rightarrow \quad 0.7 = 38.3 \times 10^{-6} R \quad \rightarrow \quad R = 18.3 \ \text{k}\Omega$$

Problem 14. Show that this is NOR gate with a LOW state of 0.2 V and a HIGH state of 5 V (Si BJTs with $\beta = 100$).



We first find the state of Q1 for the two cases of $V_1 = 0.2$ and 5 V.

BE1-KVL: $\quad v_1 = 500 i_{B1} + v_{BE1}$

For $v_1 = 0.2$ V, assume that Q1 is in cut-off ($i_{B1} = 0$ and $v_{BE1} < V_{D0} = 0.7$ V). Then, BE1-KVL gives $V_{BE1} = 0.2 < 0.7$ V and, thus, Q1 is indeed in cut-off. So:

$$v_1 = 0.2 \text{ V} \quad \rightarrow \quad i_{B1} = i_{C1} = 0, \quad v_{BE1} = 0.2 \text{ V}, \quad v_{CE1} \text{ can be anything}$$

For $v_1 = 5$ V, assume that Q1 is NOT in cut-off ($i_{B1} > 0$ and $v_{BE1} = V_{D0} = 0.7$ V). Substituting for $v_{BE1} = 0.7$ in BE1-KVL, we get $I_{B1} = 4.3/5,000 = 0.86$ mA. Since $i_{B1} > 0$, Q1 is indeed NOT in cut-off. Therefore,

$$v_1 = 5 \text{ V} \quad \rightarrow \quad \text{BJT is ON (not in cut-off)} \qquad i_{B1} = 0.86 \text{ mA} \quad v_{BE1} = 0.7 \text{ V} \quad i_{C1} > 0$$

Note that because the circuit is symmetric (*i.e.,* there is no difference between Q1 circuit and Q2 circuit), the above results also applies to Q2.

Case a: $v_1 = v_2 = 0.2$ V From above, both BJTs will be in cut-off and $i_{C1} = i_{C2} = 0$. By KCL, $I = i_{C1} + i_{C2} = 0$, and v_o can be found from Ohm's Law:

$$5 - v_o = 500 I = 0 \quad \rightarrow \quad v_o = 5 \text{ V}$$

Case b: $v_1 = 0.2$ V, $v_2 = 5$ V Since $v_1 = 0.2$ V, Q1 will be in cut-off with $i_{C1} = 0$. Since $v_2 = 5$ V, Q2 will not be in cut-off with $i_{B2} = 0.86$ mA. Assume Q2 is in saturation ($v_{CE2} = 0.2$ V and $i_{C2}/i_{B2} < \beta$). In this case, $v_o = v_{CE2} = 0.2$ V and $I = i_{C1} + i_{C2} = i_{C2}$. By Ohm's Law:

$$500 I = 500 i_{C2} = 5 - V_o = 5 - v_{CE2} = 4.8 \quad \rightarrow \quad i_{C2} = 4.8/500 = 9.6 \text{ mA}$$

Since $i_{C2}/i_{B2} = 11 < \beta = 100$, Q2 is indeed in saturation. So, in this case, $v_o = 0.2$ V.

Case c: $v_1 = 5$, $v_2 = 0.2$ V Because the circuit is symmetric (*i.e.,* there is no difference between Q1 circuit and Q2 circuit), results from Case b can be applied here. Thus, Q2 will be in cut-off with $i_{C2} = 0$ and Q1 will be in saturation with $i_{C1} = 9.6$ mA and $v_o = v_{CE2} = 0.2$ V.

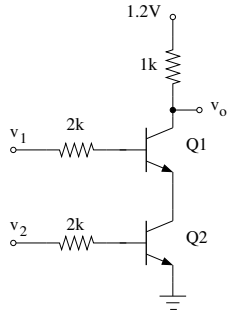
Case d: $v_1 = v_2 = 5$ V Both BJTs will be ON with $i_{B1} = i_{B2} = 0.86$ mA and $v_{BE1} = v_{BE2} = 0.7$ V. Since from the circuit, $v_{CE1} = v_{CE2}$, both BJTs will be in saturation or both in active. Assume that both are in saturation. Then, $v_o = v_{CE1} = v_{CE2} = 0.2$ V and we should have $i_{C1}/i_{B1} < \beta$ and $i_{C2}/i_{B2} < \beta$. By Ohm's Law:

$$500I = 5 - v_o = 5 - 0.2 = 4.8 \quad \rightarrow \quad I = 4.8/500 = 9.6 \text{ mA}$$

Since BJTs are identical and have same i_B, we should have $i_{C1} = i_{C2}$ and current I should be equally divided between two BJTs. Thus, $i_{C1} = i_{C2} = 0.5I = 4.8$ mA. To check if BJTs are in saturation: $i_{C1}/i_{B1} = 4.8/0.86 = 5 < \beta = 100$ and $i_{C2}/i_{B2} = 4.8/0.86 = 5 < \beta = 100$ so both BJTs are indeed in saturation and $v_o = 0.2$ V.

In summary, the output is high when both inputs are low and the output is low otherwise. Therefore, this is a NOR gate.

Problem 15. Show that this is NAND gate with a LOW state of 0.4 V and a HIGH state of 1.2 V (Si BJTs with $\beta = 200$).



	$i_{E1} = i_{c2}$
CE-KVL:	$1.2 = 10^3 i_{C1} + v_{CE1} + v_{CE2}$
	$v_o = v_{CE1} + v_{CE2} = 1.2 - 10^3 i_{C1}$
BE1-KVL:	$v_1 = 2 \times 10^3 i_{B1} + v_{BE1} + v_{CE2}$
BE2-KVL:	$v_2 = 2 \times 10^3 i_{B2} + v_{BE2}$

Case 1: $v_1 = 0.4$, $v_2 = 0.4$: Assume Q2 is off ($i_{B2} = 0$, $v_{BE2} < V_{D0}$). Substituting for $i_{B2} = 0$ in the BE2-KVL above, we get: $v_{BE2} = v_2 = 0.4 < 0.7 = V_{D0}$. Thus, Q2 is off and $i_{C2} = 0$. Since $i_{E1} = i_{C2} = 0$ and $i_{E1} = i_{C1} + i_{B1} = 0$, we should have $i_{C1} = 0$ (because $i_{C1} \geq 0$ and $i_{B1} \geq 0$) . Then, from CE-KVL above:

$$v_o = 1.2 - 10^3 i_{C1} = 1.2 \text{ V}$$

Case 2: $v_1 = 1.2$, $v_2 = 0.4$: Similar to Case 1, assume Q2 is off to find $i_{c1} = 0$ and $v_o = 1.2$ V.

Case 3: $v_1 = 0.4$, $v_2 = 1.2$: Assume Q1 is off ($i_{B1} = 0$, $v_{BE1} < V_{D0}$). Substituting for $i_{B1} = 0$ in the BE1-KVL above, we get: $v_{BE1} = 0.4 - v_{CE2}$. Since v_{CE2} cannot be negative (powered by 1.2 V),$v_{BE1} = 0.4 - v_{CE2} < 0.7 = V_{D0}$ and Q1 is off ($i_{C1} = 0$). Then:

$$v_o = 1.2 - 10^3 i_{C1} = 1.2 \text{ V}$$

Case 4: $v_1 = 1.2$, $v_2 = 1.2$: Since both inputs are high, we start by assuming that both BJTs are ON (we still need to prove it): $i_{B2} > 0$, $v_{BE2} = V_{D0} = 0.7$ V and $i_{B1} > 0$, $v_{BE1} = V_{D0} = 0.7$ V. Four possible combinations exist with Q1 and Q2 being respectively in active & active, active & saturation, saturation & active, and saturation & active. Since problem states that this is NAND gate and the low voltage is 0.4 V, a good guess is that both BJTs are in saturation $v_{CE1} = V_{sat} = 0.2$ V, $i_{C1}/i_{B1} < \beta$ and $v_{CE2} = V_{sat} = 0.2$ V, $i_{C2}/i_{B2} < \beta$.

Starting with BE1-KVL and BE2-KVL above, we get:

$$1.2 = 2 \times 10^3 i_{B2} + 0.7 \qquad \rightarrow \qquad i_{B2} = 0.25 \text{ mA}$$
$$1.2 = 2 \times 10^3 i_{B1} + 0.7 + 0.2 \qquad \rightarrow \qquad i_{B1} = 0.15 \text{ mA}$$

Since $i_{B2} > 0$, and $i_{B1} > 0$, assumption of both BJTs ON is correct. Then, CE-KVL gives:

$$1.2 = 10^3 i_{C1} + 0.2 + 0.2 \qquad \rightarrow \qquad i_{C1} = 0.8 \text{ mA}$$

Since $i_{C1}/i_{B1} = 0.8/0.15 = 5.3 < \beta = 200$, our assumption of Q1 being in saturation is justified. To find i_{C2}, we note $i_{C2} = i_{E1} = i_{C1} + i_{B1} = 0.8 + 0.15 = 0.95$ mA. Then $i_{C2}/i_{B1} = 0.95/0.25 = 3.8 < \beta = 200$, so our assumption of Tr2 being in saturation is also justified. Lastly,

$$v_o = v_{CE1} + v_{CE2} = 0.2 + 0.2 = 0.4 \text{ V}$$

Overall, $v_o = 1.2$ V or HIGH State (cases 1, 2, and 3) unless both inputs are HIGH (case 4). Therefore, this is a NAND gate.