Name PID

UNIVERSITY OF CALIFORNIA, SAN DIEGO

Electrical and Computer Engineering Department

ECE 65 – Fall 2020

Components and Circuits lab

Final Exam

You should submit your handwritten solutions in a PDF format to Gradescope by Wednesday, 12/16, at 11:00 am (Pacific Time).

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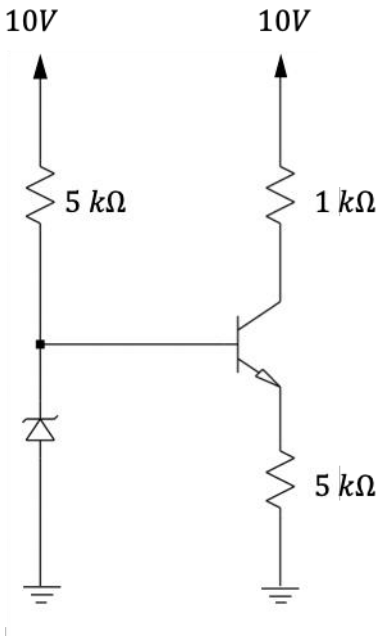
Problem 1. (5 points)

Find the node voltages and the currents in all branches in the following circuit.

Assume $V_{D0} = 0.7\,V,\ V_{sat} = 0.2\,V,\ V_z = 6.2\,V, \beta = 100$



Show your work.

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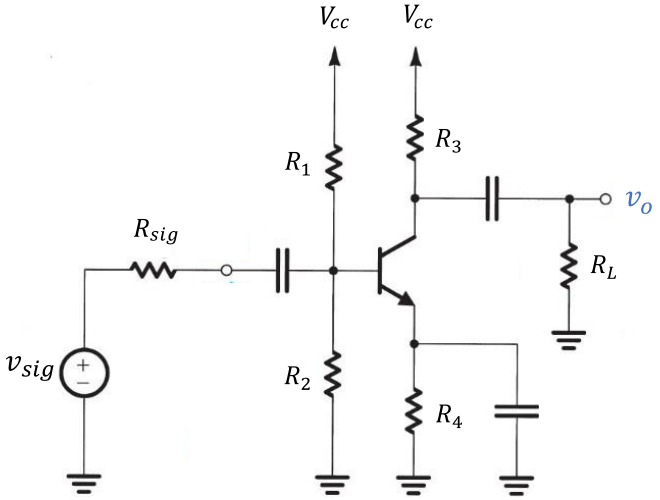
Problem 2. (10 points)

Assume

- $V_{D0} = 0.7\ V,\ V_{sat} = 0.2\ V$, and $\beta = 100$, $V_T = 26\ mV$
- The power supply available is $15\ V$.
- The output resistance of the signal source is $1\ k\Omega$ ($R_{sig} = 1\ k\Omega$) and the load resistance is $1\ k\Omega$.
- Capacitors are short in the signal circuit.
- Ignore the early effect in bias and signal circuit calculations.



Design the above amplifier circuit such that

i. The collector current is $2\ mA$.

ii. The Thevenin equivalent resistance at the base is about one tenth of R_E.

iii. The absolute value of the total gain of the amplifier ($A = \frac{v_o}{v_{sig}}$) is at least 10 V/V.

In your answers, make sure to include

a) All the resistor values.

b) All the DC node voltages.

c) The total gain of the amplifier.

d) Choose a sinusoidal signal with f = 1 kHz and sketch both v_{sig} and v_o. Make sure that the peak amplitude of v_π does not exceed 5 mV and the BJT stays in the active region.

Show your work. This is a design problem, so there are multiple answers for this problem.