ECE 65: Components & Circuits Lab

Lecture 15

CMOS introduction and transfer function

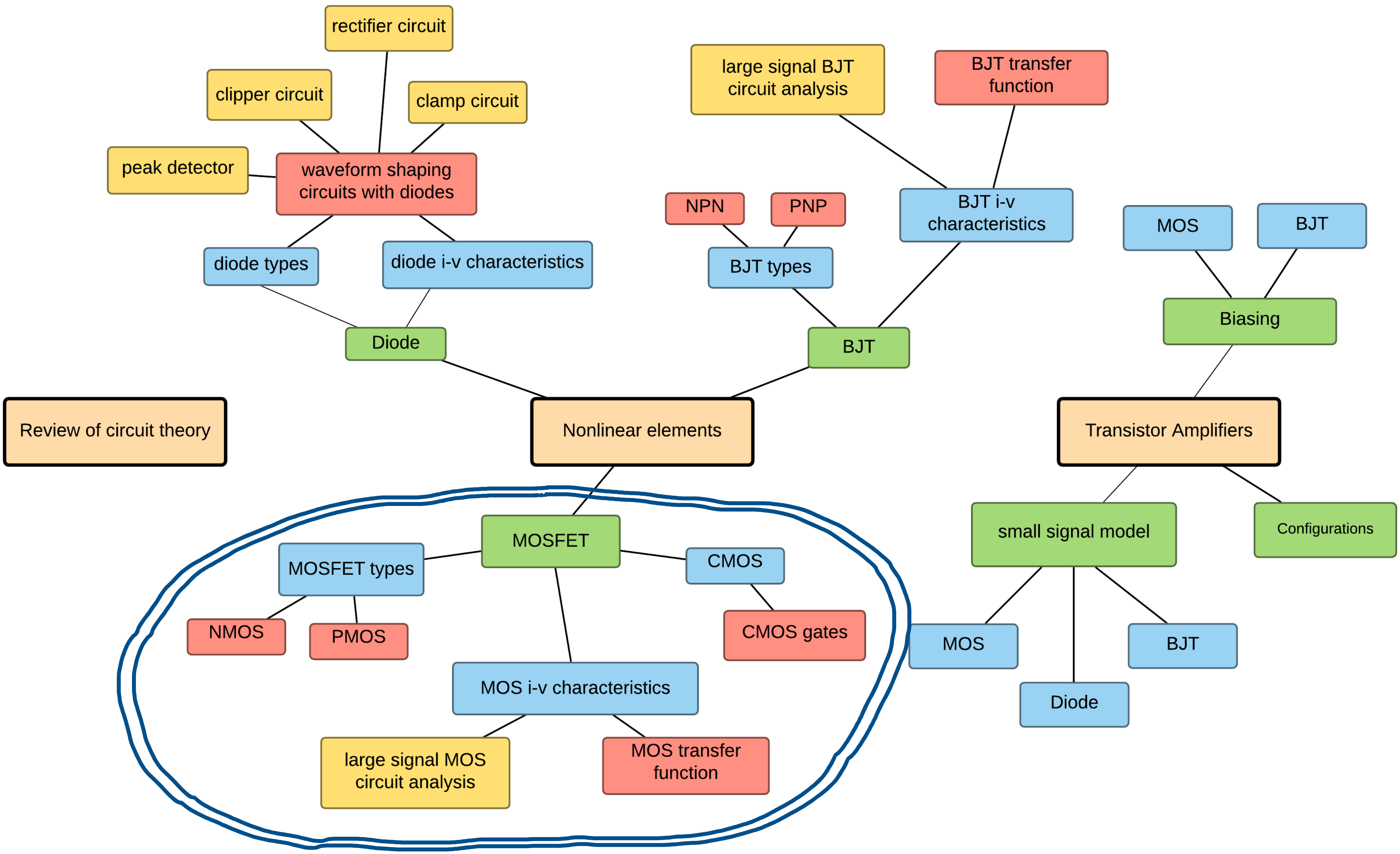
Reference notes: sections 4.4

Sedra & Smith (7th Ed): sections 5.1.8, 14.3

Saharnaz Baghdadchi

Course map

4. Metal Oxide Semiconductor Field Effect Transistor (MOSFET)



The case of $\boldsymbol{i_D = 0}$

When MOS is in cut-off, $i_D = 0$. However, $i_D = 0$, does not mean that MOS is in cut-off.

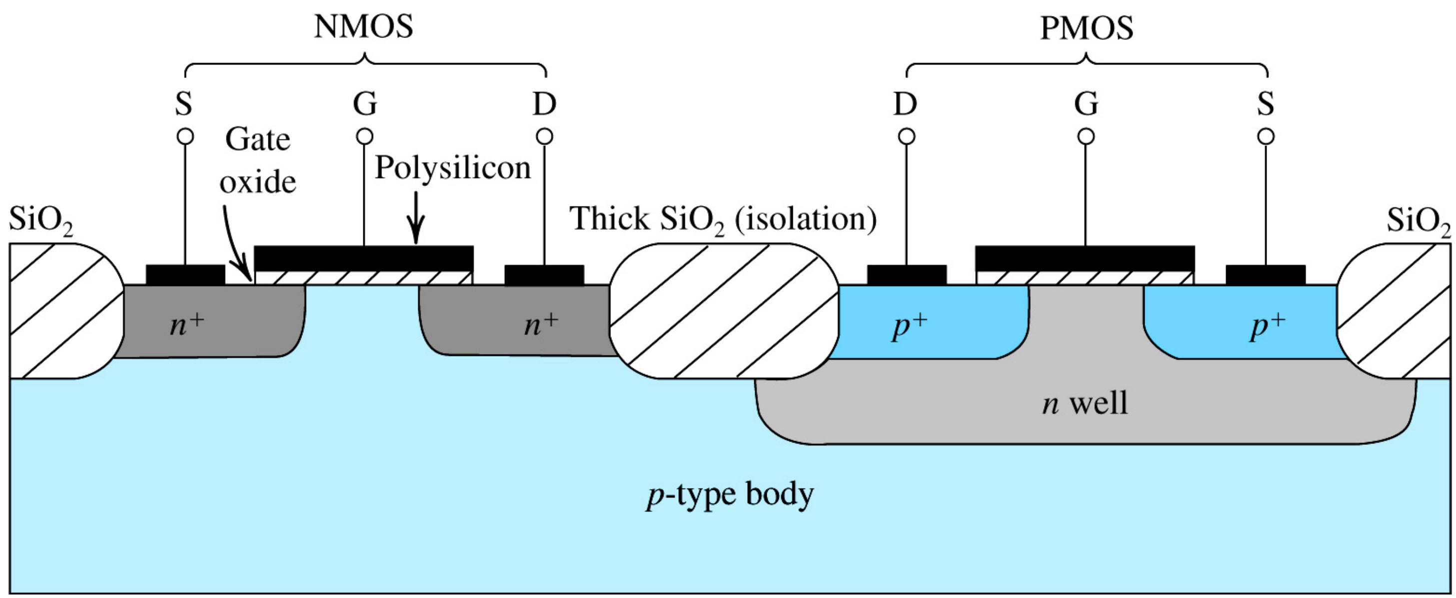
Assume that a MOS is in triode.

MOS ON: $V_{OV} > 0$ and $v_{DS} \leq V_{OV}$

Condition of $i_D = 0$ gives:

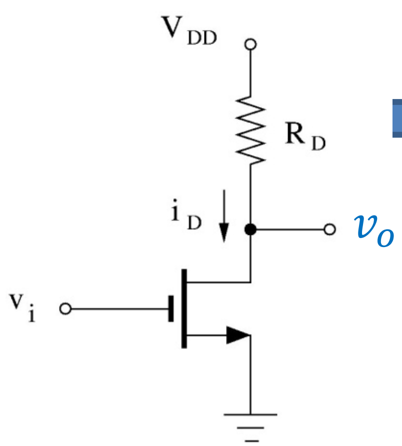
$$i_D = 0.5\mu_n C_{ox}\frac{W}{L}[2V_{OV}v_{DS} - v_{DS}^2] = 0 \quad \rightarrow v_{DS} = 0$$

Complementary MOS (CMOS) is based on NMOS/PMOS pairs



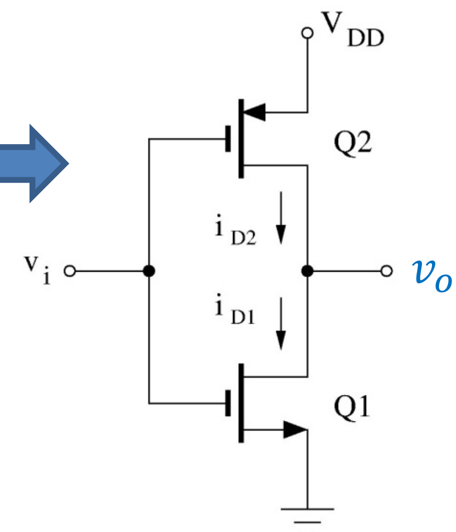
CMOS Inverter

NMOS Inverter



Replace R_D with a PMOS

CMOS Inverter



Low State: 0, High State: V_{DD}

- Maximum signal swing

Zero "static" power dissipation ($i_D = 0$ in each state).

The case of $i_D = 0$

Assume that a MOS is in saturation.

MOS ON: $V_{OV} > 0$ and $v_{DS} \geq V_{OV}$

Condition of $i_D = 0$ gives:

$$i_D = 0.5\mu_n C_{ox}\frac{W}{L}(V_{OV})^2 = 0 \quad \rightarrow V_{OV} = 0$$ Not valid

i_D can be zero if a MOS is in the triode mode **and** v_{DS} = 0.

Analysis of CMOS Inverter

Circuit equations:

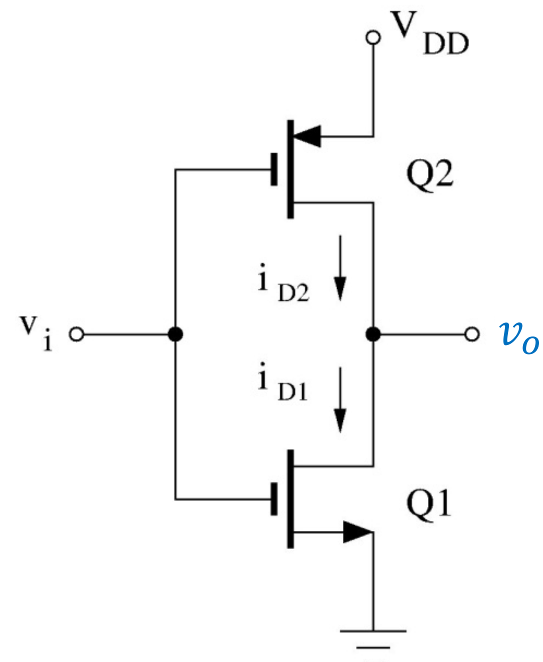
GS1 KVL: $v_{GS1} = v_i$

GS2 KVL: $V_{DD} = v_{SG2} + v_i$

DS1&2 KVL: $V_{DD} = v_{SD2} + v_{DS1}$

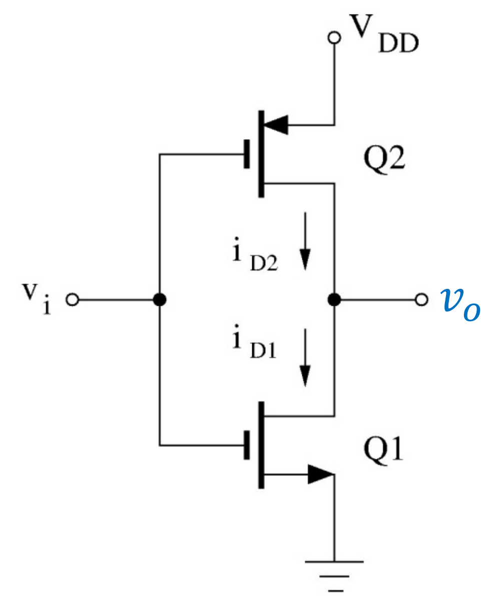
KCL: $i_{D1} = i_{D2}$

$$v_o = v_{DS1} = V_{DD} - v_{SD2}$$



Analysis of CMOS Inverter

Case 1: $\boldsymbol{v_i = 0}$



$v_{GS1} = v_i < V_{tn}$ $\rightarrow$ Q1 is OFF $\rightarrow$ $i_{D1} = 0$

$i_{D1} = 0 \rightarrow i_{D2} = 0$

$V_{DD} = v_{SG2} + v_i \rightarrow v_{SG2} = V_{DD} > |V_{tp}| \rightarrow$ Q2 is ON

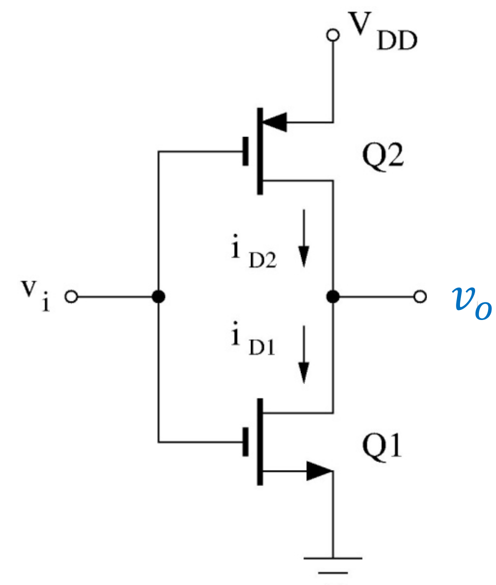
Q2 is ON and $i_{D2} = 0 \rightarrow$ Q2 is in Triode and $v_{SD2} = 0$.

For $\boldsymbol{v_i = 0}$ **,** $\boldsymbol{v_o = V_{DD} - v_{SD2} = V_{DD}}$ **, and (**$\boldsymbol{i_{D1} = 0, i_{D2} = 0}$ **)**

Gate remains in this state as long as $\boldsymbol{v_i < V_{tn}}$ **(Q1 OFF)**

Analysis of CMOS Inverter

Case 2: $\boldsymbol{v_i = V_{DD}}$



$v_{SG2} = V_{DD} - v_i = 0 < |V_{tp}| \;\rightarrow\;$ Q2 is OFF $\rightarrow\; i_{D2} = 0$

$i_{D2} = 0 \;\rightarrow\; i_{D1} = 0$

$v_{GS1} = v_i = V_{DD} > V_{tn} \qquad \rightarrow\;$ Q1 is ON

Q1 is ON and $i_{D1} = 0 \;\rightarrow\;$ Q1 is in Triode and $v_{DS1} = 0.$

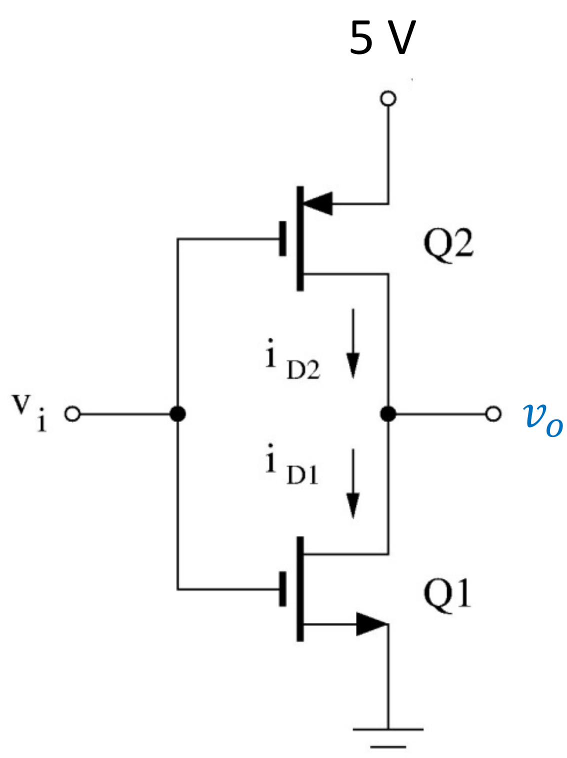
For $\boldsymbol{v_i = V_{DD},\; v_o = v_{DS1} = 0}$ and $\boldsymbol{(i_{D1} = 0,\, i_{D2} = 0\,)}$

Gate remains in this state as long as $\boldsymbol{v_i > V_{DD} - |V_{tp}|}$, (Q2 OFF)

CMOS transfer function example

In the below circuit, find v_i and i_D when both NMOS and PMOS are in saturation. What is the range of v_o in this case?

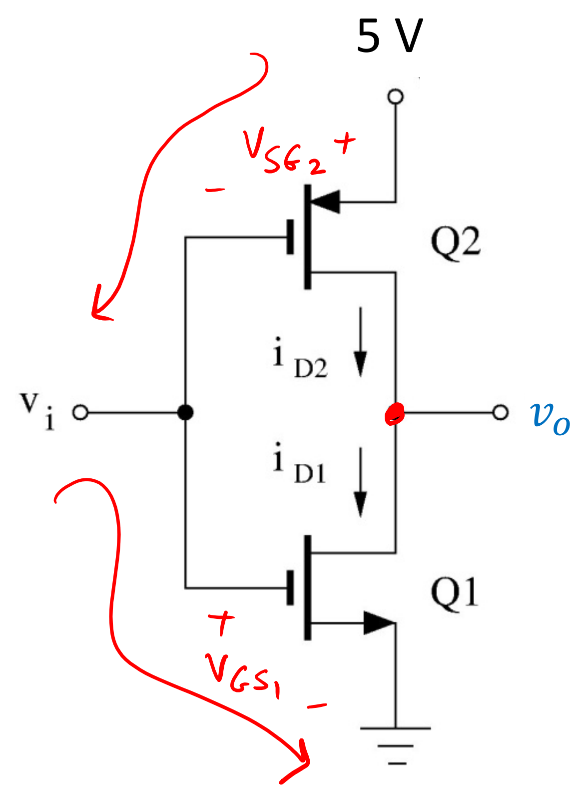
$V_{tn} = |V_{tp}| = 1\,V$, $k_n = k_p = 1\,mA/V^2$, $\lambda = 0$.



KCL at the output node: $i_{D1} = i_{D2}$

$v_{GS1} = v_i$

$v_{SG2} = 5 - v_i$



Let's first find the range of v_i for which Q1 or Q2 are off.

Q1 off : $v_{GS1} < V_{tn}$, $i_{D1} = 0$

$V_{tn} = |V_{tp}| = 1\,V \qquad v_{GS1} = v_i \rightarrow v_i < 1\,V$

$i_{D1} = i_{D2} = 0$

$v_{SG2} = 5 - v_i \rightarrow v_i = 5 - v_{SG2} < 1\,V \rightarrow v_{SG2} > 4\,V$

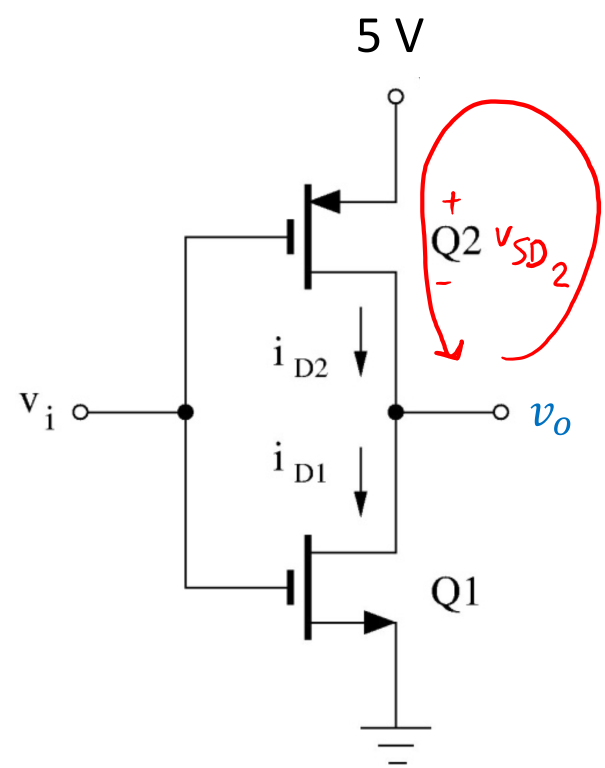
$v_{SG2} > |V_{tp}| \rightarrow$ Q2 is ON

Q2 is ON and $i_{D2} = 0$ → $v_{SD2} = 0$ and Q2 is in Triode mode.

KCL at the output node: $i_{D1} = i_{D2}$

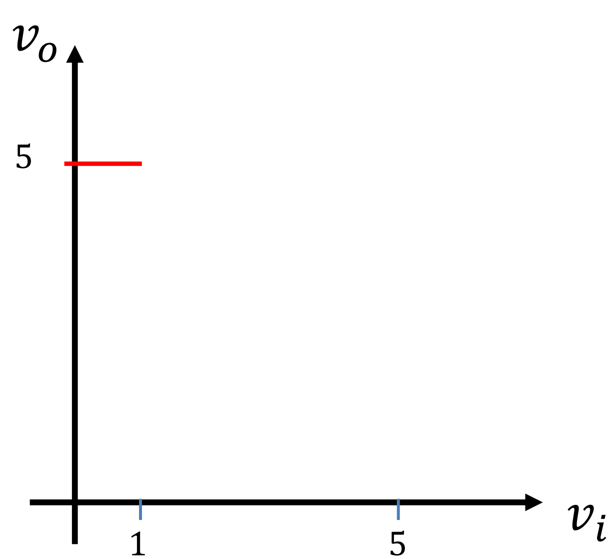
$v_{GS1} = v_i$

$v_{SG2} = 5 - v_i$



For $v_i < 1\ V$, Q1 is off and Q2 is in Triode-mode.

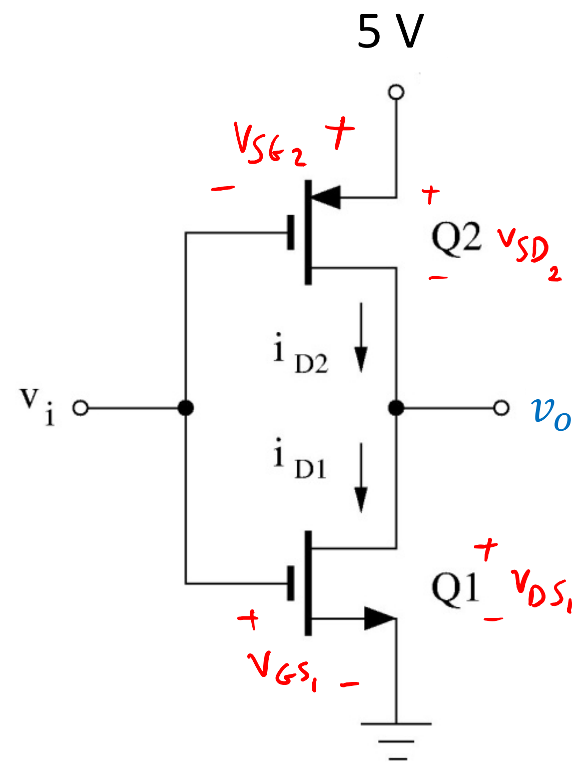
$$v_o = 5 - v_{SD2} = 5\ V$$



KCL at the output node: $i_{D1} = i_{D2}$

$\boxed{v_{GS1} = v_i}$

$\boxed{v_{SG2} = 5 - v_i}$



Q2 off : $v_{SG2} < |V_{tp}|,\ i_{D2} = 0$

$$V_{tn} = |V_{tp}| = 1\ V$$

$$v_{SG2} = 5 - v_i < 1\ V \ \rightarrow v_i > 4\ V$$

$$i_{D1} = i_{D2} = 0$$

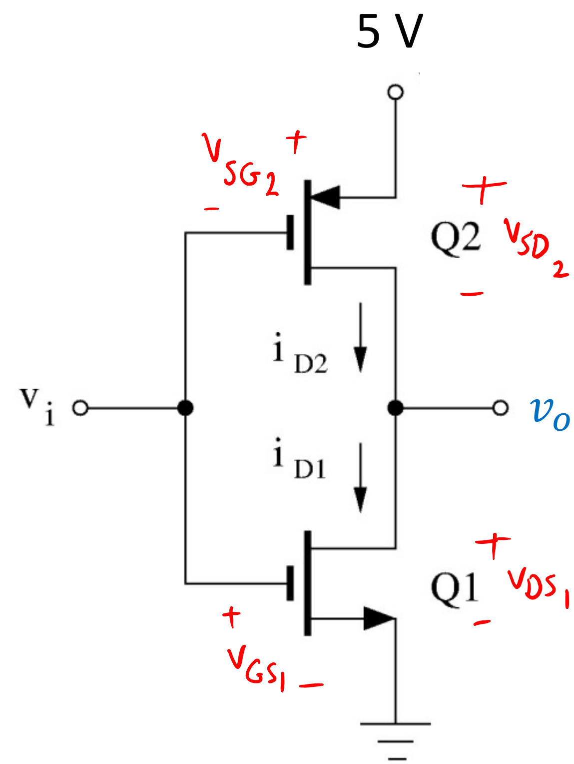
$v_{GS1} = v_i > 4\ V \ \rightarrow \ v_{GS1} > V_{tn} \rightarrow$ Q1 is ON

Q1 is ON and $i_{D1} = 0 \rightarrow v_{DS1} = 0$ and Q1 is in Triode mode.

KCL at the output node: $i_{D1} = i_{D2}$

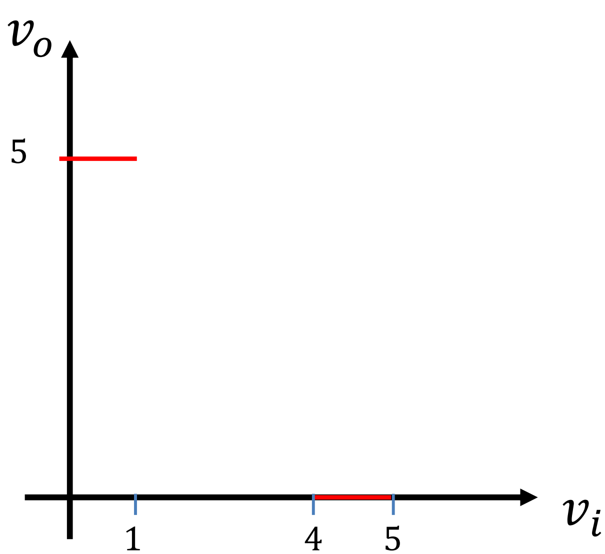
$v_{GS1} = v_i$

$v_{SG2} = 5 - v_i$



For $v_i > 4\ V$, Q2 is off and Q1 is in Triode-mode.

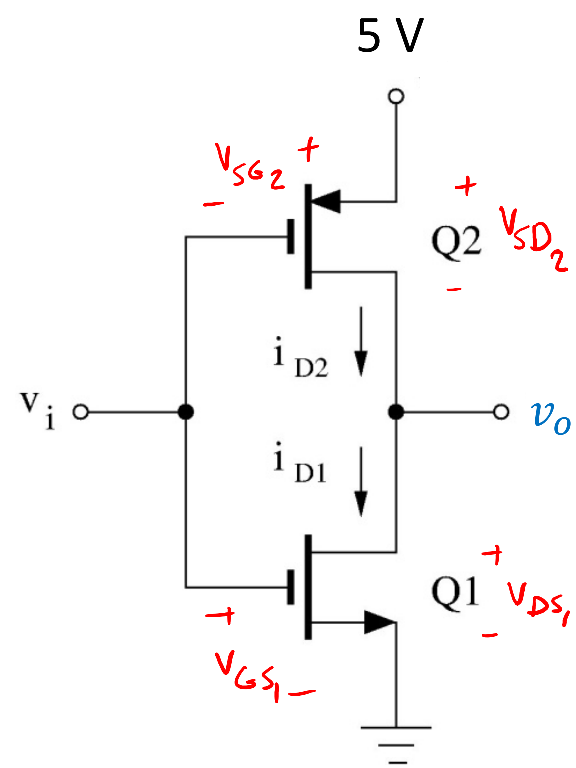
$v_o = 0$



KCL at the output node: $i_{D1} = i_{D2}$

$v_{GS1} = v_i$

$v_{SG2} = 5 - v_i$



When both Q1 and Q2 are in saturation:

$$i_{D1} = \frac{1}{2} k_n (V_{OVn})^2$$

$$i_{D2} = \frac{1}{2} k_p \left(V_{OVp}\right)^2$$

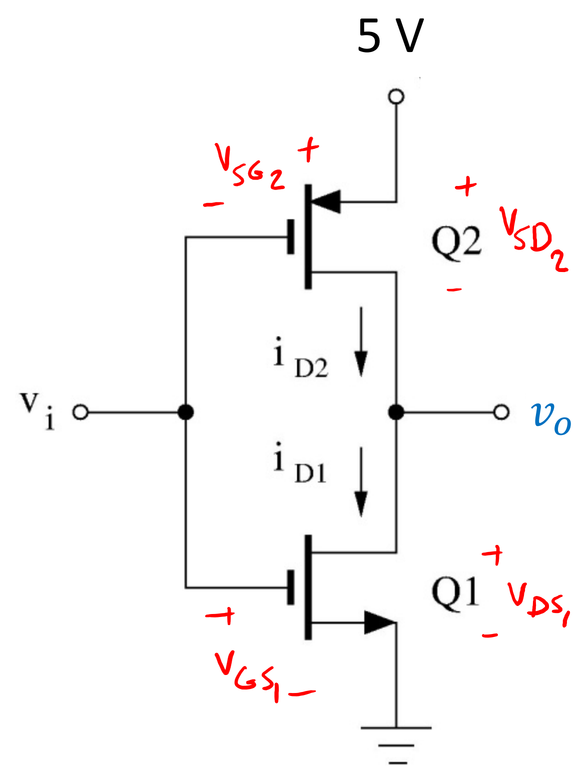
$$v_{DS1} > V_{OVn}$$

$$v_{SD2} > V_{OVp}$$

KCL at the output node: $i_{D1} = i_{D2}$

$v_{GS1} = v_i$

$v_{SG2} = 5 - v_i$



When both Q1 and Q2 are in saturation:

$$V_{OVn} = v_i - V_{tn} = v_i - 1$$

$$V_{OVp} = 5 - v_i - |V_{tp}| = 4 - v_i$$

$$i_{D1} = i_{D2} \rightarrow \frac{1}{2} \times 1 \times (v_i - 1)^2 = \rightarrow \frac{1}{2} \times 1 \times (4 - v_i)^2$$

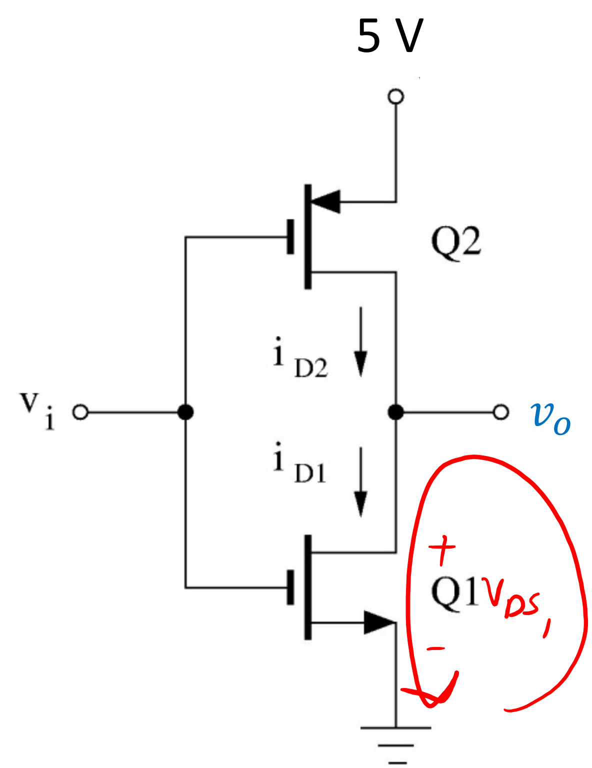
$$v_i = 2.5\ V$$

$$i_{D1} = i_{D2} = 1.125\ mA$$

KCL at the output node: $i_{D1} = i_{D2}$

$v_{GS1} = v_i$

$v_{SG2} = 5 - v_i$



When both Q1 and Q2 are in saturation:

$v_{DS1} > V_{OVn}$

$V_{OVn} = v_{GS1} - V_{tn}$

$v_{GS1} = v_i = 2.5\ V \ \rightarrow V_{OVn} = 1.5\ V$

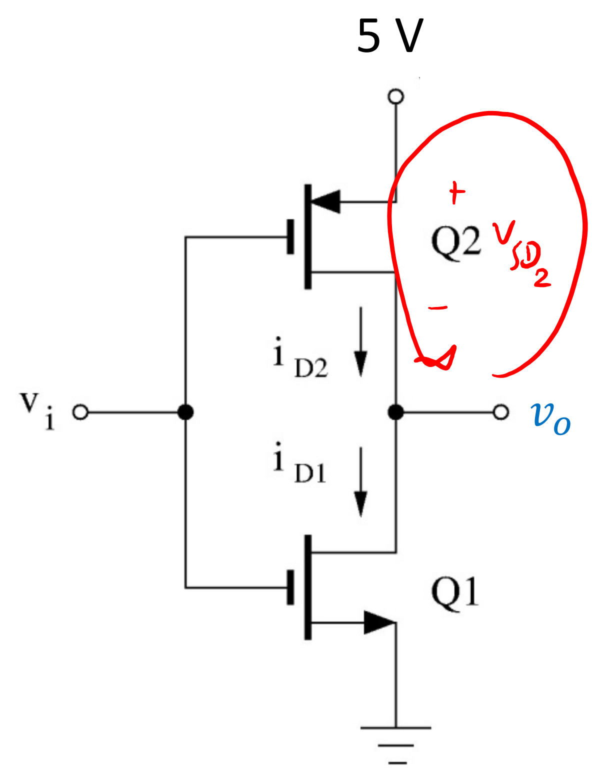
$v_{DS1} > 1.5\ V$

$v_o = v_{DS1} \quad \rightarrow \quad v_o > 1.5\ V$

KCL at the output node: $i_{D1} = i_{D2}$

$v_{GS1} = v_i$

$v_{SG2} = 5 - v_i$



When both Q1 and Q2 are in saturation:

$v_{SD2} > V_{OVp}$

$V_{OVp} = v_{SG2} - |V_{tp}|$ and $v_i = 2.5\ V$

$v_{SG2} = 5 - v_i = 2.5\ V \rightarrow V_{OVp} = 1.5\ V$

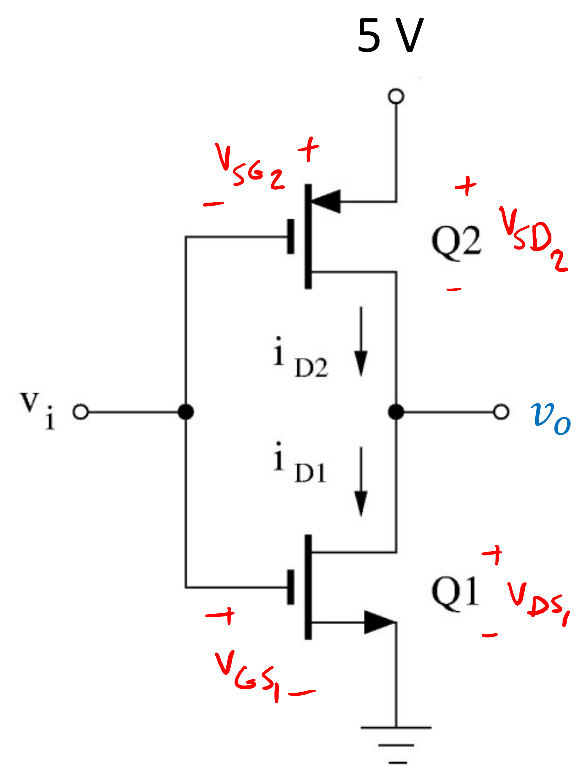
$v_{SD2} > 1.5\ V$

$v_o = 5 - v_{SD2} \rightarrow v_o < 3.5\ V$

KCL at the output node: $i_{D1} = i_{D2}$

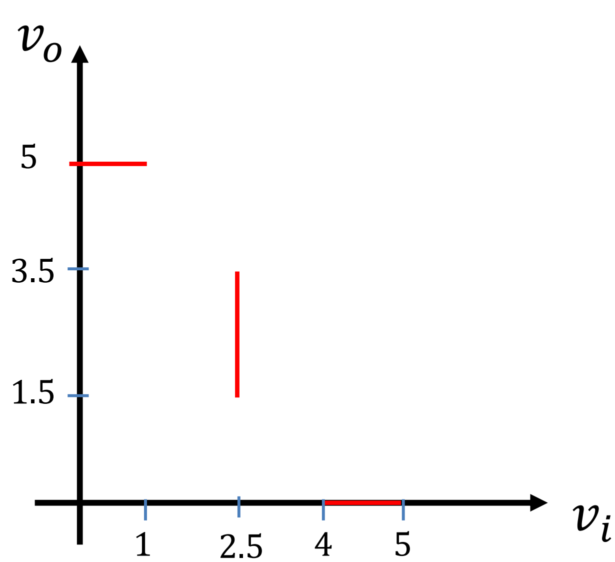
$v_{GS1} = v_i$

$v_{SG2} = 5 - v_i$



For $v_i = 2.5\ V$, Q1 and Q2 are in saturation.

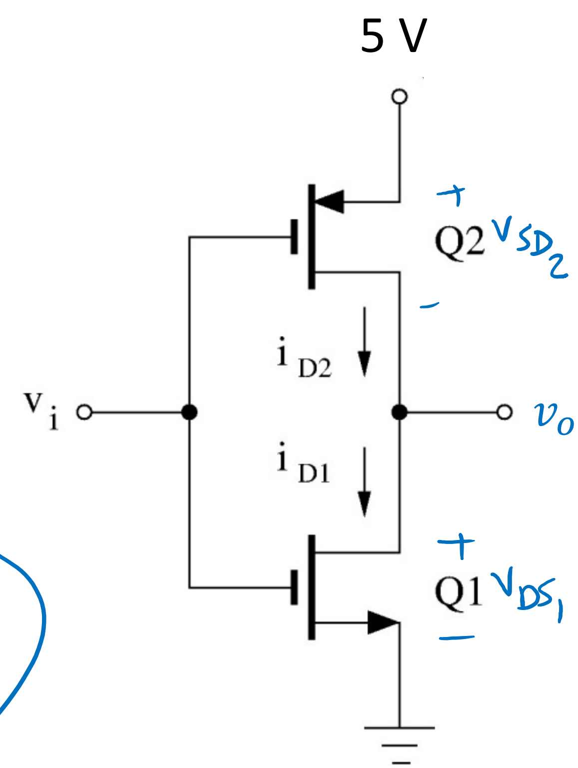
$$1.5 < v_o < 3.5\ V$$



KCL at the output node: $i_{D1} = i_{D2}$

$v_{GS1} = v_i$

$v_{SG2} = 5 - v_i$

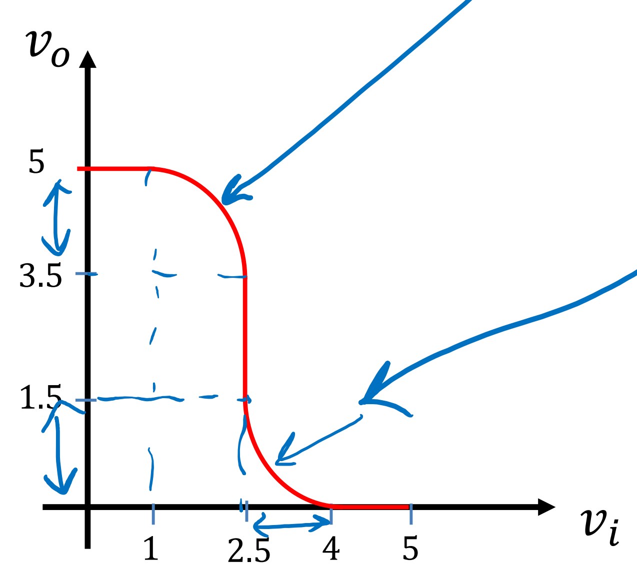


For $1\ \mathrm{V} < v_i < 2.5\ V$, Q1 is in saturation and Q2 is in triode.

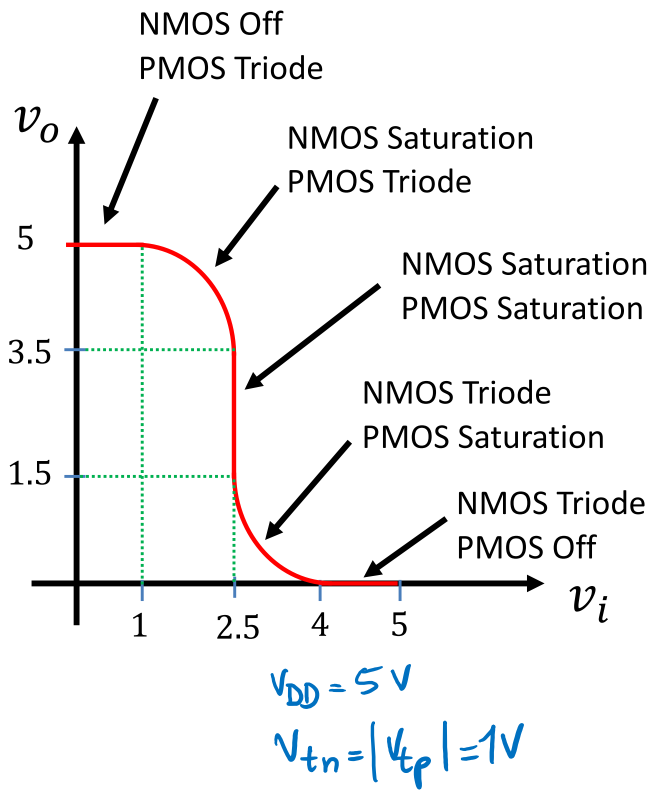
$3.5 < v_o < 5\ V$

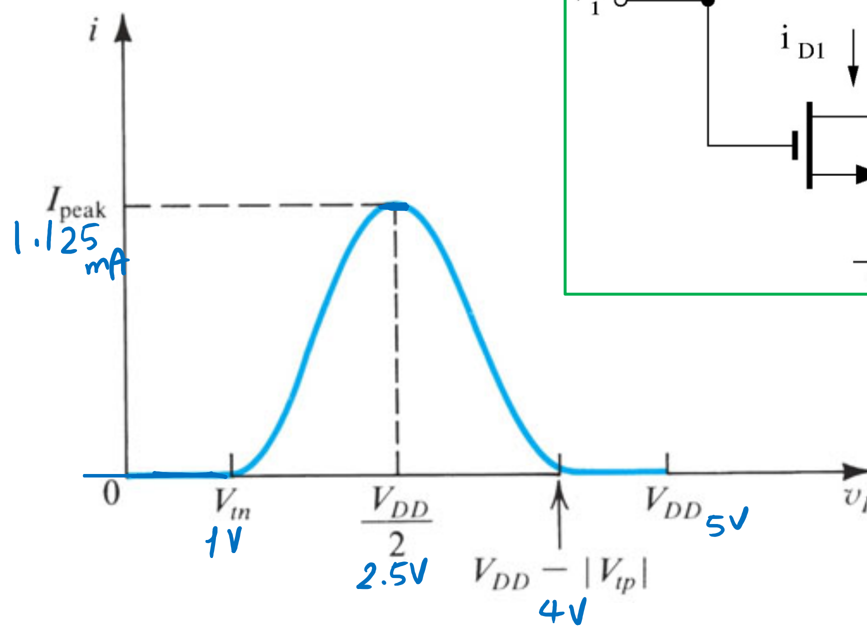
For $2.5\ \mathrm{V} < v_i < 4\ V$, Q2 is in saturation and Q1 is in triode.

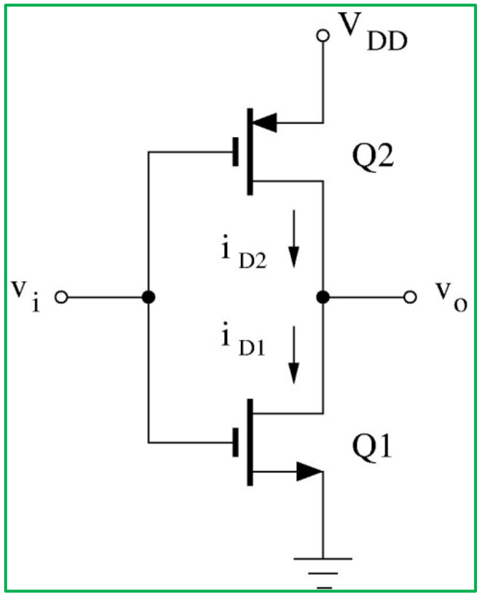
$0 < v_o < 1.5$ V



Transfer function of a CMOS inverter







Transfer function is "symmetric" for matched transistors:
$V_{tn} = |V_{tp}|$ & $\mu_n(W/L)_n = \mu_p(W/L)_p$

During transition from one state to another, $i_D > 0$

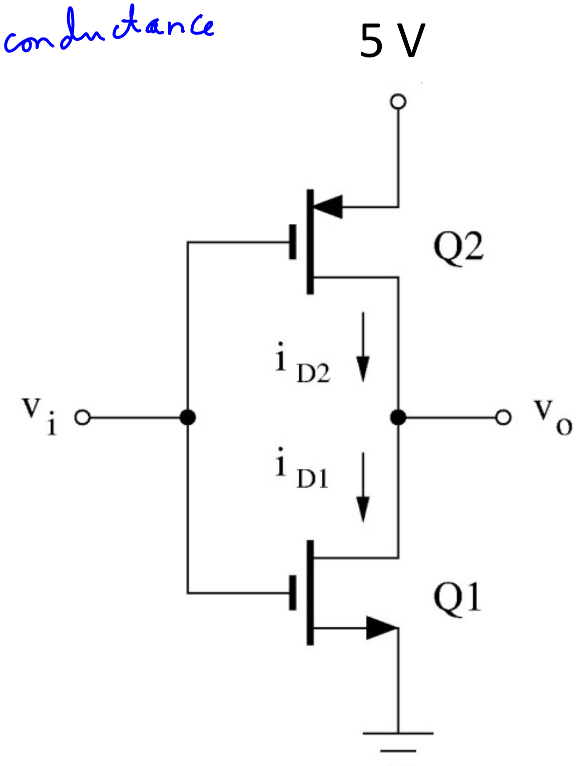
Lecture 15 reading quiz

In the circuit below, find V_i and i_D when both NMOS and PMOS are in saturation. What is the range of V_o in this case?

$V_{tn} = 1\,V$, $V_{tp} = -1\,V$ and $k_n = \mu_n C_{ox}\,(W/L)_n = 1\,mA/V^2$,

transconductance

$k_p = \mu_p C_{ox}\,(W/L)_p = 0.4\,mA/V^2$. $\lambda = 0$.



Q_2 : PMOS ,

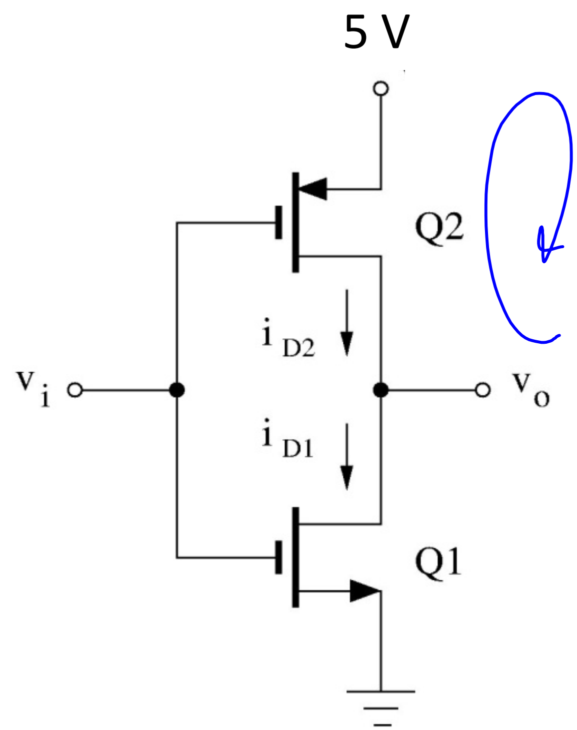
$V_{ovp} = 5 - V_i - 1 = 4 - V_i$

Q_1 : NMOS :

$V_{ovn} = V_i - 1$

$i_{D_1} = i_{D_2}$

Lecture 15 reading quiz



$i_{D_1} = \frac{1}{2} k_n V_{ov_n}^2$ ✓

$i_{D_2} = \frac{1}{2} k_p V_{ov_p}^2$ ✓ , $i_{D_1} = i_{D_2}$

$$\frac{1}{2} \times 1 \times (V_i - 1)^2 = \frac{1}{2} \times 0.4 \times (4 - V_i)^2$$

$\Longrightarrow V_i = 2.16\ V$

$i_D = 0.675\ mA$

For NMOS to be in saturation $V_{DS_1} > V_{ov_n}$, $V_0 = V_{DS_1}$

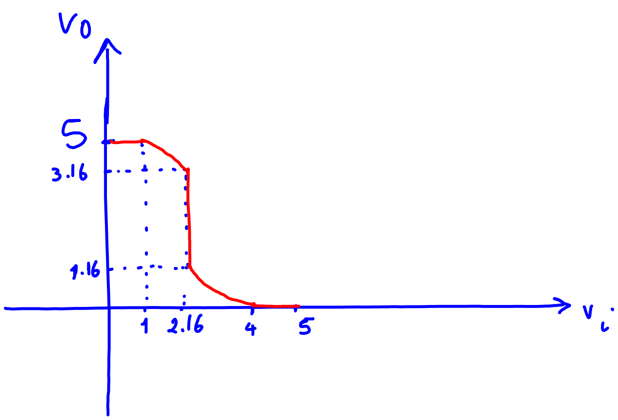
$V_0 > V_{ov_n}$, $V_{ov_n} = 1.16\ V \longrightarrow V_0 > 1.16\ V$

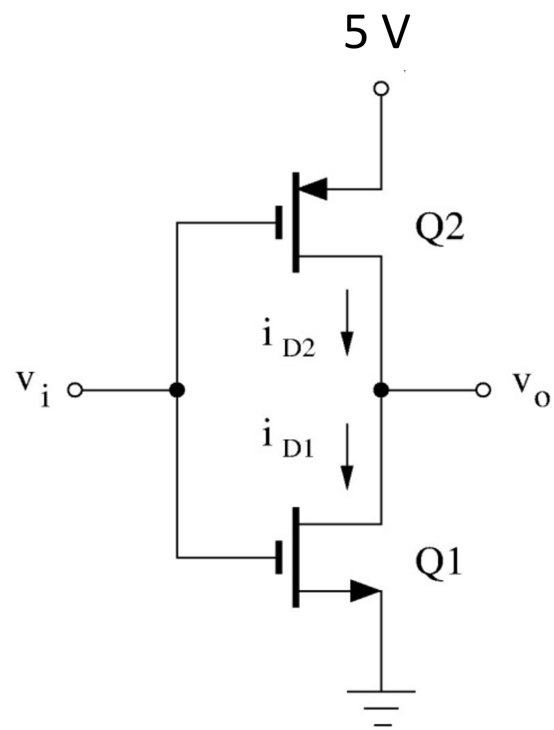
For PMOS to be in saturation: $V_{SD_2} > V_{ov_p}$, $V_0 = 5 - V_{SD_2}$

$5 - V_0 > 1.84 \longrightarrow V_0 < 3.16\ V$

Lecture 15 reading quiz

Transfer function



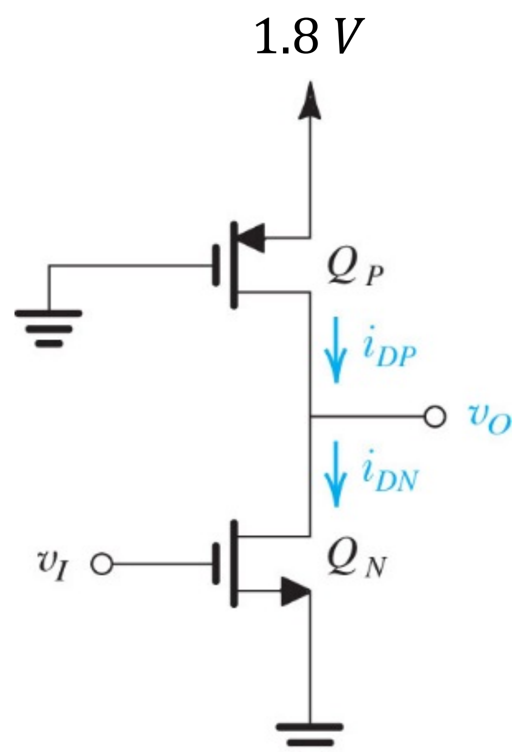


Discussion question 1. (Pseudo-NMOS inverter)

In the circuit below, find v_o for $v_I = 0$ and $v_I = 1.8\ V$.

The transistor parameters are matched $V_{tn} = |V_{tp}| = 0.4\ V$, and

$k_n = 0.3\ mA/V^2$, $k_p = 0.2\ k_n$, $\lambda = 0$.



$v_I = v_{GS1} = 0 \rightarrow Q_N$ is Off $\rightarrow$ $i_{DN} = 0$

$i_{DN} = i_{DP} = 0$

$v_{SG2} = 1.8\ V > |V_{tp}| \rightarrow Q_P$ is ON

Q_P is ON **and** $i_{DP} = 0 \rightarrow v_{SD2} = 0$

$v_{SD2} = 0 \rightarrow v_o = 1.8\ V$

Discussion question 1. (Pseudo-NMOS inverter)

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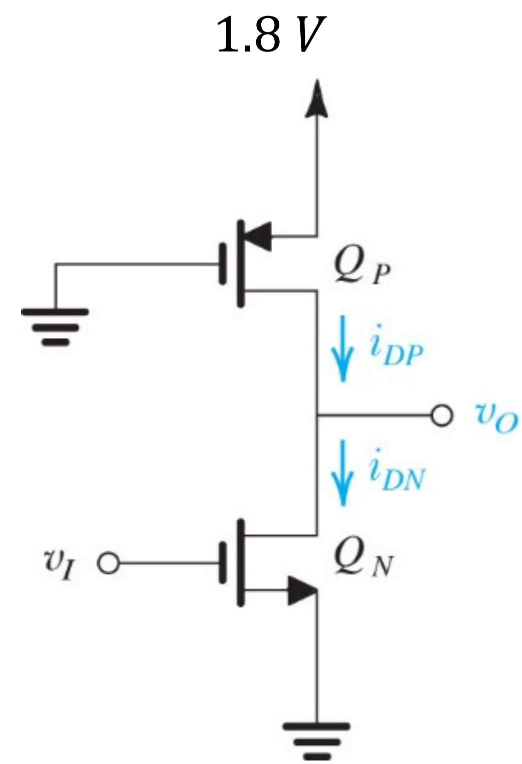

$v_I = v_{GS1} = 1.8\,V$ → Q_N is On

$v_{SG2} = 1.8\,V > |V_{tp}|$ → Q_P is ON

Because this is an inverter, we expect a low output when input is high, and since the output is equal to v_{DS1}, we expect to get a low value for v_{DS1} when $v_I = 1.8\,V$. We also know that when NMOS operates in triode, $v_{DS1} < v_{OVn} = 1.4\,V$, so most probably the low output (small v_{DS1}) will be less than 1.4V, so we assume triode region for Q_N .

Also, $v_{SD2} = 1.8 - v_{DS1}$. With small v_{DS1}, v_{SD2} will probably be a large value close to 1.8 V. v_{SD2} is likely greater than $v_{OVp} = 1.4\,V$, so PMOS probably operates in saturation.

Discussion question 1. (Pseudo-NMOS inverter)

In the circuit below, find v_o for $v_I = 0$ and $v_I = 1.8\,V$.

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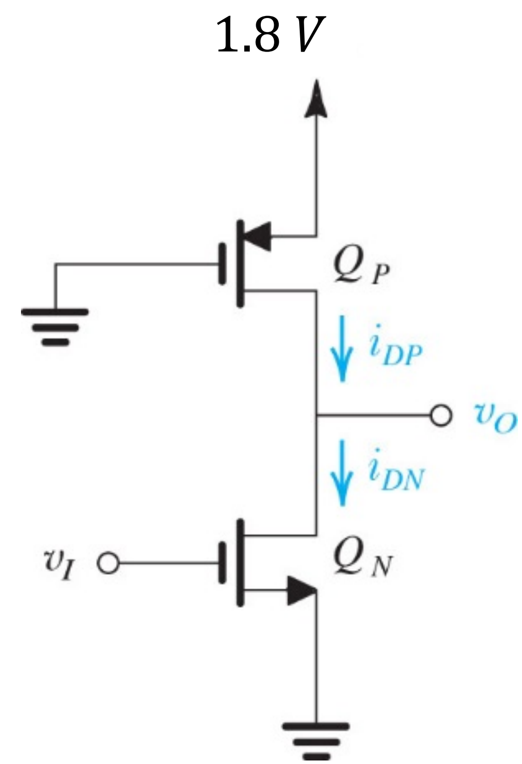

$v_I = v_{GS1} = 1.8\,V \rightarrow Q_N$ is On

$v_{SG2} = 1.8\,V > |V_{tp}| \rightarrow Q_P$ is ON

Assume Q_N is in <u>triode</u> and Q_P is in <u>saturation</u>.

$i_{DN} = i_{DP}$

$$\frac{1}{2}\,k_n[2(v_{GS1} - V_{tn})v_{DS1} - v_{DS1}^2] = \frac{1}{2}\,k_p\,(V_{DD} - |V_{tp}|)^2$$

$v_o = 0.15\,V$

$$\begin{cases} v_{SD2} = 1.8\ - 0.15\,V = 1.65\,V > V_{OVp} \\ v_{DS1} = 0.15 < V_{OVn} \end{cases}$$

Assumption was correct.