

# **ECE 65: Components & Circuits Lab**

## **Lecture 21**

### **Characterization of transistor amplifiers & Transistor amplifier configurations**

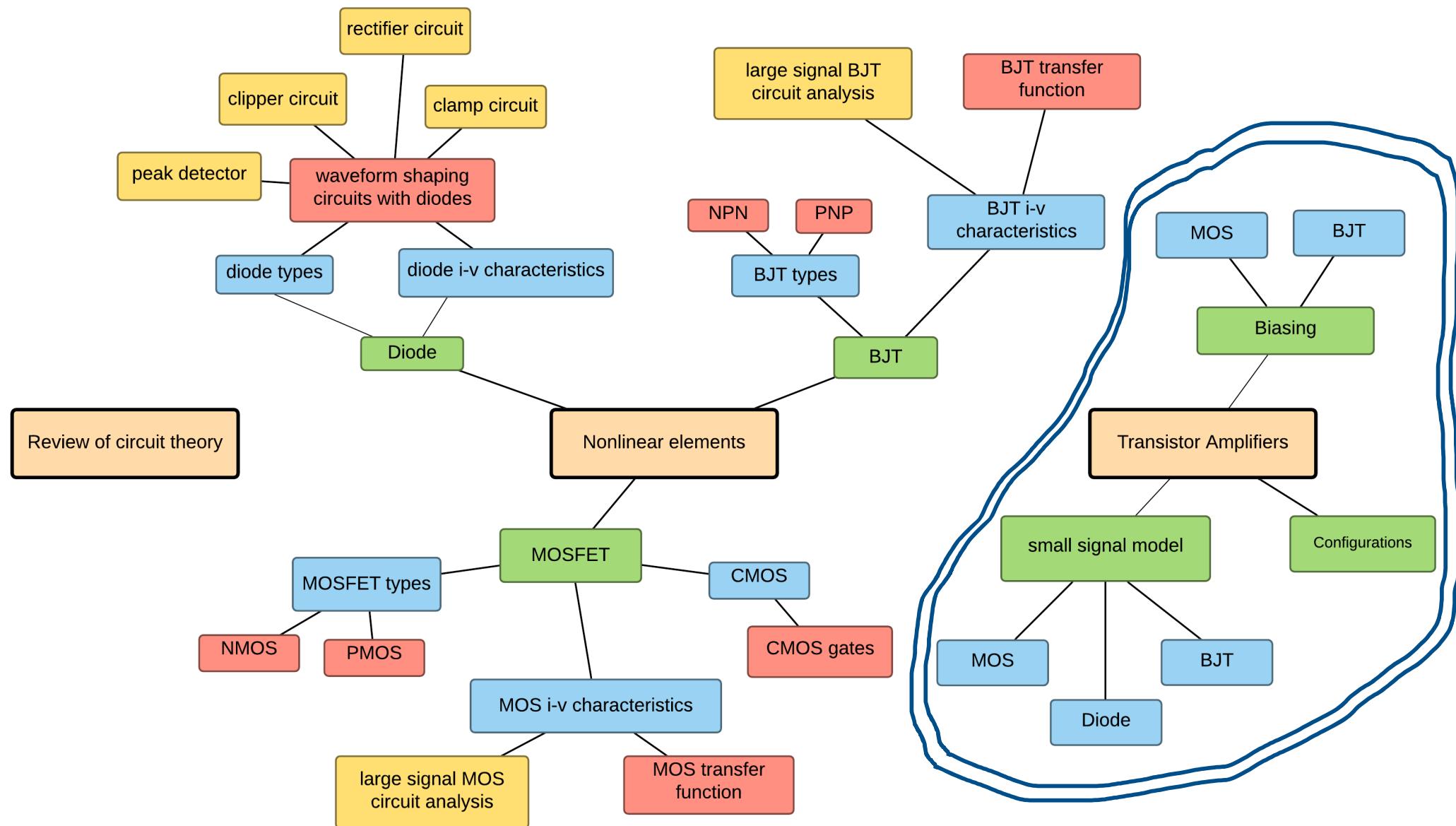
Reference notes: sections 6.1, 6.2

Sedra & Smith (7<sup>th</sup> Ed): sections 7.3

Saharnaz Baghdadchi

# Course map

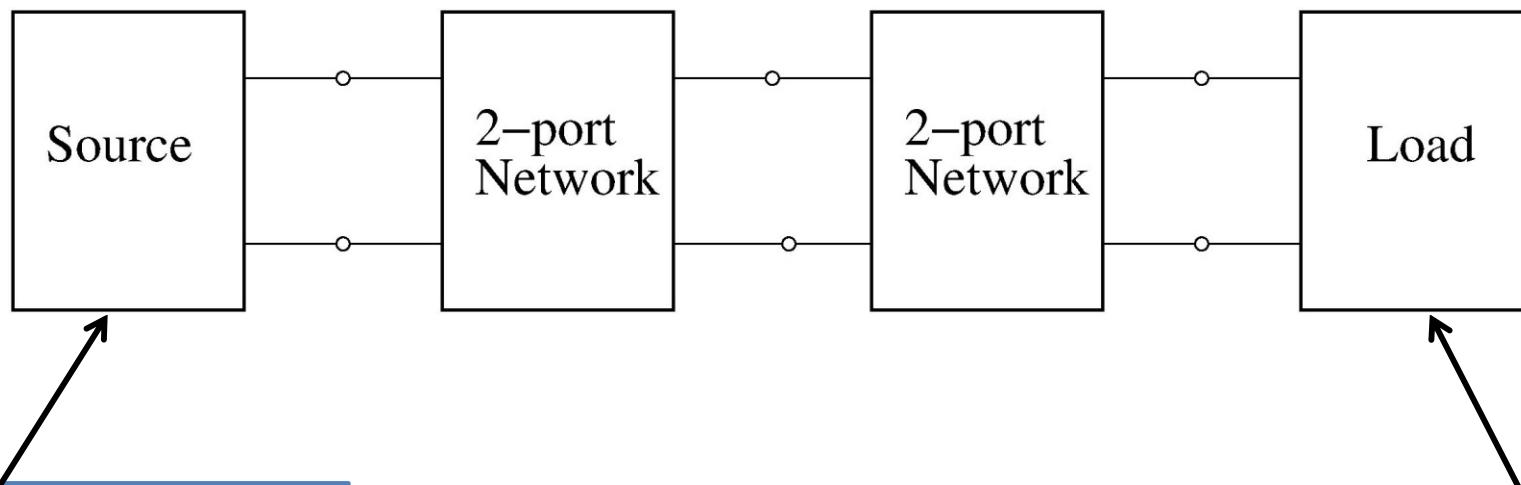
## 6. Transistor Amplifier Configurations



# **Characterization of Transistor Amplifiers**

**A typical analog circuit contains  
a load and a source (two-terminal networks)  
and several two-port networks**

**We divide the circuit into building blocks to  
simplify analysis and design**



Two-terminal network  
containing an  
independent source

Two-terminal network  
containing NO  
independent source

# What are the amplifier parameters?

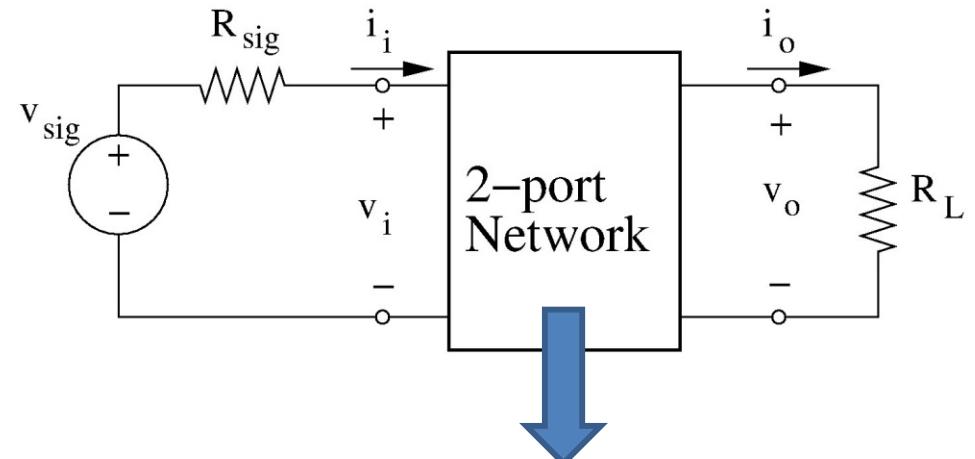
Voltage Gain of the Circuit:  $A = \frac{v_o}{v_{sig}}$

Voltage Gain of the Amplifier:  $A_v = \frac{v_o}{v_i}$

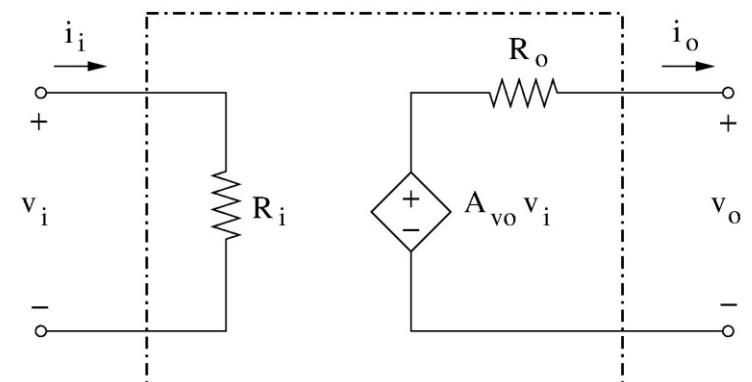
Open-loop Gain:  $A_{vo} = \frac{v_o}{v_i} \Big|_{R_L \rightarrow \infty}$

Input Resistance:  $R_i = \frac{v_i}{i_i}$

Output Resistance of Amplifier:  $R_o = -\frac{v_o}{i_o} \Big|_{v_i=0}$



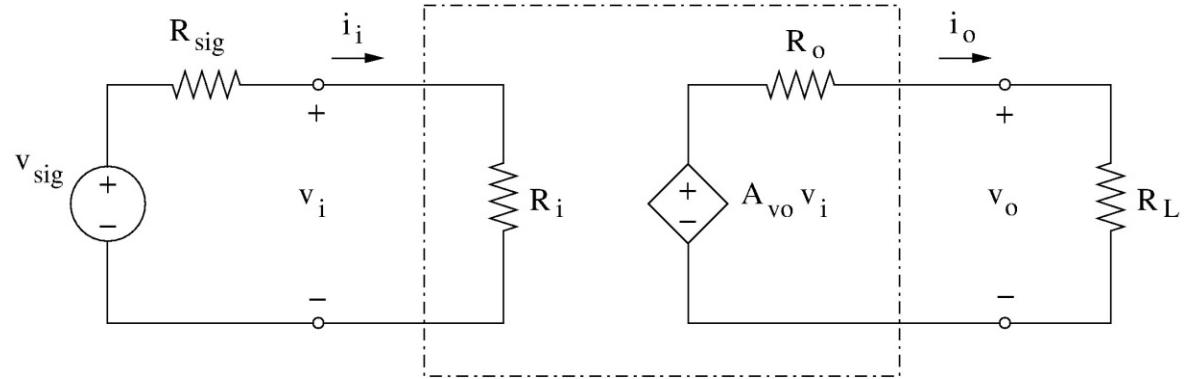
Voltage Amplifier Model



# Observations on the amplifier parameters

Overall Gain :

$$A = \frac{v_o}{v_{sig}} = \frac{v_i}{v_{sig}} \times \frac{v_o}{v_i} = \frac{R_i}{R_i + R_{sig}} A_v$$



$$\frac{v_i}{v_{sig}} = \frac{R_i}{R_i + R_{sig}}$$

Value of  $R_i$  is important.

- For  $R_i \gg R_{sig}$ ,  $v_i \approx v_{sig}$
- For  $R_i = R_{sig}$ ,  $v_i = 0.5 v_{sig}$
- For  $R_i \ll R_{sig}$ ,  $v_i \approx 0$

Prefer “large”  $R_i$

$$A_v = \frac{v_o}{v_i} = \frac{R_L}{R_L + R_o} A_{vo}$$

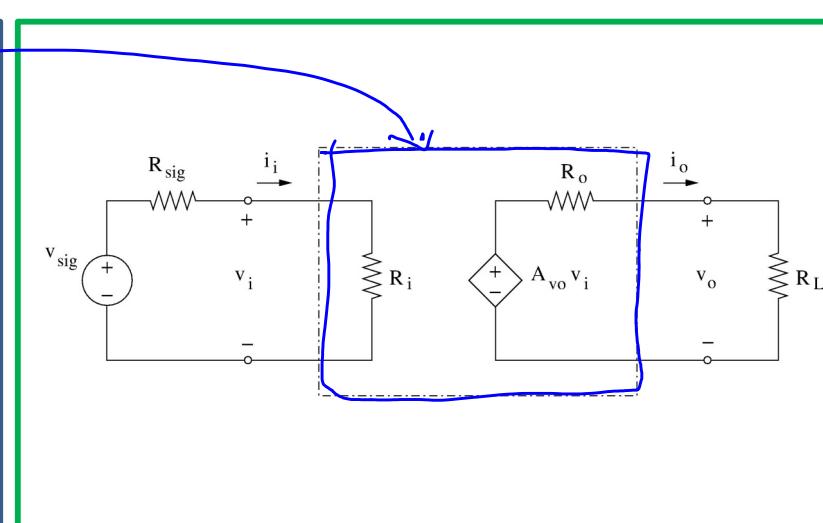
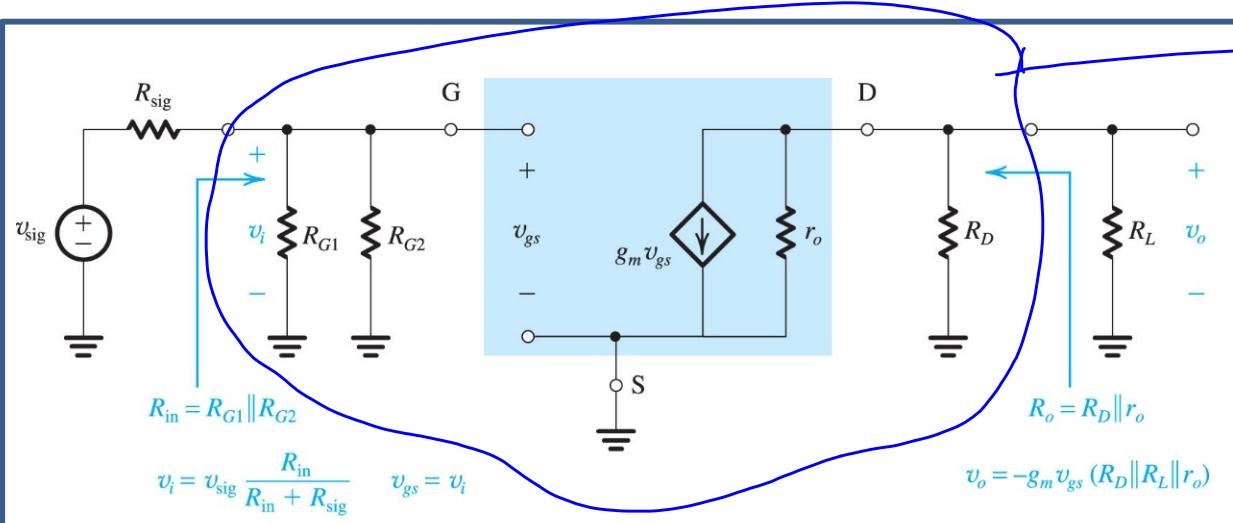
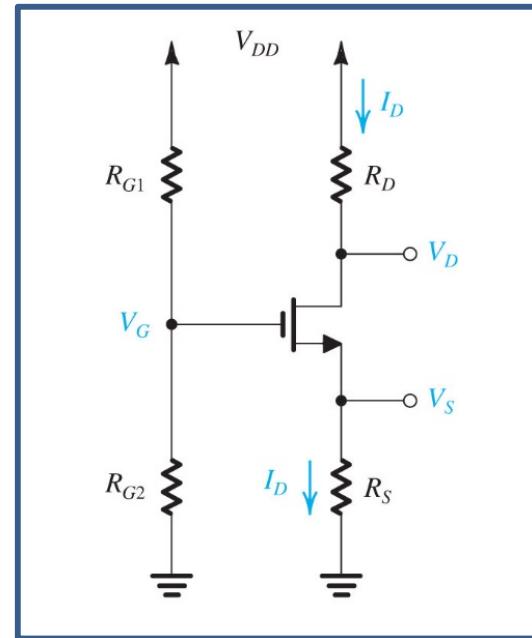
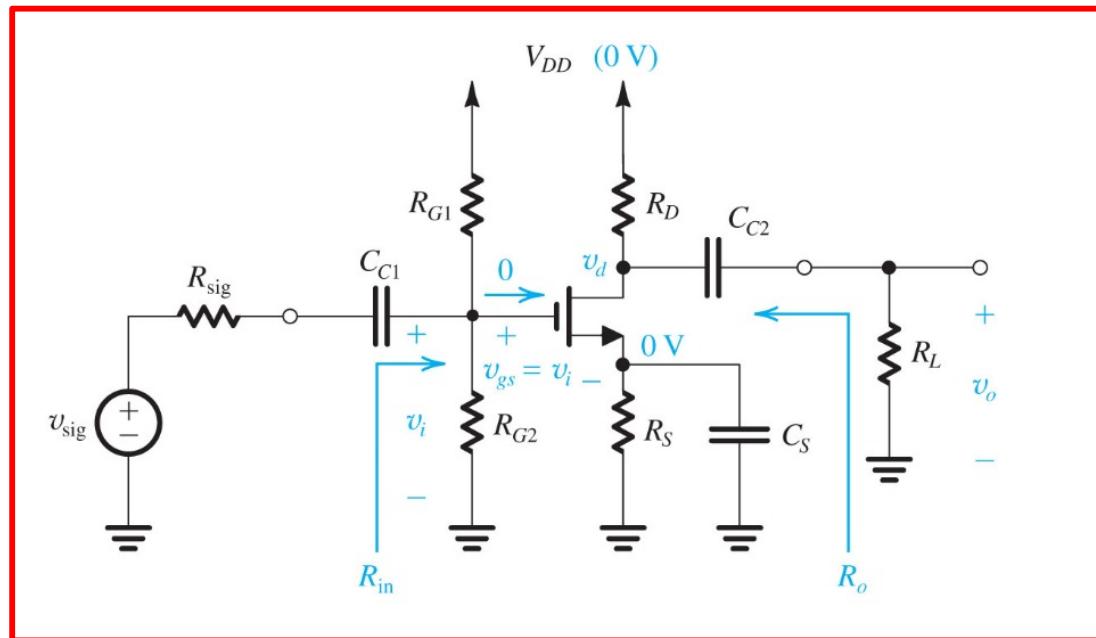
$A_{vo}$  is the maximum possible gain of the amplifier.

Value of  $R_o$  is important.

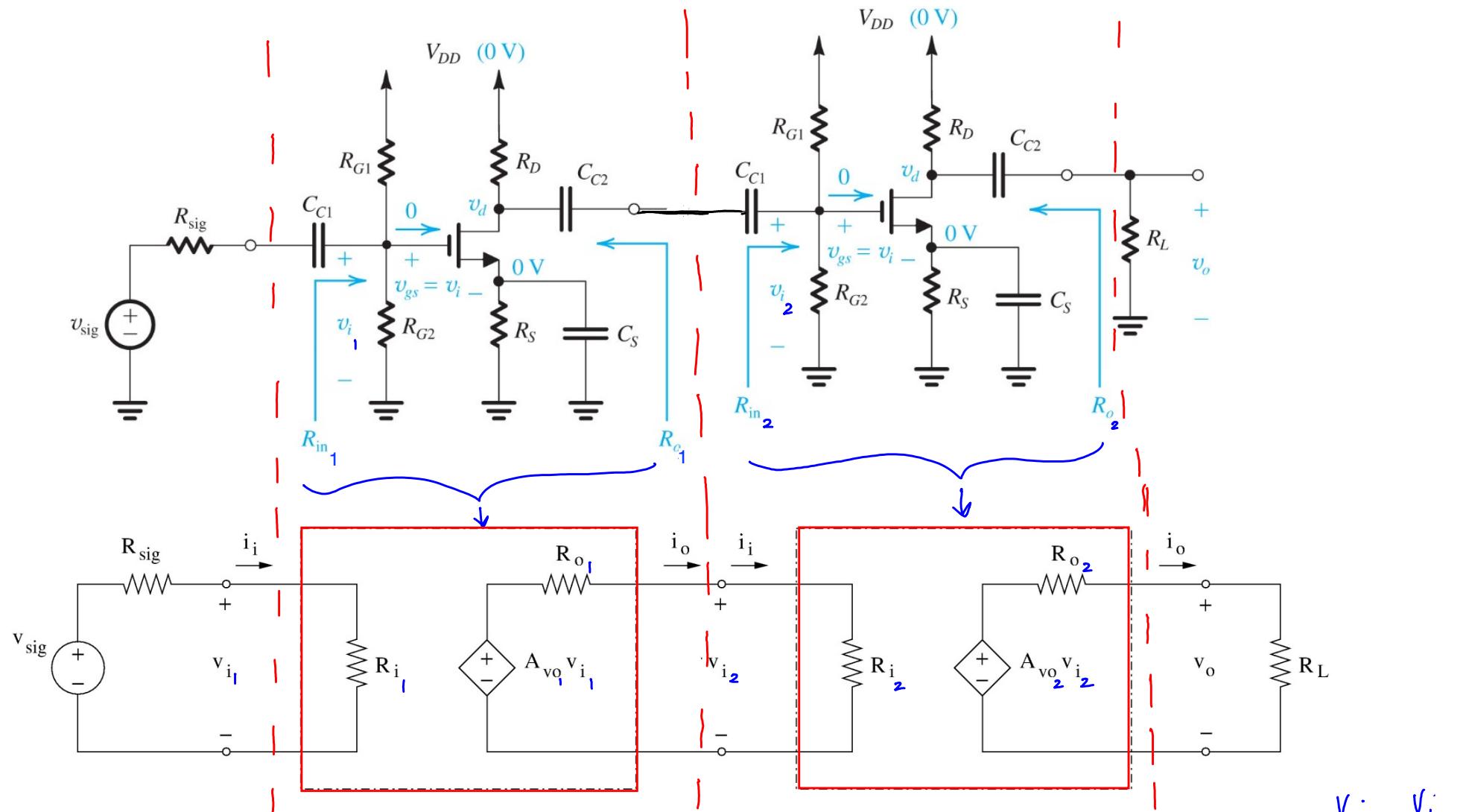
- For  $R_o \ll R_L$ ,  $A_v \approx A_{vo}$
- For  $R_o = R_L$ ,  $A_v = 0.5 A_{vo}$
- For  $R_o \gg R_L$ ,  $A_v \approx 0$

Prefer “small”  $R_o$

# From an amplifier circuit to the building block representation



# Cascade of amplifiers



$$\frac{v_o}{v_{sig}} = \left( \frac{R_L}{R_L + R_{o2}} A_{vo2} \right) \left( \frac{R_{i2}}{R_{i2} + R_{o1}} A_{vo1} \right) \frac{R_{i1}}{R_{i1} + R_{sig}}$$

$$\frac{V_o}{V_{sig}} = \frac{V_o}{V_{sig}} \cdot \frac{V_{i2}}{V_{i1}} \cdot \frac{V_{i1}}{V_{sig}}$$

# Solving the Transistor Amplifier circuits

- Draw the Bias circuit and find the Bias point
- Find the small signal parameters ( $g_m, r_o, r_\pi$ )
- Draw the signal equivalent circuit
- Find the amplifiers parameters ( $R_i, R_o, A_{v_0}$ )
- Use the voltage amplifier model and the calculated parameters to find the amplifier circuit gain (A).

# **Transistor Amplifier configurations**

# Possible BJT amplifier configurations

Common-Collector or Emitter Follower

Common-Emitter

- Common-Emitter with an Emitter resistor

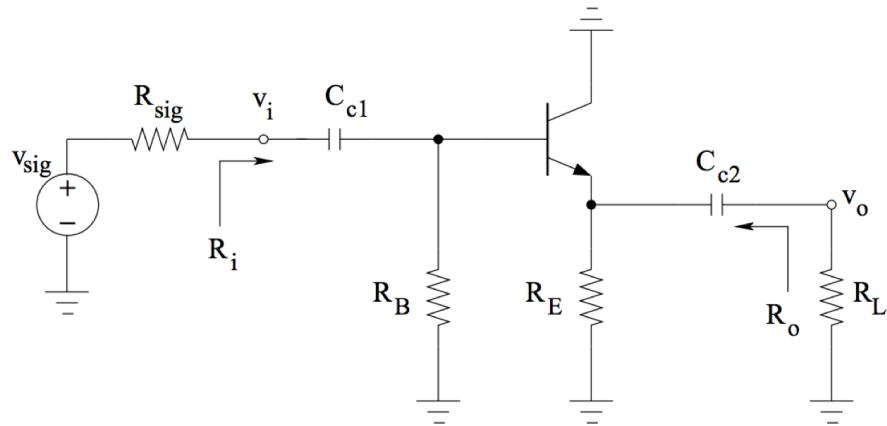
Common-Base

# Possible BJT amplifier configurations

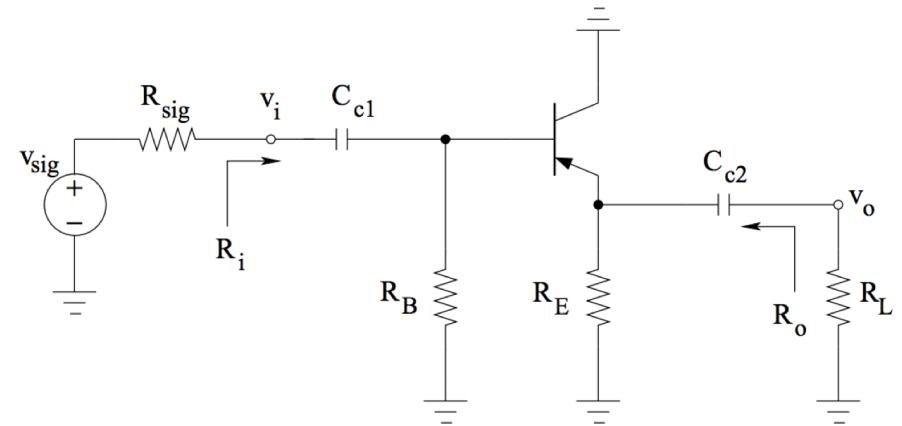
## Common-Collector or Emitter Follower

The input is applied at the base and the output is taken at the emitter.

NPN BJT

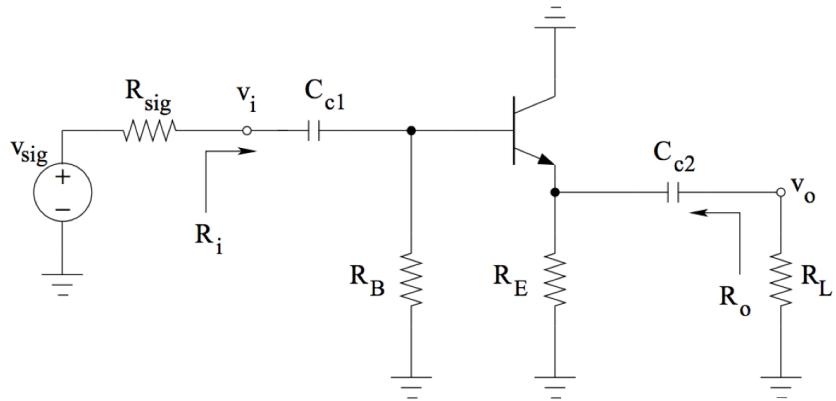


PNP BJT

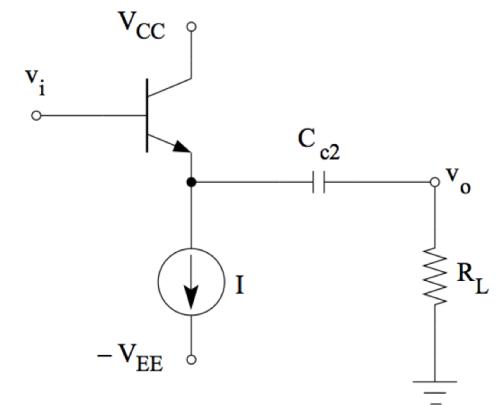
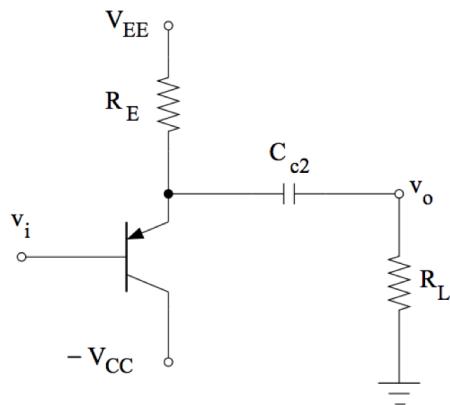
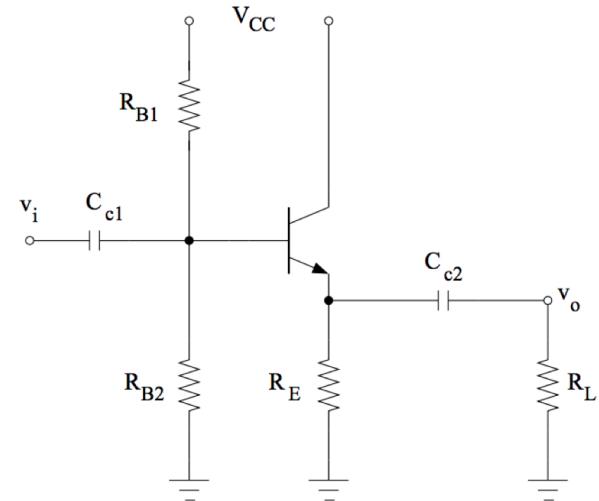


# Possible BJT amplifier configurations

## Common-Collector or Emitter Follower



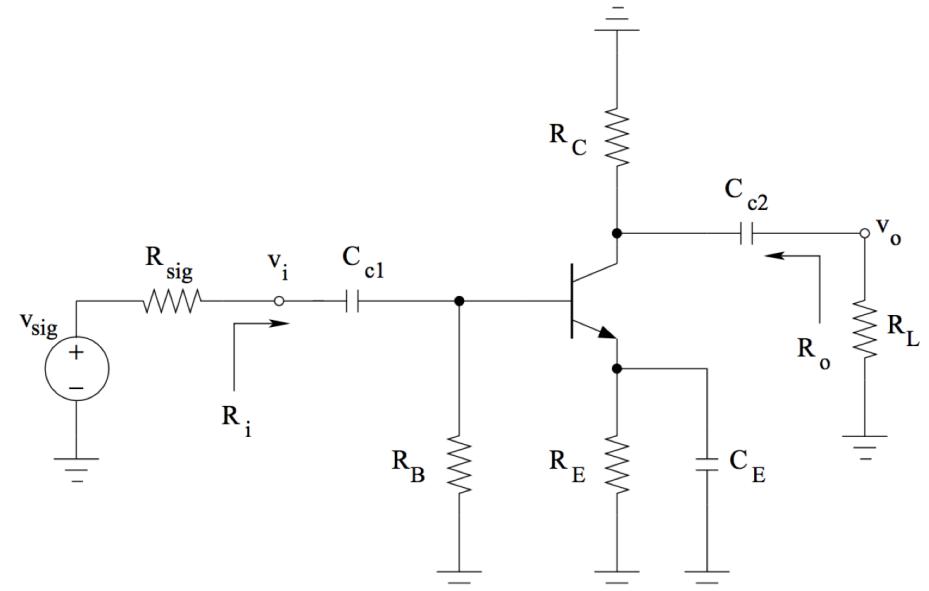
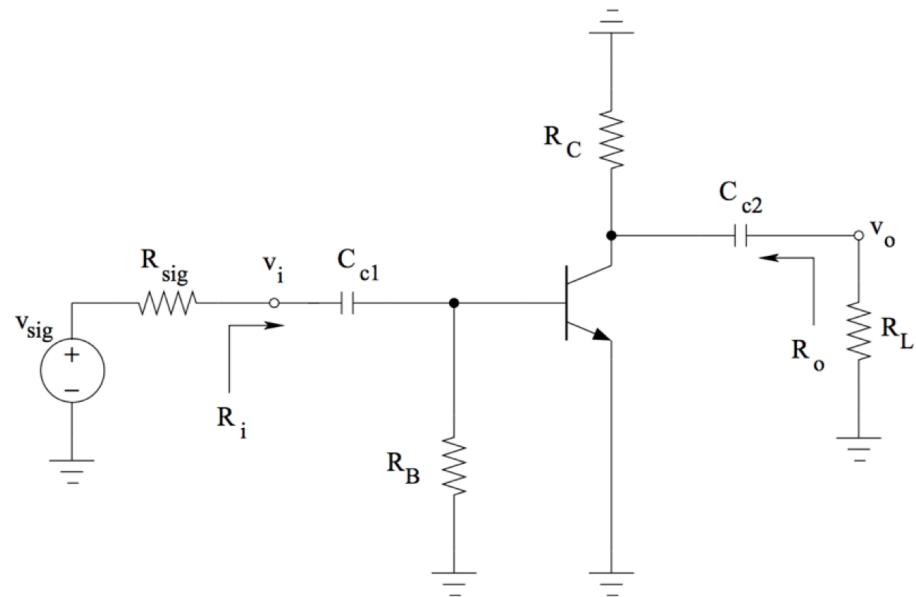
Some example (Bias + Signal) circuits in Common-Collector configuration:



# Possible BJT amplifier configurations

## Common-Emitter

The input is applied at the base and the output is taken at the collector.

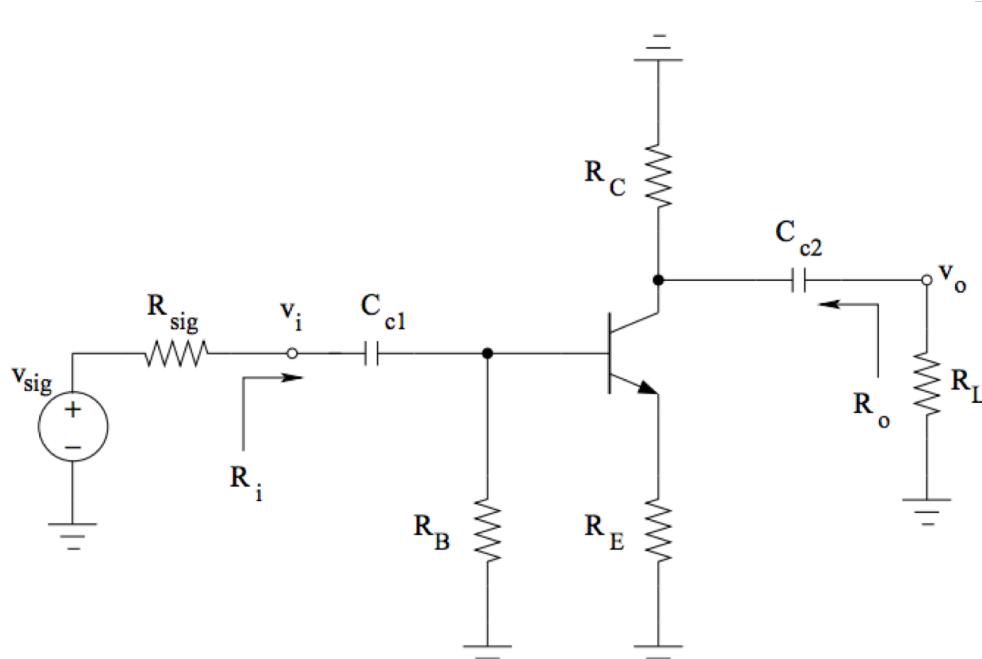


An emitter resistor is used for the Bias, but it is shorted in the signal circuit

# Possible BJT amplifier configurations

## Common-Emitter with an Emitter resistor

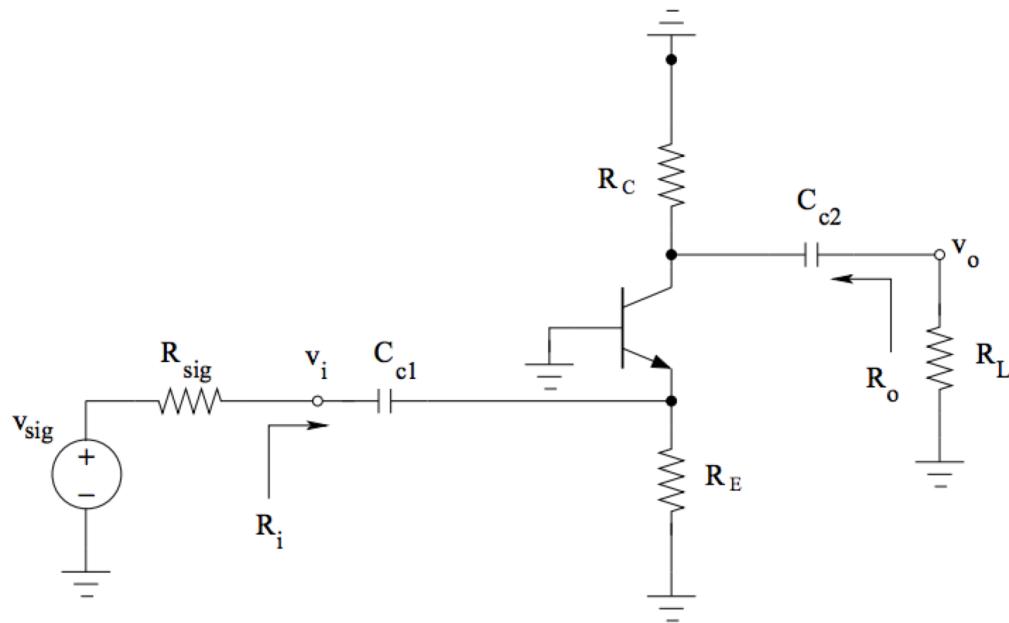
The input is applied at the base and the output is taken at the collector.



# Possible BJT amplifier configurations

## Common-Base

The input is applied at the emitter and the output is taken at the collector.



# Possible MOS amplifier configurations

Common-Drain or Source Follower

Common-Source

- Common-Source with a Source resistor

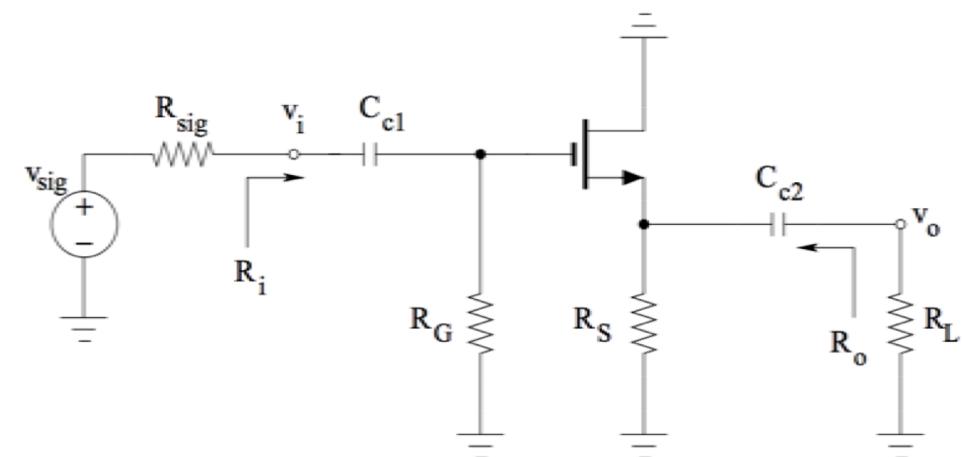
Common-Gate

# Possible MOS amplifier configurations

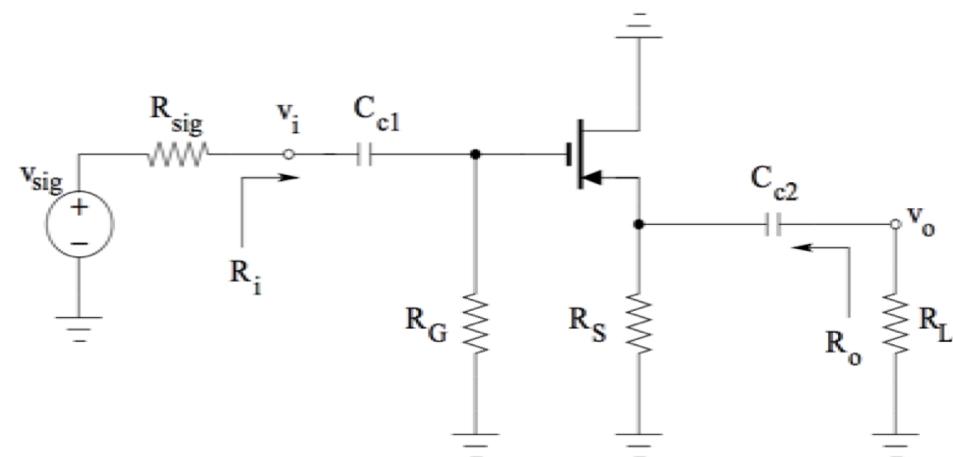
## Common-Drain or Source Follower

The input is applied at the gate and the output is taken at the source.

NMOS

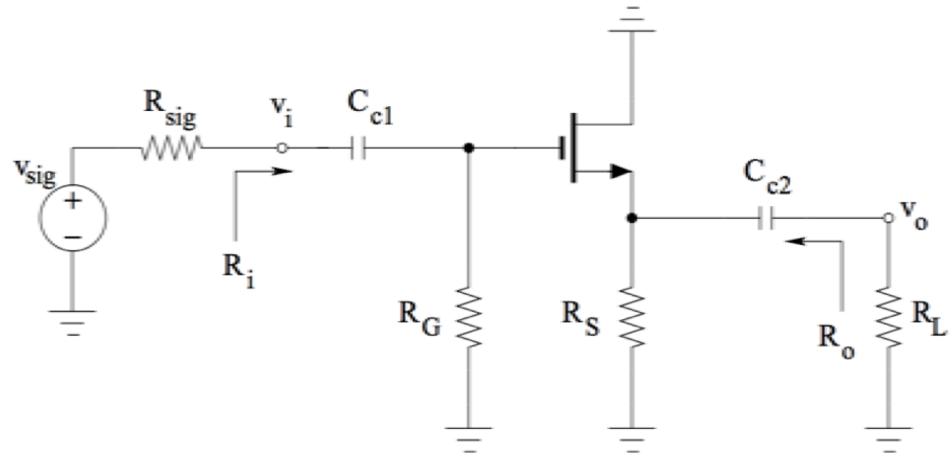


PMOS

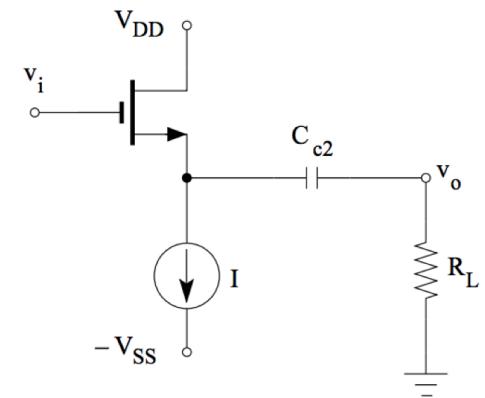
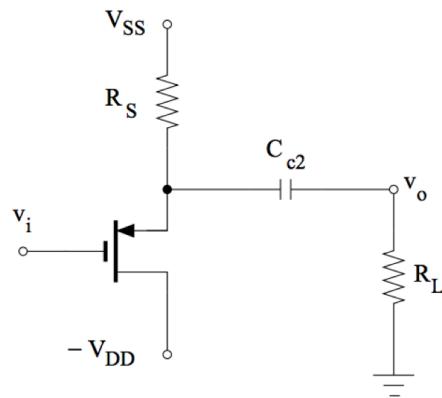
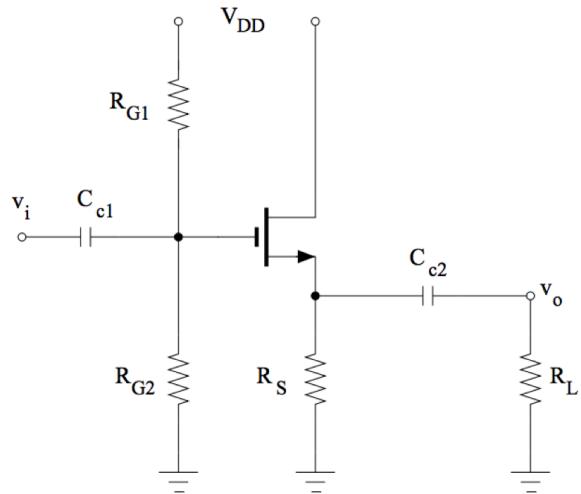


# Possible MOS amplifier configurations

## Common-Drain or Source Follower



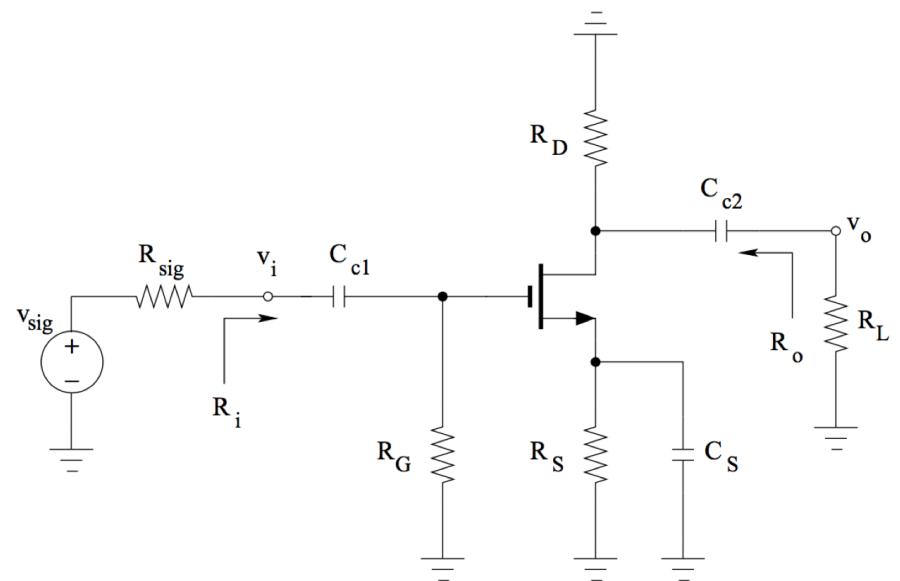
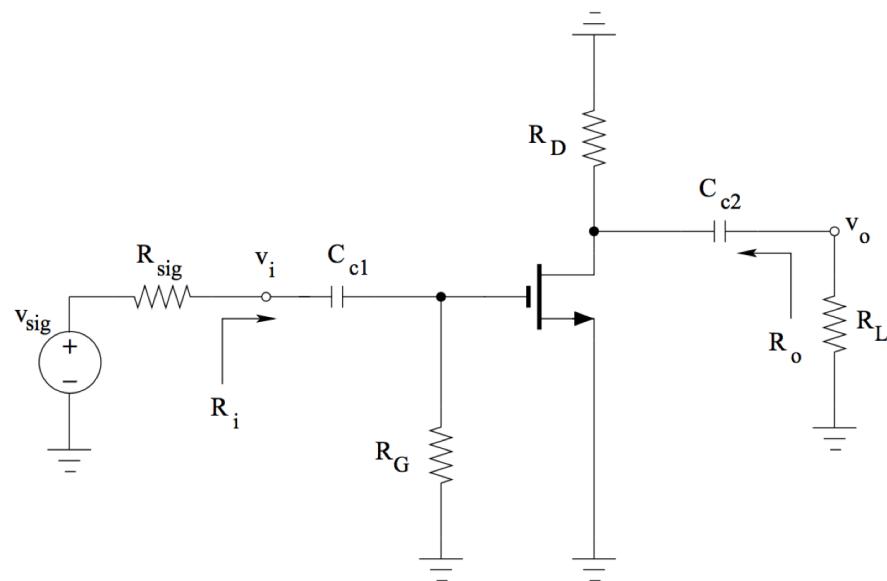
Some example (Bias + Signal) circuits in Common-Drain configuration:



# Possible MOS amplifier configurations

## Common-Source

The input is applied at the gate and the output is taken at the drain.

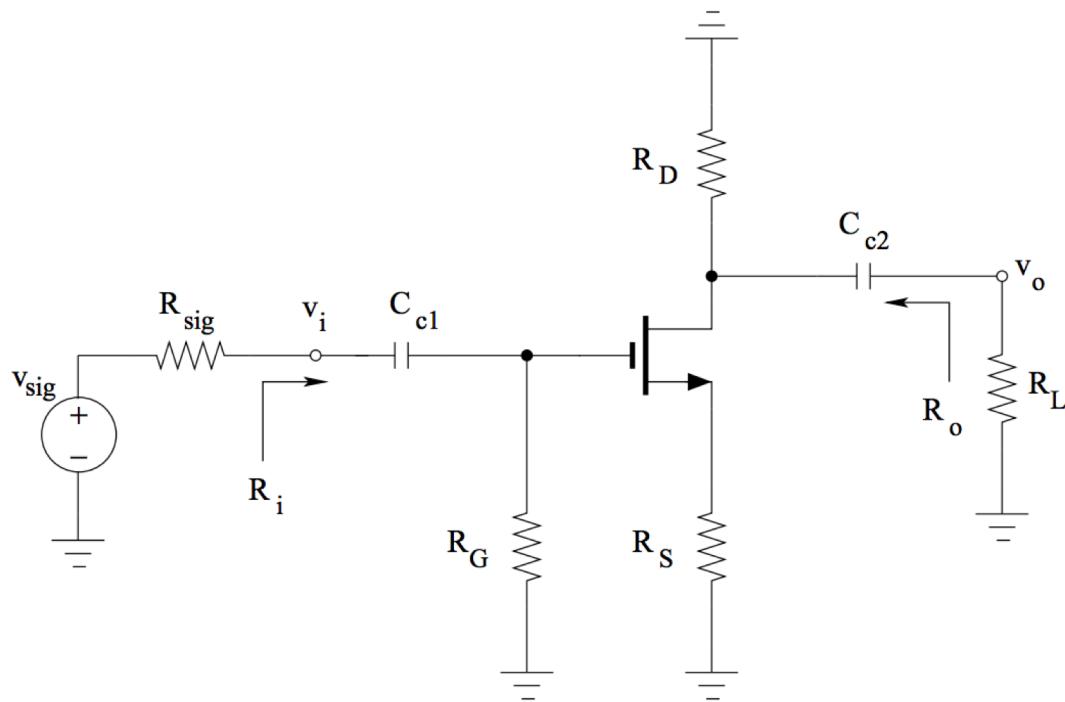


A source resistor is used for the Bias,  
but it is shorted in the signal circuit

# Possible MOS amplifier configurations

## Common-Source with a Source resistor

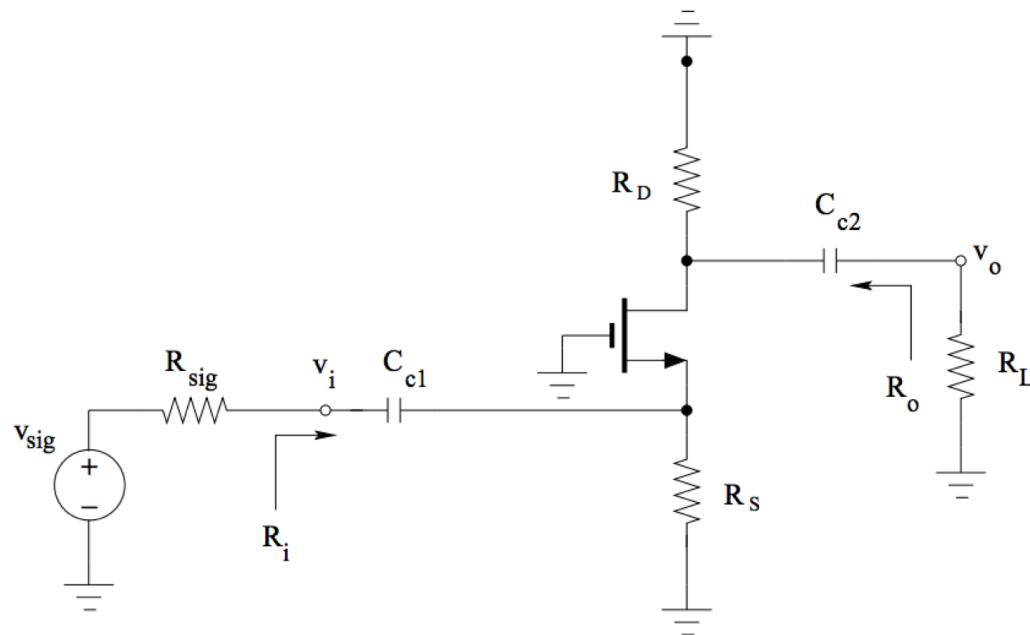
The input is applied at the gate and the output is taken at the drain.



# Possible MOS amplifier configurations

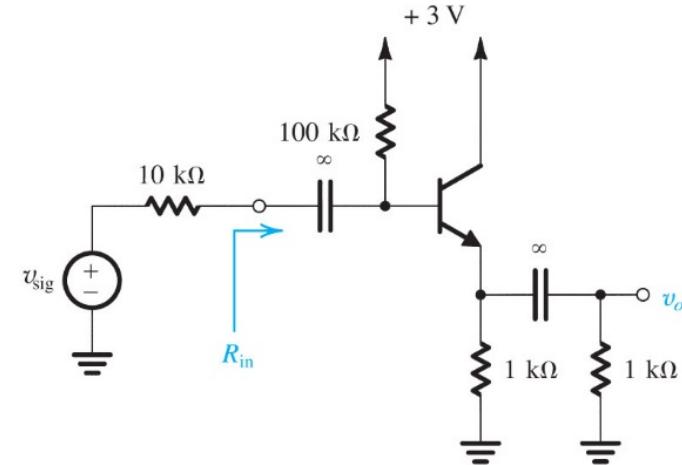
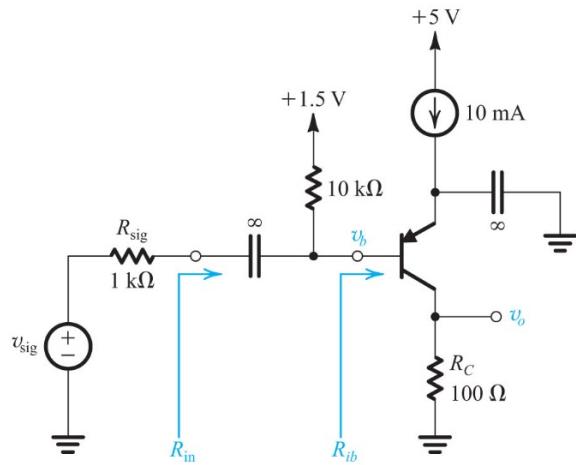
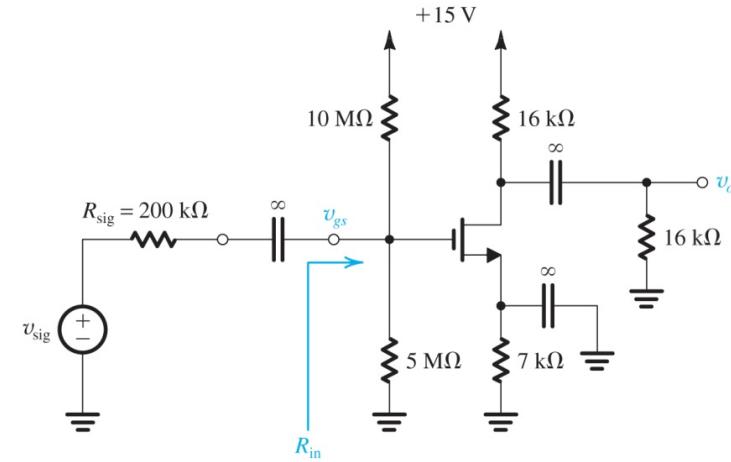
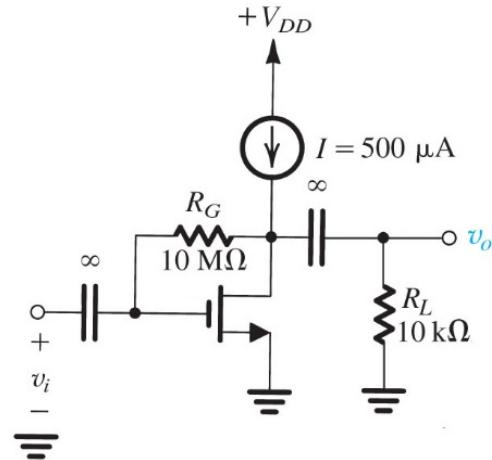
## Common-gate

The input is applied at the source and the output is taken at the drain.



# Lecture 21 reading quiz

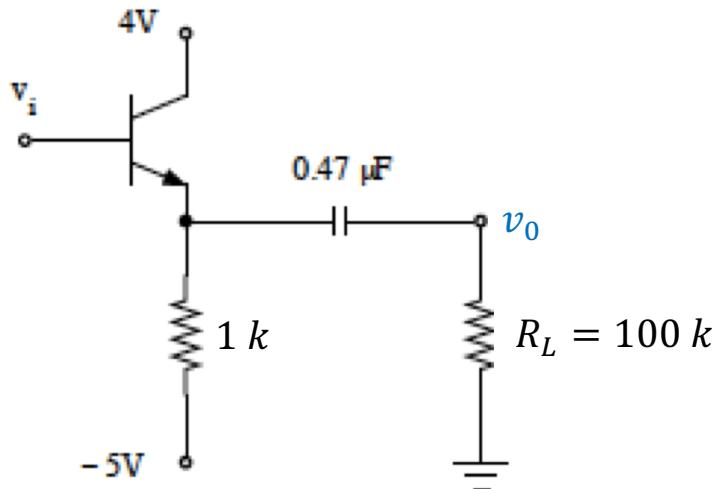
Which one of the answers is correct about the configuration of the given amplifiers:



# Clicker question 1.

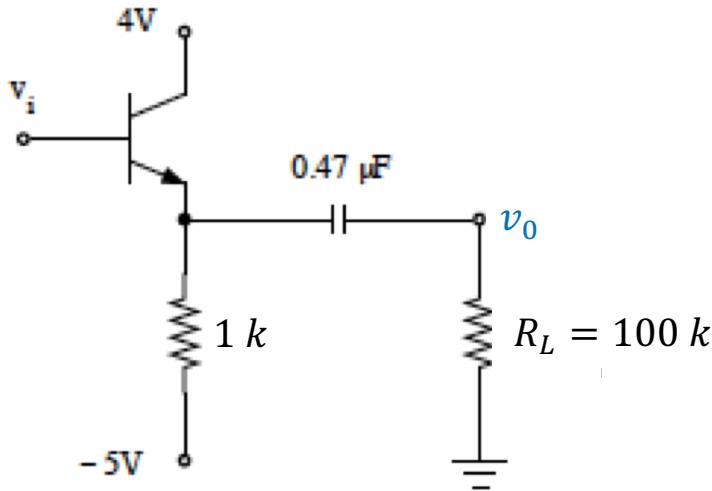
What is the amplifier configuration for the following circuit?

- A. Common-Base
- B. Common-Emitter
- C. Common-Collector



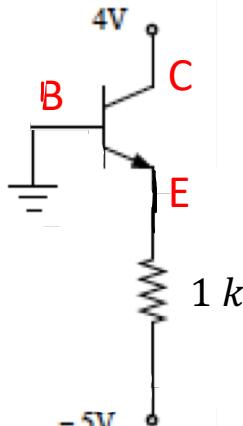
## Clicker question 2.

Draw the signal circuit and find the open loop voltage gain of the amplifier ( $A_{vo} = \frac{v_o}{v_i} \Big|_{R_L \rightarrow \infty}$ ) for this circuit. Let  $\beta = 100$ ,  $V_T = 25 \text{ mV}$ ,  $V_A = 150 \text{ V}$ .



- A.  $A_{vo} = 0.67 \text{ V/V}$
- B.  $A_{vo} = 0.99 \text{ V/V}$
- C.  $A_{vo} = 0.53 \text{ V/V}$
- D.  $A_{vo} = 0.49 \text{ V/V}$

Bias circuit, Bias point and small signal parameters:



$$I_C \approx I_E = 4.3 \text{ mA}$$

$$V_{CE} = 4.7 \text{ V}$$

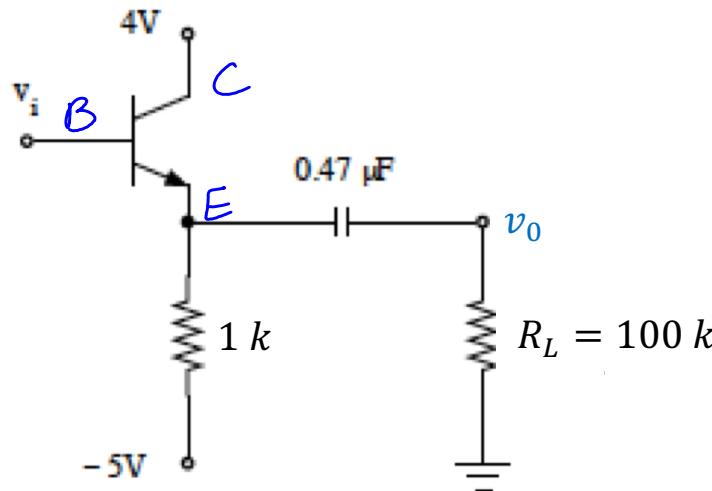
$$r_\pi = \frac{V_T}{I_B} = 581.4 \Omega$$

$$r_o = \frac{V_A}{I_C} \approx 35 \text{ k}\Omega$$

$$g_m = \frac{I_C}{V_T} = 0.172 \text{ A/V}$$

Hints:

## Clicker question 2.



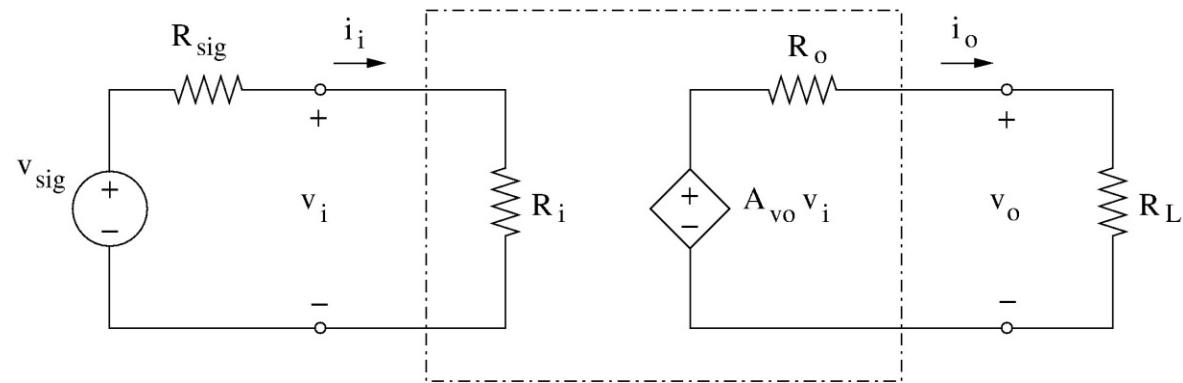
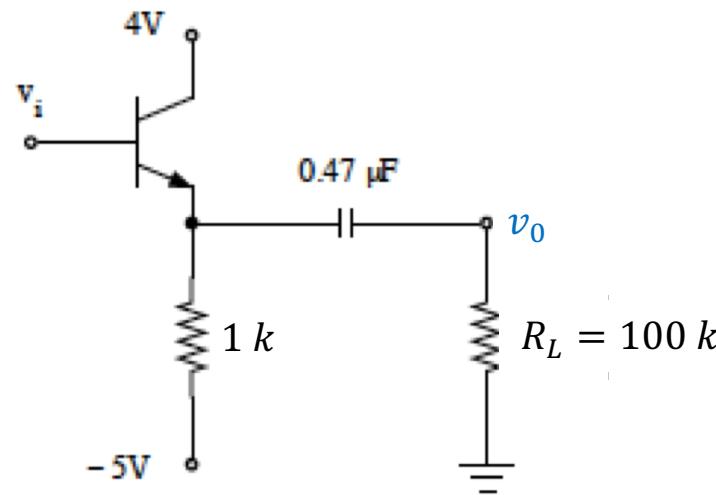
$$r_\pi = \frac{V_T}{I_B} = 581.4 \Omega \quad r_o = \frac{V_A}{I_C} \approx 35 \text{ k}\Omega$$

$$g_m = \frac{I_C}{V_T} = 0.172 \text{ A/V}$$

- Draw the signal circuit using the rules you learned in previous lectures.
- The goal is to solve the signal circuit to find an equation relating  $v_o$  to  $v_i$ . Since the question asks for the open-loop gain, replace  $R_L$  with an open circuit.
- Write a KCL at the emitter (output) node (in the signal circuit). This will give you an equation in terms of  $v_o$  and  $v_{\{\pi\}}$ . You have the values of all other parameters in that equation.
- Write a KVL in the BE loop (in the signal circuit). That will give you an equation in terms of  $v_i$ ,  $v_{\{\pi\}}$ , and  $v_o$ .
- Using the above two equations to get an equation in terms of  $v_o$  and  $v_i$  and find the open-loop voltage gain of this amplifier.

## Discussion question 1.

The output resistance ( $R_o$ ) of the following amplifier circuit is  $5.72 \Omega$ , use the calculated open loop voltage gain ( $A_{vo}$ ) and the voltage amplifier model to find the voltage gain ( $A_v$ ) of this amplifier.



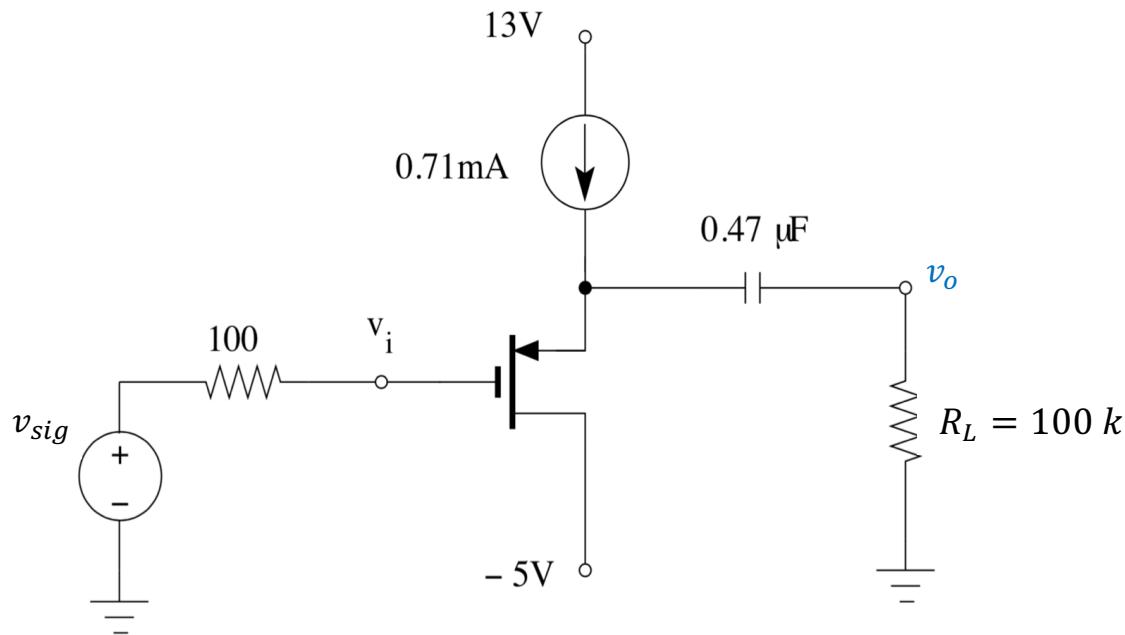
$$A_v = \frac{v_o}{v_i} = \frac{R_L}{R_L + R_o} A_{vo}$$

## Discussion question 2.

In this amplifier circuit,

1. Find the Bias point.
2. Find the small signal parameters.
3. Find the open loop voltage gain ( $A_{vo}$ ).

Let  $V_{tp} = -4 V$ ,  $k_p = 0.4 \text{ mA/V}^2$ ,  $\lambda = 0.01 \text{ V}^{-1}$ , and ignore the channel-length modulation effect in biasing calculations.

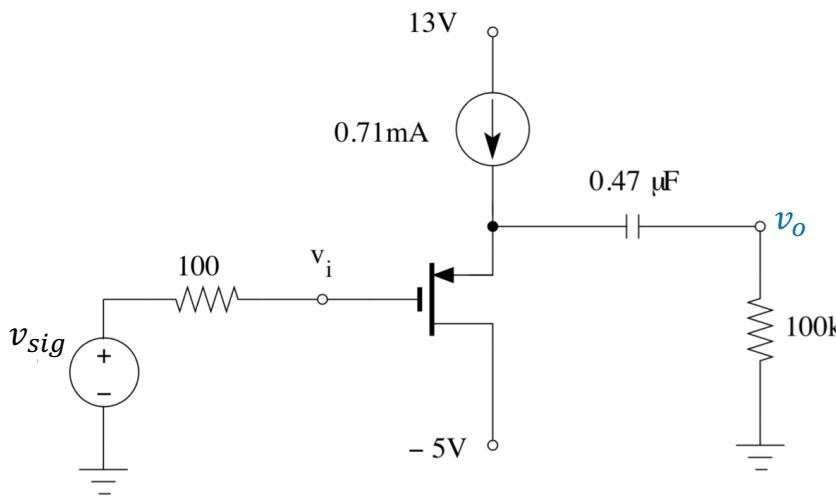


$$g_m = \frac{2I_D}{V_{OV}} \quad r_o = \frac{1}{\lambda I_D}$$

Hints:

## Discussion question 2.

Let  $V_{tp} = -4 V$ ,  $k_p = 0.4 \text{ mA/V}^2$ .  $\lambda = 0.01 \text{ V}^{-1}$ .



- To draw the Bias circuit, short  $v_{sig}$  and open the capacitor.
- Solve the Bias circuit. The MOSFET is in saturation.
- Using the equations of the small signal parameters, find those values.
- Draw the signal circuit. DC source will be zeroed. The capacitor will be shorted.
- Solve the signal circuit to find an equation relating  $v_o$  to  $v_i$ . Replace  $RL$  with open circuit, because you are asked to find the open-loop voltage gain.

- Write a KCL at the output node. This will give you an equation relating  $v_o$  to  $v_{gs}$ .
- Write another KVL equation in the gate to source loop to relate  $v_i$  to  $v_{gs}$  and  $v_o$ .
- Combine the above two equations to find an equation relating  $v_i$  to  $v_o$ .