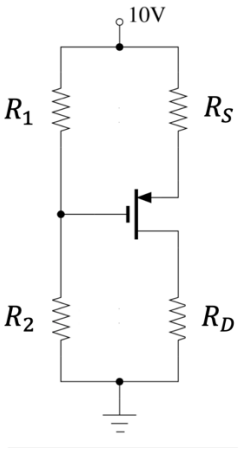
ECE 65 HW 3 No submission is required

Problem 1.

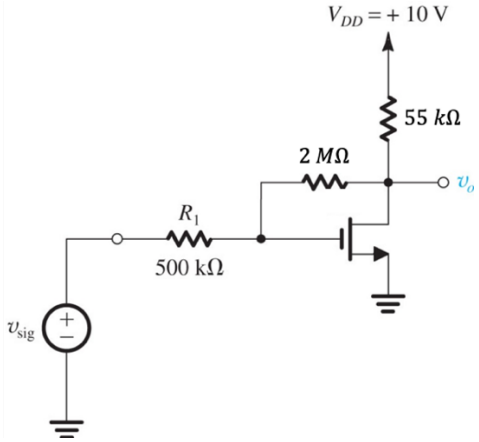
Design the below circuit so that the transistor operates in saturation with V_{SD} biased 1-V from the edge of the saturation, with $I_D = 1\ mA$, and $V_D = 3\ V$. Use a 10 μA current in the voltage divider. $|V_t| = 1\ V$ and $k_p = 0.5\ mA/V^2$.



Problem 2.

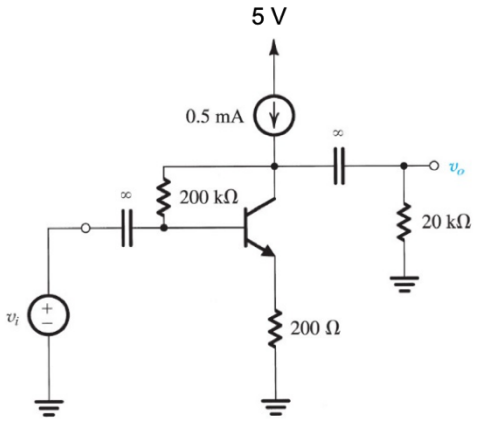
In the following circuit, solve the Bias circuit, find the small signal parameters and draw the signal circuit (assume capacitors are short for signal). Solve the small signal circuit to find the total circuit gain (v_o/v_{sig}).

$V_{tn} = 0.6\ V$, $k_n = 5\ mA/V^2$. $V_A = 60\ V$. Ignore the channel-length modulation effect in biasing calculations.



Problem 3.

The BJT in the below circuit has $\beta = 100, V_{Do} = 0.7\,V$, $V_A = \infty, V_T = 26\,mV$. Find the DC collector current and the DC voltage at the collector. Draw the signal circuit.
(assume capacitors are short for signal).



Problem 4.

In the following circuit, BJT has $\beta = 100,\ V_{D0} = 0.7\,V,\ V_A = \infty,\ V_T = 25\,mV$.

a) Find the value of R_E to establish a dc emitter current of 0.5 mA.
b) Find the value of R_C to establish a dc collector voltage of 0.5 V.
c) Draw the signal equivalent circuit and find the small signal parameters.
d) Find the input and output resistances and the open loop voltage gain of the transistor.
e) If $R_L = 100$ kΩ, determine the total circuit gain (A).