

ECE 65 – Components and Circuits Lab

Lab 2 Report – Operational Amplifier circuits

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Andrew Onozuka, Riku Nagareda

PID:A16760043, A18555891

Professor: Saharnaz Baghdadchi

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Abstract

The purpose of this lab is to explore the behavior of operational amplifier circuits in various configurations, including their use as voltage amplifiers and weighted summers.

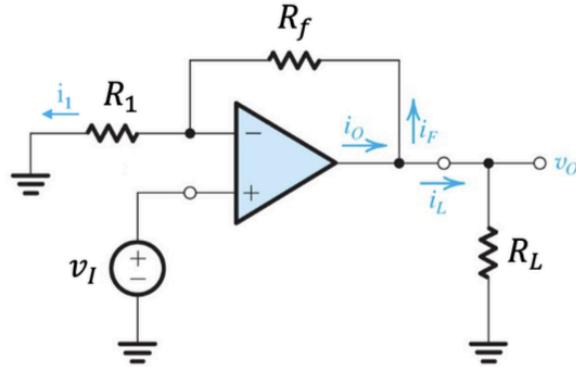
We performed simulations using LTspice to test saturation limits, voltage gains, and output behavior under varying input signals and load resistances, and built physical circuits on a breadboard to analyze and validate their real-world performance.

We concluded that operational amplifiers effectively perform linear mathematical operations, such as summation and amplification, within their design constraints. However, these design constraints include how their performance is limited by saturation voltage and maximum output current capabilities, which we have to deal with in determining real-world performance and behaviors.

Experimental Procedures and Results

Experiment 1: Op-amp as a voltage amplifier and large-signal limits

One way to use operational amplifiers (op-amps) is as linear voltage amplifiers. A common configuration is the non-inverting amplifier. The op-amp will work as a linear amplifier if the output voltage and the op-amp output current are within the saturation limits. The aim of this experiment is to test the saturation limits and measure the outputs for different input and load conditions. You will use an LM741 op-amp in ECE65 labs. The maximum output current of this Op-amp is about 25mA, and the saturation voltage is about $\pm 14V$ when $\pm 15V$ DC power supplies are used to power up the op-amp chip. You will use $\pm 15V$ DC power supplies for powering up the op-amp in simulations and lab experiments.



Include your explanations, circuit analysis, plots, etc. here.

Prelab:

Circuit analysis

1. Using $R_1 = 1k\Omega$, find the value of R_f to achieve a voltage gain of $10V/V$.

$$10 \frac{V}{V} = A_v = 1 + \frac{R_f}{R_1} = 1 + \frac{R_f}{1k\Omega}$$

$$R_f = 9k\Omega$$

2. Analyze the circuit and write the equations that relate i_o , i_L , and i_f to v_i .

KCL at the Op-Amp Output Node

$$i_o = i_F + i_L$$

Ohm's Law for i_L (Load Current)

$$i_L = \frac{v_o}{R_L}$$

Ohm's Law for i_F (Feedback Current)

$$i_F = \frac{v_o - v_-}{R_f}$$

Relationship between v_- and v_I (Virtual Short)

$$v_- \approx v_+ \quad v_- = v_I$$

Ohm's law for i_1 (Current Through R_1)

$$i_1 = \frac{v_I}{R_1}$$

KCL at inverting input, since the current flowing into the inverting terminal of the op-amp is zero in an ideal assumption:

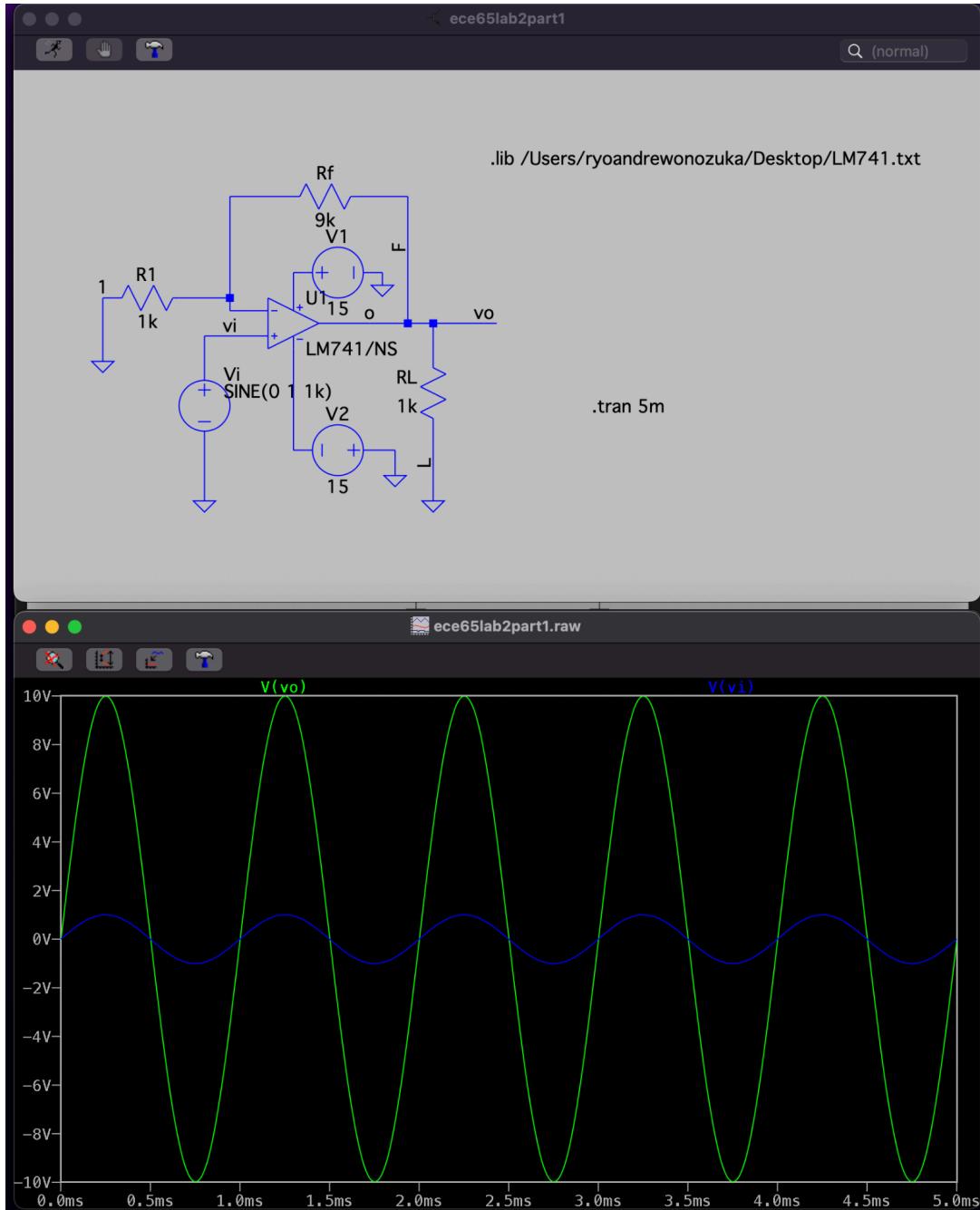
$$i_1 = i_F$$

Simulation

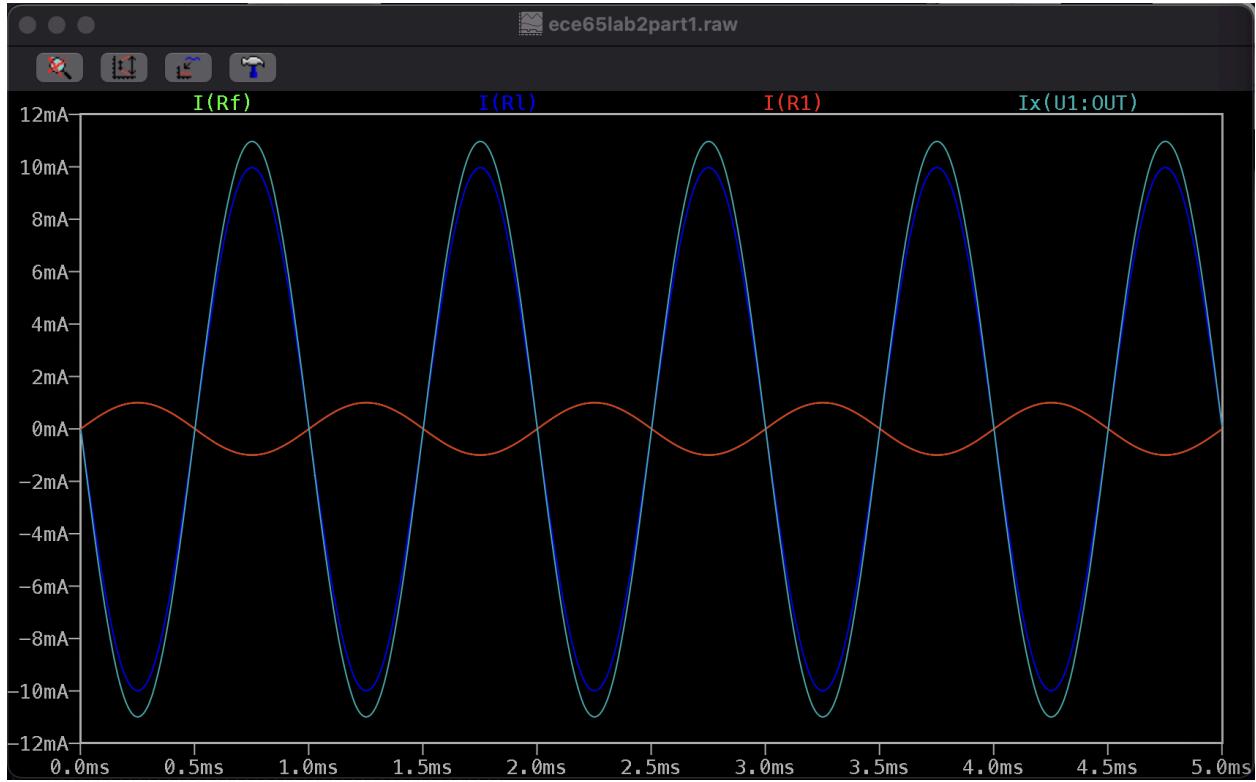
Part 1:

Simulate the circuit with PSpice/LTspice using a sinusoidal signal (v_i) with the peak amplitude $V_p = 1V$ and the frequency $f = 1\text{ kHz}$. Use the load resistor $R_L = 1k\Omega$.

1. Run Transient (Time domain) Analysis for 5 ms.
2. Plot the input and output waveforms on the same graph. Does the graph match your expectations?



3. Plot the output current of the op-amp (i_o), the load current (i_L), and the currents that flow through R_f and R_1 as labeled on the circuit. Do they match your expectations?



On the graph R_f is under R_1 .

4. What are the peak amplitudes of i_o , i_f , i_L , and i_L ?

i_o : 11 mA

i_f : 1.0 mA

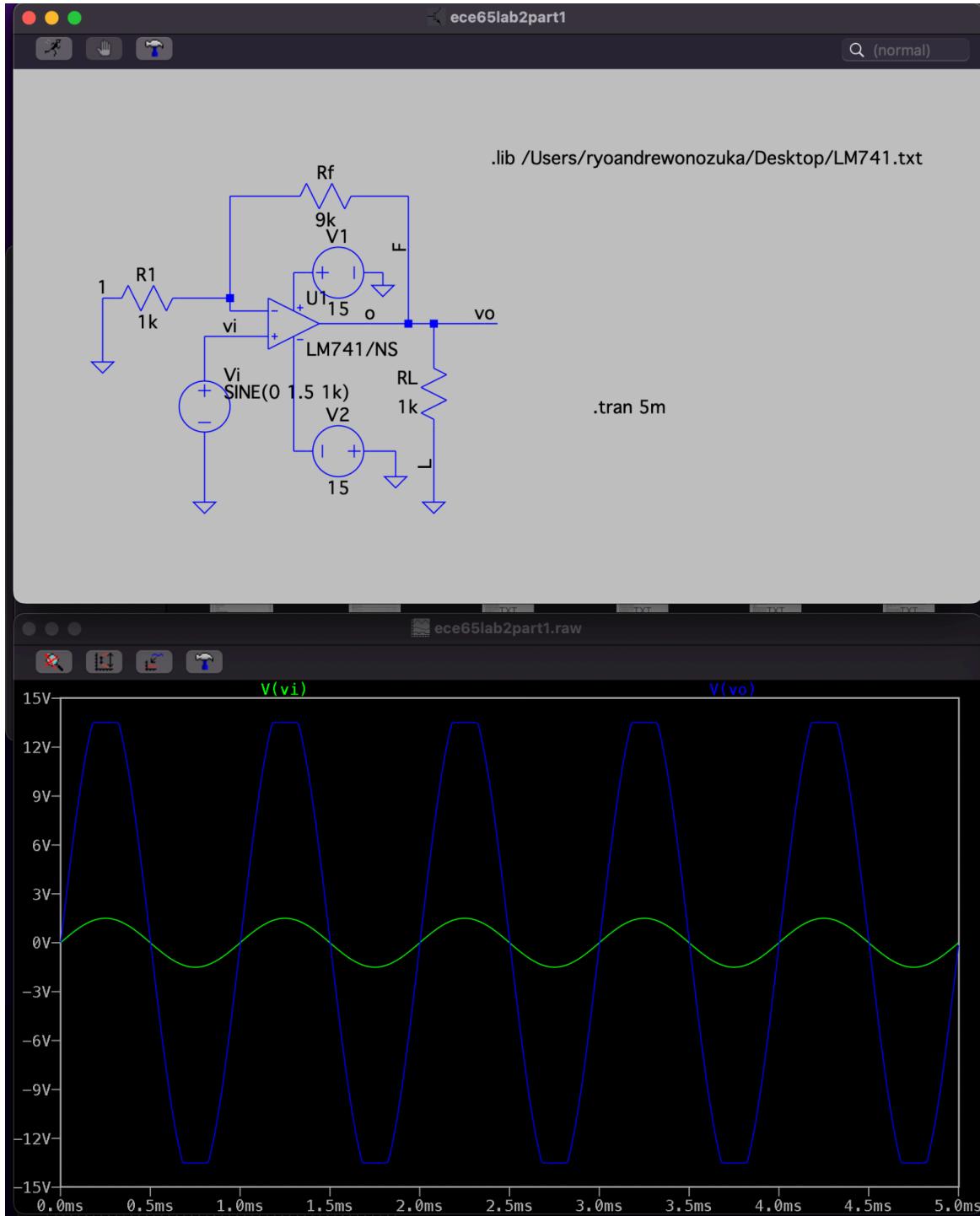
i_L : 1.0 mA

i_L : 10 mA

Part 2:

Simulate the circuit with PSpice/LTspice using a sinusoidal signal (v_i) with the peak amplitude $V_p = 1.5V$ and the frequency $f = 1\text{ kHz}$. Use the load resistor $R_L = 1k\Omega$.

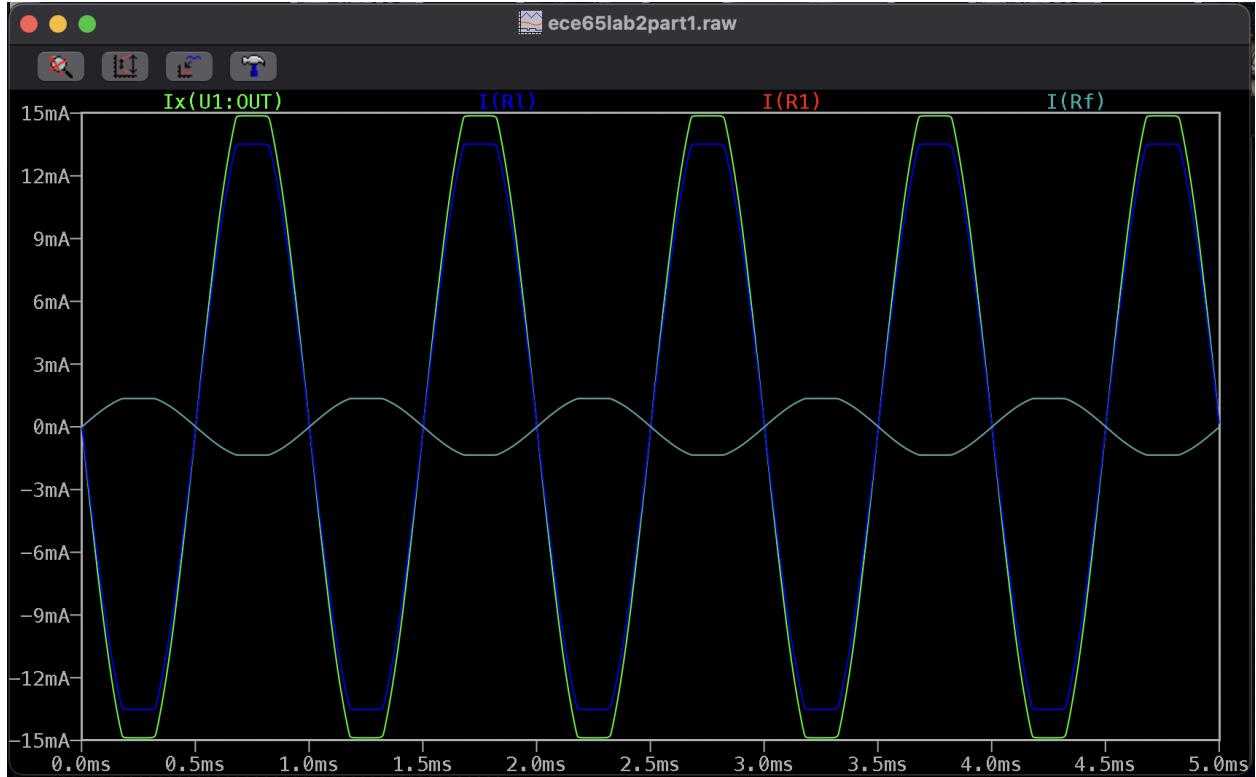
1. Run Transient (Time domain) Analysis for 5 ms.
2. Plot the input and output waveforms on the same graph.



3. How do you compare the output waveform in this part with the one you found in part 1?

They are similar but the output voltage in these waveforms are capped because of the maximum possible set by the saturation voltage.

4. Plot the output current of the op-amp (i_o), the load current (i_L), and the currents that flow through R_I and R_f as labeled on the circuit.



On the graph R_f is under R_I .

5. What are the peak amplitudes of i_o , i_f , i_I , and i_L ?

i_o : 15 mA

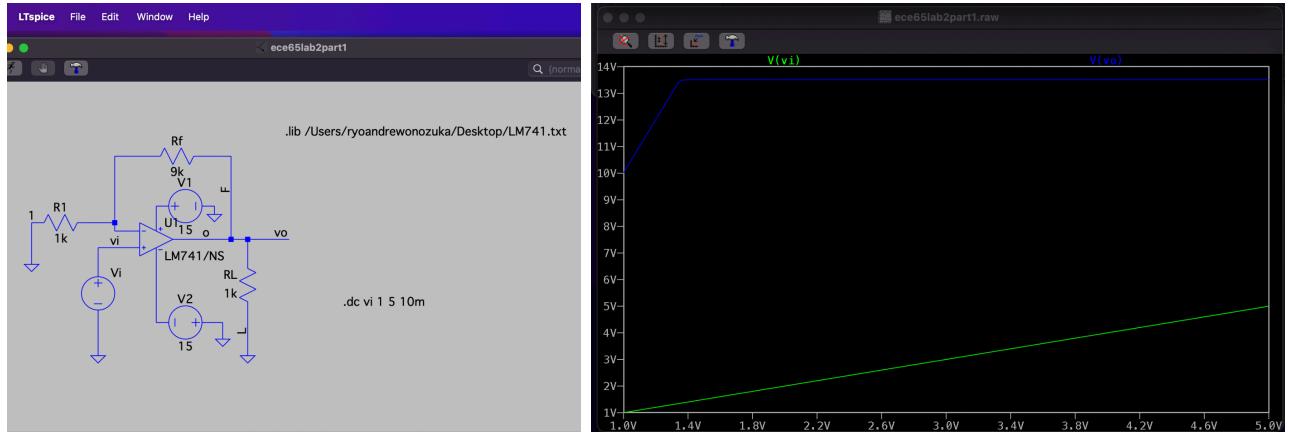
i_f : 1.34 mA

i_I : 1.34 mA

i_L : 13.4 mA

Part 3:

Using PSpice/LTspice with load resistor $R_L = 1k\Omega$, run a DC SWEEP on the input voltage v_I and plot the output voltage for v_I values between 1V and 5V ($1V < v_I < 5V$). Use the step size of $10mV$.



- For what value of v_I (approximately) will the output of the op-amp saturate?

1.4 V

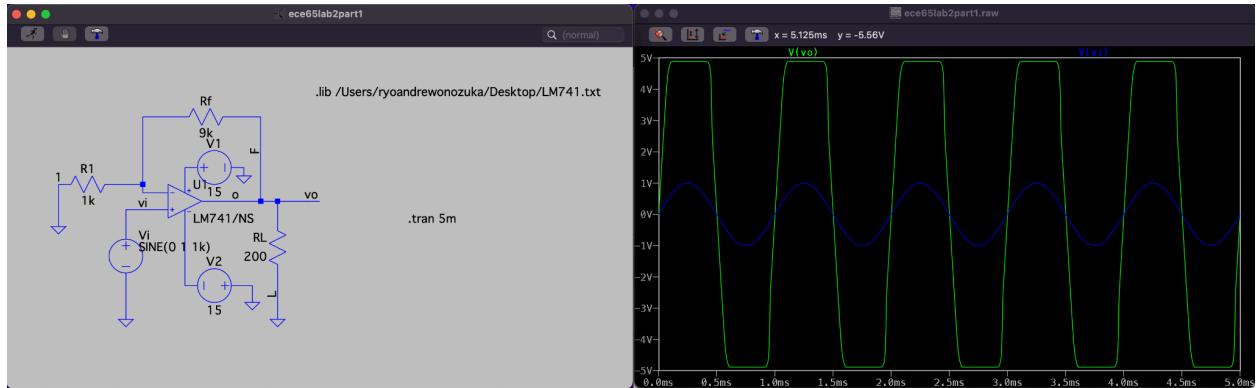
- Plot the output current of the op-amp (i_o), the load current i_L , the current that flows through R_1 and R_f as labeled on the circuit.



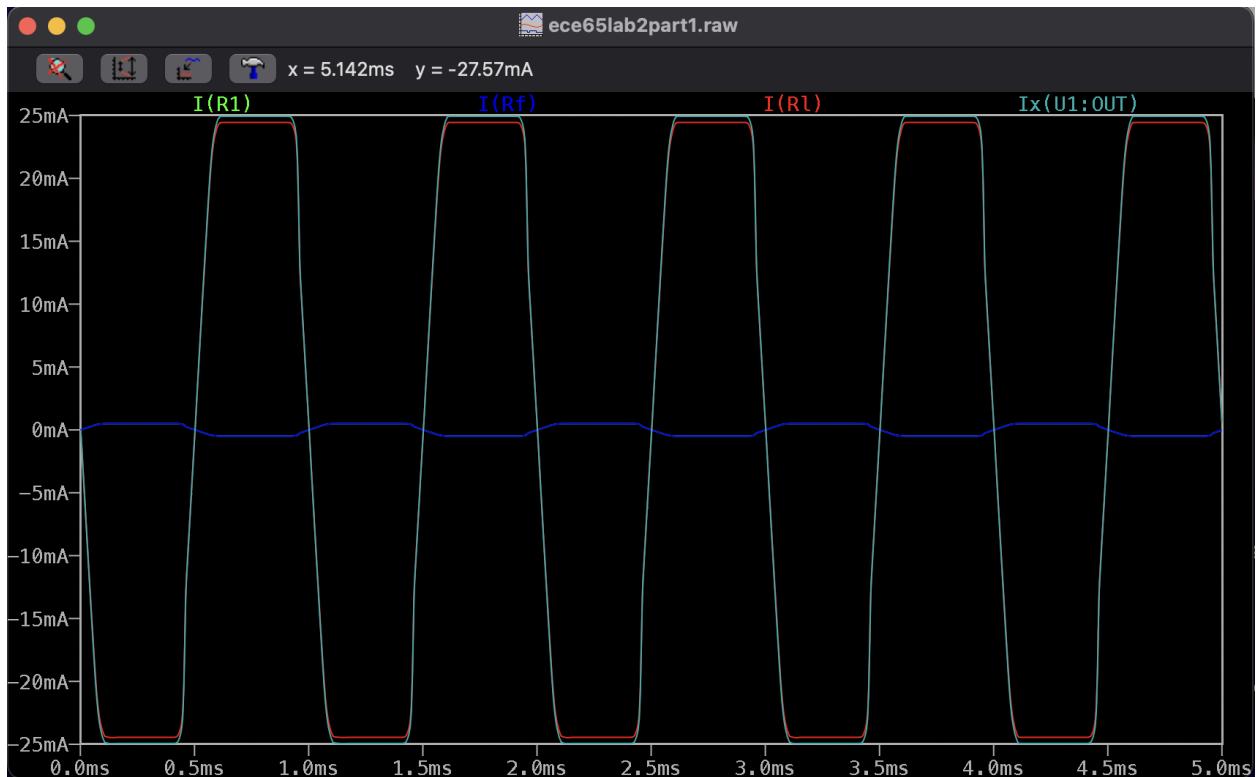
Part 4:

Simulate the circuit with PSpice/LTspice using a sinusoidal input signal v_i with the peak amplitude $V_p = 1V$ and the frequency $f = 1\text{ kHz}$. Use the load resistor $R_L = 200\Omega$.

1. Run Transient (Time domain) Analysis for 5 ms.
2. Plot the input and output waveforms on the same graph.



3. What is the peak value of the output voltage waveform? $\sim 4.8\text{ V}$
4. Plot the currents i_o , i_f , i_L , and i_{R1} .



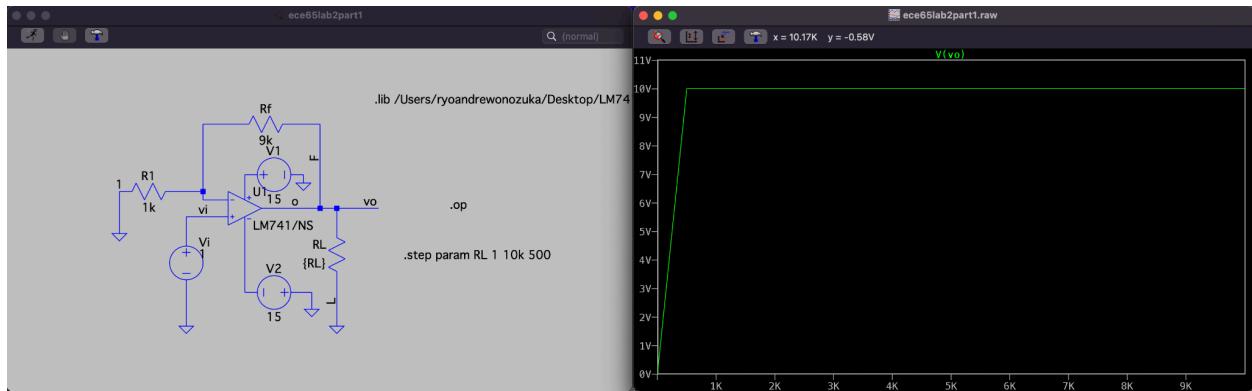
$I(R1)$ and $I(Rf)$ both alternate between $\pm 500\mu\text{A}$.

5. Explain your observation.

The output voltage v_o is limited by the op-amp's maximum output current, which is why we see that it is not consistent with the expected gain amplitude. The LM741 op-amp cannot maintain the ideal gain of 10 when the load demands a current exceeding its limit, resulting in saturation at $\pm 5V$.

Part 5:

Simulate the circuit with PSpice using a DC input signal ($v_i = 1V$).



1. Run a parametric SWEEP to generate a plot of v_o as a function of R_L for R_L ranging from 1Ω to $10\text{ k}\Omega$ (step size $500\text{ }\Omega$).
2. What is the maximum amplitude of v_o ?

10V

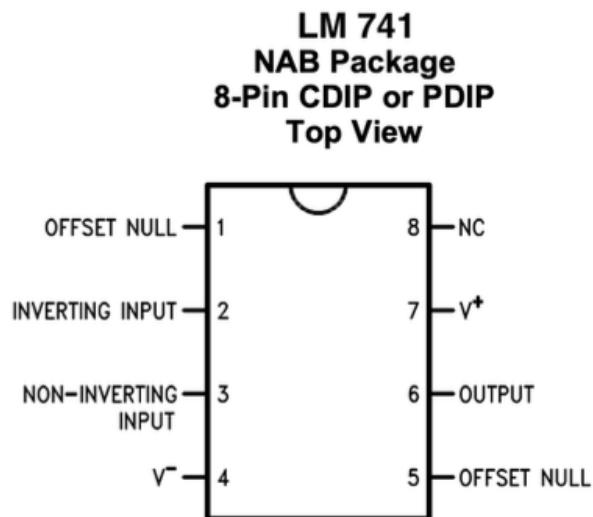
3. Does the result match your expectations?

Yes, the expected gain was 10V.

Lab exercise:

Build the circuit on the breadboard using an LM 741 chip. The supply terminals, pin 4 and pin 7 must be connected to $\pm 15V$. The balance terminals and pin 8 can be left "floating," i.e., not connected. Connect the resistors in the appropriate fashion to form the non-inverting amplifier.

LM741 pinout:



ti.com

Part 1:

Set the function generator to generate a sinusoidal waveform with a peak amplitude $V_p = 1V$ and the frequency $f = 1\text{ kHz}$ and use this waveform as the input voltage signal (v_I). Use $R_L = 1\text{k}\Omega$ in your circuit.

1. Measure the input and output waveform using the Oscilloscope.

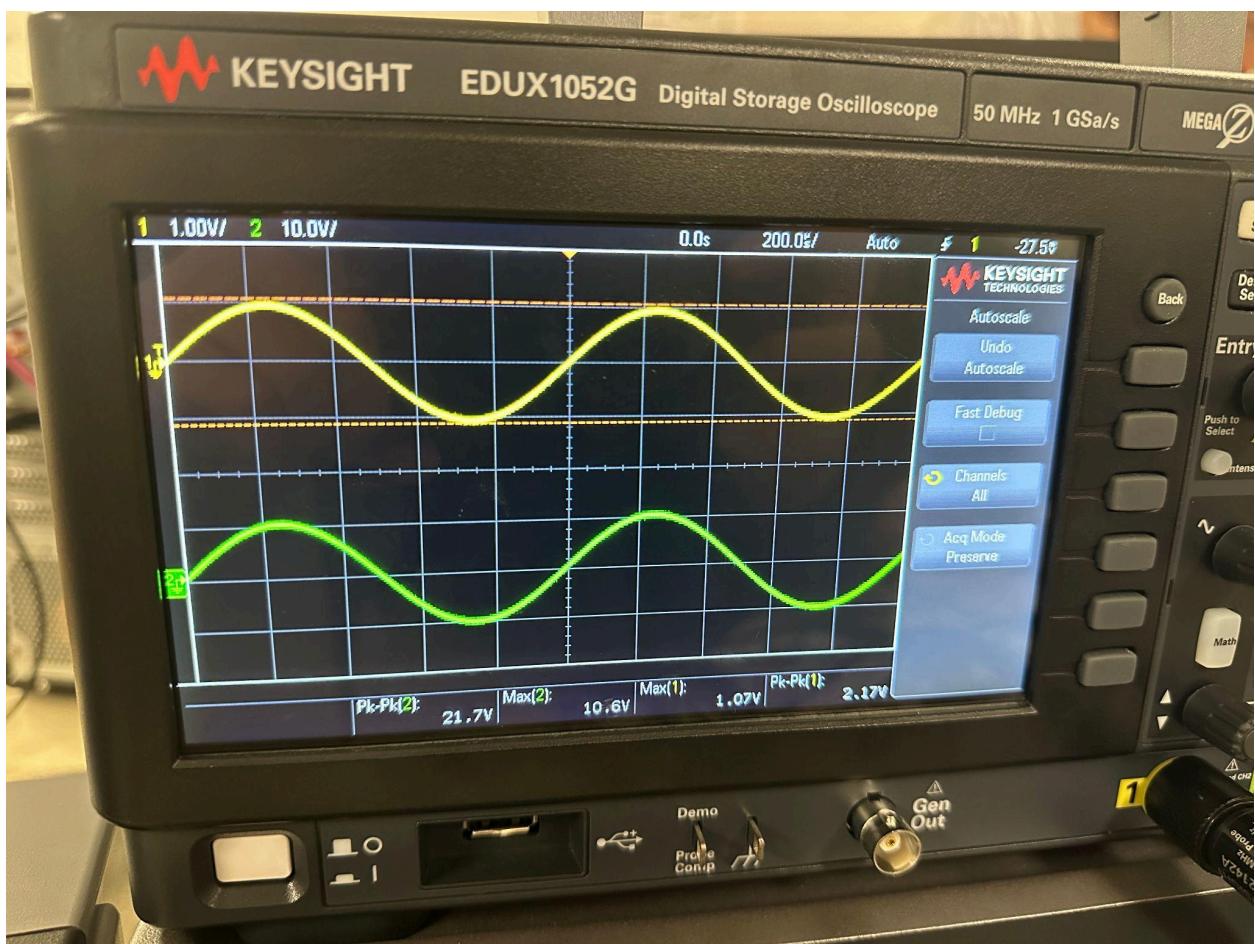
Output max: 10.6V

Input max: 1.07 V

2. Is the gain of the circuit as expected by the equations?

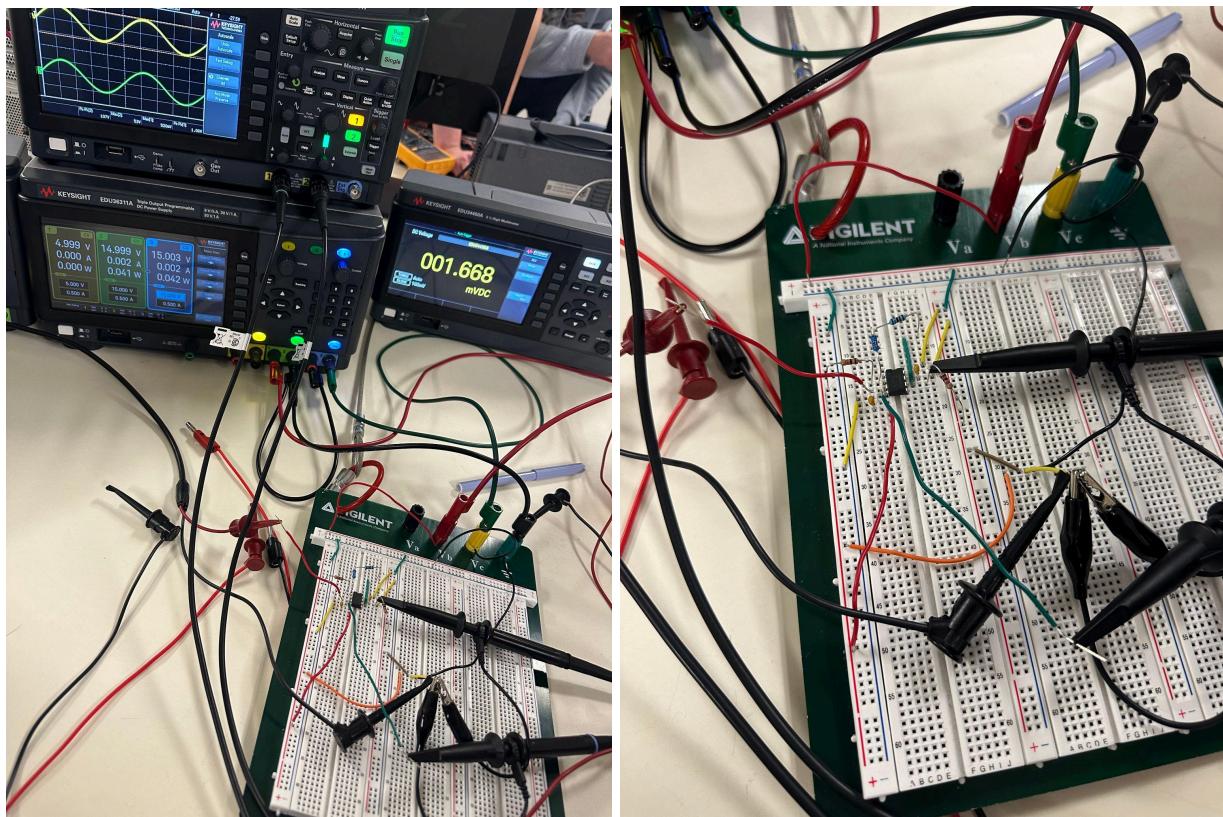
This gain is expected as it is around the ~ 10 amplifier as we were expecting from the calculations in the prelab.

3. Include the graphs of the waveforms in your lab report.



yellow: input
green: output

4. Include a photo of your circuit setup in your lab report.



Part 2:

Repeat Part 1 for a sinusoidal waveform with a peak amplitude $V_p = 1.5V$ and the frequency $f = 1\text{ kHz}$, and $R_L = 1k\Omega$

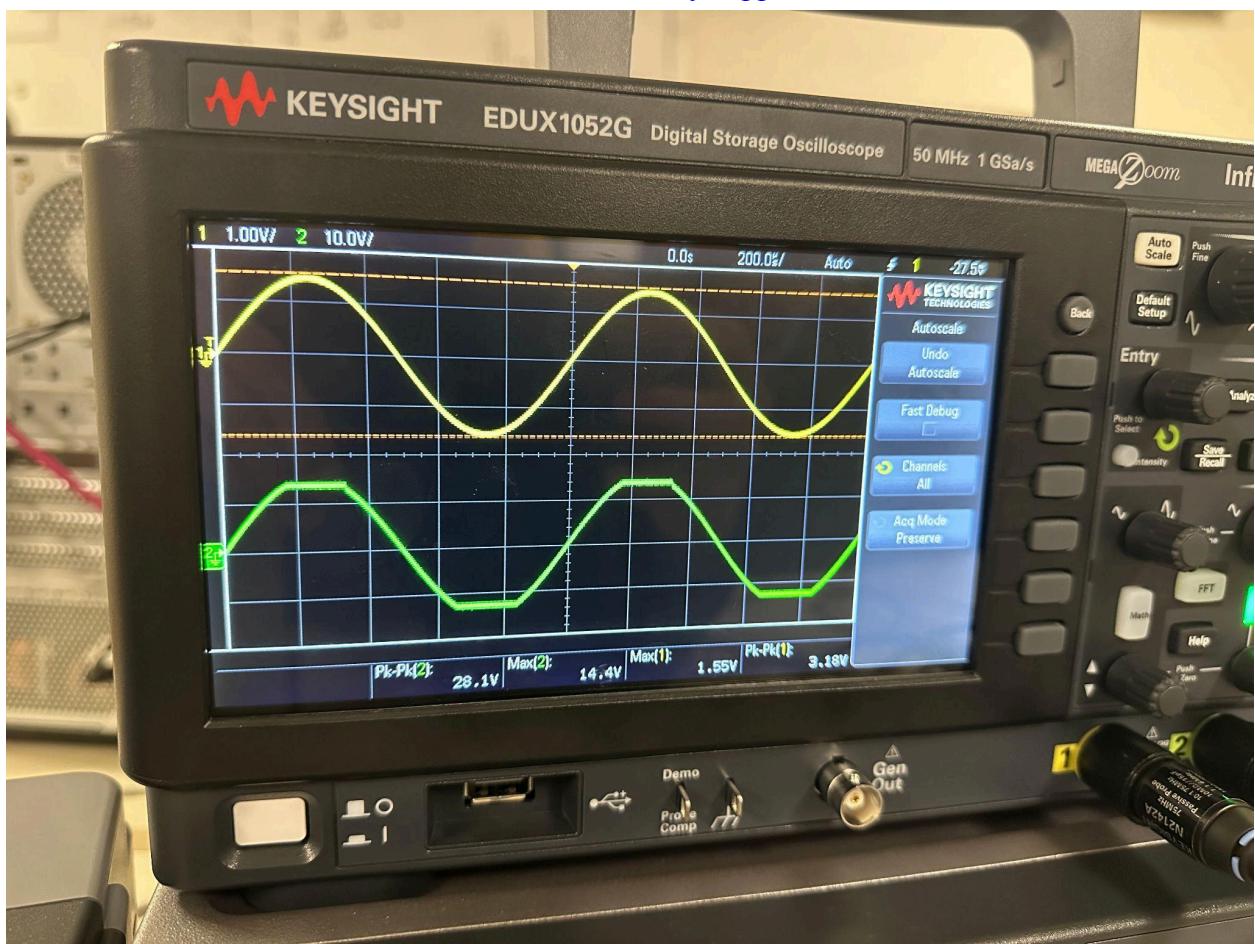
1. Measure the input and output waveform using the Oscilloscope.

Output max: 14.4 V

Input max: 1.55 V

2. Is the output waveform any different from the previous one? Explain your observation.

The output waveform is different, as we can see that we reach the saturation voltage which is around 14 volts. unlike the previous part where they were both smooth and similar looking sine waves, but here, we see that the bottom wave is clearly capped at the 14.4 V mark.



3. Measure the total output current



0.463mA

4. What is the limiting factor of the amplitude of the input signal?

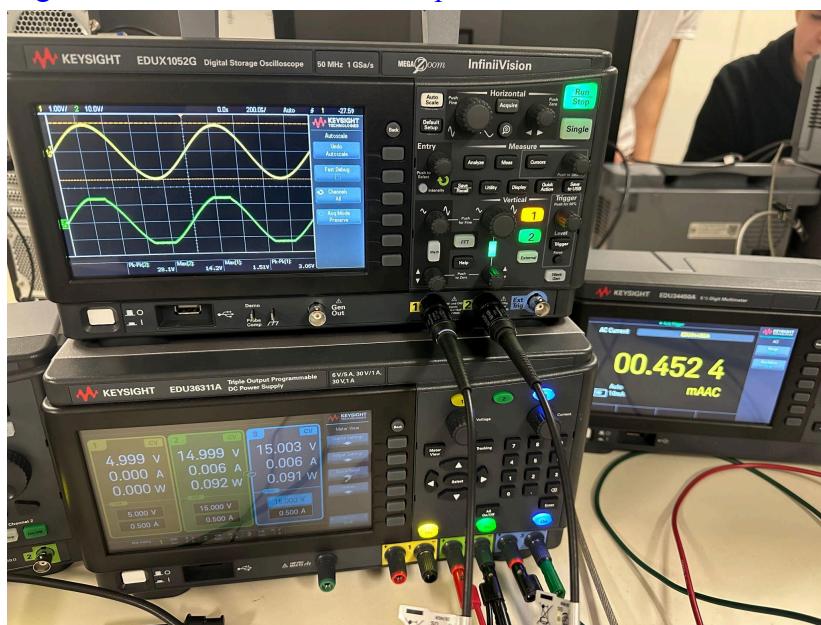
DC power supplies which in this case +/- 15V are limiting the output voltage. But this is the ideal number, so in real life, we got +/- 14 V as a saturated output voltage.

Part 3:

Keeping $R_L = 1k\Omega$ and using a sinusoidal input voltage, find the peak amplitude of the input voltage at which the output of the op-amp saturates.

1. What is the peak amplitude of the output current for this value of V_p ?

We adjusted V_p with values 2.5, 2.7, 2.8, 2.9 until we saw that the voltage values of the output no longer were 10 times that of the input. The current at 2.9 was ~0.45 mA.



Part 4:

Keeping $R_L = 1k\Omega$ and using a sinusoidal input voltage, find the peak amplitude of the input v
Set the function generator to generate a sinusoidal waveform with the peak amplitude of $V_p = 1V$ and the frequency $f = 1 kHz$ and use this waveform as the input voltage signal (v_i). Use a $10k\Omega$ potentiometer as the load. Set the value of the potentiometer to its maximum $10k\Omega$ and gradually decrease R_L .

1. How does the output voltage waveform change when you reduce the value of R_L ?

As R_L decreases, the output voltage drops and eventually saturates due to the op-amp's current limit.

2. For what R_L value will the output of the op-amp saturate?

$\approx 560mA$

3. What is the maximum peak amplitude of the op-amp output current?

$25mA$

Experiment 2: Op-amp weighted summer

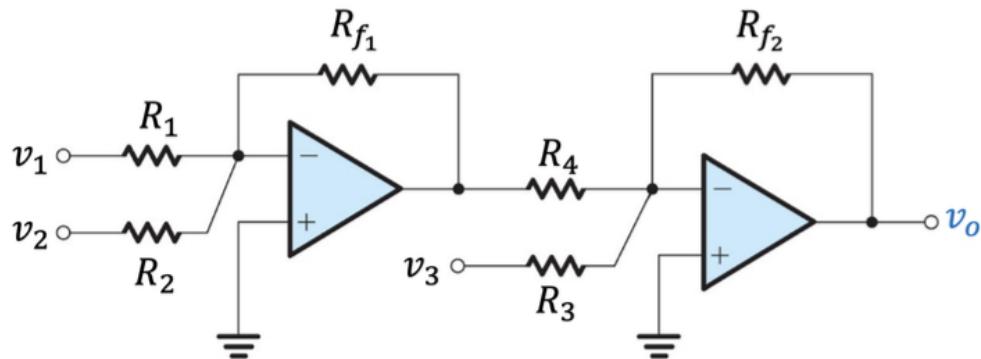
In this part of the experiment, we will design a summing amplifier in the inverting configuration. This circuit can be used to design and test standard mathematical linear equations and see the different results in terms of the output signals. The following diagram represents a summing amplifier.

Include your explanations, circuit analysis, plots, etc. here.

Prelab:

Circuit analysis

1. Using commercially available resistors, design the following circuit to implement the function of: $v_o = 2v_1 + v_2 - 4v_3$ Use resistor values between 500Ω and $100 \text{ k}\Omega$ in your design.



$$R_f1 = 2 \text{ k}\Omega * 6 = 12 \text{ k}\Omega$$

$$R_1 = 1 \text{ k}\Omega * 6 = 6 \text{ k}\Omega$$

$$R_2 = 2 \text{ k}\Omega * 6 = 12 \text{ k}\Omega$$

$$R_f2 = 2 \text{ k}\Omega * 6 = 12 \text{ k}\Omega$$

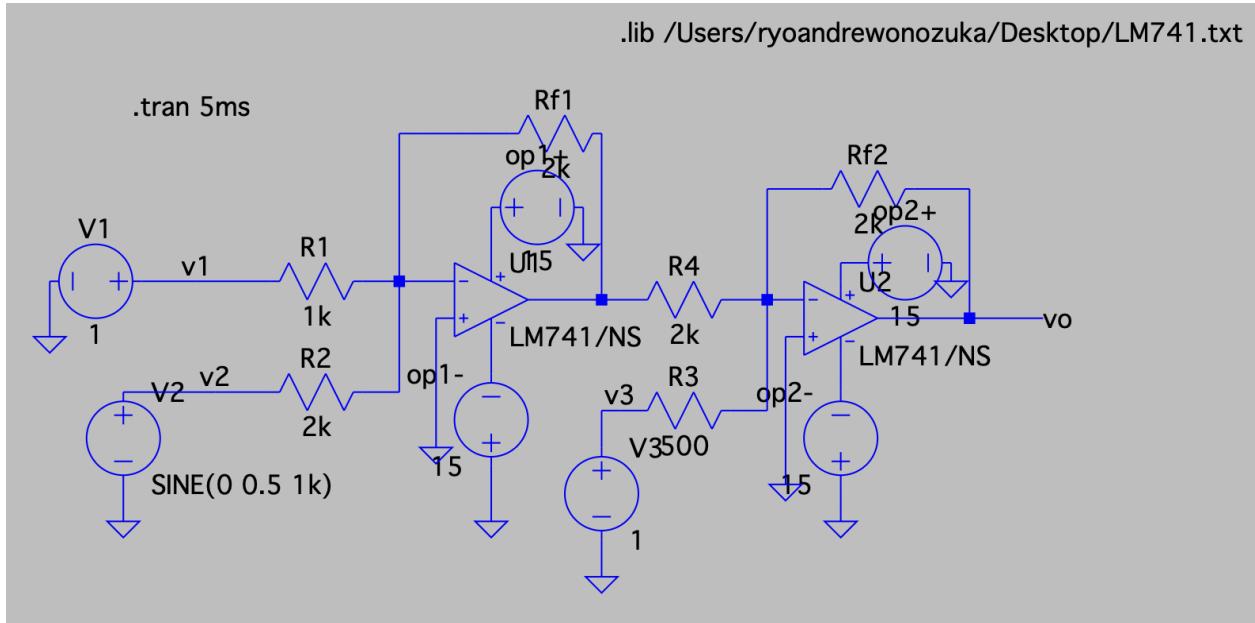
$$R_3 = 500 \Omega * 6 = 3 \text{ k}\Omega$$

$$R_4 = 2 \text{ k}\Omega * 6 = 12 \text{ k}\Omega$$

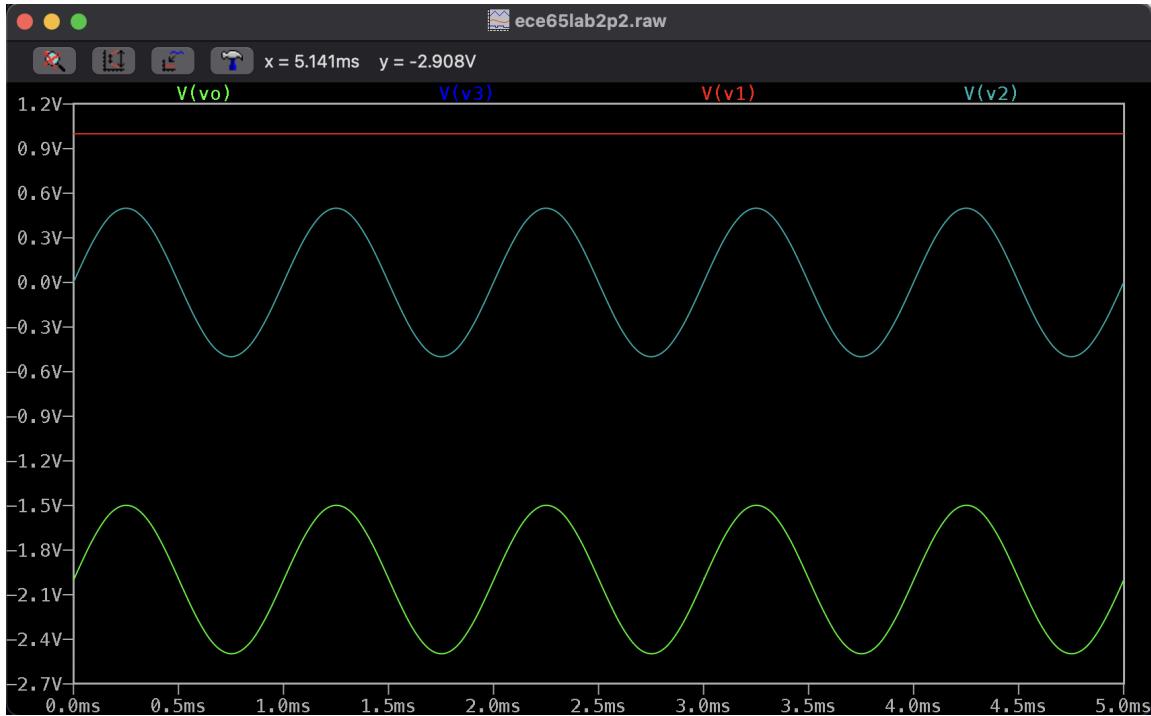
for our actual circuit we multiplied by 6 as there were not enough $1 \text{ k}\Omega$ resistors left.

Simulation

1. Use two DC voltages sources as v_1 and v_3 and a sinusoidal with $f = 1 \text{ kHz}$ from the function generator as source voltages. Use the voltage source amplitudes that you calculated in your prelab.



2. Run Transient (Time domain) Analysis for 5ms.
3. Plot v_1 , v_2 , v_3 , and v_o waveforms on the same graph.

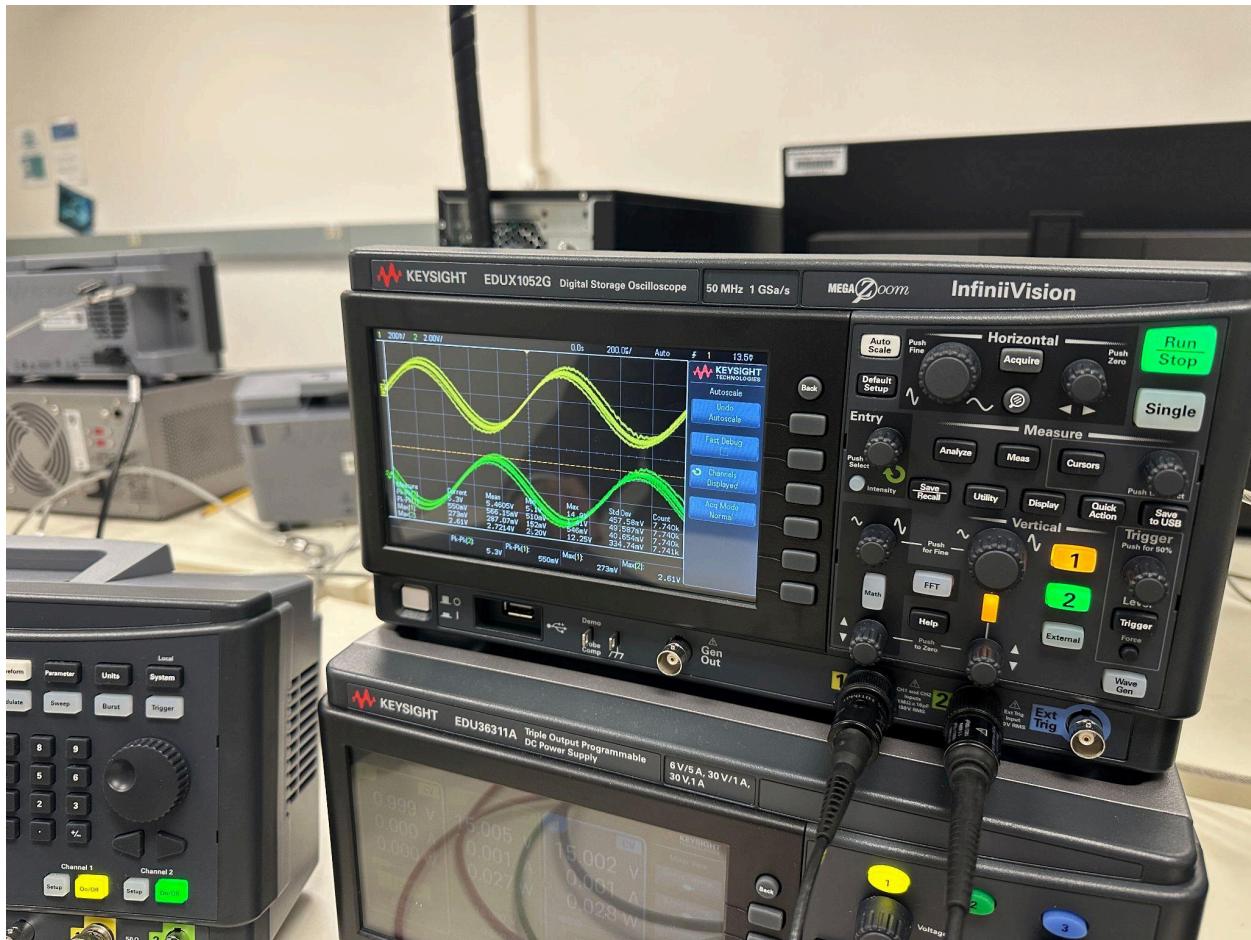


V1 and V3 both 1V.

Lab exercise:

Build the circuit on the breadboard using two LM741 op-amps.

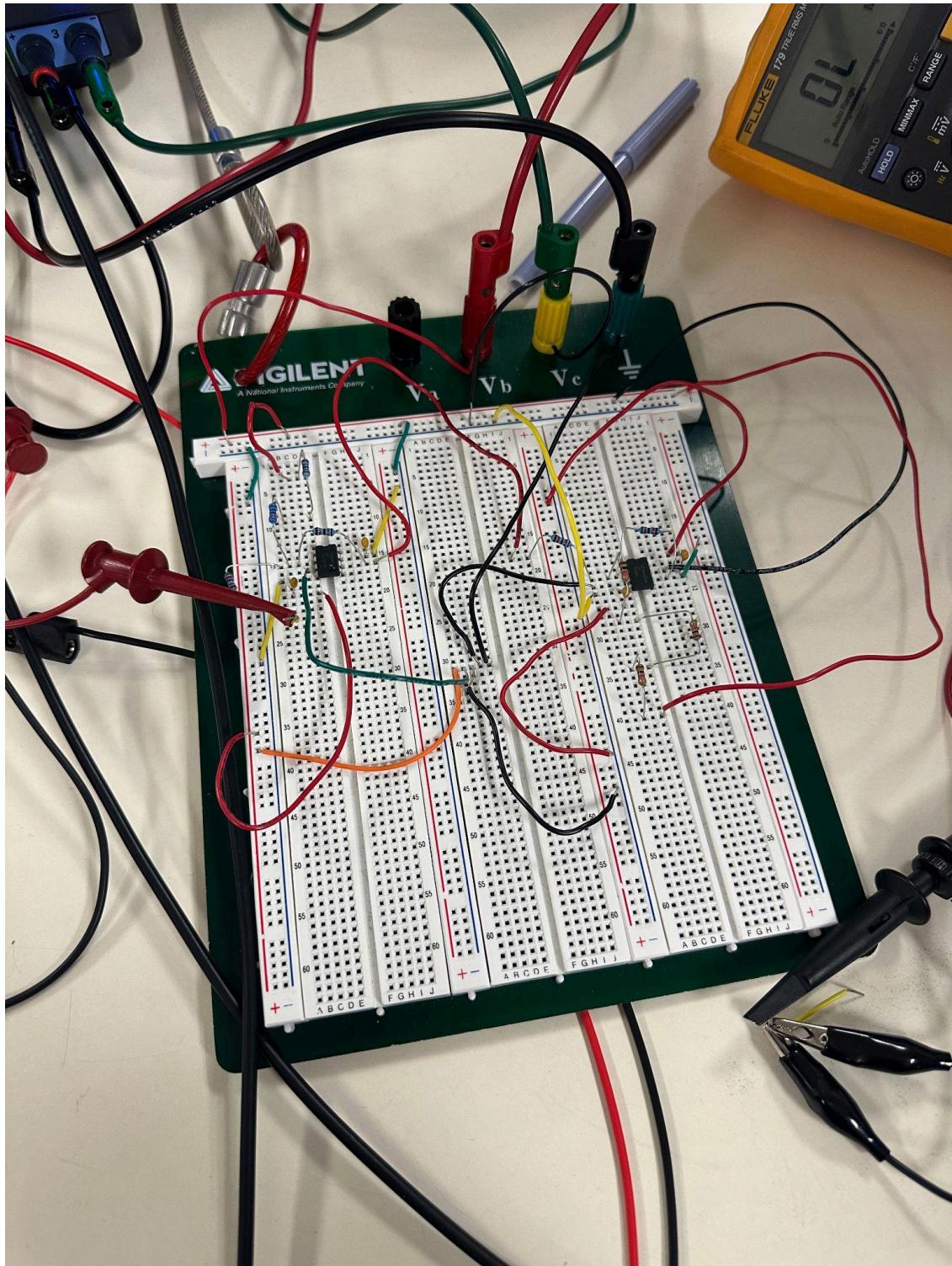
1. Use two DC voltages sources as v_1 and v_3 and a sinusoidal with $f = 1 \text{ kHz}$ from the function generator as source voltages. Use the voltage source amplitudes that you calculated in your prelab.
2. Measure the voltage waveforms at the output of each op-amp using the oscilloscope and include a photo of these waveforms in your report.



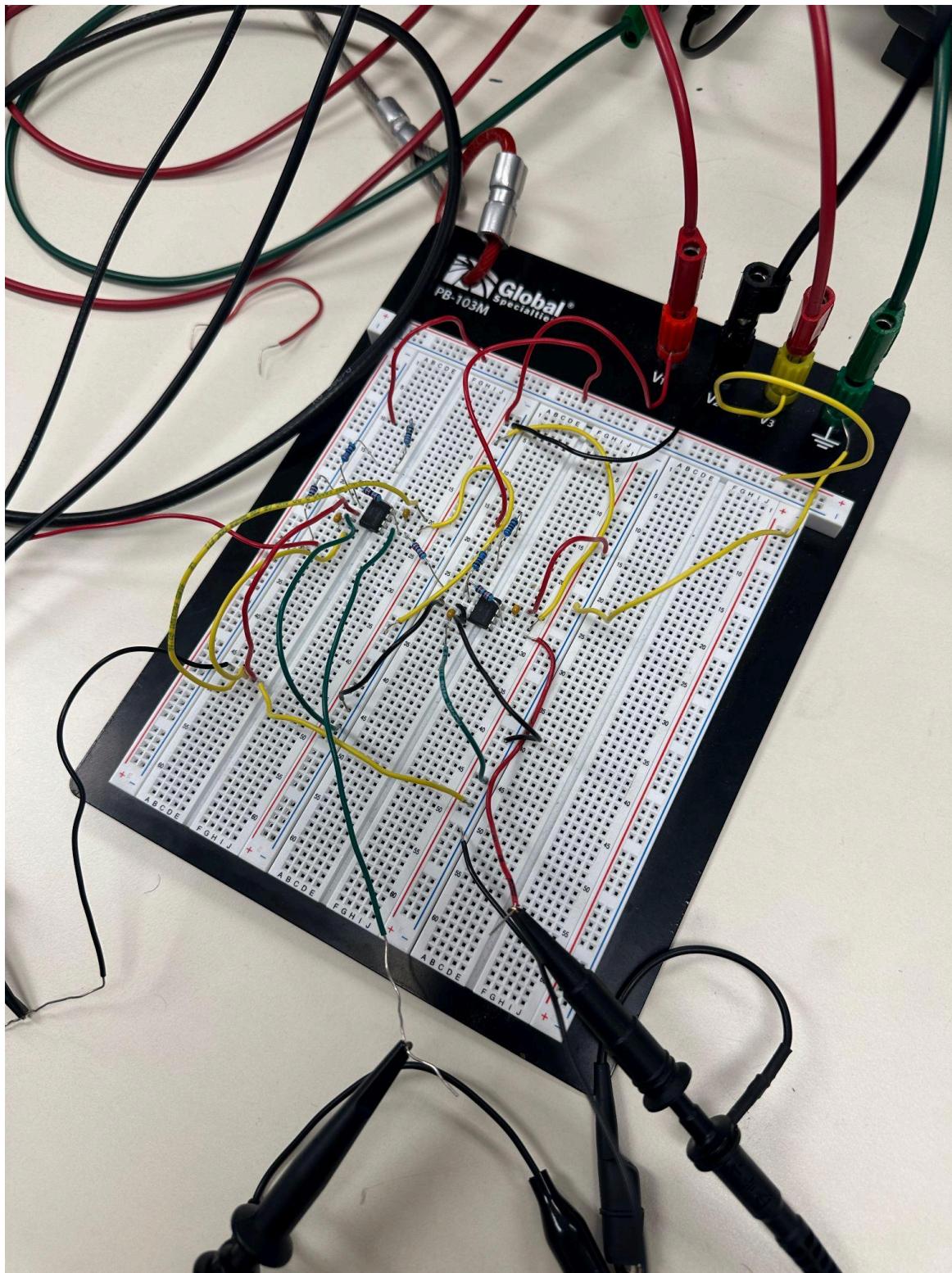
3. Do the results match your expectation?

We were unable to get the same results as the simulation (not sure if the oscilloscope probes were on amplifier mode or not). We ran out of time in our regular lab hours where we were unable to get an output despite help from our TA David Salzmann. Riku and I ended up going to the lab and we were able to make the circuit work and produce an output, but we were unable to make the graph stabilize (even with capacitors), due to some issue with the input voltage v_1 into the inverting input of the first opamp.

4. Include a photo of your circuit setup in your lab report.



Thursday January 16, 2025 during regular Lab Hours, unable to get an output reading



Tuesday January 21, 2025 came on our own to try and finish output reading

Conclusion

Include your conclusion here.

In this lab, we investigated the behavior of operational amplifier circuits in two configurations: as a voltage amplifier and as a weighted summing amplifier. Through the prelab and lab portions, we observed how the LM741 op-amp works.

In the first experiment, we analyzed the LM741 op-amp as a voltage amplifier. Simulations demonstrated that the op-amp operates linearly within its saturation limits, achieving a gain of approximately 10 as expected. The output voltage saturated at around $\pm 14V$, constrained by the $\pm 15V$ power supply and the internal limitations of the op-amp. The maximum output current was observed to reach the specified limit of 25 mA when the load resistance decreased significantly, which led to output voltage distortion. We were able to verify the theoretical and simulated expectations during the lab and see the op-amp's behavior under different input and load conditions.

In the second experiment, we designed and implemented a weighted summing amplifier to achieve the mathematical function $v_o = 2v_1 + v_2 - 4v_3$. Due to limited availability of standard resistors, we scaled the resistor values in the circuit design during the prelab. LTspice validated that the circuit met the desired function with accurate output waveforms reflecting the weighted contributions of v_1 , v_2 , and v_3 . For the lab portion, while we successfully implemented the circuit after troubleshooting and adjustments, stabilizing the output remained challenging due to input voltage inconsistencies. At the very least, however, we were able to achieve an output voltage graph and check to see that the summing amplifier was working.