# Silicon Detector Fabrication Overview

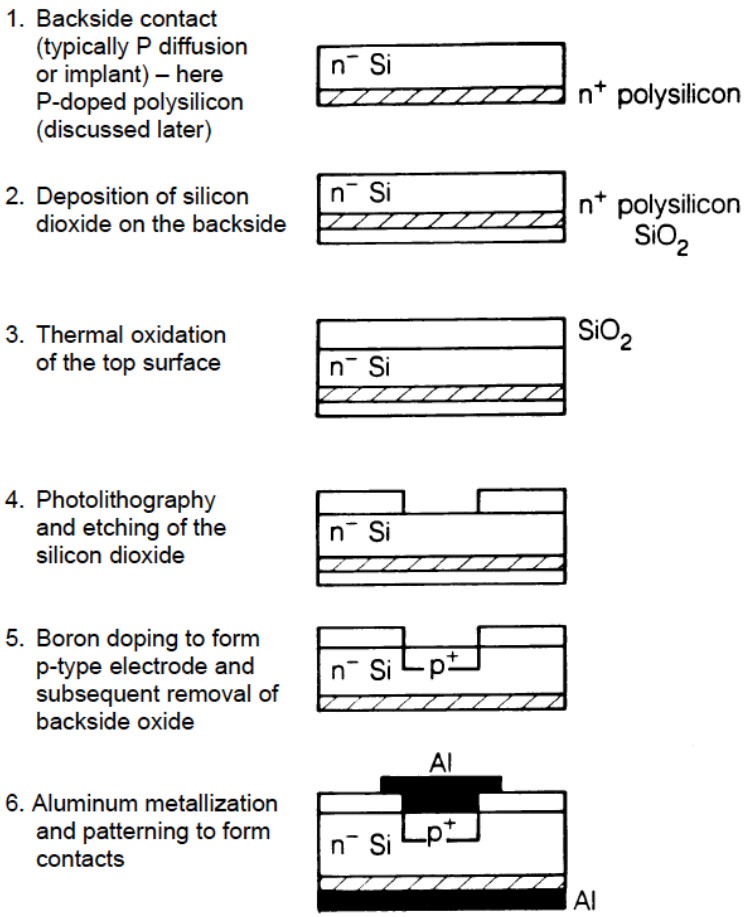
Ronald Lipton, Fermilab

Thanks to Thomas Bergauer for helpful comments

# Introduction

We will provide an overview of the fabrication process development and implementation for silicon diode detectors. Along the way we will provide examples from work with NHanced, Infineon and HPK.

- Materials
- Impurities and leakage currents
- Patterning and masks
- Etching
- Implantation
- Annealing
- Oxide growth
- Backside contacts
- Passivation and sintering
- Process Modelling
- Examples

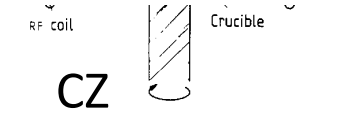


# Materials

Most silicon detectors begin with silicon boules with high resistivity material. This can be:

- Czochralski – pull from crucible melt
  - Impurities migrate from crucible
- Float zone
  - Mobile impurities are removed by “zone refining” passing heated coil through a polycrystalline rod – no crucible
- Epitaxial - Deposit silicon layer on existing crystal surface from precursor gas in reactor
  - Limited thickness, prone to stacking faults
  - Resistivity can be controlled and varied during the deposition
- Bonded wafers
  - Directly bond wafers of different resistivities
  - Issues with voids, crystal continuity

Wafers must be cut from boule, ground and single or double sided polished. Standard thickness for 8” is 725 microns.




CZ

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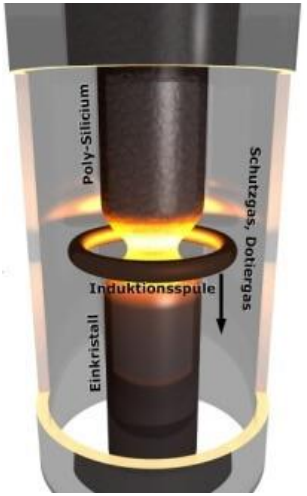
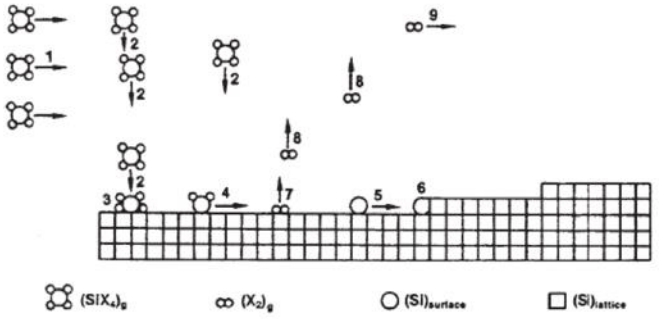
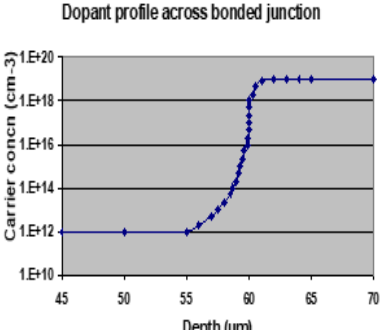
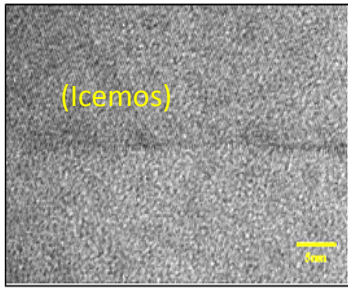
FZ




Silicon gas-phase epitaxy




High resolution TEM image of SiSi wafer interface



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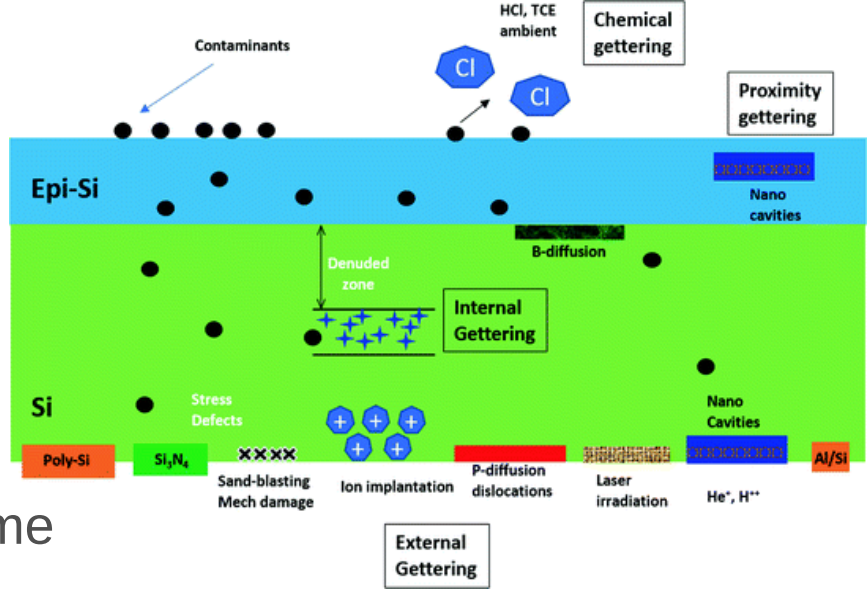
# Impurities

Even after FZ refining the silicon will contain impurities

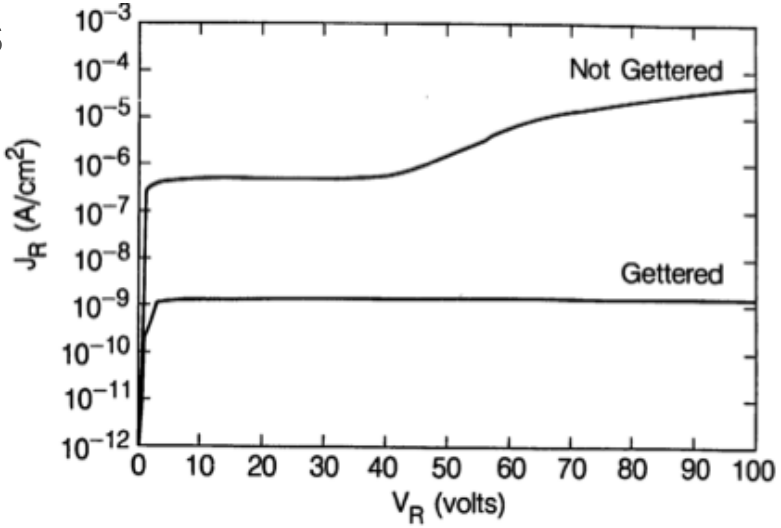
- Impurities, especially metal and alkali act as sources of leakage current
- Impurities are often mobile, not incorporated in the lattice – can cause time and bias dependent effects

Wafers can be gettered to remove impurities. Non-crystalline areas collect mobile impurities

- Intrinsic (gettering centers) / Extrinsic (surface treatments)
- Polysilicon backside deposits (LBL-CCD)
- Sacrificial oxide layer (SLAC/NHanced)
- Surface roughening (Nhanced – before SOI wafer bonding)
- Highly doped regions (Nhanced)




Claeys C., Simoen E. (2018) Gettering and Passivation of Metals in Silicon and Germanium. In: Metal Impurities in Silicon and Germanium-Based Technologies




(S. Holland)



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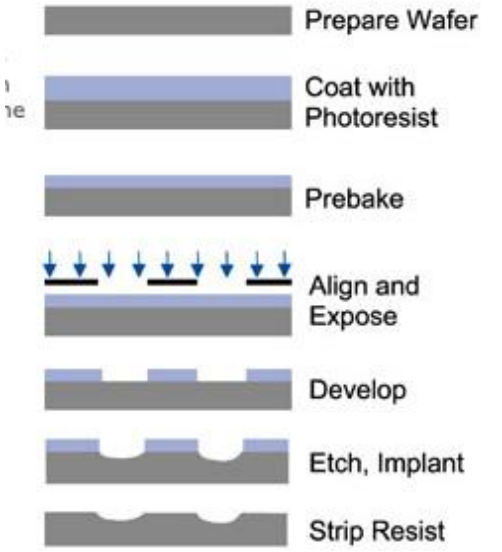
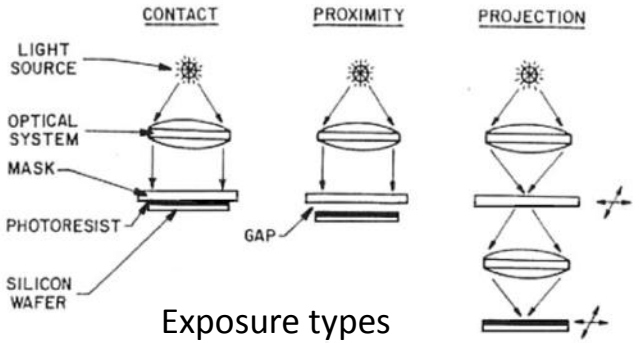
# Patterning

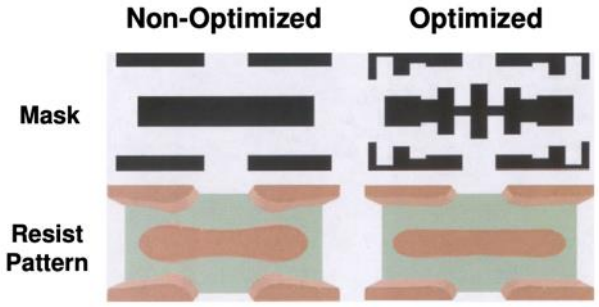
Patterns of implants, oxide openings and metalization are defined by photolithography. This uses masks to define affected areas.

- Masks are used to expose photoresists which are then developed to provide openings. Usually chrome on glass or quartz
- Full wafer masks (contact or proximity) have limited resolution, but can provide the complex HGCAL structures
  - Proximity resolution depends on gap and λ
- ICs are produced with reticule masks (~2x3 cm) with significant demagnification and complex optics.
  - Usually limited to one repeated set of devices – HPK used a few different reticules for 8” prototypes.
  - Can be “stitched” to provide more area – CMOS sensor R&D
  - Many tricks for deep submicron diffraction and sub λ effects– Proximity correction, phase shift masks, EUV
- Inter-mask alignment is critical – each vendor has recommended marks – start with L0 etch mark
- Direct electron beam writing on the resist can be used




Exposure types




Source: Socha, ASML (2004)

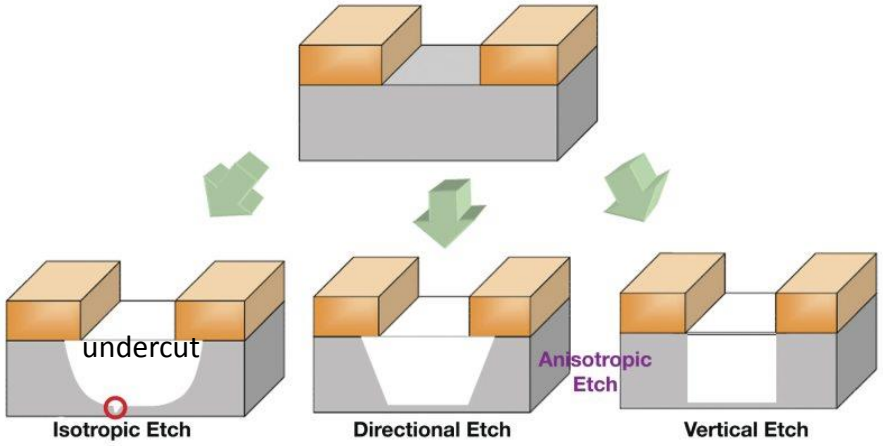
# Etching

Various layers must be etched to achieve the required pattern

Each etched material has specific characteristics – silicon/oxide/metal

- Etch rate and selectivity (mask choice)

Silicon can be etched chemically (wet) or by plasma (dry)




- Isotropic vs anisotropic
- Wet etch depends on crystal orientation and etch chemical – can be used for micromachining – beams and sensors

Plasma etch can reproduce mask shape with high aspect ratio and significant depth

- 3D detectors use Bosch etch – incrementally add material to sidewalls for high AR
- MEMs, trenches, isolation structures …

Variants/recipes to etch Al, $SiO_2$, SiN …

- Usually wet, but can use RIE

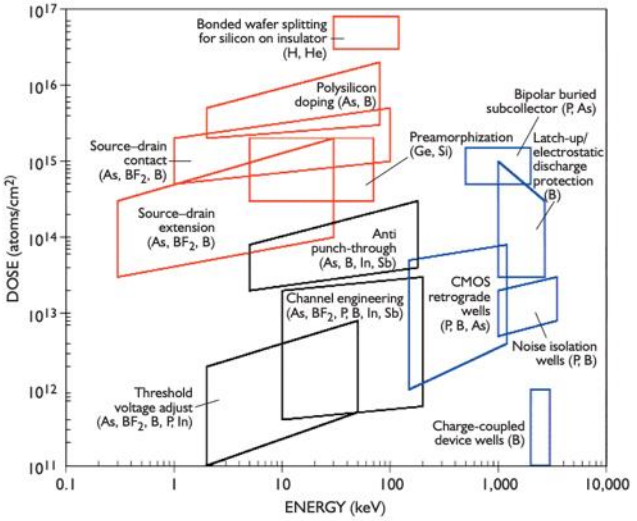
Etch stops can be used for precise control -removal of silicon on $SiO_2$, doping dependent etch rate

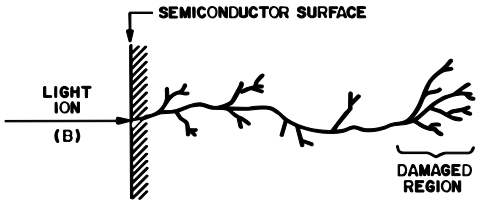
Burn resist off via plasma (ashing) or remove chemically

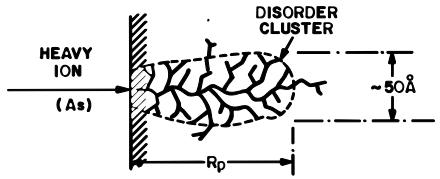
# Ion Implantation

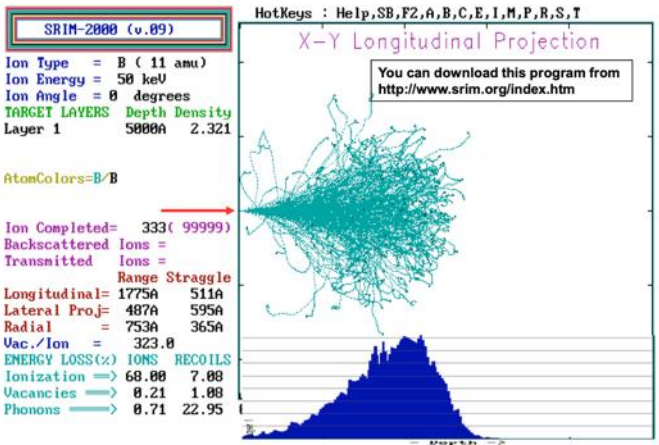
Controlled deposition of impurities to create junctions, wells and contacts. Usually accelerator-based implantation (diffusion also used).

- Pattern defined by resist/oxide mask
  - Oxide can be used to complement resist - compatible with high temp processes (SLAC)
- Energy controls depth and distribution
  - Multi-charged ions to increase energy (LGAD)
- Each ion type has characteristics
  - Light ions, HE - electronic stopping
  - Heavy ions, LE – nuclear stopping
    - More crystal damage (amorphisation)
  - SRIM MC simulation and TCAD
- Implant at angle to avoid channeling
- Measure with SIMS or profile resistance
- Implanted ions damage the crystal structure and need to be incorporated into the crystal lattice. -> annealing



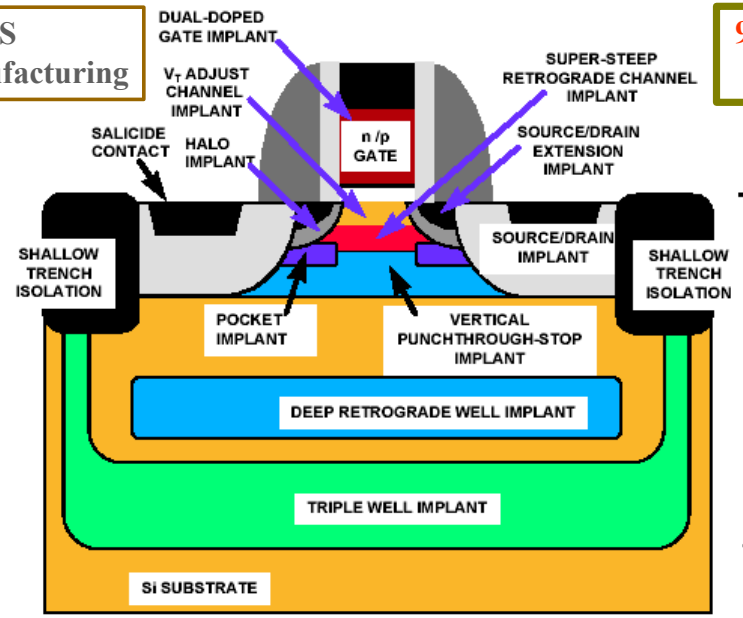



# Implantation - Examples

CMOS Manufacturing

9-10 different I/I identified !

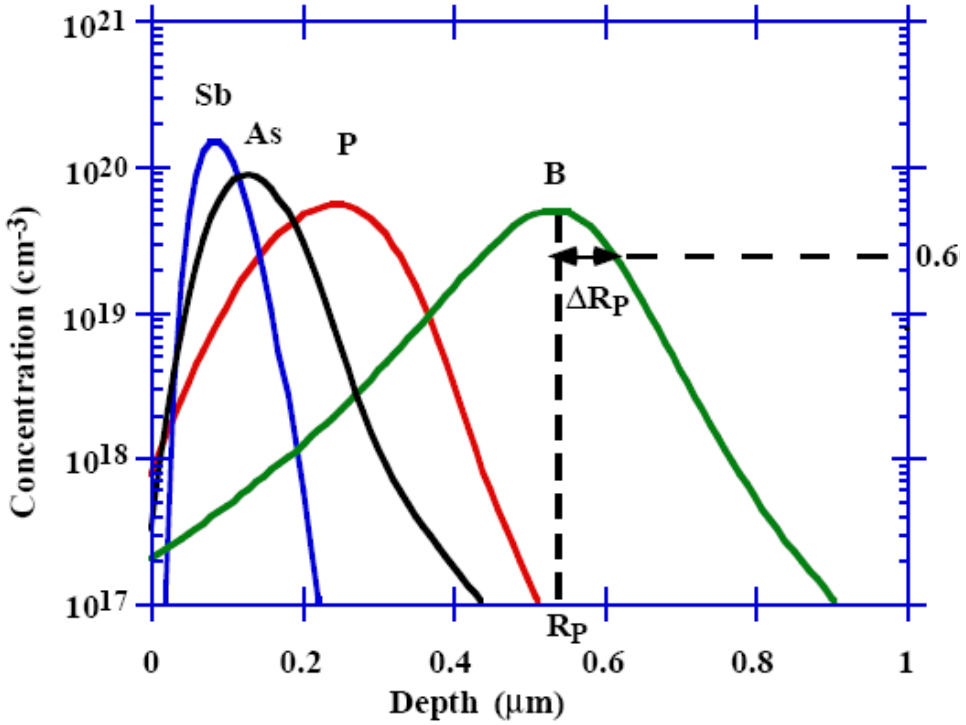



Source/Channel/Drain
50-200 nm deep
$10^{17}$-$10^{20}$ atoms/cm$^3$

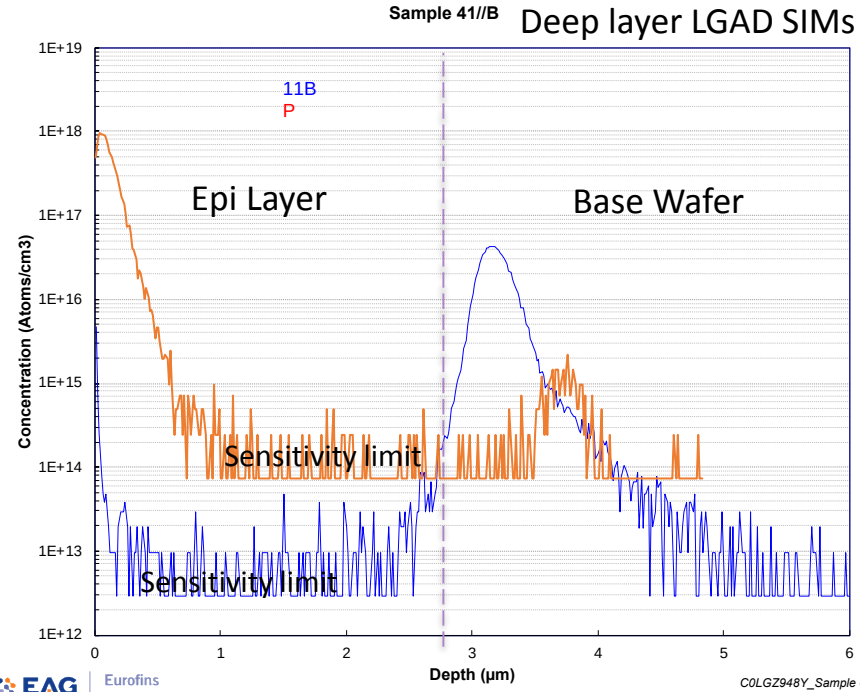
CMOS Well
500-3000 nm deep
$10^{15}$-$10^{17}$ atoms/cm$^3$

Implants in a CMOS transistor

50 keV ions of various species




Deep layer LGAD SIMs



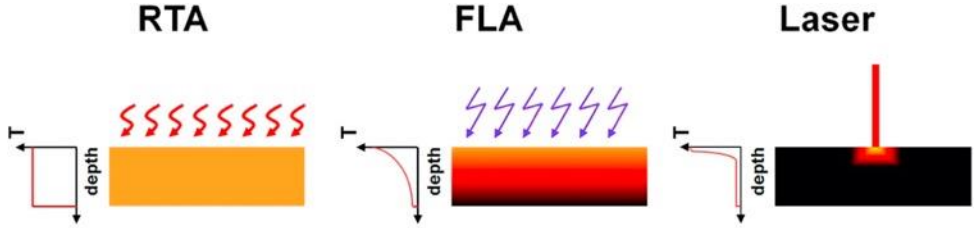

EAG Laboratories | Eurofins Materials Science

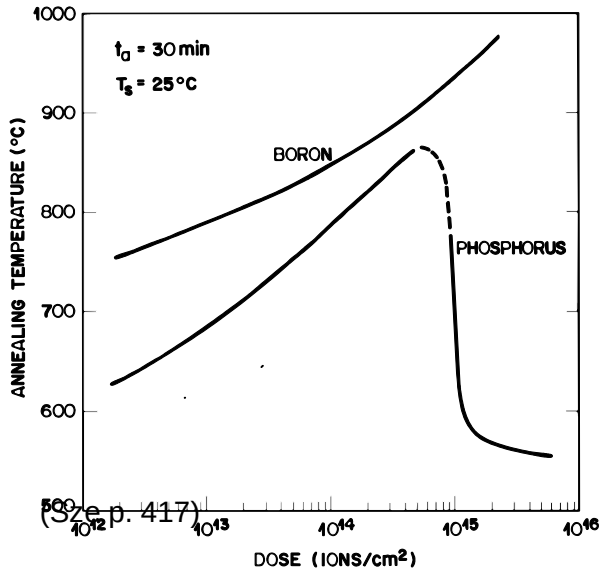
C0LGZ948Y_Sample 41 B
12/15/2020

# Annealing

The implanted wafer must be annealed to restore the crystal structure and incorporate dopants into the lattice

- Not all dopants are activated – measure resistivity
- Thermal annealing causes diffusion of the implants – could be an issue (CMOS, LGAD)
- Usually a high temperature process – must be done before metalization
  - Furnace anneal 900-1100 deg
  - Rapid thermal anneal (RTA) – limit diffusion – infared lamps
  - Laser anneal – local heating (preserve top metal) – minimal diffusion
  - Microwave anneal also limits diffusion




(S2e p. 417)

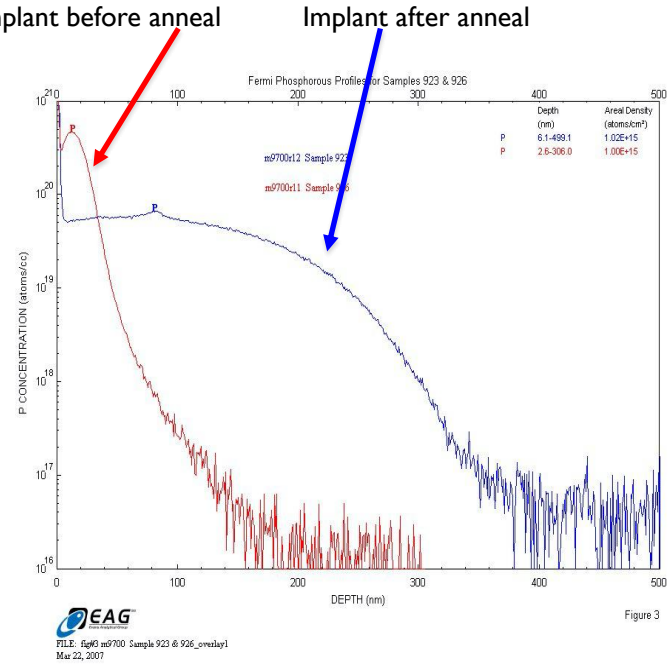
Fig. 30 Annealing temperature versus dose for 90% activation of boron and phosphorus ions.[2, 18]

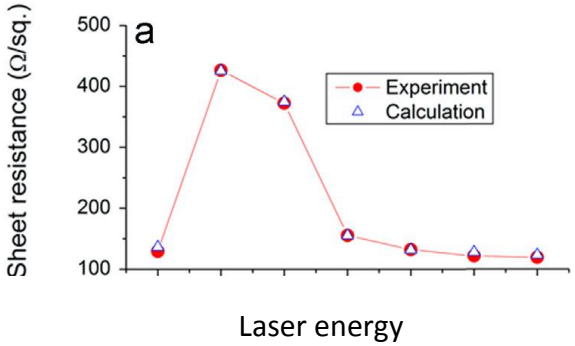


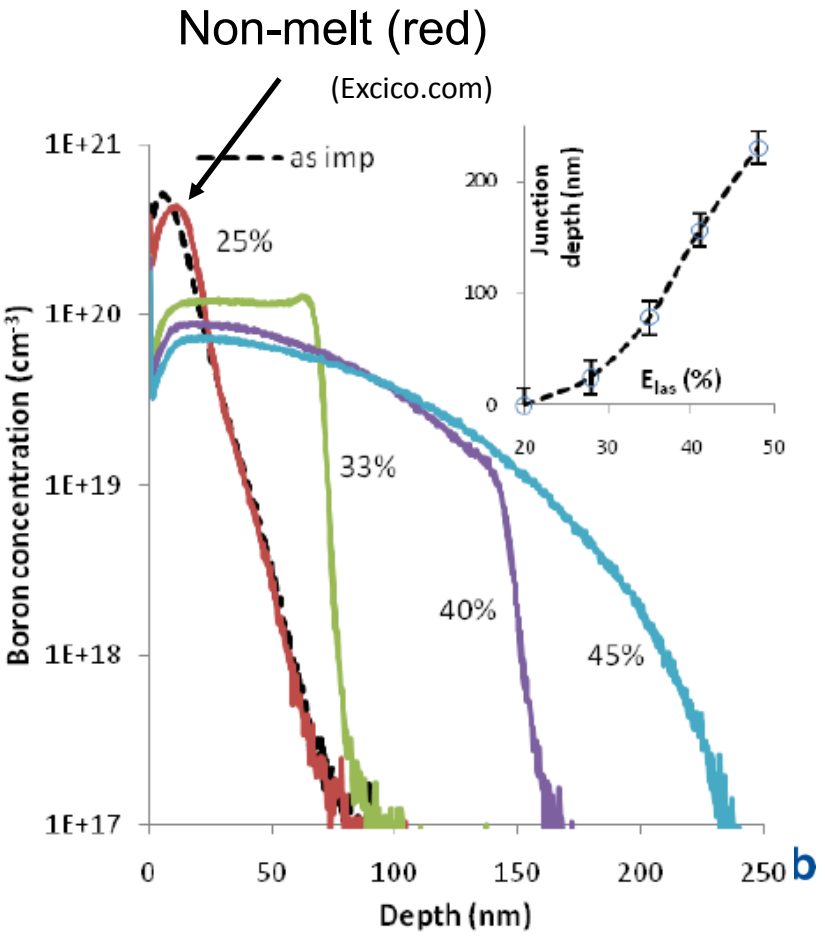
Materials Science in Semiconductor Processing
Volume 62, May 2017, Pages 115-127

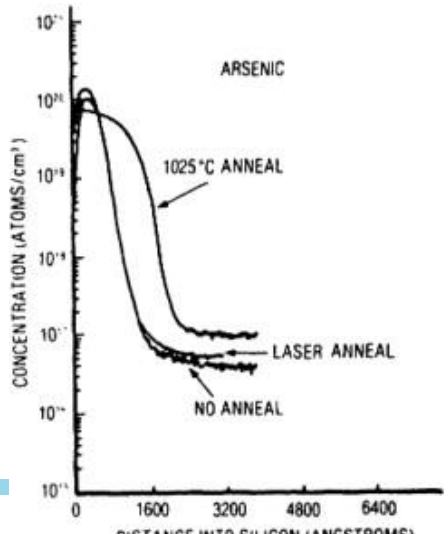
# Annealing examples

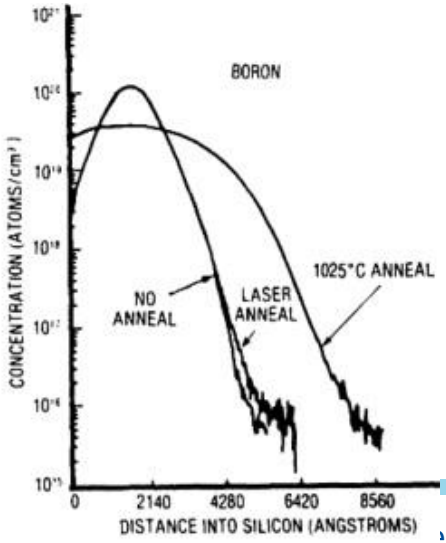
FNAL/Cornell
ILC studies



# Oxide Growth

One reason Si is the dominant semiconductor is the convenience of it's oxide as an insulator and base of subsequent layers.

- Oxide is grown at 800-1200 deg in either a dry or "wet" atmosphere

$$\mathrm{Si} + 2\mathrm{H_2O} \rightarrow \mathrm{SiO_2} + 2\mathrm{H_2}$$

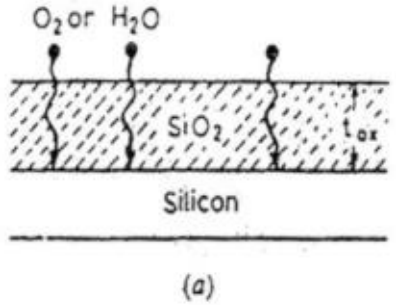
$$\mathrm{Si} + \mathrm{O_2} \rightarrow \mathrm{SiO_2}$$

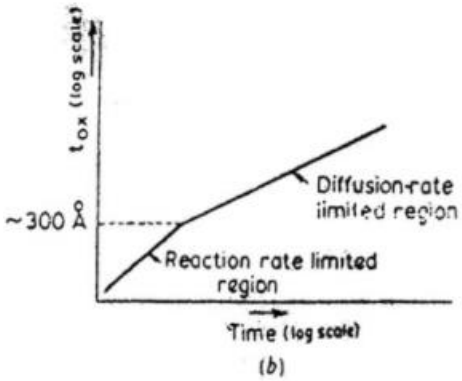
  - Wet is faster, but has more dangling bonds
  - Adding Cl can help immobilize sodium, increase rate..
  - Rate is orientation dependent (<100> slow)
- $O_2$ or $H_2O$ must diffuse through the existing oxide – growth rate slows with thickness
- Thermal oxidation "eats" silicon from the surface – the resulting device can have significant topography + stress
- Dopants can be incorporated or expelled – altering near-surface distributions
- Sandwich-structures are often used, the top layer is often doped glass to increase the conductivity slightly to prevent static charge-up

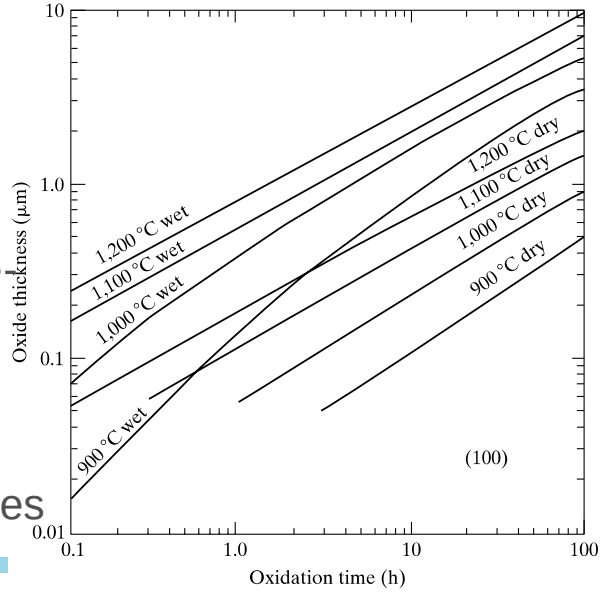
Deposited SiN is often used to improve HV performance and mask

Oxide layer can also be formed by chemical vapor deposition.

- This is less clean than thermal oxide, used in later stage processes



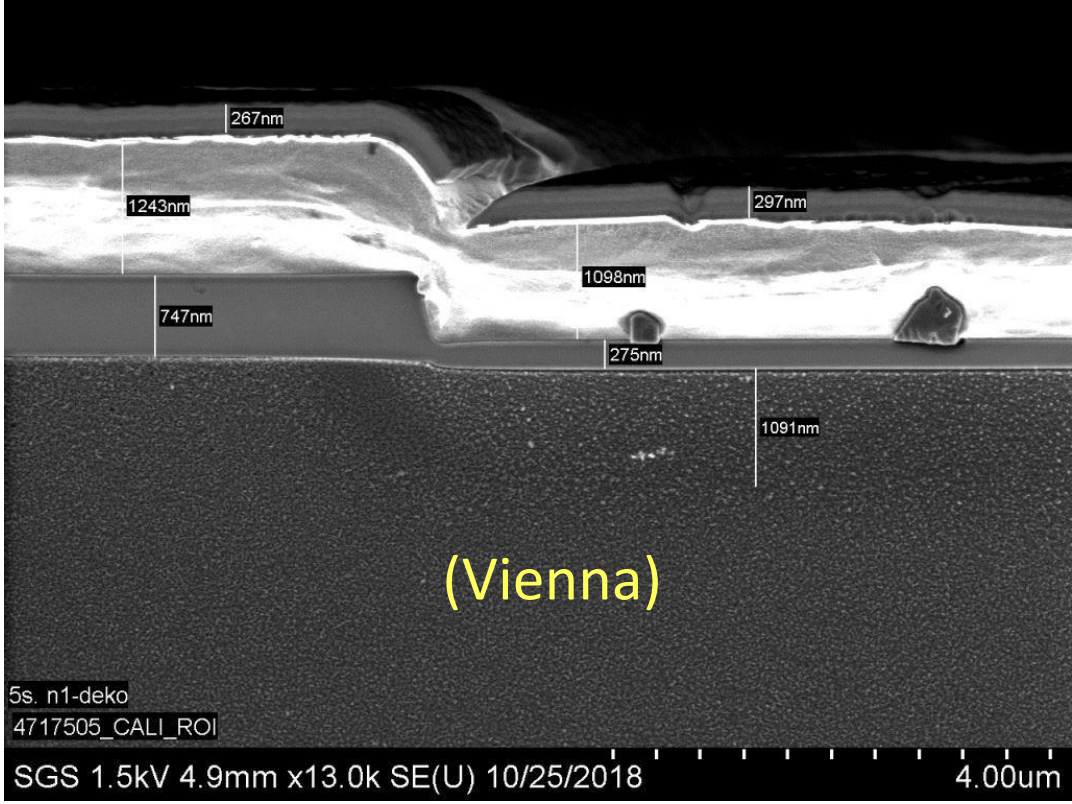




Chu - Device Fabrication Technology

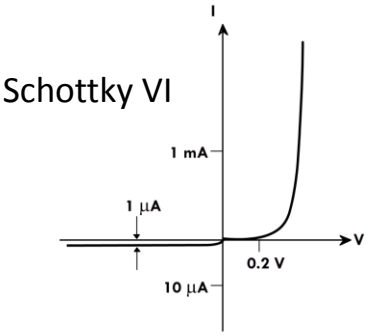
# HPK Stack

Dielectric is thicker in the un-implanted regions, and thinner above implants

- Oxide over implant is etched for implantation – generates topology
- Metal is 1243-1098 microns
- Passivation is 267-297 nm



# Contacts



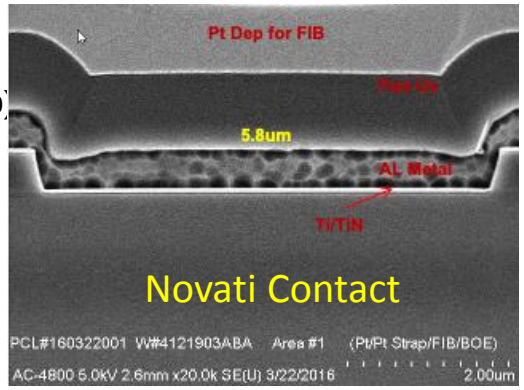

Contacts between silicon and the outside world need to be made

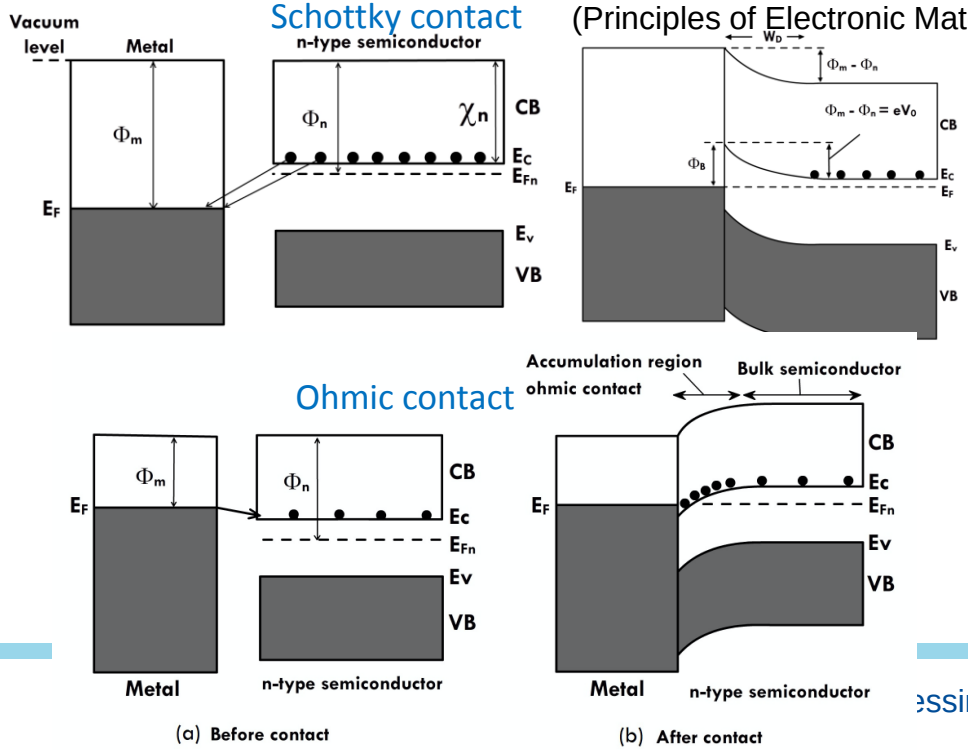
- Ohmic if possible – requires low resistivity silicon to metal
- Schottky – rectifying contact polarity dependent
- Sputtered or evaporated metal

Our contacts to the are typically ohmic with heavy (n+, P+) doping that minimizes barrier width ($X_{dep} \sim 1/N_{dop}$) and promotes tunneling through the metal-semiconductor junction.

Aluminum-silicon contacts are subject spiking – penetration of Al into the silicon bulk

- Avoided by adding 1-2% Si to aluminum (solubility limits Si diffusion into Al)
- Commercial devices usually use barrier metal stacks (Ni, W …)




Fermi levels line up after contact formation.

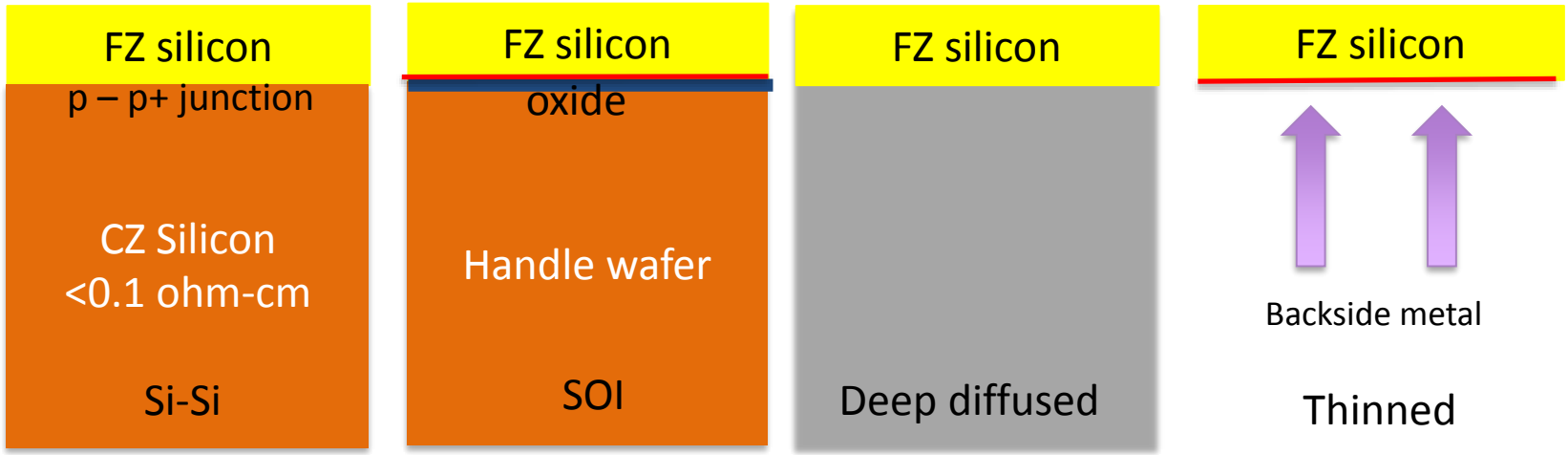
Shottky – electrons transfer to the metal, bands bend up, depletion region formed

Ohmic – electrons transfer to the semiconductor – high conductivity accumulation region formed.

# Backside Contacts

A central problem for our 8” wafers is the backside contact. Wafers are typically 725 microns thick. We must thin and implant a backside contact after frontside processing. If there is frontside metal we must limit annealing temperature to < ~ 500 degrees. There are several ways to do this:

- Process frontside metal on thin wafer (LBL CCD, Infineon)
- Bond FZ to low resistivity wafer (SiSi) – results like epitaxy …
- Implant backside before processing and bond device wafer to a support wafer (SOI, Novati/Nhanced)
- Fully process the front side and then implant and laser anneal the backside (CCDs, HPK?) The melt zone is limited to a small region in depth.
- Deep diffusion is not available on 8”

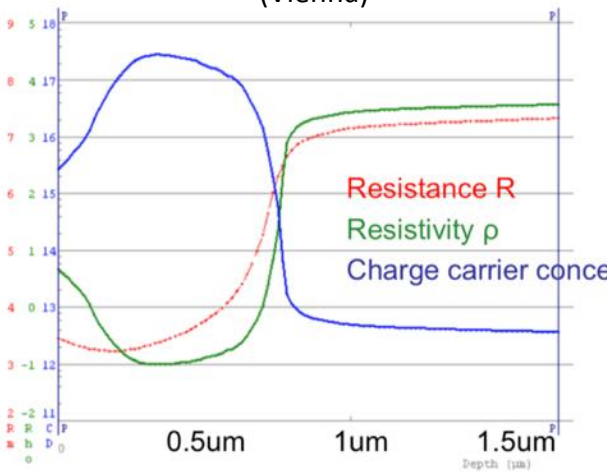


# HPK Guess

My guess is that HPK uses a laser anneal process

- They probably have one in house for their CCDs
- The depth of the annealed layer is limited by the laser anneal melt zone - related to the silicon melting point and thermal conductivity. This could be why the backside sensitivity cannot be avoided by increasing the implanted region.
- Profile not unlike high exposure laser – but not as deep (700 microns?)
- Other processes are likely more expensive – require wafer bonding or considerable special handling

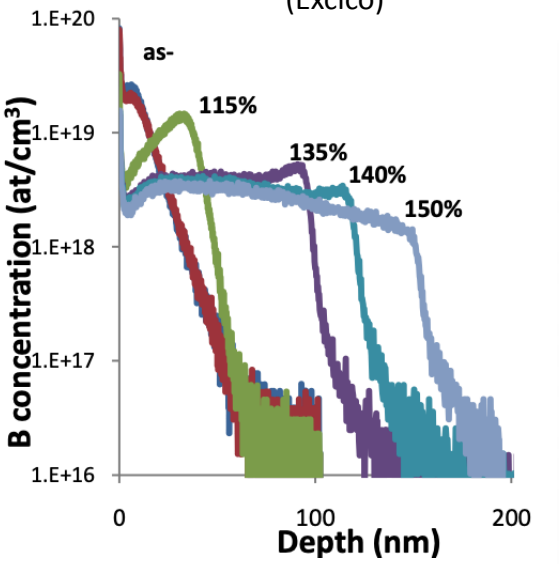
(Vienna)




Results for 8" HGCal sensors:

- **Backside doping depth ~ 0.7 µm!**
- Low doping concentration ~ $5*10^{17}$ / $cm^3$

(Excico)

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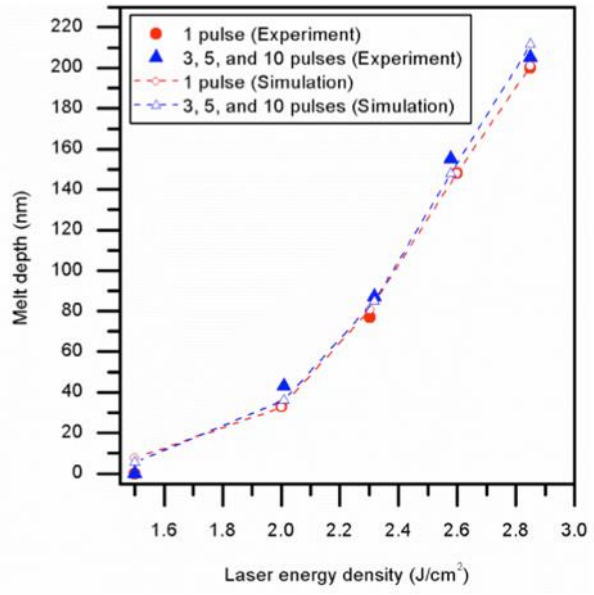
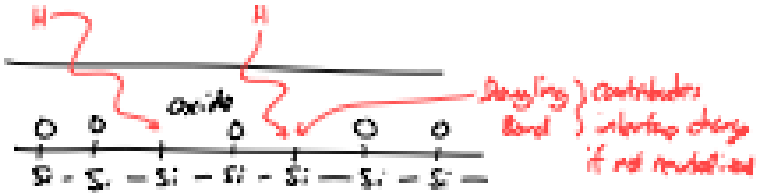


# Passivation and Sintering



Typically, wafers are sintered (heated to about 450º in forming ($H_2$+N) gas

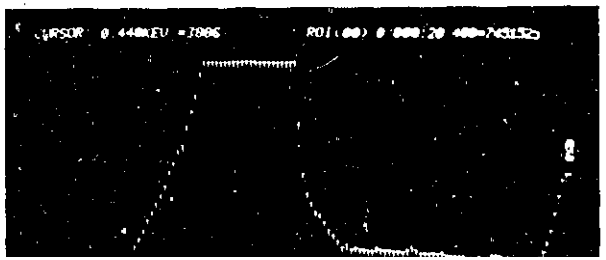
- $H_2$ passivates interface states
- This improves the Al-Si junction, repairs some oxide damage, reduces leakage currents, reduces spiking

Overall surfaces are then typically passivated:

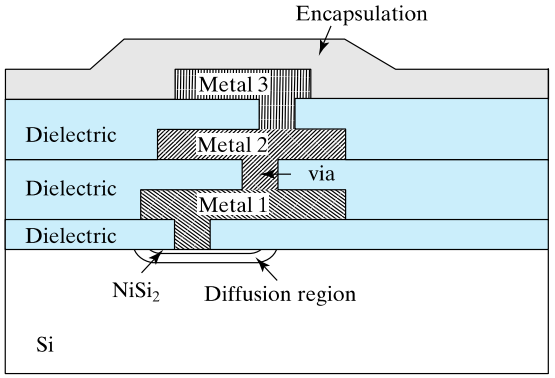
- Thin grown oxide to passivate Si surface
- Chemical Vapor Deposition (CVD) oxide
- Polyimide can also be used
- Can for the base of a multilayer metal stack

Modern ICs use a “Damacene” process for flat layers

- Finished surface is polished (CMP) to provide a flat surface for additional layers

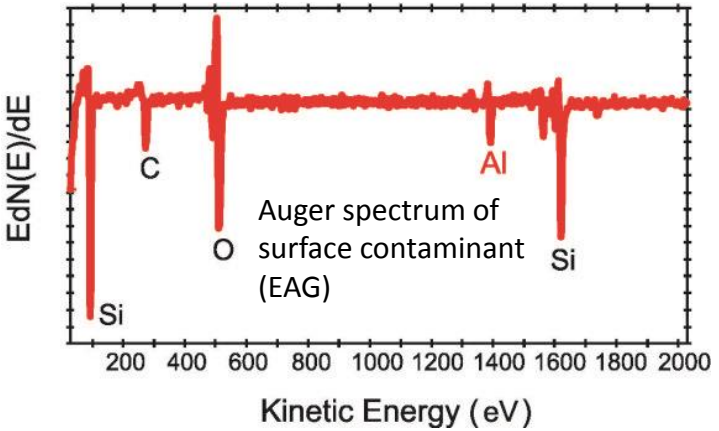


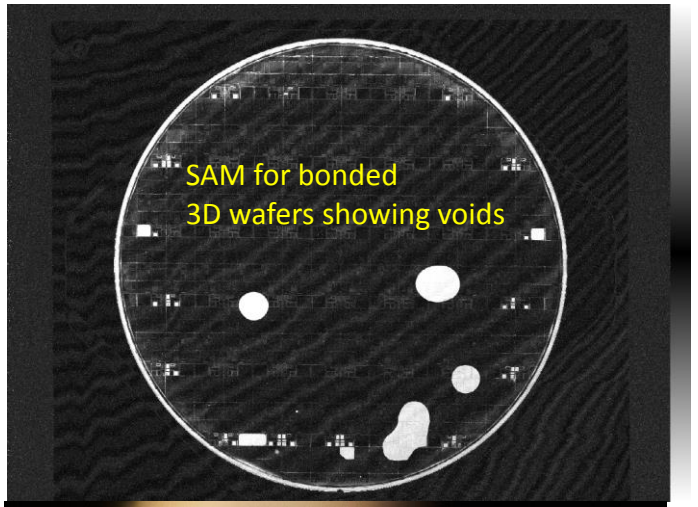
(Chen et al BNL)

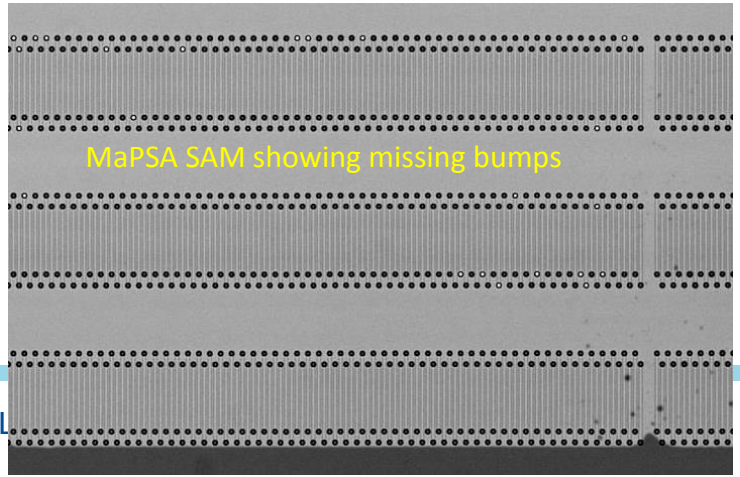


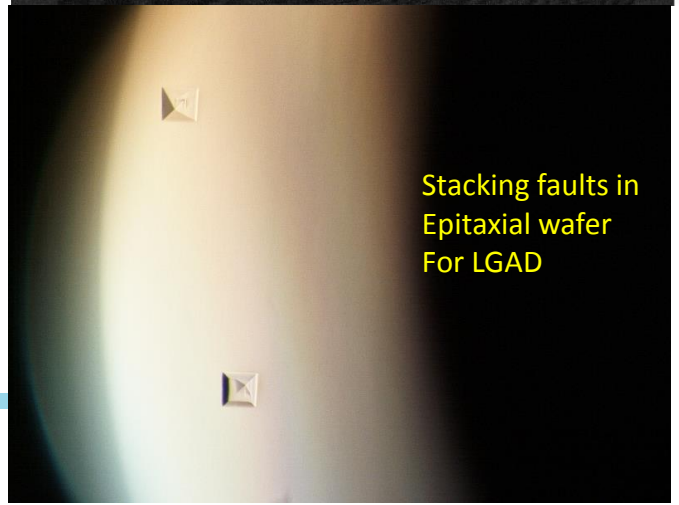
# Subtleties and Diagnostics

- Wafer stresses, warp, and topography
  - Compensating layers
- Focussed Ion Beam editing
- Surface scans (Auger spectroscopy + )
- Film thickness and composition
  - X-ray fluorescence, Ellipsometry
  - Sheet & spreading resistance, SIMS
  - Probe (4-pt) and remote capacitive probe
- Carrier lifetimes
  - PhotoConductance Decay
- Scanning electron microscopy
  - Ion milling
- Secondary Ion Mass Spectroscopy, spreading resistance
- Scanning acoustic microscopy (SAM)



# Novati DC Process

For Novati we simulated each step in the process in Silvaco TCAD. FNAL, LBL, SLAC defined the process along with Nhanced /Novati. AC process more complex

Includes cleaning and stripping

| | Process Steps | |
|---|---|---|
| 1 | HF clean for native oxide | |
| 2 | Grow gettering oxide, 1000C, 60min | |
| 3 | Strip gettering oxide | |
| 4 | Blanket B implant: implant boron dose=3.5E12 energy=25 tilt=7 rotation=0 | P-spray |
| 5 | Litho for Zero & Etch | |
| 6 | Split #4<br>Grow FOX layer: 1000C, 80min, target = 5,000A, ***Split WET vs DRY Oxidation*** | Masking oxide |
| 7 | Litho for FOX & Etch | |
| 8 | Ash/clean wafers | |
| 9 | Backside strip of SiO2 on SEZ | |
| 10 | Grow pad oxide: thickness target = 100 A | Implant through oxide |
| 11 | Litho for p-stop opening | P-stop |
| 12 | Split #5<br>Implant B for p-stop: Dose : **Splits,** energy=80 tilt=7, rotation= 0<br>Backside B Implant only on Thin 500um WFs(dose=2e15 energy=80 tilt=7, rotation=0) | |
| 13 | Ash PR, clean | |
| 14 | Litho for n+ | |
| 15 | Implant P for n+: implant phosphor dose=1e15 energy=100 tilt=7, rotation =0 | |
| 16 | Ash PR, clean | |
| 17 | CVD Oxide deposition 0.5um | |
| 18 | Litho for Contact & Etch | Contact oxide etch |
| 19 | Ash/Clean | |
| 20 | Al1%Si deposition, t=0.5um(Ti:250A/TiN:400A/AlSi:0.5um) | |
| 21 | Litho for Al Metal & Etch | |
| 22 | Ash, Clean | |
| 23 | Passivation Oxide dep (target= 1um) | |
| 24 | Litho for Passivation Ox & Etch | |
| 25 | Ash, Clean | |
| 26 | Backside HF strip (queue time to PVD <60min) only on Thick Bonded WFs | |
| 27 | Backside PVD Al1%Si , t=1um, Only on Thin WFs | |
| 28 | All sinter (anneal) at 400C in FG, 40 min | |

# AC SOI process

**Table 2**. Summary of process flows for DC and AC runs.

| Process steps | DC | AC | Comments |
|---|---|---|---|
| Initial SOI, SiSi wafer preparation | • | • | Implant (SOI), bond to handle |
| Grow/Remove gettering oxide | • | • | Getter impurities |
| Blanket p-spray implant | • | | Not used for runs 3,4 |
| Grow masking oxide | • | • | |
| Pattern n and p implants in $SiO_2$ | • | • | Oxide openings define n+ and p |
| Pattern and implant top | • | • | n+, p-stop, p-edge |
| Anneal | • | • | Remove implant oxide |
| Grow final oxide | • | • | |
| Dep/pattern/etch polysilicon | | • | |
| Pattern/etch Capacitor Oxide | | • | Remove oxide for AC coupling |
| Dep/pattern/etch capacitor | | • | $SiO_2$-SiN-$SiO_2$ dielectric |
| Pattern/etch contacts | | • | Bias and resistor contacts |
| Dep/pattern/etch aluminum | • | • | Top metal |
| Dep/pattern/etch passivation | • | • | Top $SiO_2$ |
| Bond to top handle | | • | Thinned SOI process |
| Remove back handle, etch BOX | | • | Thinned SOI process |
| Deposit backside *Al*, remove handle | | • | Thinned SOI process |

# Nhanced Process

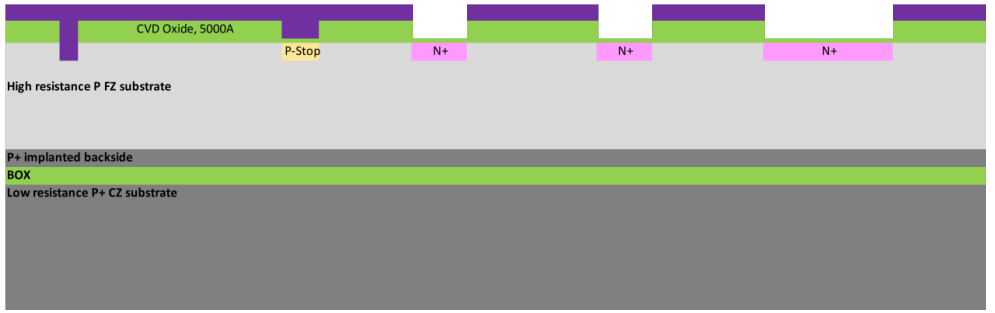
## 8” wafer SOI AC process

1. Starting substrate: SOI type,
   P+ Implanted on the back of high resistive P type (FZ thickness=200um)
2. RCA clean
3. Novati zero mask litho/Si etch for align key generation
4. CVD (5,000A) deposition and active mask & etch

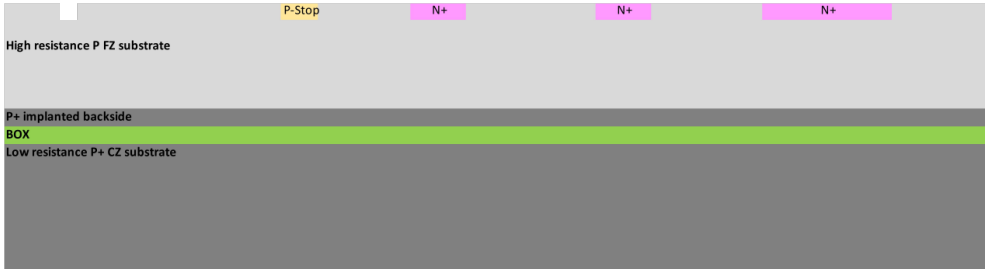

5. PR strip and clean followed by 100A pad oxide deposition


6. P-stop mask and implantation

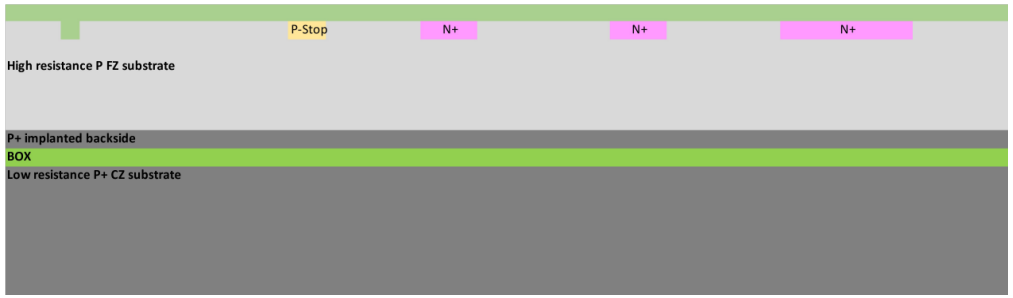

7. N+ mask and implantation



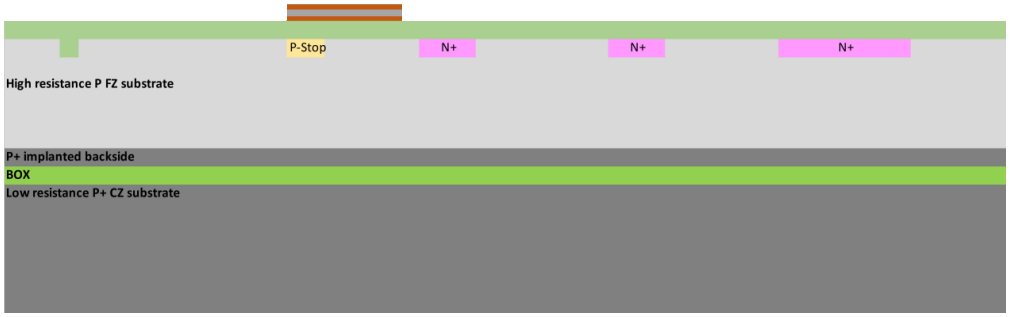

8. Strip pad-oxide and CVD Oxide



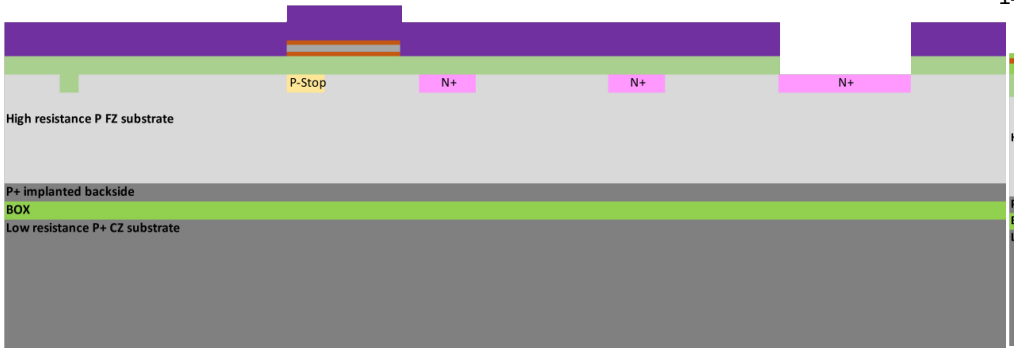
9. Thermal Oxide growth : t = 5000A



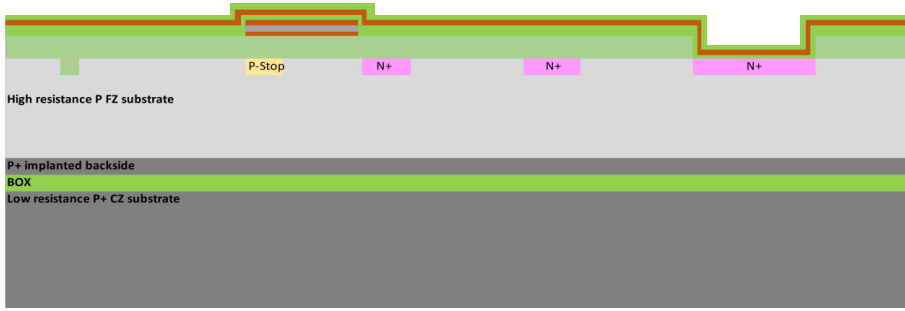

10. Poly Resistor Deposition, Litho, Etch (SiN 500A/Doped poly 2500A/SiN 500A)



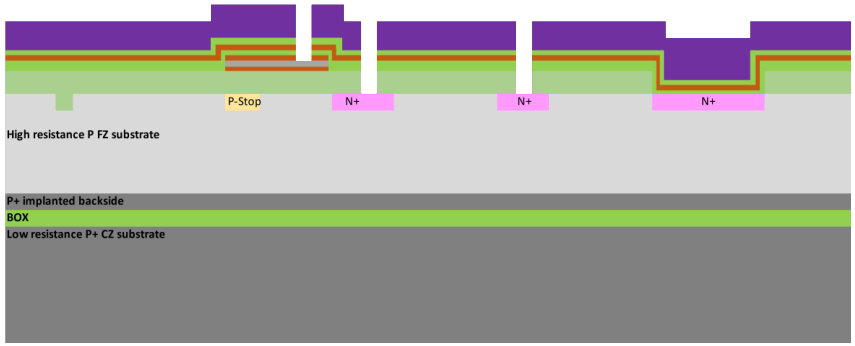

11. Capacitor Litho / Etch



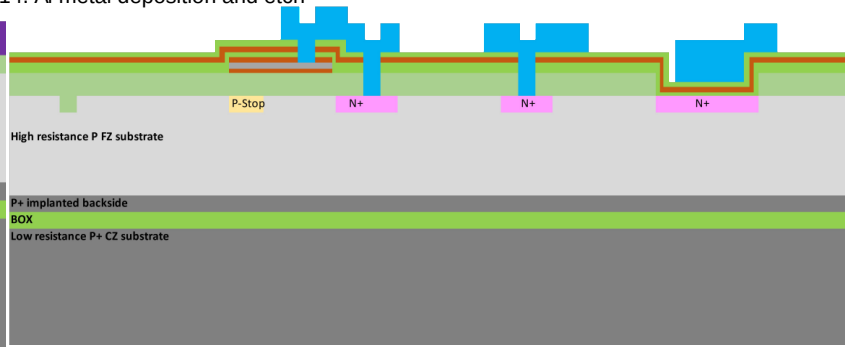

12. ONO Capacitor dielectric deposition : ONO=Thermal oxide 200A/ CVD SiN 2000A/CVD Oxi



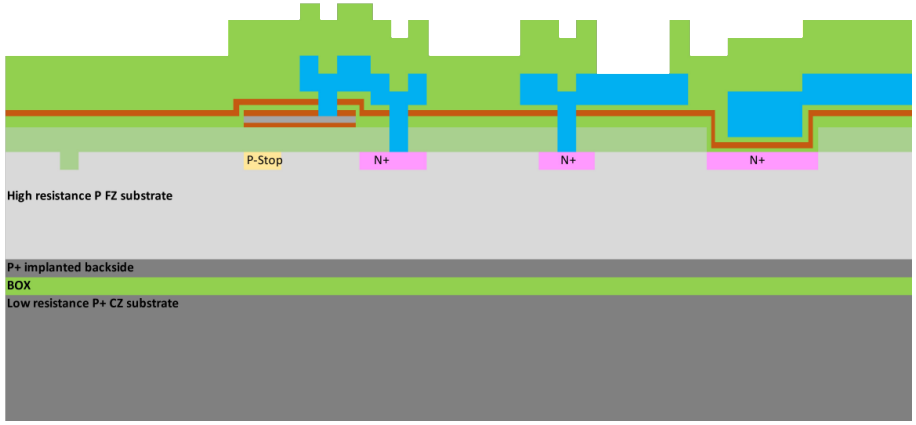

13. Contact Mask and Etch



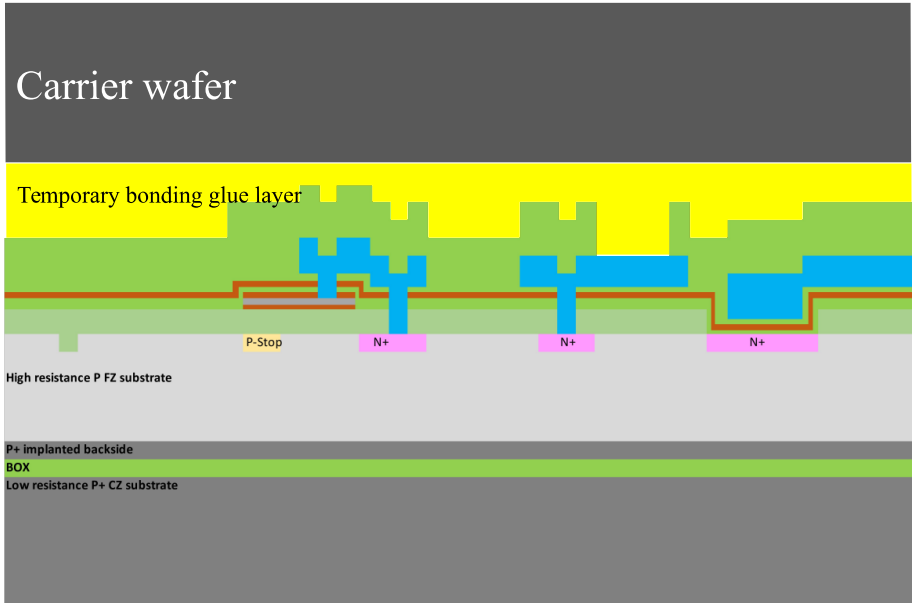

14. Al metal deposition and etch



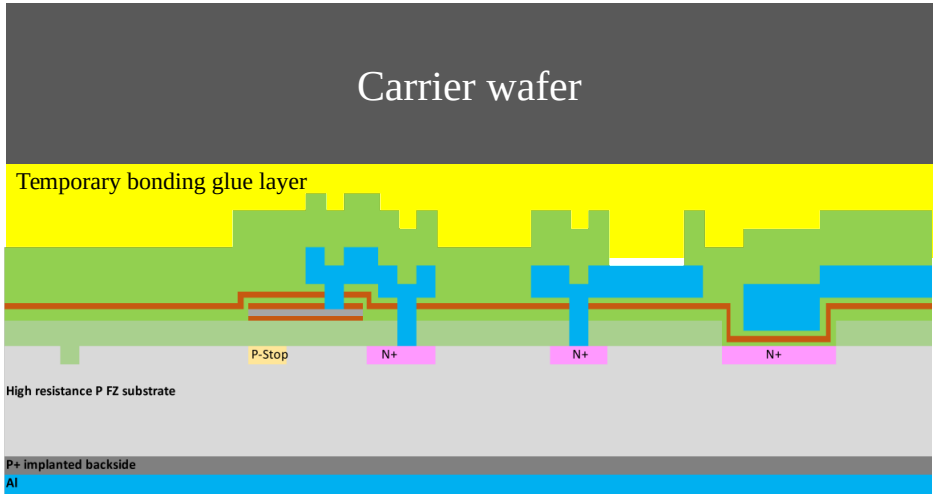
15. Passivation Oxide (1um) deposition and pad-open



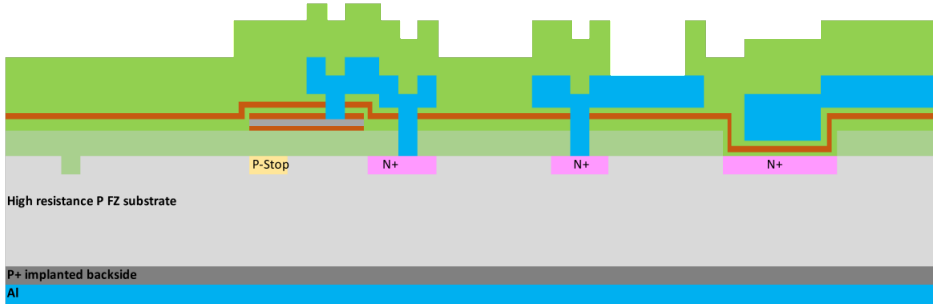

16. Temporary bonding to carrier wafer




17. Thinning SOI bottom Si and remove Box followed by Al (1um) deposition

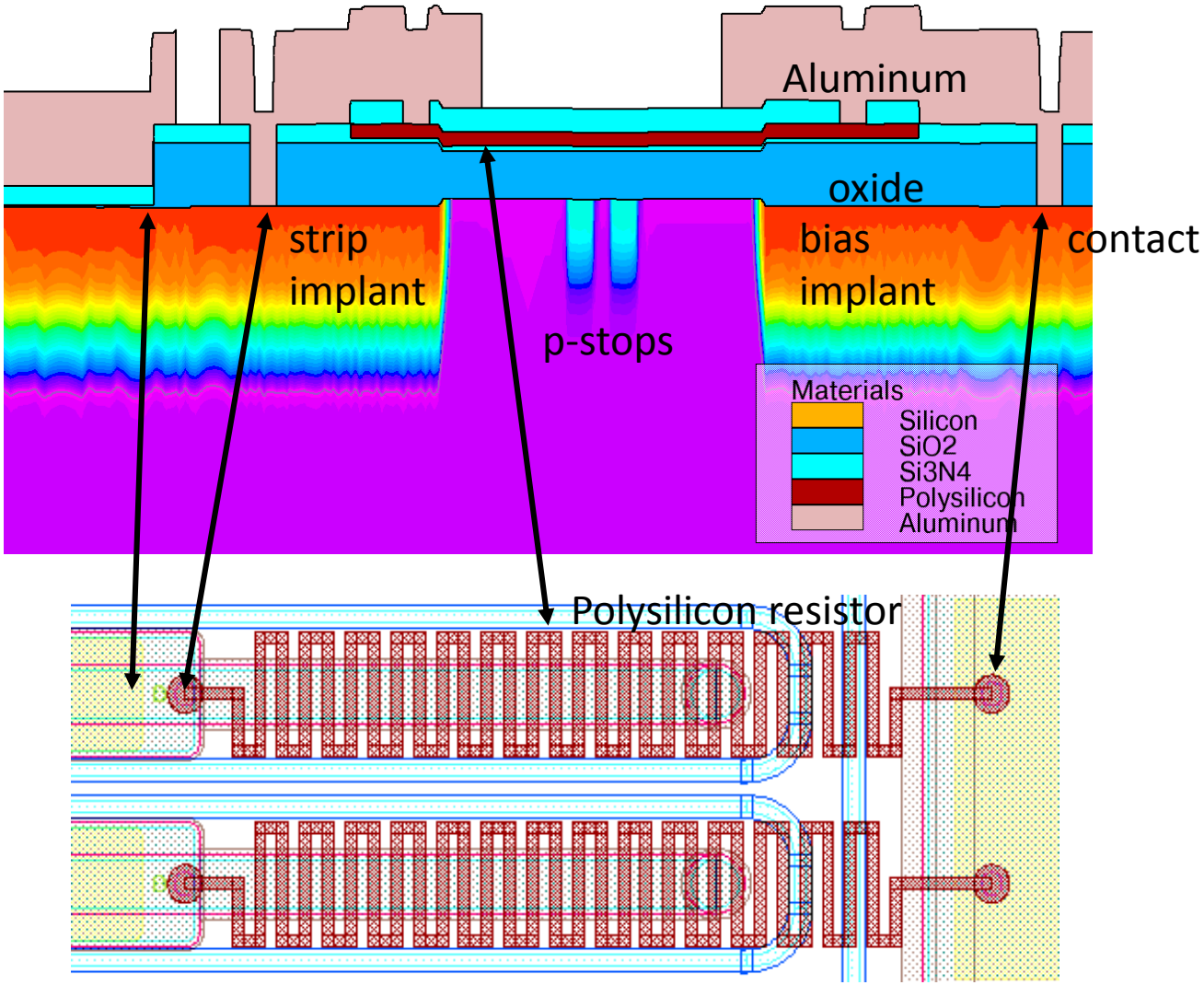



18. Remove carrier wafer by de-bonding the temporary bonding

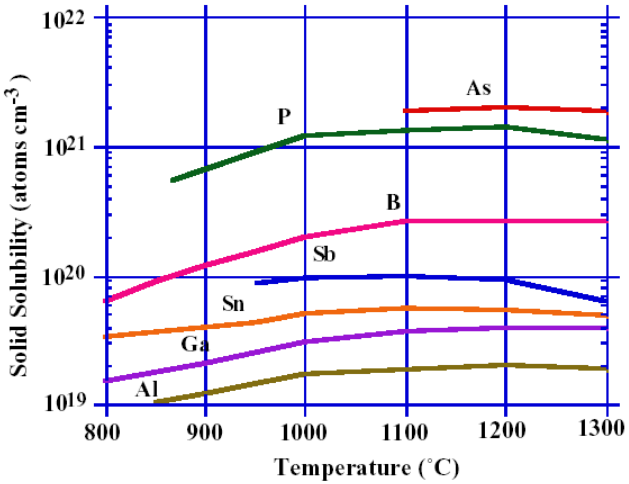


# TCAD AC detector Process Model

https://www.dropbox.com/s/50mwud1k6zt21nh/Cap_process_poly2.in?dl=0



# Questions?




n-type: P, As, Sb

p-type: B, Al, Ga, Al

-for most dopants highest concentration below the melting point of Si