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New leakage current, noise and depletion voltage expectations for Run IIb

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Abstract

This note gives an update on leakage current, noise and depletion voltage estimates for Run IIb.

1 Introduction

A general overview of radiation damage in silicon detector can be found in DØ note [1]. The leakage current of silicon detectors increases with irradiation dose due to the creation of additional gap states which will lead to more electron-hole pair generation and thus to an increase in bulk or generation current. This generation current is by far the dominating part of the entire leakage current after the silicon has been irradiated. The increase in leakage current can be parameterized as

$$I = I_0 + \alpha \cdot \Phi \cdot A \cdot d \tag{1}$$

where I_0 is the bias current before irradiation, α is a damage coefficient usually defined at $T = 20^\circ$C and dependent on particle type, Φ is the particle fluence given in particles per cm^2, A the detector area and d the thickness of the detector. The exact value of α depends on particle type and energy and varies between 2 and $3 \cdot 10^{-17} A/cm$ once the silicon is completely annealed. The leakage current rises linearly with fluence and does depend neither on silicon detector properties nor on special process characteristics during the silicon detector manufacturing. The leakage current in silicon detectors due to generation of electron-holes pairs is strongly temperature dependent and the ratio of currents at two temperatures T_1, T_2 is given by

$$\frac{I_2(T_2)}{I_1(T_1)} = \left(\frac{T_2}{T_1}\right)^2 \exp\left(-\frac{E_g}{2k_b}\frac{(T_1 - T_2)}{T_1 \cdot T_2}\right) \tag{2}$$

with k_b being the Boltzmann constant ($k_b = 8.6 \cdot 10^{-5} eV/K$) and E_g the gap energy in silicon ($E_g = 1.2eV$).

The change in the effective impurity or doping concentration $N_{eff} = 2\epsilon\epsilon_0/(ed^2) \cdot V_{depl}$ measured as a function of the particle fluence for n-type starting material shows a decrease until the donor concentration equals the acceptor concentration or until the depletion voltage V_{depl} is almost zero, indicating *intrinsic* material. Towards higher fluences the effective concentration starts to increase again and shows a linear rise of acceptor like defects. This phenomena of changing from n-type to p-type like material has been confirmed by many experimental groups and usually the detector is said to have undergone a "type inversion" from n-type to p-type. The change of the effective doping concentration can be parameterized as

$$N_{eff}(\Phi) = N_{D,0} \cdot \exp(-c_D\Phi) - b \cdot \Phi \tag{3}$$

where the first term describes a donor removal from the starting donor concentration $N_{D,0}$ and b indicates the rate of the radiation induced acceptor state increase. Hence donor removal happens exponentially whereas acceptor states are created linearly with fluence. Type inversion for standard resistivity n-type material with $\rho \approx 5k\Omega cm$ typically occurs at a fluence of about $1 - 2 \cdot 10^{13} cm^{-2}$.

2 Fluence estimation for RunII

Several fluence predictions for Run II have been given by Frautschi et al. [3], Matthews et al. [4] and Ellison et al. [5]. The most solid expectations are based on leakage current measurements performed on the CDF SVX and SVX' silicon detectors as a function of sensor radius from the beam and delivered luminosity during Run Ia+b. The derived charged particle fluence quantities vary among the various authors between $1.5 \cdot 10^{13} MIPs/cm^2/fb^{-1}$ and $1.9 \cdot 10^{13} MIPs/cm^2/fb^{-1}$ for the new SVX II layer 0 detectors, which are located at a radial distance of r=2.416 cm and r=2.438 cm from the beam axis. All the mentioned CDF expectations have in common that the radial scaling of the fluence occurs with $r^{-1.68}$, a fact which has been verified by independent doses measurements in the CDF detector.

In a DØ specific Monte Carlo study done by Ellison et al., the authors concluded with a charged particle fluence estimation of $1.7 \cdot 10^{13} MIPs/cm^2/fb^{-1}$ if normalized to the CDF SVX II layer 0, so well in between the given range of the CDF extrapolations. However, Ellison et al., are using a r^{-2} scaling of the charged particle fluences, which would be justified if the charged particle fluence is solely coming from physics processes and no beam losses are expected.

To normalize the observed CDF leakage current measurements to a standard neutron or proton fluence, assumptions about the radiation damage constant α of equation (1) have to be made. Matthews [4] has given an equivalent 1 MeV neutron fluence per fb^{-1} of $2.19 \pm 0.63 \cdot 10^{13} \cdot (r[cm])^{-1.68} [cm^{-2}/fb^{-1}]$. In his fluence determination he assumed a

frequently used α value for 1 MeV neutrons in order to convert the observed current increase to an effective 1 MeV neutron fluence. In his paper he took an α-value of $2.86 \pm 0.18 \cdot 10^{-17} A/cm$, which is still today a good value for neutrons [6], if most of the annealing of the leakage currents has happened. Since the CDF strip measurements are not done in a fully annealed state, he applied a factor of 1.1 to α according to common annealing parameterisations [7] in order to take the present annealing of the detector currents into account. Matthews propagated the uncertainties on silicon temperature, leakage current measurements and α-value into a final fluence uncertainty of $\pm 30\%$.

In a recent reevaluation of the fluence predictions for Run II, S. Worm [9] has used a 40% higher number of α[1], therefore reducing the effective 1 MeV neutron fluence by the same amount. After consultation with M. Moll, I believe, that this value for α could probably be too high and does not reflect the annealing of the currents completely. We will therefore stick to the previous fluence estimation by Matthews.

The number of secondary particles produced in the Be-beam pipes of the CDF and DZERO experiment should be rather similar. The only difference may occur in the number of curling particles which are caused by different magnetic fields strength of 1.5T compared to 2T for CDF and DZERO respectively and are traversing the silicon layers more than once. In the MC study by Ellison et al., an estimation for the contribution of the looping particles to the total charged particle fluence was done. They found that 50% of the total fluence will come from looper particles in the DZERO magnetic field. Frautschi, who has done similar studies for CDF assumed a 30% contribution only.

The strategy of the predictions for the leakage current rise and depletion voltage changes for Run II presented in this note will be as follows: For the leakage current estimations we are using the measured strip current numbers by CDF in Run I and scale to the appropriate DZERO geometries and Temperatures. This approach is essentially independent on the α value, but assumes the same fluences of charged particles in the CDF and DZERO experiment. In order to estimate the upper uncertainties for the leakage currents, we varied the temperature at which the CDF strip leakage current measurements took place according to their given uncertainties. Furthermore, we increased the CDF strip currents and hence the fluence by another 20%, in order to take a possible difference of the numbers of looper between DZERO and CDF into account.

The proposed 1 MeV equivalent neutron fluence of $2.19 \pm 0.63 \cdot 10^{13} \cdot (r[cm])^{-1.68}[cm^{-2}/fb^{-1}]$ by Matthews can be translated into an equivalent fluences of any other particle at any kinetic energy by knowing the corresponding so-called nonionising energy loss (NIEL) damage or displacement damage cross section value of the particle at a given energy. These NIEL values for neutrons, protons, pions and electrons at different kinetic energies are normalized to the standard displacement damage cross section for

[1] S. Worm's value of α was 4 and he has applied the same 1.1 correction factor for the partial annealing, ending up with an effective α of 4.4.

1 MeV neutrons according to an ASTM standard and are tabulated in an useful online compilation in reference [8].

In a recent DZERO irradiation study [11], which was carried out to investigate the radiation hardness of Run2b prototype sensors, the depletion voltage and leakage currents on CDF-type L00-sensors manufactured from Hamamatsu, Micron, ELMA and ST were measured after an irradiation in the Fermilab Booster area with 8 GeV protons. The 8 GeV protons are MIP-particles in silicon and hence 1 MRad corresponds to a MIP-fluence of 3.5 10^{13} $MIPs/cm^{-2}$. Their NIEL value normalized to 1 MeV equivalent neutrons is 0.521, meaning that a fluence of 3.5 10^{13} p/cm^{-2} of 8 GeV protons (=1 MRad) is equivalent in NIEL or displacement damage to a 1 MeV neutron fluence of 1.82 10^{13} n/cm^{-2}.

For the depletion voltage predictions, which we are going to present in this note, the 1 MeV neutron fluence number as given by Matthews is taken and under the assumption of the NIEL hypothesis, we calculate the depletion voltage changes according to the latest parameters of the Hamburg model [10], which gives up to date the best phenomenological description of the change in effective doping concentration in silicon during hadron irradiation. To obtain an upper error bound on the depletion voltage after irradiation, a safety factor of 1.5 in agreement with CDF is applied and the 1 MeV equivalent neutron fluence is varied accordingly. Note, that the fluence uncertainty, which was originally suggested by Matthews in his analysis is already 30%.

3 Parameters of the DZERO RunIIb detector

The following table 1 contains the design parameters of the DZERO RunIIb silicon detector. Their values have been used to perform the leakage current and depletion voltage change calculations. The parameter table lists not only the readout strips but also the intermediate strips, which produce leakage currents as well, since they are kept under bias. The thickness of the silicon sensors is taken to be 320 μm.

For the calculations of the leakage current and ENC noise we have always assumed the maximum strip length of the silicon modules. The terminology 'modules' is used in this write-up to define a silicon unit in the sense of the readout, i.e. what the preamplifer sees. Such a readout unit with own preamplifiers can consist of one or two silicon sensors. So-called ganged modules share the same low voltage and high voltage services, but have different readout units.

4 Leakage current extrapolations for RunII

Strip leakage current measurements have been performed in the CDF SVX and SVX' silicon detectors as a function of sensor radius from the beam and delivered luminosity during Run Ia+b. From the measured values in the innermost layer at $r = 3\ cm$

Table 1: Geometrical Parameters of the DZERO RunIIb detector

Layer	min radius (cm)	max active length (cm)	pitch (μm)	strip volume (mm^3)
L0-A	1.78	7.67	25	0.614
L1-A	3.48	7.67	29	0.712
L2-A	5.32	19.66	30	1.887
L3-A	8.62	19.66	30	1.887
L4-A	11.69	19.66	30	1.887
L5-A	14.7	19.66	30	1.887

and $T = 24 \pm 2^{\circ}C$, CDF could derive [2] an average increase in the strip currents of $I_{SVX} = 0.8\ nA/strip/pb^{-1}$ and $I_{SVX'} = 0.63\ nA/strip/pb^{-1}$. The radial dependence of the leakage currents or the fluence was found from these measurements to scale with $r^{-1.7}$. To obtain a leakage current prediction for Run II the measured $I_{avg} = (I_{SVX} + I_{SVX'})/2$ can be scaled from CDF's strip geometry in RunI (pitch $60\mu m$, length 25.5cm) to any new DØ configuration as given in table 1. The average temperature of $T = 24^{\circ}C$ for SVX and SVX' needs also to be taken into account. The radial scaling to the other layers mentioned in table 1 is done by using a $r^{-1.7}$ behaviour.

The uncertainties in the measured CDF strip currents were 10%. In addition, there is a temperature uncertainty of $\pm 2^{\circ}C$. By changing the operation temperature of SVX and SVX' from $T = 24^{\circ}C$ to $T = 22^{\circ}C$ our estimation produces 15-20% higher leakage current results. The leakage current values in the tables however, include a more conservative upper estimation. In addition to the temperature uncertainty of the leakage current measurements, the value itself was increased by 20%, taking into account the possibility of the different charged particle fluences between DZERO and CDF since the number of curling particles traversing the silicon detectors changes with the magnetic fields. The resulting upper leakage current values obtained from these error sources are given in the tables. This approach should be conservative enough to estimate the expected leakage currents and hence the shot noise levels for Run2b in a safe way.

The table 2 gives the upper estimate of the strip leakage currents in nA and per fb^{-1} for the various layers of the DZERO RunIIb detectors as a function of five different Temperatures. Note, that not only a readout strip, which is AC coupled to the preamplifer, but also an intermediate strip produces the same current. Therefore we do not distinct between the two cases, if only strip currents are considered. The calculations assume, that the silicon sensors generating the leakage currents are held uniformly at the considered temperature . In reality however, the silicon sensors have temperature drops along the silicon length and an attempt to include the temperature gradient along the silicon sensors is given in the next section.

Table 2: Expected strip leakage currents in nA/fb^{-1}

Layer	T=-10C	T=-5C	T=0C	T=+5C	T=+10C
L0-A	14.0	23.7	39.4	64.7	104.2
L1-A	5.2	8.8	14.6	24.0	38.7
L2-A	6.7	11.3	18.9	31.0	49.8
L3-A	2.9	5.0	8.3	13.6	21.9
L4-A	1.7	3.0	4.9	8.1	13.1
L5-A	1.2	2.0	3.4	5.5	8.9

Table 3: Expected module leakage currents in $\mu A/fb^{-1}$

Layer	number of strips	T=-10C	T=-5C	T=0C	T=+5C	T=+10C
L0-A	511	7.2	12.1	20.2	33.0	53
L1-A	767	4.0	6.7	11.2	18.4	29.7
L2-A	1277	8.5	14.5	24.1	39.5	63.6
L3-A	1277	3.7	6.4	10.6	17.4	28.0
L4-A	1277	2.2	3.8	6.3	10.4	16.7
L5-A	1277	1.5	2.6	4.3	7.0	11.3

In table 3 the total currents in μA per fb^{-1} are shown based on the module geometry of table 1. The maximum strip length for layer 2-5 modules is assumed and the upper estimated limit on the strip currents is taken.

The values from table 3 can be compared to the results of a recent DZERO irradiation study [11]. For CDF L00-type silicon sensors with an active area quite similar to the DZERO L0-type sensors, leakage current values around 100 μA at bias voltages between 150 V and 500 V after an irradiation of 10 MRad of 8 GeV protons have been found (see the corresponding figure 19 of reference [11]. This leakage current measurement was recorded at T=-12°C. By applying the NIEL scaling factor of 0.521 for 8 GeV protons, the 10 MRad 8 GeV proton irradiation dose converts into a 1 MeV neutron fluence of 1.82 10^{14} cm^{-2}. Since the Matthew-fluence for RunIIb is $2.19 \cdot (r[cm])^{-1.68}[cm^{-2}/fb^{-1}]$, the silicon sensors in DZERO layer L0-A, which are located at a radius of $r = 1.78$ cm, are expected to receive a 1 MeV neutron fluence of 8.310^{12} cm^{-2}/fb^{-1}. This means that the equivalent 10 MRad of 8 GeV protons would be reached in layer L0-A after an accumulated luminosity of 22 fb^{-1}. Our expected module currents in L0-A (see table 3) at T=-10°C are then $I_{pred} = 7.2\ \mu A/fb^{-1} \cdot 22\ fb^{-1} = 158\ \mu A$. The agreement is even better, if the

temperature dependent leakage current correction from T=-10°C to T=-12°C are applied (see equation 2), which would give a factor of 0.8, i.e. $I'_{pred} = 158\ \mu A * 0.8 = 127\ \mu A$. This agreement to the measured $100\mu A$ shows two things:

- the measured leakage currents of the silicon sensors after 10 MRad irradiation in the DZERO study behaved in a normal way, i.e. the radiation damage is not too far off from what is expected (assuming the NIEL hypotheses)
- if the Matthew fluence is the correct 1 MeV neutron fluence for Run2b, then the irradiation test with 8 GeV protons of up to 10 MRad or even 15 MRad provides with a very comfortable safety margin the maximum expected leakage currents in Run2b, since 10 MRad protons would already correspond to 22 fb^{-1} of running for layer 0.

Table 4 gives the predicted total module or ladder current for ganged modules. It is somehow important to estimate those currents, since the low- and high voltage services are connected in L2-L5 for two (ganged) modules each. Due to the irradiation induced leakage currents, it has to be therefore checked, if there is a current limitation constraint set by the HV power supplies. The ganging scheme for the LV and HV services is different from layer to layer and the expected currents drawn from the power supplies after a luminosity period of 15 fb^{-1} for the present ganging scheme is finally given in table 4. Here, every row in table 4 contains the leakage current entries after 15 fb^{-1} in μA at different temperatures for the various ganging types. To be conservative and to evaluate carefully, if the power supplies will run into their current limit, an additional safety factor of 2 to the currents listed in the table might be applied.

The shot noise in ENC which is caused by the strip leakage currents is obtained in the following way [14]: $ENC_{shot} = \sqrt{12 \cdot I[nA] \cdot \tau}$, where τ is the shaping time of the amplifier in ns. After discussions with A. Nomerotski and M. Merkin we agreed to include also the shot noise contributions from the two intermediate strip which are neighboured to one readout strip, since they divide the generated signal and noise according to the size of their interstrip capacitance and backplane capacitances.

The table 5 shows the expected noise in ENC after 15 fb^{-1} for the DZERO RunIIb detector. A further extrapolation to 20 fb^{-1} for the ENC noise caused by the leakage current is done for layer 0-2 in table 6.

It is important to remark here, that the predictive power of this approach has some limitations: It can be only applied for detectors which are slightly above depletion voltage and are far away from the junction breakdown. However, the large radiation damage in RunIIb will force us to run in a mode in which the detectors are significantly overbiased to compensate any charge collection deficiencies. The biasing above depletion voltage will eventually increase the leakage currents even more since the detector may be operated close or even at junction breakdown. Therefore, for a realistic current estimation, an

Table 4: Expected total leakage currents for ganged modules after a period of 15 fb^{-1} in μA

ganging type	T=-10C	T=-5C	T=0C	T=+5C	T=+10C
L0-79	107	181	303	496	799
L1-79-79	119	202	337	553	890
L2-200-100	191	325	542	889	1432
L2-100-100	128	217	362	592	954
L3-200-100	84	143	239	391	630
L3-100-100	56	95	159	261	420
L4-200-200	67	114	190	311	501
L4-100-100	33	57	95	155	250
L5-200-200	45	77	128	210	339
L5-100-100	23	39	64	105	170

Table 5: Expected strip noise in ENC after 15 fb^{-1}

Layer	T=-10C	T=-5C	T=0C	T=+5C	T=+10C
L0-A	814	1061	1370	1753	2225
L1-A	496	646	834	1068	1355
L2-A	563	733	947	1212	1539
L3-A	373	487	628	804	1021
L4-A	288	376	485	621	788
L5-A	237	309	399	511	649

Table 6: Expected strip noise in ENC for layers 0-2 after 20 fb^{-1}

Layer	T=-10C	T=-5C	T=0C	T=5C	T=20C
L0-A	940	1225	1581	2024	2569
L1-A	572	746	963	1233	1565
L2-A	649	847	1094	1400	1777

additional safety factor in the leakage currents of 1.5 translating into a 22% increase in ENC noise should most likely be applied.

5 Leakage currents for a realistic silicon temperature profile

The calculations of the leakage currents and hence shot noise in the previous section assumed uniform temperatures along the silicon sensors. Due to the assembly of the hybrid on top of the silicon sensors, the temperature along the silicon is not constant and large temperature drops in the silicon are possible. In a finite-element analysis (FEA) study [12] the temperature gradient along the silicon sensors has been determined for layer 1 and layer 2 modules based on a realistic modelling of the power dissipation, the heat transfer of the cooling fluid and the thermal impedances. The coolant temperature was set to $T_{coolant} = -15°\mathrm{C}$. The temperature profiles obtained for layer 2 will also apply for the outer layers 3-5, since the stave design and thermal impedances are the same.

The FEA based temperature gradients will be used in the following to estimate an equivalent average temperature T_{equiv}, at which the same leakage current output would have been produced as if the sensor would have been uniformly kept at this temperature.

Figure 1 shows the anticipated temperature distribution along the z axis for a circulating coolant of $T_{coolant} = -15°\mathrm{C}$ in case of layer 2 modules. Note, that the same temperature profile applies also for modules in layer L3-L5. The corresponding layer 1 temperature profile however, is different from that due to an independently designed cooling circuit and another stave layout for that layer. Its temperature profile based on $T_{coolant} = -15°\mathrm{C}$ is represented in figure 2.

The warmest region of $T \sim 0°\mathrm{C}$ in the silicon sensor for layer 2 (or layer 3-5) modules is, where the readout chips on the hybrid are located. This statement is of course also true in the case of layer 1. The graphs of figure 1 and figure 2 contain further the strip leakage current in $\mathrm{nA/fb}^{-1}$ normalized to a strip unit length of 3 mm for layer 2 and 6 mm for layer 1, respectively. These strip lengths have been used for the binning in the FEA.

To obtain the total strip currents for the layers, the differential strip currents along the ladder modules are summed up. Table 7 lists the calculated strip (either readout or intermediate strip) leakage currents for two different module lengths of layer 2-5 readout modules as well as the calculated currents in layer 1 modules. The strip currents in case of the longer L2-A (or L3-L5) module have to be compared to the corresponding entries of table 2 for layer 2 modules. Based on the produced currents of the assumed temperature profile of the silicon, the equivalent temperature T_{equiv} for a long module -kept at a uniform temperature- would be T_{equiv}=-8°C. A short L2-A module having only half of the strip volume does not generate only half of the leakage currents in case of a non-uniform temperature profile as the second entry of table 7 shows. The currents are larger and therefore T_{equiv} shifts towards higher values. If a coolant with temperature

Table 7: The expected strip currents in nA/fb^{-1} and the module currents in μA/fb^{-1} for L1 and L2-L5 layers, taking a realistic temperature profile from the FEA into account. The terminology strip refers to any biased strip in the sensor, i.e. either a readout or an intermediate strips.

layer	module length (mm)	strip current (nA/fb^{-1})	module current (μA/fb^{-1})	T_{equiv} (°C)
L1-A	76.7	8.7	6.7	-5
L2-A	196.6	8.8	11.2	-8
L2-A	98.3	5.5	7.1	-5
L3-A	196.6	3.9	4.9	-8
L3-A	98.3	2.4	3.1	-5
L4-A	196.6	2.3	2.9	-8
L4-A	98.3	1.5	1.9	-5
L5-A	196.6	1.6	2.0	-8
L5-A	98.3	1.0	1.3	-5

$T = -15°$C is circulated, the equivalent temperature for a short L2-A module is only $-5°$C. The higher temperature is due to the hybrid location, which is at the end of the sensor and therefore the temperatures profile from the FEA is not mirror symmetric. The equivalent temperature T_{equiv} for layer 1 modules is at T_{equiv}=-5°C.

6 Depletion voltage

As previously mentioned, the depletion voltage predictions we are presenting are based on the 1 MeV neutron equivalent fluence assumptions for Run II by Matthews et al. In addition we are applying a safety factor of 1.5 to that fluence. The latest parameters for the stable damage constants, the beneficial annealing and the reverse annealing constants have been used [6] in the Hamburg-model together with the following assumptions for the Tevatron running scenario of Run IIb, which are presented in the table 8. The obtained depletion voltage predictions are called standard depletion voltage predictions.

In the standard predictions, it is assumed that the silicon detector is kept cold entirely during the luminosity runs as well as during the shutdown periods. This operation temperature is assumed to be uniform. The resulting standard depletion voltages for different operating temperatures in layer 0, 1 and 2 are shown in Figure 3. We present three calculations for layer 0 at uniform silicon temperatures of -10°C, 0°C and +10°C and with a starting depletion voltage of 150V as well as one scenario for layer 0 with starting depletion voltage of 50V only. Furthermore, we give two standard depletion

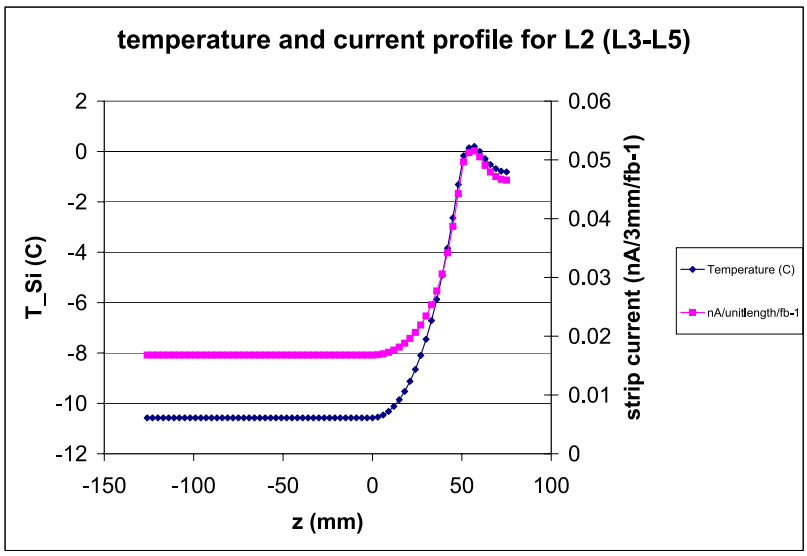

Figure 1: Expected temperature gradient and strip (either readout or intermediate strip) currents per unit length (3 mm for layer 2) and per fb^{-1} in layer 2 as a function of z. The temperature calculations have been performed by FEA.

Table 8: The Tevatron Run IIb operation scenario

year	max. lumi. pb-1/wk	shutdown (months)	lumi. fb-1/year	total lumi. fb-1
2005	61	4	1.81	1.81
2006	81	1	3.38	5.19
2007	81	1	3.85	9.04
2008	81	1	3.85	12.89

Table 9: Characteristic time constants τ for the beneficial and reverse annealing. The time constants are obtained from M.Moll [6].

Temperature	τ for benefical annealing (days)	τ for reverse annealing (days)
-10°C	306	180000
-5°C	125	60000
0°C	53	22000
10°C	23	3000
20°C	2.4	470
30°C	0.5	84
40°C	0.14	16

voltage predictions for layer 1 in figure 3 and one prediction for layer 2.

In the standard Run2b scenario, the depletion voltage of layer 0 will reach values of around 300 V as long as the silicon temperature does not exceed T=0°C. It does not matter for the final depletion voltage, if the initial depletion happens to be at around 150 V or only 50 V, as the estimations of figure 3 show. If layer 0 is permanently kept at a warm temperature of $T = 10^\circ$C, then the sensors will reach their depletion rather at 400 V than at 300 V.

Layer 1 is expected to deplete at around 100V at the end of the standard running period. It is surprising, that the final depletion voltage of layer 1 is the same for two presented calculations using very different assumptions: $T = -10^\circ$C and $U_{depl} = 150$ V versus $T = 0^\circ$C and $U_{depl} = 50$ V. It can be explained by a suppression of the reverse annealing term even at $T = 0^\circ$C. Indeed a calculation (not shown in figure 3) having layer 1 at $T = +10^\circ$C would reach a final depletion of 140 V and hence shows the first signs of reverse annealing effects, which now begins to dominate over the beneficial annealing mechanism. For a better understanding of the influence of the reverse and beneficial annealing effects, their characteristic time constants in days at different temperatures are presented in table 9. It becomes now obvious, that reverse annealing starts to become important already at $T = 10^\circ$C, since a time constant of 3000 days (at $T = 10^\circ$C) has to be compared to the operation period of 1500 days.

Finally, figure 3 contains a depletion voltage prediction for Layer 2, which seems to deplete below 80 V at the end of the standard running. This value is obtained even at a moderately high temperature of $T = +10^\circ$C. Note, that all the presented depletion voltages represent only the value of the depletion voltage itself and do not guarantee a full charge collection efficiency in the silicon. A safety margin of at least a factor of 1.5 in the bias voltage should be applied in order to have enough flexibility in overbiasing the

detectors and to compensate potential ballistic charge losses due to mobility decreases of the charge carriers after irradiation. Therefore, we have specified the breakdown of the layer 0 sensors to be above 700V to provide for such a safety margin.

There is some variation in the radiation damage constants and reverse annealing parameters used in the Hamburg model for different silicon wafer materials. However, theses uncertainties are absorbed in the fluence safety factor of 1.5, which we have included in the depletion voltage calculations.

As it was demonstrated in figure 3 and in table 9, temperature effects of reverse annealing tend to saturate below 0°C, and the depletion voltage values for T=0°C and T=-10°C do not differ much. However, reverse annealing increases rapidly if the operation temperature reaches higher temperature values of +10°C or more. At such high temperatures the reverse annealing makes a significant contribution and cannot be neglected anymore. This could be a concern for the detector operation if a warming-up periods due to cooling problems or simply an access at room temperature happen. Moreover, it would be interesting to project the depletion voltages beyond the standard run2b scenario, in order to estimate the lifetimes of our detectors. Therefore, we extend the Run IIb scenario now over a total of 6 years and calculate the anticipated depletion voltage after having accumulated a total luminosity of 20 fb^{-1}. In addition, warming-up periods ar room temperature are introduced. Figure 4 contains such depletion voltage graphs for layer 0, 1 and 2.

In the extended scenario, the layer 0 sensors are expected to deplete now at around 450V (without warm-up) and since we are specifying the sensor breakdown to be at least 700V, we would still have enough margin in the biasing to accommodate a longer Tevatron running of up to 20 fb^{-1}. In addition, figure 4 contains two other layer 0 depletion voltage graphs for this expanded running scenario: Four warming-up periods each lasting 4 weeks at room temperature are included, in order to see the reverse annealing effects. One calculation was done keeping the sensor normally at T=-10°C and the other one at T=0°C. The depletion voltage changes become now much more dramatic, if such maintenance periods at room temperature are considered. The reverse annealing will dominate after irradiation, if the detectors are being warmed up and will shift the depletion voltages to much higher levels of around 700V. It is therefore quite important to avoid any warm-up after the detector has been irradiated.

Another interesting observation can be made by comparing figure 3 and figure 4. It seems in figure 3 that layer 0 depletes at slightly less voltages if the layer is kept at T=0°C than at T=-10°C, but only if no real warming up periods are included in the running scenario. This is in fact the result of the short beneficial annealing periods, which are detectable only during the accelerator shutdown. The beneficial annealing has a time constant of about 310 days (53 days) if the detectors are at T=-10°C (0°C), meaning that the drop of the depletion voltage during accelerator shutdown periods occurs faster at higher temperatures. If the detector is warmed up, the reverse annealing will

overwhelm any beneficial annealing effects and dominates the depletion voltage change in the maintenance periods, since the time constant of the beneficial annealing at room temperature is only in the order of 2 days. By including warming up periods in the running scenario, a complex interplay between reverse and beneficial annealing takes place. Based on the Hamburg model calculations, it seems to be more advantageous and safer to have the silicon detectors maintained at T=-10°C during the running rather than at T=0°C, as the graphs of figure 4 shows. Therefore, we should point out that for the operation of the silicon detectors in layer 0 and layer 1, a temperature of -10°C is much safer against reverse annealing than keeping them at 0°C, especially if warming up periods - either through accidents or done by purpose - are included in the depletion voltage scenarios and calculations.

7 Signal to noise ratio

The performance of a silicon detector is mainly measured in its signal to noise ratio that ultimately limits the detector lifetime. Based on previous studies and CDF experience in Run I, S/N starts affecting b-tagging efficiency seriously [13], when it degrades below a value of 5. Our design goal is to keep the S/N conservatively above 10 for all layers of the detector. The S/N should remain above this limit even for an extended RunIIb of up to 20 fb^{-1}. In addition we prefer to set the operation temperatures such, that the S/N of the silicon layers should not degrade by more than 15% over the expected running time of RunIIb (15 fb^{-1}) in order to ensure a stable and robust S/N over the full lifetime of the silicon detector.

In the signal over noise ratio estimates we assume that the sensors can be fully depleted and that one MIP produces 23000 e in 300 μm silicon. We have considered the following contributions to the total noise:

- Noise in the front-end due to the capacitive load: The analog cable in layer 0 contributes with 0.4 pF/cm to the total load. The silicon sensors are conservatively assumed to have a total load capacitance of 1.4 pF/cm, dominated by the interstrip capacitance. The ENC noise behavior of the front-end chip (SVX4) is taken to be $450 + 43 \cdot C_{load}[pF]$ according to the specifications.

- Noise due to the series resistance of the aluminium traces of the silicon sensors and - for layer 0 only - the copper traces of the analog cable. The serial noise varies between $\sim 210e$ for the short layer 1 sensors and $\sim 780e$ for 19.7 cm long modules in layer 2-5.

- Shot noise contribution from detector leakage current as calculated before.

- Thermal noise due to the finite value of the bias resistor ($\sim 250e$).

The first plot of figure 5 shows the S/N behavior as a function of luminosity for layer 0 modules. This innermost layer is a special case, since it has an up to 450 mm long long analog cables to route the signals to the hybrids. These cables will be designed to have a maximum capacitance of not more than $\sim$ 20 pF [15], so that the total capacitance load of the silicon ladder including the analog cable can be kept around 30 pF. Due to this large load capacitance and the serial resistance of the cable, which can not be neglected at all, the noise in the front end chip will keep the initial S/N close to 11:1 and any further degradation by additional shot noise should carefully be avoided. Therefore, the best strategy would be to keep the detectors in the innermost layer as cold as possible, i.e. at an operating temperature of -10°C. The S/N will then remain larger than 10:1 even after 20 fb^{-1}. It is therefore very important, to provide the cooling for this layer such, that silicon temperatures of -10°C should be reached at the end of the running period.

Generally, a much higher S/N is achieved with modules from layer 1 due to the absence of the analog cable and the short sensor length. The S/N of layer 1 is shown in the center plot of figure 5. A very high and robust S/N of more than 19:1 can be maintained if layer 1 is kept at T=-5°C or lower during the complete RunIIb period with 15 fb^{-1}. Under such conditions the S/N performance loss due to radiation induced shot noise increase is mitigated to less than 15% only.

The detectors in layer 2-5 represent with a maximum active length of 19.66 cm a total capacitive load of almost $\sim$ 28 pF. Since, the noise figure of the SVX4 chip is taken to be $450 + 43 \cdot C_{load}[pF]$, as requested in the design specifications, we estimate a noise as high as $\sim$ 1840 e for two-sensor modules in layers 2-5 including serial and thermal noise sources. The last plot in figure 5 shows the S/N values for layer 2 and layer 3 again as a function of luminosity and for different temperatures. Generally, the S/N of the layer L2 does not fall below 10:1, if these detectors are kept at temperatures around T=0°C. The S/N performance loss in layer 2 is then reduced to less than 15%. For the other outer layers, an operation temperature of T=+5°C seems to be sufficient.

8 Conclusion

Based on our estimates of leakage currents, depletion voltages and S/N as function of operation temperatures of the silicon detectors in the various layers we would suggest to keep the silicon sensors depending on the layer generally at temperatures between +5°C and -10°C any time. The closer to the beam pipe the silicon layer is, the colder it has to be operated. Note, that the silicon sensors are assumed in the calculations to be kept uniformly at those temperatures.

The silicon detectors of layer 3-5 can be kept between T=+5°C and T=0°C over the entire Run IIb, since leakage current noise will not be the dominant noise source. Having the possibility to run layers 3-5 at T=0°C should provide enough safety margin against

higher radiation levels or current limitations in the HV supplies.

In layer 2 the S/N performance degradation is below 15%, if the detectors are kept at 0°C. This temperature might be sufficient at the end of the running, but it should be also clearly stated that the cooling in layer 2 should wisely be designed in a way that temperatures down to T=-5°C can be reached, so that a reasonable operation margin is achieved.

The split mechanical design of layer 0 and 1 on the one side and layer 2-5 on the other side, will allow an independent cooling passage for the two innermost layers. We would suggest to design the cooling of the inner layers such, that they are able to operate at temperatures as low as -10°C. This low temperature operation limits the shot noise contribution and helps in suppressing the reverse annealing effect if potential warming up periods are happening. Especially for layer 0 silicon detectors, a low temperature operation at -10°C has to be reached. For the silicon detectors in layer 1, the S/N ratio is higher than the detectors of layer 0. A 10% performance loss in layer 1 after 15 fb^{-1} translates into an operation temperature of T=-5°C. The FEA analysis suggests that this low temperature in layer 1 can be achieved, so that a comfortable safety margin against higher radiation doses levels exists. The S/N performance of layer 1 detectors can be considered as very stable and robust against radiation damages over the full course of RunIIb.

Based on a FEA obtained temperatures profile, an equivalent temperature T_{equiv} for a Layer 2 module was determined. The result of this calculation showed, that a circulating coolant at $T = -15°C$ would result in an equivalent temperature in a L2 silicon detector of $T_{equiv} = -8°C$ and $T_{equiv} = -5°C$ for a long and short L2-module. This two equivalent temperatures are identical in case of L3-L5, since the therml profile along the stave is the same. For layer 1, however, another temperature profile based on a FEA has to be considered. The resulting equivalent temperature is then determined to be $T_{equiv} = -5°C$ for a circulating fluid of $T = -15°C$.

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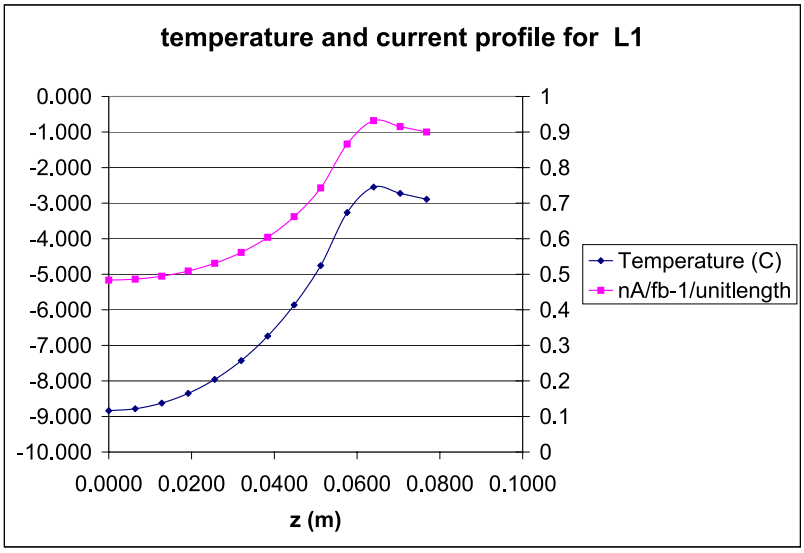


Figure 2: Expected temperature gradient and strip (either readout or intermediate strip) currents per unit length (6 mm for layer 1) and per fb^{-1} in layer 1 as a function of z. The temperature calculations have been performed by FEA.

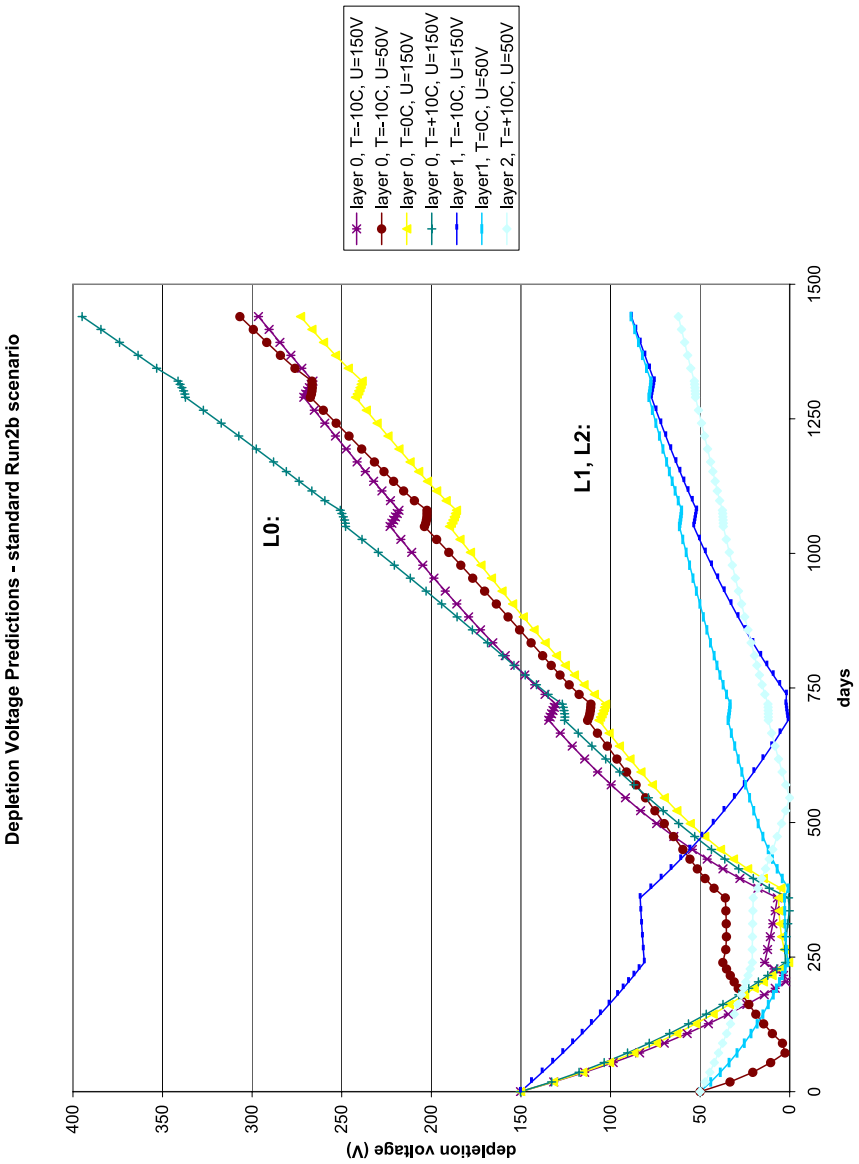


Figure 3: Standard depletion voltage estimates as a function of time (days) over the course of the operation years as given in table 8. The standard scenario corresponds to a cumulated luminosity of 13 fb^{-1} and assumes the silicon always cold at the indicated temperatures.

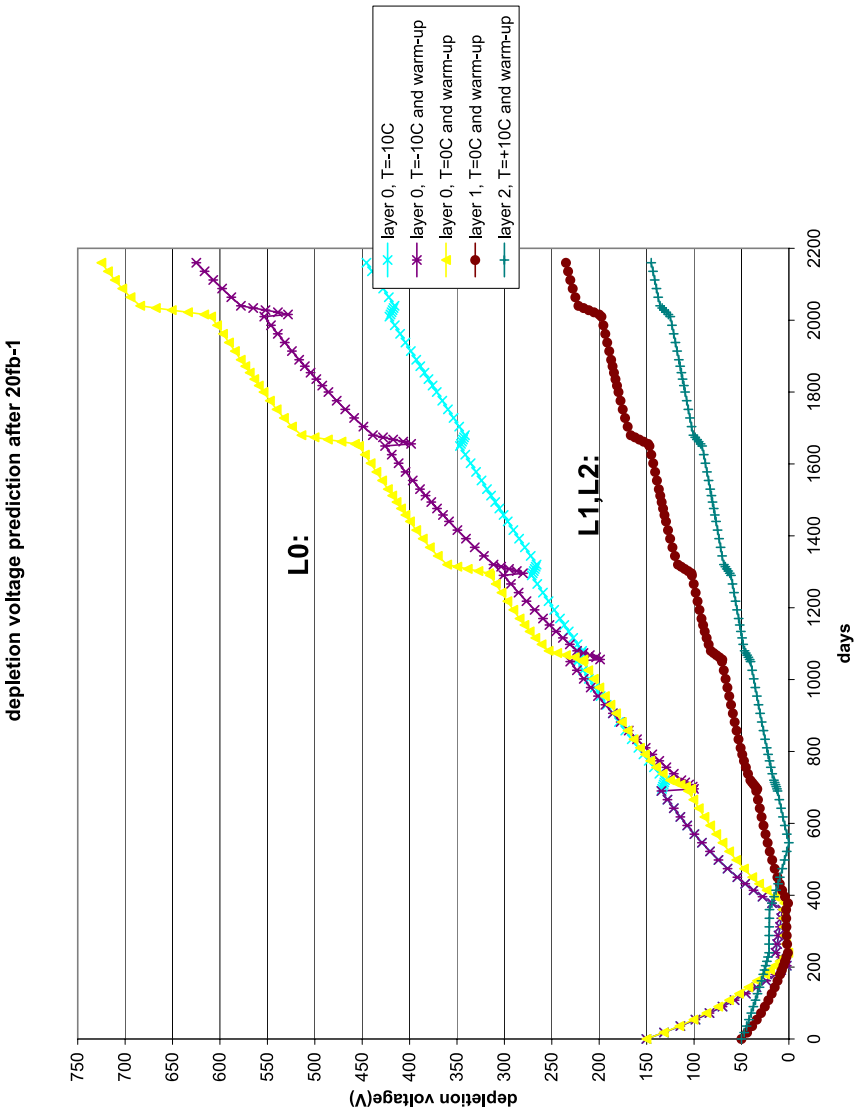
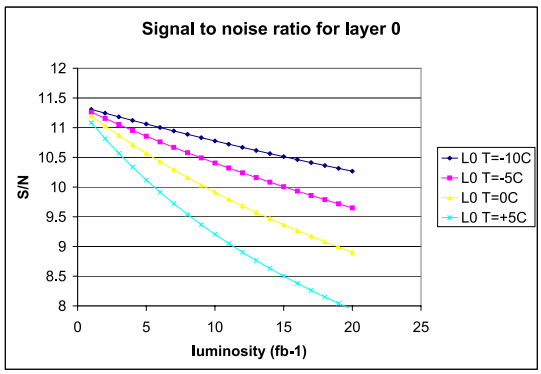
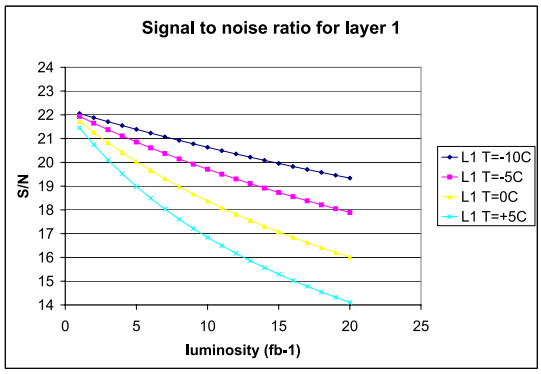


Figure 4: Expected depletion Voltage as function of time over the course of 6 years corresponding now to a cumulated luminosity of 20 fb^{-1}





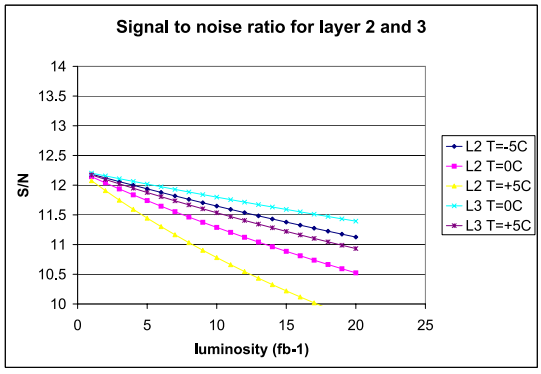


Figure 5: Expected signal to noise ratios as function of luminosity for different layers at different operation temperatures. The first or top plot is for layer 0, the second plot refers to layer 1 and the last plot contains the S/N of layer 2&3.