3 SILICON SENSORS

3.1 Introduction

The main requirements for the silicon detector are: efficient and reliable tracking, precise vertex measurement, and radiation hardness. As described above, this is achieved with a 6-layer device. The four outer layers are constructed of 60 μm readout pitch silicon sensors and provide hits essential for pattern recognition in a high-occupancy environment. In addition, two inner layers (layer 0 and 1), constructed with 50/58 μm readout pitch silicon sensors with intermediate strips at 25/29 μm, provide precise coordinate measurement essential for good secondary vertex separation. Reliable operation of silicon sensors in a high-radiation environment is critical to the experiment's success. Over the operating period, the inner layers of the Run IIb silicon detector will be subject to a fluence of about 2×10^{14} equivalent 1 MeV neutrons per cm^2. We were guided in our design and technology choice by our experience in Run IIa detector construction as well as by recent research and development in the radiation hard technology.

3.1.1 Lessons from Run IIa

Several difficulties were encountered by DØ during the Run IIa silicon detector prototyping and construction. The gained Run IIa experiences and important conclusions are:

- Sophisticated double-sided silicon sensors were difficult to produce and lead to lower yield and hence significant delays. Single-sided sensors however, which have been produced both by Elma for the H-disks and Micron for the 1^{st} and 3^{rd} layers of barrels 1 and 6 for the Run IIa detector, had higher yields and caused much less trouble due to their simplicity.

- The introduction of an alternative vendor at the later stages helped to speed up production.

- The large number of sensor types complicated the production process.

- Double-sided sensors proved to be very difficult to handle.

- Radiation studies have shown that double-sided (and especially 90^o double-metal) silicon sensors have limited radiation hardness (more details in "Radiation testing")

- Detailed pattern recognition studies have shown that in high occupancy environment, "ghost" hits produced in 90^o sensors lead to a significant fraction of fake tracks and increased reconstruction time.

For the Run IIb silicon sensors, we adopted the following guidelines:

- Use only single sided silicon sensors.

- Try to identify alternative vendors whenever possible.

- Limit the number of sensor types to 3.
- Use only small stereo angles, achieved by sensor rotation.
- Avoid double metallization.

In our choice of radiation hard technology we have benefited greatly from radiation hard silicon R&D studies motivated primarily by the needs of LHC experiments.

3.1.2 Radiation damage in silicon

The most important damage mechanism in silicon is the bulk damage due to the non-ionizing part of the energy loss, which leads to a displacement of the silicon atoms in their lattice. It causes changes in doping concentration (and, eventually, silicon type inversion), increased leakage current, and decreased charge collection efficiency. Surface damage due to ionizing radiation results in charge trapping at the surface interfaces and leads to increased interstrip capacitance and electronics noise. A general overview of radiation damage in silicon detectors can be found in DØ Note 3803.

The change in the effective impurity or doping concentration $N_{eff} = [2\varepsilon\varepsilon_0/(ed^2)]\cdot V_{depl}$ measured as a function of the particle fluence for n-type starting material shows a decrease until the donor concentration equals the acceptor concentration or until the depletion voltage V_{depl} is almost zero, indicating *intrinsic* material. Towards higher fluences the effective concentration starts to increase again and shows a linear rise of acceptor like defects. The phenomena of changing from n-type to p-type like material has been confirmed by many experimental groups and usually the detector is said to have undergone a "type inversion" from n-type to p-type. The change of the effective doping concentration can be parameterized as

$$N_{eff}(\Phi) = N_{D,0} \cdot \exp(-c_D\Phi) - g_c\Phi$$

where the first term describes donor removal from the starting donor concentration $N_{D,0}$ and g_c indicates the rate of the radiation induced acceptor state increase. Hence donor removal happens exponentially whereas acceptor states are created linearly with fluence. Type inversion for standard n-type material with resistivity $\rho \approx 5k\Omega cm$ typically occurs at a fluence of about $(1\text{-}2)\times10^{13}cm^{-2}$.

The radiation-induced changes of the doping concentration are initially not stable and exhibit two main components with different time behaviors and temperature dependences. With time constants in the range of a few days a decrease in the radiation induced changes occurs soon after irradiation. This effect is called short-term annealing or beneficial annealing, because it mitigates the acceptor creation and hence the type inversion process. However, at room temperature an increase in the acceptor states appears after about two weeks of annealing leading to even higher depletion voltages. This long term or reverse annealing is a major concern because of its limiting factor for long-term operation of silicon detectors in high fluence regions. Reverse annealing can be almost completely suppressed by cooling the detector to 0^oC or less and by minimizing the maintenance periods of the silicon detectors at room temperature.

For the operation of detectors the control of leakage current is important in two aspects, one is the resulting higher shot noise, the other is the increased bulk heat production in silicon which may lead to a thermal runaway if the silicon detector is not properly cooled. The leakage current of silicon detectors increases with radiation dose due to the creation of additional gap states which will lead to more electron-hole pair generation and thus to an increase in bulk or generation current. This generation current is by far the dominant part of the entire leakage current after the silicon has been irradiated. The increase in leakage current can be parameterized as:

$$I = I_0 + \alpha \cdot \Phi \cdot A \cdot d$$

Where I_0 is the bias current before radiation, α is a damage rate coefficient usually defined at T=20°C and dependent on particle type, Φ is the particle fluence given in particles per cm^2, A is the detector area, and d is the thickness of the detector. The exact value of α depends on particle type and energy and varies between (2-3) $\times 10^{-17}$ A/cm once the silicon is completely annealed and α reaches a constant value. The leakage current rises linearly with fluence and does not depend on either the silicon detector properties or special process characteristics during the silicon sensor manufacturing. The leakage current in silicon sensors due to generation of electron-hole pairs is strongly temperature dependent and the ratio of currents at two temperatures T1 and T2 is given by

$$I_2(T_2) / I_1(T_1) = (T_2/T_1)^2 \cdot \exp(-[E_g(T_1-T_2)]/[2\kappa_b T_1 \cdot T_2])$$

With κ_b being the Boltzmann constant ($\kappa_b = 8.6 \times 10^{-5}$ *e*V/K) and E_g the gap energy in silicon (E_g = 1.2*e*V).

A third effect from radiation is the reduced charge collection efficiency. The primary mechanism leading to a decrease in the collection of electrons or holes is charge trapping at defect sites, i.e. a decrease of the carrier lifetime with increasing fluence. In addition surface damage in the silicon oxide due to ionizing radiation results in the creation of fixed positive charge at the surface boundary between silicon and silicon oxide. This leads to increased interstrip capacitances and, therefore, higher electronic noise.

Seriously damaged detectors will require high bias voltages to operate efficiently. The deteriorated charge collection can be efficiently recovered by applying a bias exceeding the depletion voltage. This overbiasing also reduces to normal values the increased interstrip capacitance due to the surface charge accumulation. High voltage operation is therefore crucial for radiation hard silicon and the breakdown voltage of the device will determine the limits of survivability.

3.1.3 Radiation hard designs

The CMS collaboration designed single-sided 300 μm thick n-type sensors, which were reliably working after heavy irradiation at bias voltages up to 500 V[2]. The main features of the design are p+ strips in n-bulk silicon, which are biased with polysilicon resistors and are AC coupled to the readout electronics. The front side of the detector (with p+ strips) has a peripheral n+ implantation (n-well) at the edge and is followed by a p+ single guard ring structure to prevent junction breakdowns. This guard ring design has been optimized in cooperation with Hamamatsu and is also successfully implemented with other producers. It is proven to be radiation hard and CDF is using this type of sensors for the L00 of SVX in Run IIa. Other radiation hard designs reduce the risk of an early breakdown at the edges of the silicon by including a multi-guard ring structure[3].

We note here that in the case of AC-coupled double-sided sensors (as presently used by CDF and DØ in Run IIa) the high bias voltage is applied across the coupling capacitor on one of the sides (unless the electronics is floating at the same potential). Together with considerably higher costs related to the double-sided wafer processing, the requirement that AC capacitors hold off the bias voltage is a strong limitation for the double-sided detectors and we are not considering using them for the upgrade.

Another option to improve the radiation hardness at moderate fluences is the use of low-resistivity silicon as an initial detector material[4]. Low bulk resistivity of silicon corresponds to high depletion voltage of the device. For example, a 300 μm thick detector with bulk resistivity of $r \approx 1.0 k\Omega \cdot cm$ depletes at $V_{depl} \approx 300\,\mathrm{V}$. High initial depletion voltage values shift the type-inversion point towards higher fluences, and limits the depletion voltage growth after the type inversion, thus improving the radiation hardness of the sensor in the moderate fluence regime of up to 10^{14} cm^{-2}.

A new technological development driven by the R&D work of the ROSE collaboration[5] uses oxygenated silicon materials to improve the radiation hardness of silicon detectors. Oxygen concentrations ($[O_i] \approx 10^{17} cm^{-3}$) in silicon considerably improves the radiation hardness of the detector for charged particle fluence and effectively lowers the needed bias voltage for radiation damaged detectors. No improvement was observed for damage caused by neutrons. The charged particle component is expected to dominate (for example at CMS only 1/10th of the damage is accounted for by neutrons). There are indications also that the reverse annealing saturates at high fluences for oxygen enriched silicon.

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[2] S. Braibant et al., Investigation of design parameters for radiation hard silicon, Nucl.Instr.Meth A485:343-361,2002.
[3] A. Bischoff et al., Breakdown protection and long term stabilization for Si-detectors, Nucl. Instr. & Meths. **A326** (1993)27-37.
[4] RD20 collaboration, "Radiation damage studies of field plate and p-stop n-side silicon microstrip detectors", Nucl. Instr. & Meths. **A362** (1995) 297-314, 1995.
[5] Rose Collaboration, Nucl. Instr. & Meth. in Phys. Res. **A466** (2001) 308-326

High oxygen concentrations reduce the donor (n-impurity) removal rate significantly and can mitigate the acceptor (p-impurity) creation. The simplest way to enrich silicon material with oxygen is a diffusion process in the $\sim 1200^{o} C$ oxygen atmosphere of a quartz oven. This technology is easy and economic and has been successfully transferred to a number of silicon detector vendors.

Finally there is an alternative to use n+ strips on n type silicon. It has been shown that they offer a better charge collection efficiency at under-depleted voltages and, therefore, would improve the performance after irradiation. However, the detectors technologically are more complicated and require further R&D efforts. Since for $n^{+}n$ sensors certain techniques like p-stop or p-spray are necessary to maintain the strip isolation, the detectors are becoming more and more complex which would considerably drive up the costs. Furthermore, it is not clear that such a fine pitch structure of 25μm we are requiring for layer 0 is technologically feasible on $n^{+}n$ devices. Except LHCb, which is pursuing a $n^{+}n$ option for its vertex microstrip detector, neither of the other LHC silicon strip detectors will use $n^{+}n$ and we are considering this technology as too risky for the tight Run IIb schedule.

In summary, three approaches have been successfully explored so far:

- Special designed guard ring structures. Such guard rings are important in order to keep the breakdown voltage before and after irradiation as high as possible.

- Low-resistivity silicon sensors. Increasing initial donor concentration leads to type inversion after higher radiation doses, thus slowing the radiation damage.

- Oxygenated silicon. Controlled increase in oxygen concentration slows down the growth of depletion voltage with irradiation dose.

It is possible to combine all three approaches. The techniques have been transferred to multiple silicon vendors.

3.2 Silicon Sensors for Run IIb

For the construction of the Silicon Microstrip Tracker for Run IIb DØ we propose the use of AC-coupled, single-sided single-metal p^{+} on n-bulk silicon devices with integrated polysilicon resistors as baseline sensors. Only bias resistors based on polysilicon are capable of sustaining the high radiation level the Run IIb detector will experience. Either a multiguard structure (see Figure 7a) or a single guard ring structure with a peripheral n-well at the scribing edge (see Figure 7b), developed in cooperation with Hamamatsu's design engineers, is necessary to allow operation at high bias voltages.

a) b)

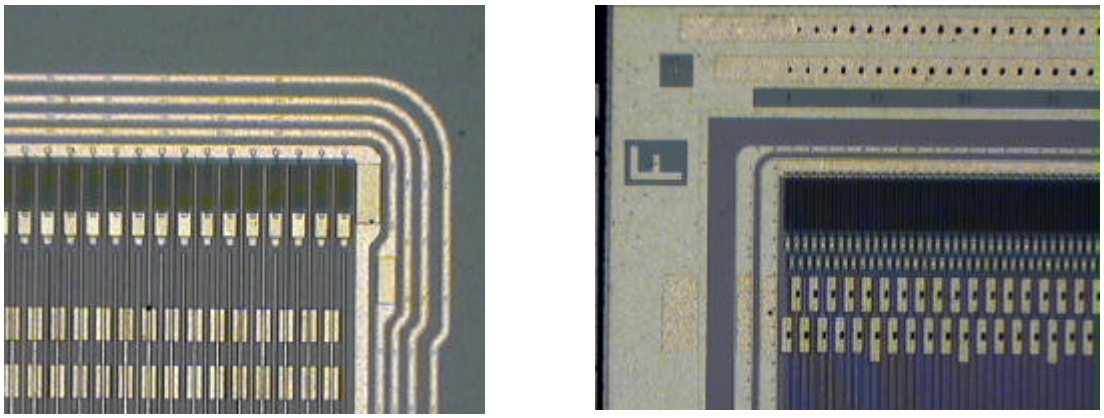

Figure 7 a) Multiguard ring structure of ELMA prototype sensors. b) Hamamatsu's sensor with a single guard ring structure and a peripheral n-well.

We prefer a silicon microstrip vendor capable of doing multilayered dielectric substrates for the coupling capacitors for two reasons. First, it will significantly reduce the number of pinholes and therefore shorted capacitors in the detector. Secondly, by using silicon nitride (Si_3N_4) in addition to silicon oxide, the coupling capacitor value can be increased while leaving the thickness of the dielectric substrate constant.

Oxygenation is considered as a serious option for the inner layers 0 and 1 in order to improve the radiation hardness further.

DØ envisions using 3 sensor types for Run IIb. Their geometric parameters are summarized in Table 2.

Table 2 Geometric parameters of silicon sensors.

Layers	Active Length (mm)	Active Width (mm)	Strip pitch /readout pitch (μm)	# readout channels	# of sensors + spares
0	77.36	12.8	25/50	256	144+50%=216
1	77.36	22.272	29/58	384	144+50%=216
2-5	98.33	38.372	30/60	639	1896+20%=2280

All outer layers are constructed from sensors of the same type. In the specified geometry, two such sensors can fit on one 6" silicon wafer. Unfortunately, 6" technology is not widely used among companies capable of producing silicon sensors. Hamamatsu, ST Microelectronics, SINTEF and Micron Semiconductors are the only vendors which have implemented 6" technology successfully so far. We have contacted all of the mentioned vendors above and

believe that only Hamamatsu and ST Microelectronics are able to produce the amount and quality we require for the Run IIb detector at decent costs. Since ST Microelectronics is presently processing only 6''-wafers with a thickness of 500μm, the number of potential vendors is reduced to one company: Hamamatsu. The other vendors, which could manufacture silicon strip sensors, continue to produce sensors using 4" or even 5'' technology. Although it would be possible to modify the design to use two 50-mm long sensors to fit on a 4" wafer, instead of one 100-mm long sensor, this choice has many drawbacks: increased number of parts; additional wire bonding and sensor testing load; increased dead area; and, most importantly, significant increase in cost.

Upon our request, the company ST Microelectronics is currently evaluating if their 5''-wafer production line is suited for the fabrication of fine pitch microstrip silicon detectors in the wafer thickness we are requesting. One L2-L5 sensor would fit on a 5''-wafer. However, we have to wait for the outcome of the evaluation study at ST, in order to understand if ST could be considered as an additional potential vendor.

We have chosen to use sensors with an active length of 77.36 mm for layers 1 and 0 to minimize occupancy and noise, and more importantly, to take advantage of a wider choice of vendors. These sensors can be fabricated with two L0 type sensors or one L1 type sensor on a single 4" wafer. Since these sensors will be subject to a very harsh radiation environment, it is critical to choose a vendor that can provide radiation-resilient devices.

Table 3 The main specifications for layer 0 and 1 and the outer layers 2-5.

Specifications:	**Layer 0/1**	**Layer 2-5**
Wafer thickness	320±20μm, wafer warp less than 50μm	320±20μm, wafer warp less than 50μm
Depletion voltage	V<300V	V<300V
Leakage current	<100nA/cm2 at RT and FDV+10%V, total current < 4μA at 700V	<100nA/cm2 at RT and FDV+10%V, total current < 16μA at 350V
Junction breakdown	>700V	>350V
Implant width	7μm	8μm
Al width	2-3 μm overhanging metal	2-3 μm overhanging metal
Coupling capacitance	>10pF/cm	>12pF/cm
Coupling capacitor breakdown	>100V	>100V
Interstrip capacitance	<1.2pF/cm	<1.2pF/cm
Polysilicon bias resistor	0.8±0.3 MΩ	0.8±0.3 MΩ
Not working strips	<1%	<1%

We plan to use intermediate strips in all sensors to improve the single hit resolution. A multiple guard-ring, or alternatively, a Hamamatsu-style single guard-ring structure is necessary to ensure high breakdown voltage after irradiation. The two aforementioned structures occupy roughly a 1-mm wide area on each edge of a silicon sensor. The main parameters of the silicon sensors are given in Table 2 and Table 3.

3.3 Fluence Estimation for Run IIb

Several fluence predictions for Run II have been given by Matthews *et al*[6], Frautschi *et al*.[7] and Ellison *et al*.[8] Leakage current measurements performed on the CDF SVX and SVX' silicon detectors as a function of sensor radius from the beam and delivered luminosity during the Run

[6] John A. J. Matthews et al., CDF Notes 3408 and 3937.
[7] M. Frautschi, CDF Note 2368.
[8] J. Ellison and A. Heinson, "Effects of Radiation Damage on the DØ Silicon Tracker", DØ Note 2679 (July 1995).

Ia+b provide us with a solid basis for expectations. The derived charged particle fluence quantities vary among the various authors between 1.5×10^{13} MIPs/cm^2/fb^{-1} and 1.9×10^{13} MIPs/cm^2/fb^{-1} for the new SVXII layer 0 detectors which are located at a radial distance of r≈2.42cm from the beam axis. All of the mentioned CDF expectations have in common that the radial scaling of the fluence occurs as $r^{-1.68}$, a fact, which has been verified by independent dose measurements in the CDF detector.

To normalize the observed CDF leakage current measurements to a standard neutron or proton fluence, assumptions about the radiation damage rate constant α have to be made. Matthews[9] has given an equivalent 1 MeV neutron fluence per fb^{-1} of $(2.19\pm0.63)\times10^{13}\cdot r[cm]^{-1.68}[cm^{-2}/fb^{-1}]$. In his fluence determination, he assumed a frequently used α value for 1 MeV neutrons in order to convert the observed current increase to an effective 1 MeV neutron fluence. He took α to be $(2.86\pm0.18)\times10^{-17}$ A/cm, which is still a good value for neutrons[10] if most of the annealing of the leakage currents has occurred. Since the CDF strip measurements are not done in a fully annealed state, he applied a factor of 1.1 to α according to common annealing parameterizations[11] in order to take the partial annealing of the detector currents into account. Matthews propagated the uncertainties on silicon temperature, leakage current measurements, and α value into a final fluence uncertainty of ±30%.

The number of secondary particles produced in the Be beam pipes of the CDF and DØ experiment should be rather similar. The only difference may occur in the number of curling particles which are traversing the silicon layers more than once (caused by different magnetic field strengths in each experiment). CDF has a solenoid with 1.4T while DØ has a 2T field for their magnet. In the study of Ellison et al, it was found that 50% of the total fluence will come from looper particles in the DØ magnetic field. Frautschi, who has done similar studies for CDF assumed only a 30% contribution.

The strategy of the predictions for the leakage current rise and depletion voltage changes for Run IIb presented here will be as follows: For the leakage current estimations we are using the measured strip current numbers by CDF in Run I and scale to the appropriate DØ geometries and temperatures. This approach is essentially independent of the α value, but assumes the same fluences of charged particles in the CDF and DØ experiments. In order to estimate the upper uncertainties for the leakage currents, we varied the temperature at which the CDF strip leakage current measurements took place according to their given uncertainties. Furthermore, we then increased the CDF strip currents and hence the fluence by another 20% in order to take into account a possible difference in the numbers of looper particles between DØ and CDF. More details on this approach and on the results can be found in DØ Note 3959.

The proposed 1 MeV equivalent fluence of $(2.19\pm0.63)\times10^{13}\cdot r[cm]^{-1.68}[cm^{-2}/fb^{-1}]$ by Matthews can be translated into an equivalent fluence of any other particle at any kinetic energy by knowing the corresponding so-called non-ionizing energy loss (NIEL) damage or displacement damage cross section value of the particle at a given energy. These NIEL values for neutrons,

[9] J. Matthew et al., CDF Notes 3408 and 3937.
[10] M. Moll, private communication.
[11] R. Wunstorf, Ph.D. Thesis, Hamburg, 1992.

protons, pions and electrons are normalized to the standard displacement damage cross section for 1 MeV neutrons according to an ASTM standard and are tabulated in a useful online compilation[12].

For the depletion voltage predictions, the 1 MeV neutron fluence number as given by Matthews is taken, and under the assumption of the NIEL hypothesis, we calculate the depletion voltage changes according to the latest parameters of the Hamburg model, which gives the best current phenomenological description of the change in effective doping concentration in silicon during hadron irradiation. To obtain an upper bound on the depletion voltage after irradiation, a safety factor of 1.5 (in agreement with CDF) is added and the 1 MeV equivalent fluence is varied accordingly.

3.4 Silicon Sensor Performance Extrapolations for Run IIb

3.4.1 Leakage current and shot noise estimations

Strip leakage current measurements from CDF as a function of sensor radius from the beam and delivered luminosity are used to derive an average increase in the strip currents at T=(24±2)°C which can be scaled from their strip geometry to the DØ configuration as shown in Table 4. The thickness of the silicon sensors is taken to be 320μm. Radial scaling is taken to be $r^{-1.7}$.

The strip leakage currents in nA and per fb^{-1} for the various layers of the DØ Run IIb detectors at five different temperatures, which are of interest for the operation in Run IIb, are given in Table 5. Note that not only a readout strip, which is AC coupled to the preamplifier, but also an intermediate strip produces the same current. Therefore we do not distinguish between the two types of strips if only strip currents are considered. The calculations assume that the silicon sensors generating the leakage currents are held uniformly at the considered temperature. In reality however, the silicon sensors have temperature drops along the silicon length and an attempt to include the temperature gradient along the silicon sensors is given in the next section.

[12] A. Vasilescu and G. Lindstrom, Displacement damage in silicon, online compilation, http://sesam.desy.de/gunnar/Si-dfuncs.html

Table 4 Sensor parameters used to extrapolate Leakage Current and Depletion Voltage Measurements.

Layer	Min. radius (cm)	Max active Length (cm)	Pitch (μm)	Strip Volume (mm^3)
0-A	1.78	7.74	25	0.619
1-A	3.48	7.74	29	0.718
2-A	5.32	19.66	30	1.887
3-A	8.62	19.66	30	1.887
4-A	11.69	19.66	30	1.887
5-A	14.7	19.66	30	1.887

Finally, the shot noise that is caused by the strip leakage currents is obtained in the following way[13]: ENC_{shot} = SQRT(12·I[nA]·τ) electrons Equivalent Noise Charge (ENC) where τ is the shaping time of the amplifier in ns, which is taken to be 132 ns. The shot noise calculations assume that the intermediate strips fully couple their noise through interstrip capacitances to the two neighbor readout strips. For fine-pitch detectors the interstrip capacitance dominates the total strip capacitance. We conservatively assume that the noise of the intermediate strips is fully coupled to the readout strips and do not include the reduction of noise due to coupling to the backplane. The expected strip noise in ENC after 15 fb^{-1} is shown in Table 6, again at different temperatures.

[13] H. Spieler, IEEE Trans. Nucl. Sci. NS-32, 419 (1985)

Table 5 Expected strip leakage currents in nA/fb^{-1}

Layer	T = -10°C	T = -5°C	T = 0°C	T = +5°C	T=+10°C
0A	14.0	23.7	39.4	64.7	104.2
1A	5.2	8.8	14.6	24.0	38.7
2A	6.7	11.3	18.9	31.0	49.8
3A	2.9	5.0	8.3	13.6	21.9
4A	1.7	3.0	4.9	8.1	13.1
5A	1.2	2.0	3.4	5.5	8.9

Table 6 Expected strip noise in ENC after 15 fb^{-1}

Layer	T = -10°C	T = -5°C	T = 0°C	T = +5°C	T=+10°C
0A	814	1061	1370	1753	2225
1A	496	646	834	1068	1355
2A	563	733	947	1212	1539
3A	373	487	628	804	1021
4A	288	376	485	621	788
5A	237	309	399	511	649

The uncertainties in the measured CDF strip currents were 10%. In addition, there is a temperature uncertainty of ±2°C. By changing the operation temperature of SVX and SVX' from T=24°C to T=22°C, our estimate produces higher leakage currents by 15-20%. In addition to the temperature uncertainty of the leakage current measurements, the value itself was increased by 20% to take into account the possibility of different charged particle fluences between DØ and CDF due to the number of curlers in the higher DØ field. Studies using DØ radiation monitors at r=3 cm indicate that this effect is small between 1.5 and 2 Tesla.[14] The combined resulting upper leakage current values are given in the table. This approach should be

[14] Naeem Ahmed, private communication of "Looper Studies" in progress, August 23 2002.

conservative enough to estimate the expected leakage currents and hence the shot noise levels for Run IIb in a safe way.

3.4.2 Leakage currents for a realistic silicon temperature profile

The calculation of the leakage currents and hence shot noise in the previous section assumed a uniform temperature along the silicon sensors. Due to the assembly of the hybrid on top of the silicon sensors, the temperature along the silicon is not constant and large temperature drops in the silicon itself are possible. In a finite-element analysis (FEA) study, the temperature gradient along the silicon sensors has been determined for layer 1 and layer 2 modules based on a realistic modeling of the power dissipation, the heat transfer of the cooling fluid and the thermal impedances. The coolant temperature was set to $T_{coolant}$=-15ºC. The FEA based temperature gradients have been used to estimate an equivalent average temperature T_{equiv} , at which the same leakage current output would have been produced, as if the sensor would have been uniformly kept at this temperature. The Figure 8 shows the anticipated temperature distribution along the z-axis for a layer 2 module. The strip leakage currents are in nA/fb^{-1} normalized to a strip unit length of 3 mm (used as binning in the FEA) and are shown as well. Since the stave design is identical in the other outer layers, the same thermal profile is expected for layers 3-5.

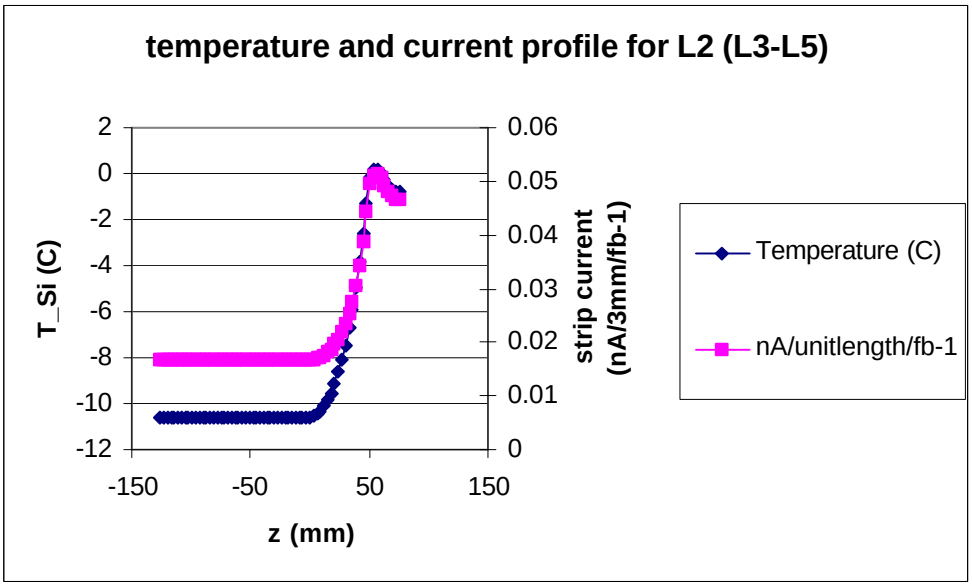

Figure 8. Expected temperature gradient and strip currents in nA per unit length (3mm) and per fb^{-1} as a function of z. The temperature profile has been obtained by FEA.

The warmest region of T~0ºC in the silicon sensor is, where the readout chips on the hybrid are located. To obtain the total strip currents for the layers, the differential strip currents along the ladder modules have been summed. Based on the produced currents of the assumed temperature profile of the silicon, the equivalent temperature T_{equiv} for a long module – if kept at uniform temperature – would be T_{equiv}=-8ºC. This reference temperature is valid for a coolant at $T_{coolant}$=-15ºC and can be used to estimate the leakage current values, which are tabulated in Table 5. In another FEA study the thermal performance of the layer 1 design has been addressed in order to

obtain the corresponding layer 1 thermal profile. In that case, we found the layer 1 equivalent temperature to be T_{equiv}=-5ºC, if the coolant is circulated at $T_{coolant}$=-15ºC.

3.4.3 Depletion voltage predictions

As previously mentioned, the depletion voltage predictions we are presenting are based on the 1 MeV equivalent fluence assumptions for Run II by Matthews *et al*. In addition we apply a safety factor of 1.5 to that fluence. The latest parameters for the stable damage constants, the beneficial annealing and the reverse annealing constants of the so-called Hamburg model have been used along with the Tevatron running scenario listed in Table 7. The obtained depletion voltage predictions are called standard depletion voltage predictions.

Table 7: The Tevatron Run IIb running scenario used for the calculation of the depletion voltage changes.

Year	Max luminosity pb-1/week	Shutdown (months)	max luminosity fb-1/year	Cumulated luminosity fb-1
2005	61	4	1.81	1.81
2006	81	1	3.38	5.19
2007	81	1	3.85	9.04
2008	81	1	3.85	12.89

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In the standard predictions, it is assumed that the silicon detector is kept cold entirely during the luminosity runs as well as during the shutdown periods. This operation temperature is assumed to be uniform. The resulting standard depletion voltage for different operating temperature for the layers 0, 1 and layer 2 are shown in Figure 9. We present three calculations for layer 0 at uniform silicon temperatures of –10ºC, 0ºC and +10ºC and with a starting depletion voltage of 150V as well as one scenario for layer 0 with starting depletion voltage of 50V. Furthermore, we give two standard depletion voltage predictions for layer 1 and one prediction for layer 2.

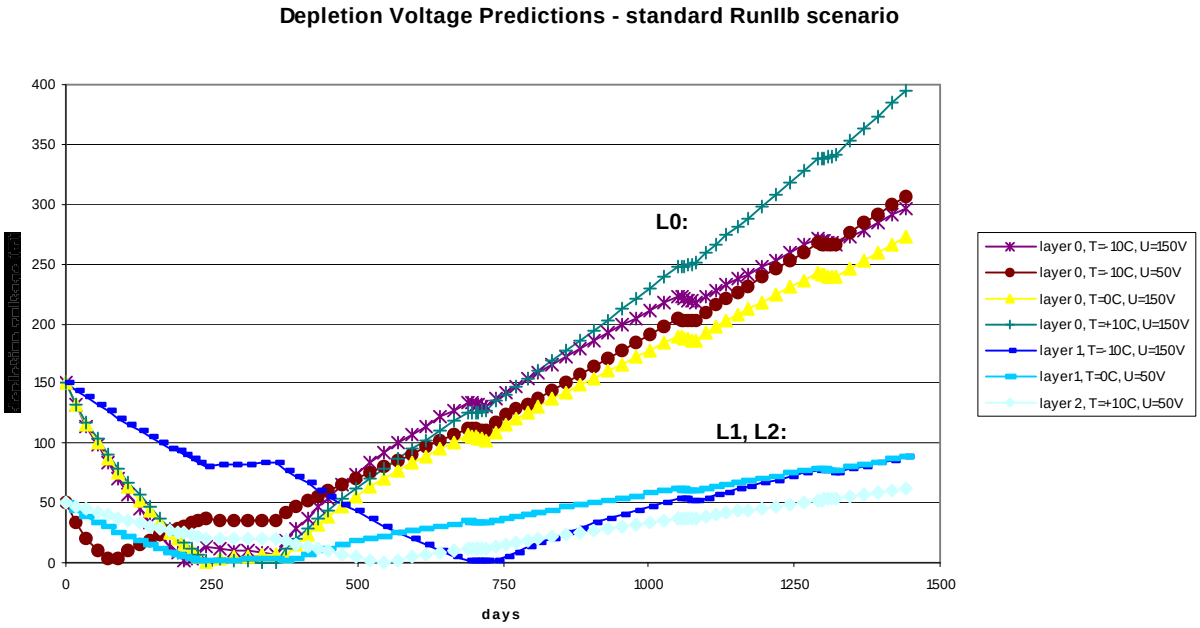

Figure 9. - Depletion voltage for layer 0 and layer 1 sensors as a function of days in Run IIb. The running scenario is given in table5. The 1460 days of running correspond to an integrated luminosity of 12.9 fb-1.

In the standard Run IIb scenario, the depletion voltage of layer 0 will reach values of around 300V as long as the silicon temperature does not exceed T=0ºC. Estimates show that it does not really matter for the final depletion voltage if the initial depletion voltage happens to be around 150V or only 50V. Layer 1 is expected to deplete at around 100V at the end of the standard running period. It is surprising that the final depletion voltage of layer 1 is the same for two presented calculations using very different assumptions: T=-10ºC and U_{depl}=150V compared to T=0ºC and U_{depl}=50V. This can be explained by a suppression of the reverse annealing term even at T=0ºC. Indeed, a calculation (not shown in the figure) having layer 1 at T=+10ºC would reach a final depletion voltage of 140V and hence shows the first signs of reverse annealing effects, which now begin to dominate over the beneficial annealing mechanism. Finally, Figure 9 contains a depletion voltage prediction for layer 2, which depletes below 80V at the end of the standard running. This value is obtained even at a moderately high temperature of T=+10ºC.

Note, that these values represent only the value of the depletion voltage itself and do not guarantee full charge collection in the silicon. A safety margin of at least a factor of 1.5 in the bias voltage should be applied in order to have enough flexibility in overbiasing the detectors and to compensate potential charge losses due to ballistic deficits after irradiation. Therefore, we have specified the breakdown voltage of the layer 0 sensors to be above 700V to provide for such a safety margin.

There is some variation in the radiation damage constants and reverse annealing parameters used in the Hamburg model for different silicon wafer materials. However, these uncertainties are absorbed in the fluence safety factor of 1.5, which we have included in the depletion voltage

calculations. Moreover, we feel that it is important to irradiate samples of detectors used in Run IIb to verify that the damage response is consistent with an operation of up to 15MRad, corresponding to more than twice the expected dose of layer 0 in Run IIb.

As it was demonstrated in Figure 9, temperature effects of the reverse annealing in the standard running scenario tend to saturate already at T=0ºC, and the depletion voltage values for T= 0ºC and T=-10ºC did not differ much. However, reverse annealing increases rapidly if the operation temperature reaches higher temperatures of T=+10ºC or more. At such high temperatures the reverse annealing makes a significant contribution and cannot be neglected anymore. This could be a concern for the detector operation if a warming up period due to cooling problems or simply an access at room temperature happens. In addition we have to investigate the operation of our silicon sensors if the radiation levels are higher than expected or if the Tevatron running extends over the standard scenario. Therefore we have expanded the standard Run IIb scenario now over a total of 6 years and calculate the anticipated depletion voltage after having accumulated a total luminosity of 20 fb^{-1}. Moreover, periods at room temperature have been included in this scenario.

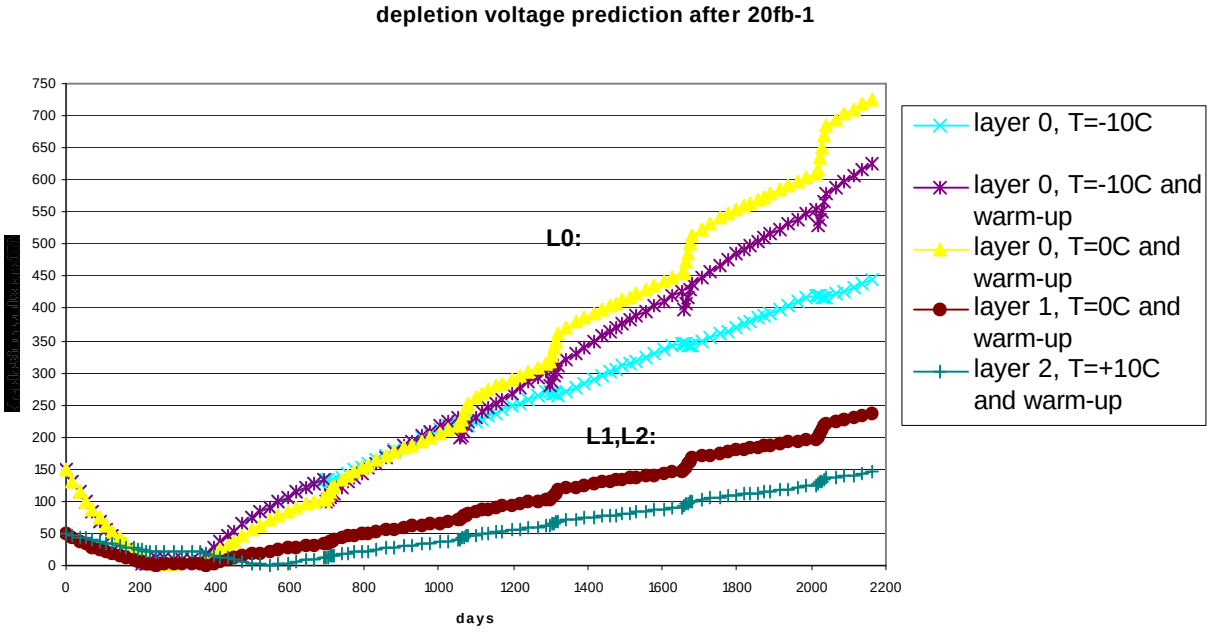

Figure 10. Depletion voltage prediction after 20 fb^{-1}.

Figure 10 contains such depletion voltage graphs for layer 0, 1 and 2. In this extended scenario the layer 0 sensors are expected to deplete now at around 450V (without warming up) and since we are specifying the sensor breakdown to be at least 700V, we would still have enough margin in the biasing to accommodate a longer Tevatron running of up to 20fb^{-1}.

In addition this plot contains two other layer 0 depletion voltage graphs: Four warm periods, each lasting 4 weeks at room temperature are included, in order to estimate the reverse annealing effects. One calculation was done keeping the sensors normally at T=-10ºC and the other one at

T=0ºC. The reverse annealing will now dominate and will shift the depletion voltage to much higher levels of around 700V. It is therefore quite important to avoid any warm up after the detector has been irradiated. We should point out, that for the operation of the silicon detectors in layer 0 and 1, a temperature as cold as possible is safer against reverse annealing, especially if warm periods are included in the depletion voltage scenario.

3.4.4 Signal to noise ratio

Signal to noise ratio (S/N) is an important parameter that ultimately limits the detector lifetime. Based on previous studies and CDF experience in Run 1, S/N starts affecting b-tagging efficiency seriously when it degrades below a value of 5 [15]. Our design goal is to keep the S/N conservatively above 10 for all layers of the detector. The S/N should remain above this limit even for an extended Run IIb of up to $20fb^{-1}$. In addition we prefer to set the operation temperatures such, that the S/N of the silicon layers should not degrade by more than 15% over the course of the Run IIb period in order to ensure a stable and robust S/N over the full lifetime of the silicon detector.

In our signal-to-noise (S/N) estimates we assume that sensors can be fully depleted and that one MIP produces a most probable charge value of 23,000 e^- in 320 μm silicon. We have considered several contributions to the total noise:

- Noise in the front end due to capacitive load: the analog cable in layer 0 contributes with 0.4 pF/cm to the total capacitive load. The silicon sensors are conservatively assumed to have a total load capacitance of 1.4pF/cm, dominated by the interstrip capacitance. The ENC noise behavior of the front end chip (SVX4) is taken to be 450+43*C(pF) according to the specifications.

- Noise due to the series resistance of the aluminum traces of the silicon sensors and – for layer 0- the copper traces of the analog cable. The serial noise varies between ~210e for layer 1 sensors (only 7.66cm long) and ~780e for 19.7 cm long modules in layer 2-5.

- Shot noise from detector leakage current as calculated before. A shaping time of 132 ns is assumed

- Thermal noise due to the finite value of the bias resistor (~250e).

[15] J. Albert et al. " The relationship between signal-to-noise ratio and b-tag efficiency." CDF Note #3338.

In the following, we will present the expected signal to noise ratio based on the noise input assumptions mentioned above as a function of luminosity for layer 0, layer 1 and layer 2 and 3. We plot the S/N for different temperatures in order to derive temperature bounds for the operation of the various layers.

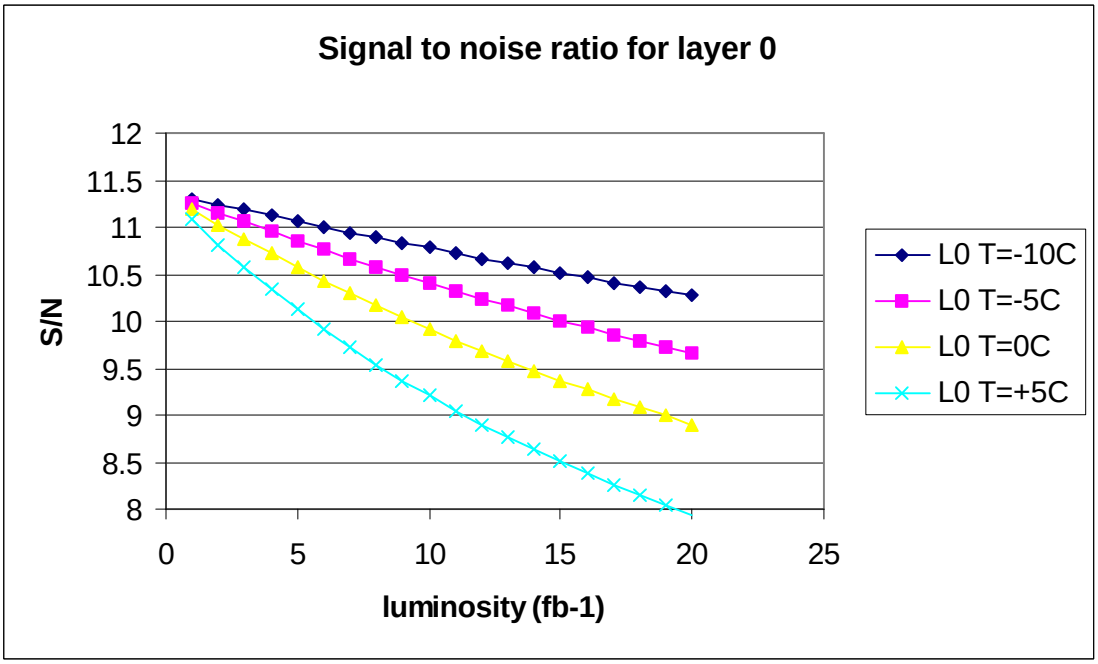

Figure 11. - Signal to noise ratio for layer 0 modules as a function of luminosity for different running temperatures. The noise expected from the analog cable is included.

Figure 11 shows the S/N behavior as a function of luminosity for layer 0 modules. This innermost layer is a special case since is has an up to 450 mm long analog cable to route the silicon signals to the hybrids. These cables will be designed to have a maximum capacitance of not more than ~20 pF[16] so that the total capacitive load of the silicon ladder including the analog cable can be kept around 30 pF. Due to this large load capacitance and serial resistance of the cable, the S/N will be not much higher than 11:1 and any further degradation by additional shot noise should be carefully avoided. Therefore, the best strategy would be to keep the detectors in the innermost layer as cold as possible, i.e. at a temperature of T=-10°C. The S/N will then remain larger than 10 even after 20 fb^{-1}. It is therefore very important to provide the cooling for this layer such that silicon temperatures of T=-10ºC can be reached at the end of the running period. This will give additional safety margin against reverse annealing in case of warming up periods.

Generally, a much higher S/N is achieved with modules from layer 1 due to the absence of the analog cable and the short module length. The S/N of layer 1 is visible in Figure 12. A very high and robust S/N of more than 19:1 can be maintained if layer 1 is kept at T=-5C or lower during

[16] K. Hanagaki, DØ Note 3944

the complete Run IIb period. Under such conditions the S/N performance loss due to the radiation induced shot noise increase is mitigated to less than 15%.

The detectors in layer 2-5 represent with a maximum active length of 19.66 cm a total capacitive load of almost 28 pF. We estimate the noise before irradiation for these layers as high as 1840e for the two-sensor modules. Figure 13 shows the S/N values for layer 2 and layer 3 again as a function of luminosity and for different temperatures. Generally, the S/N of the outer layers does not fall below 10, if they are kept at temperatures around T=0°C. The S/N performance loss in layer 2 can be reduced to less than 15%. For the other outer layers, an operation temperature of T=+5ºC seems to be sufficient.

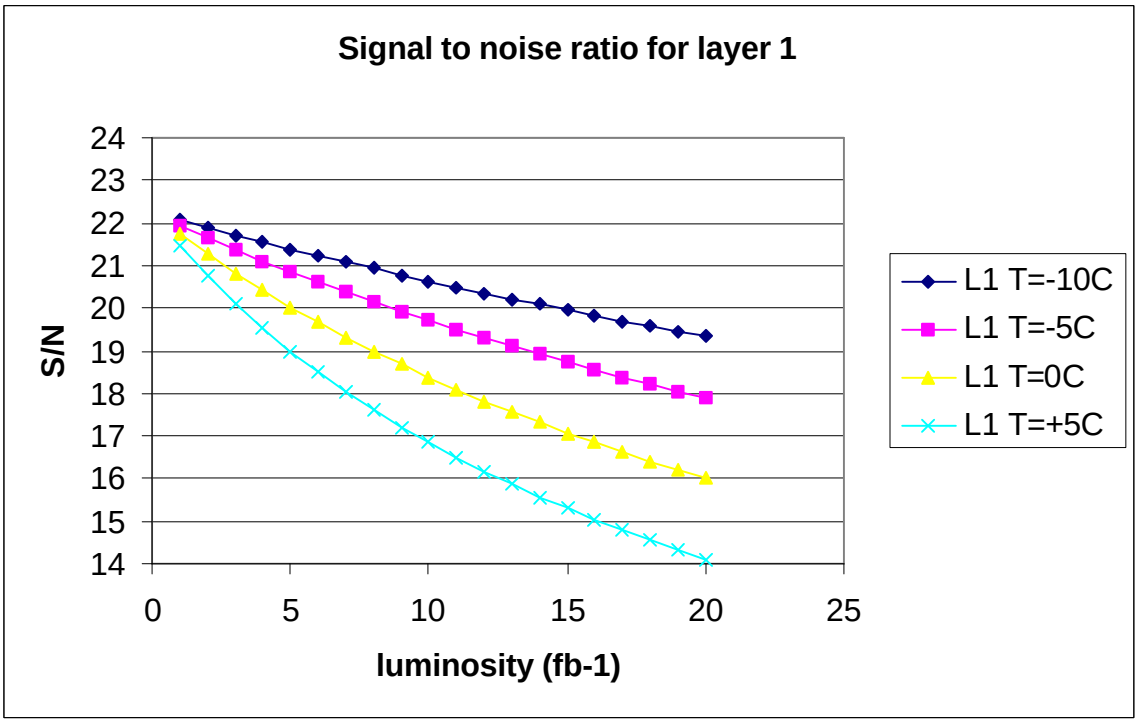

Figure 12: Signal to noise ratio for layer 1 as a function of luminosity for different running temperatures.

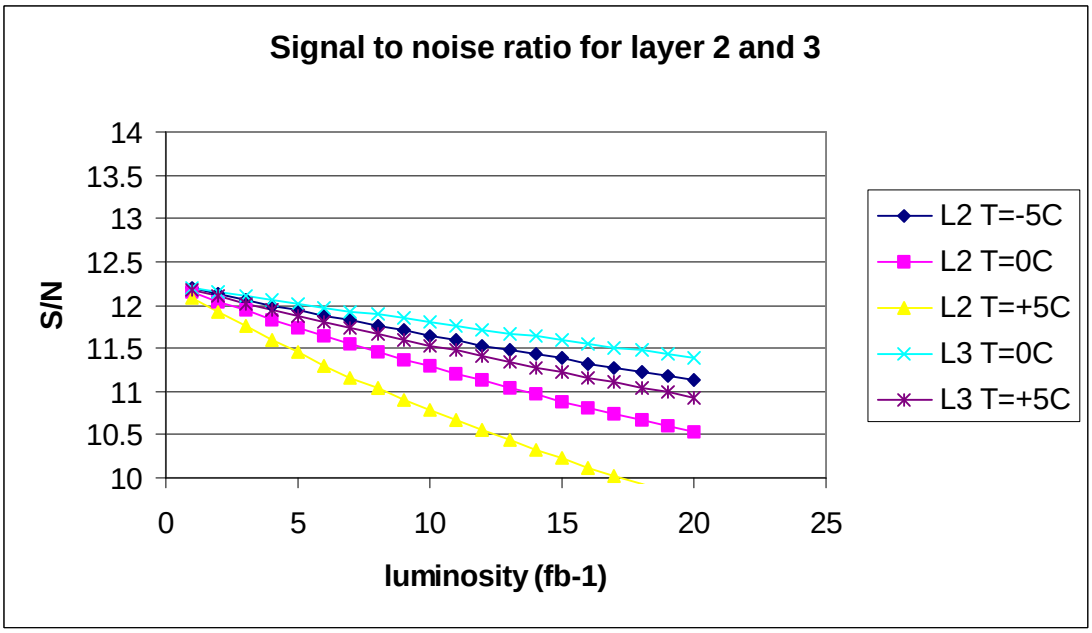

Figure 13. Signal to noise ratio for layer 2 and layer 3 at different temperatures.

In summary, based on our estimations of leakage currents, depletion voltage and S/N we intend to keep the silicon sensors (depending on the layer)at temperatures between T=–10°C and T=+5°C all times. The closer the silicon layer to the beam pipe is, the colder it should be operated.

The sensors of layer 3-5 can be kept between T=+5°C and T=0°C over the entire Run IIb since leakage current noise will not be the dominant noise source. Having the possibility to run layers 3-5 at T=0°C provides additional margin against higher radiation levels or current limitations in the HV supplies. In layer 2 the S/N performance degradation is below 15% if the sensors are maintained at 0°C. The S/N performance loss of 10% for layer 1 after $15fb^{-1}$ translates into an operating temperature of T=–5°C. The thermal profile of the FEA analysis suggests that such a low equivalent temperature for layer 1 can be reached by setting the coolant in the cooling circuit to –15°C. Finally, layer 0 has to be operated at T=–10°C. This low temperature limits shot noise and helps in suppressing the reverse annealing effects, especially if warm-up periods occur.

To check the breakdown behavior of the silicon sensors after irradiation and to compare our predictions to measured depletion voltage values, we have tested silicon sensors from several potential Run IIb vendors at the Radiation Damage Facility in the Fermilab Booster.

3.5 Radiation Testing of Silicon Sensors

3.5.1 Radiation Damage Facility

Radiation tests described here were carried out at the Radiation Damage Facility in the Fermilab Booster. The facility provides 8 GeV protons for various irradiation studies. The beam is ~0.5 cm in radius and is typically $>3x10^{11}$ protons per pulse, with a typical repetition rate of one pulse/3 sec. Beam flux is measured by a toroid and confirmed by irradiation of aluminum foils.

Detectors are mounted in a cold box, which maintains detector temperature at 5°C and allows for detector bias and monitoring. The box is in turn mounted on a x-y table which scans the detector assembly through the beam; insuring uniform irradiation.

Irradiation typically takes one shift. This intense irradiation can leave a substantial charge in the oxide and on detector surfaces. Detectors are then left at 5°C to "cool down" and anneal for ~1 week before testing.

3.5.2 Run IIa detector irradiation studies

To understand the expected lifetime of the Run IIa detector we performed a series of measurements with spare or grade B modules. These tests are described in detail in Ref. [17]. We used 3 different ladder/wedge types of double-sided detectors and one type of single sided detector. All detectors are processed on n-type bulk silicon material with a typical thickness of 300μm with integrated AC coupling and polysilicon bias resistors. The double-sided ladders had either 6, 9 or 14 readout chips on the their front end hybrid, which was directly glued on the silicon. The 6-chip detector is manufactured on a 6"-wafer technology and has 90° stereo strips on the n-side. The 9-chip detector is a stereo detector with a small angle view of 2°. The 14-chip module is a double-sided wedge-shaped detector with varying strip length and angle of ±15° on both sides.

The lifetime of the Run IIa detectors is likely to be determined by the limited voltage that can be applied across the AC coupling capacitors. These capacitors break down near 150 V and can only be safely operated to ~100 V. Thus, with split bias we expect to be limited to a total bias of 200 V. In addition during ladder testing we found that the Micron detectors are subject to microdischarge breakdown on the junction side. The breakdown voltage varies on a detector-to-detector basis but can limit the junction side bias to as low as 10 V. This effect switches sides upon type inversion and is partially mitigated on the n side by compensating effects of oxide charge.

In order to characterize the performance of the irradiated detectors and to understand their behavior after irradiation the following measurements have been carried out:

- leakage current measurements
- depletion voltage determination
- average noise determination
- number of noisy channels

Depletion voltage was measured by measuring the response to a 1064 nm laser, noise and current measurements were performed using our standard set of detector burn-in tests.

[17] J. Gardner et al. "Results from Irradiation Tests on DØ silicon Detectors at the Radiation Damage Facility at Fermilab", DØ Note in progress.

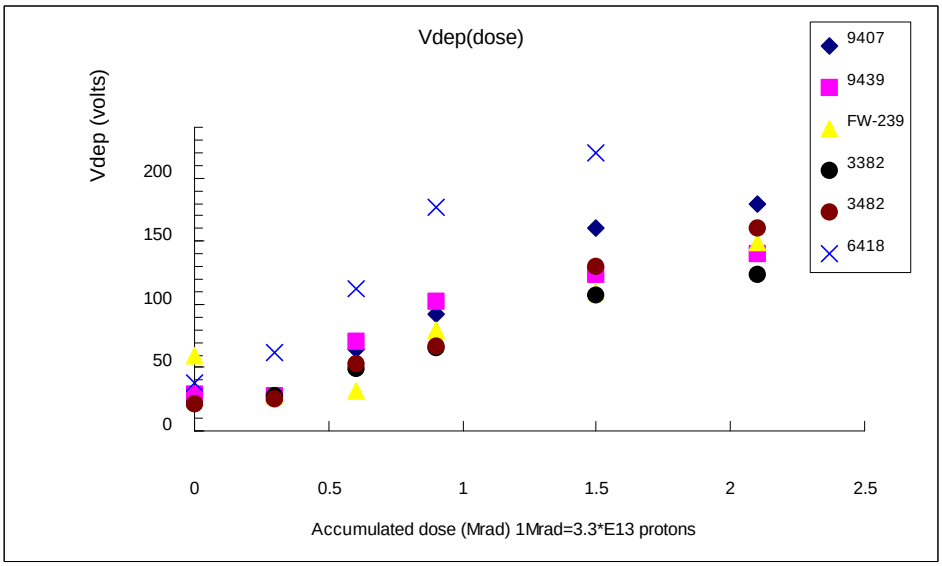

Figure 14. - Depletion voltage as a function of accumulated dose. Detector types 9xxx-layers 2,4; FWxxx-F wedge; 3xxx layers 1,3 barrels 1 and 6 (single sided); 6xxx – layers 1 and 3 barrels 2-5 (double sided double metal)

Figure 14 shows our results for depletion voltage and Table 8 gives the values. With the exception of the double sided double metal (DSDM) devices all detectors perform as expected. The DSDM detectors seem to have a depletion voltage at 1.5 MRad almost a factor of two higher than other devices. Since these detectors are at the inner radius of the silicon detector they will limit the lifetime of the tracker. The cause of this effect is not understood. All detectors were exposed at the same time and tested with identical setups. It is possible that the DSDM detectors are more susceptible to surface charge than simpler devices. We have performed additional irradiation studies with test structures to try to understand if this effect is due to bulk silicon properties or an effect of the fabrication. The tests indicate no problems with the bulk silicon.[18]

Table 8 Depletion Voltage measurements of detectors before and after irradiation.

N of the detector	Vd before irradiation	Vd after 2.1 MRad	Ratio
9407	29 ± 5	180 ± 30	6.2
9439	29 ± 5	140 ± 25	4.8
FW-239	59 ± 9	149 ± 25	2.5
3382	22 ± 4	124 ± 20	5.6
3482	22 ± 4	160 ± 25	7.3
6418	38 ± 6	Not found	

Figure 15 and Figure 16 show the noise in the ladders as a function of dose as measured in the burn-in test. The most probable pulse height for a MIP is ~26 ADC counts. The contribution

[18] S. Lager, Stockholm University Master's Thesis "Proton-Induced Radiation Damage in Double Sided Silicon Diodes and a General User Interface for the DØ Sequencer Low Voltage Power Supply.

from shot noise is ~0.8 ADC counts at 2.1 MRad. In general the noise rises from 1.5-2.0 counts to ~3 counts, giving a worst-case signal/noise ratio of 9:1. The DSDM detector (6418) has additional noise which rises to 5 counts on the n-side at 2.1 MRad. This is due to the onset of microdischarge on the n side of this ladder.

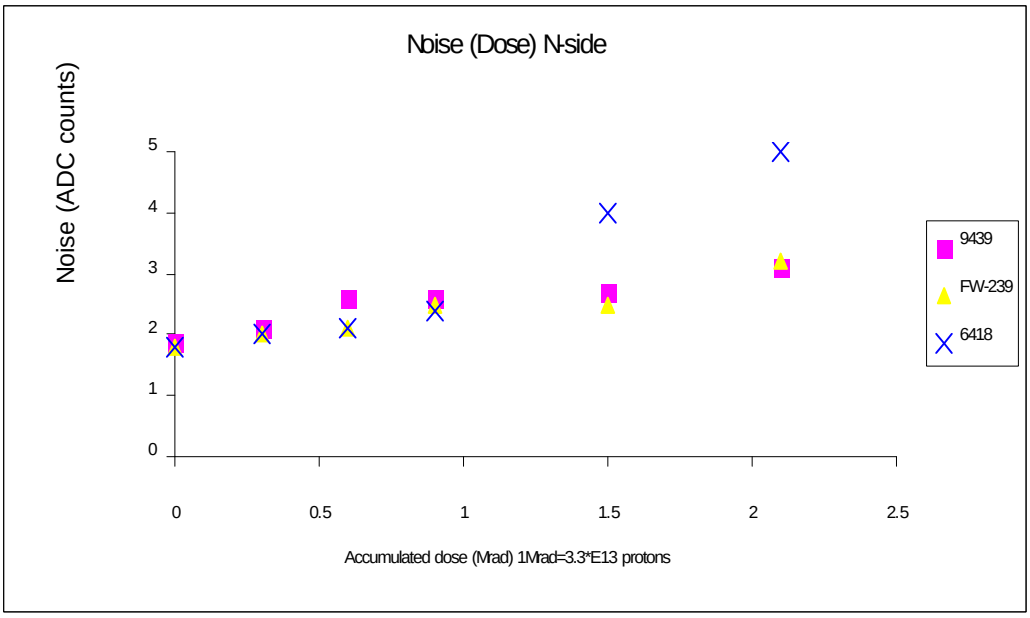

Figure 15 Noise in n-side of Run IIa ladders as a function of radiation dose.

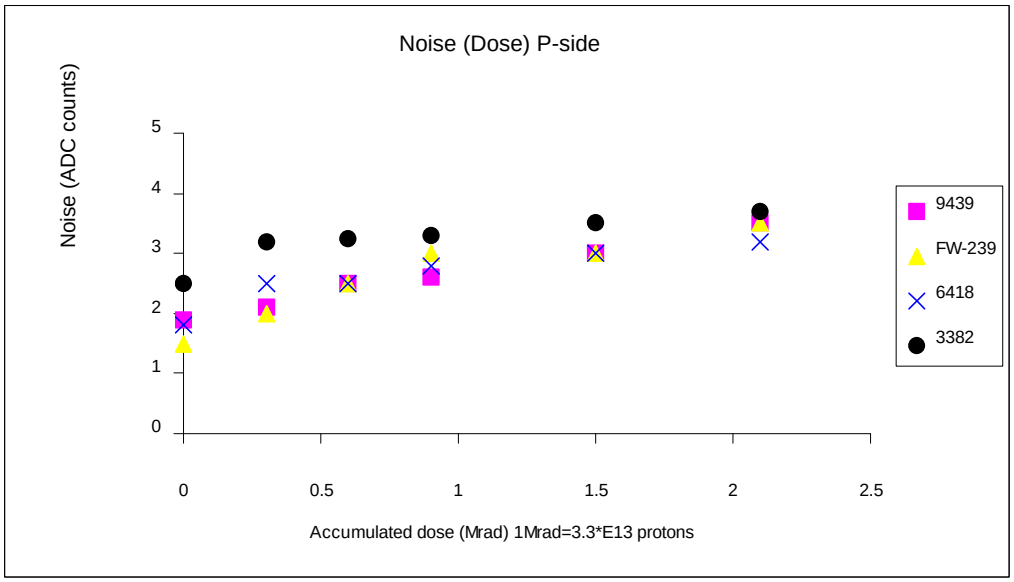

Figure 16. - Noise in p-side of Run IIa ladders as a function of radiation dose.

3.5.3 Run IIb detector irradiation studies

We have performed a set of irradiation studies on single sided detectors of the type to be used for Run IIb.[19] The detectors used were either CDF layer 00 devices (Hamamatsu, Micron, ST) or prototypes specifically for DØ (ELMA). Two Micron detectors were oxygenated, the ELMA devices were also oxygenated, but at a level too low to affect the depletion voltage. These detectors were exposed to 5, 10 and 15 MRad doses. We measured depletion voltage and leakage current after each exposure.

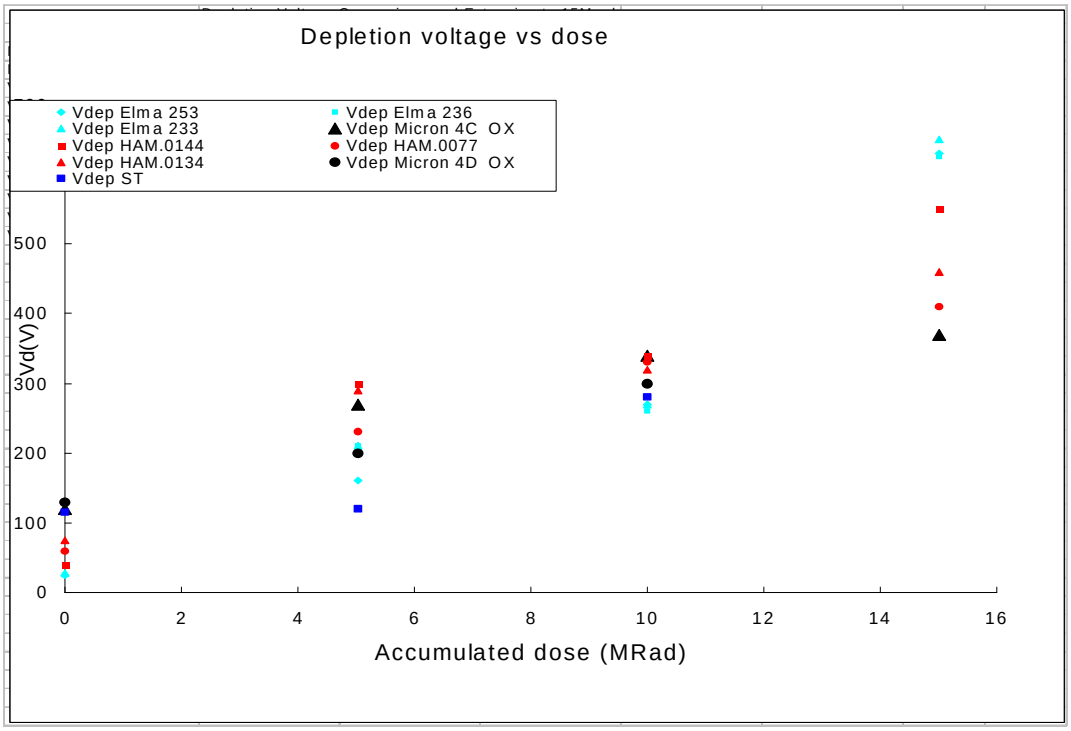

Figure 17. - Depletion voltage as a function of irradiation for Run IIb detectors.

Figure 17 shows the measured depletion voltage as a function of dose. The depletion voltage is estimated from the plateau of the detector response to a 1064 nm laser and has ~20% errors. The devices behave roughly as expected, although there is a considerable spread in the depletion voltage at 15 MRad. The ELMA detectors, which are fabricated using non-oxygenated silicon with a crystal orientation of <111>, have the worst behavior. The spread in depletion voltage is consistent with the variations among silicon types and manufacturers observed by LHC experiments.

[19] J. Gardner et al., "Studies on the Radiation Damage to Silicon Detectors for use in the DØ Run IIb Experiment", DØ Note 3958.

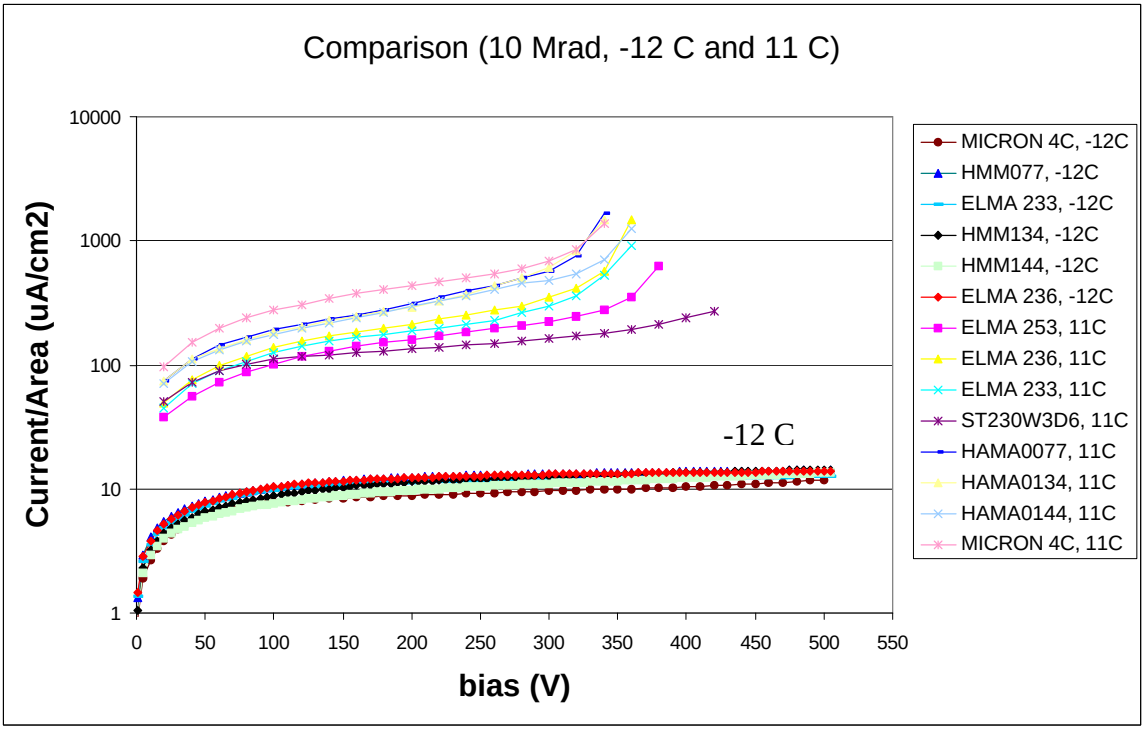

Figure 18 Leakage currents at +11 and –12 degrees C after 10 MRad

Leakage currents for all devices, presented in were found to be consistent with the usual $\alpha=3x10^{-17}$ A/cm^2 damage constant. The breakdown voltage depends on operating temperature as well as annealing time after the intense irradiation. None of the devices showed breakdown before full depletion under laser test conditions (near +10°C). Additional operating margin is available at our expected operating temperature of –10°C.

The results of these studies give us confidence that we can build a detector which can operate to 15 fb^{-1} and beyond. We plan to irradiate samples of prototype and production detectors to confirm their performance. We also expect to irradiate ladders bonded to SVX4 chips to measure ladder noise performance after irradiation.

3.6 Conclusion

The high integrated luminosity of Run IIb will necessarily result in a particularly harsh radiation environment. Reliable operation of silicon sensors in such conditions is crucial to the experiment's success. We were guided in our design and technology choice by our experience in Run IIa detector construction as well as by recent advancements in radiation hard silicon technology motivated primarily by the needs of LHC experiments. In Run IIb, DØ plans to use only single-sided single-metal silicon sensors, limiting them to only 3 types. Our estimates, supported by the results of the irradiation tests, show that these sensors will be able to withstand the radiation dose equivalent to more than 15 fb^{-1} with a significant safety margin in layers 0-5.

The depletion voltage for layer 0 sensors is expected to reach 300V for the assumed Tevatron Run IIb scenario of accumulating a luminosity of 13 fb^{-1} within 4 years. The layer 0 sensors will be specified to breakdown not earlier than 700V, providing enough flexibility in overbiasing these detectors. Warm periods of several weeks for maintenance should be carefully avoided in order to prevent reverse annealing. As an additional safety measure against the depletion voltage rise, the layer 0 sensors could be oxygenated. An oxygenation of these sensors is expected to slow down the depletion voltage growth after the type inversion. Further R&D studies are needed to confirm this approach.