Foundations of Computer Science – Exercise 3

2.

a	b	s	!s	a AND !s	b AND s	(a AND !s) OR (b AND s) = o
0	0	0	1	0	0	0
0	0	1	0	0	0	0
0	1	0	1	0	0	0
0	1	1	0	0	1	1
1	0	0	1	1	0	1
1	0	1	0	0	0	0
1	1	0	1	1	0	1
1	1	1	0	0	1	1

3. a) Buses:

- CC: 22-bit control bus, MIR guides data transfer.

- DC1, DC2: 16-bit data/address buses, providing inputs to ALU.

- DC3: 16-bit data/address bus, transferring results from ALU to the desired register.

b) Stages of the clock:

• Stage 1: contents of MDR or number 1 is written in DC1 and content of the register A, B, C or D will be written in DC2 for arithmetic processing in ALU.

• Stage 2: The result from ALU is written from DC3 to some of the registers MAR, MDR, A, B, C or D.

• Stage 3: Contents of MDR are written to address given by MAR in MM or contrariwise, contents of the MM address given by MAR will be written to MDR.

• Stage 4: New value of MPC will be calculated.

• Stage 5: MPC gets a new value (automatically no control bit!), and the microinstruction specified in MPC will be transferred to MIR register.

4.

```
        B:=0
        MAR:=A
        MDR:=(MAR)
        A:=MDR
if:     skip A = 0
```

```
      jump pass
      skip A < 0
      B:=A+1
      shiftleft(A)
      jump if
pass:
```

```
1:0+0→B; ;1+MPC →MPC
2: 0+A →MAR; (MAR) →MDR;
1+MPC →MPC
3: MDR+0 →A; ; 1+MPC →MPC
4: ; ; (A=0)+MPC →MPC
5: ; ; 1010₂→MPC
6:; ; (A<0)+MPC →MPC
7: 1+C →C; ; 1+MPC →MPC
8:(0+A)x2 →A; ; 1+MPC → MPC
9:; ; 100₂→MPC
10:
```