REV.	Description	Date
00	SPEC ISSUE (NEW MODEL) ADP-65JW Y2A	12/11'20
	102A-211065	
01	ITEM 13.Loop gain 測試	01/15'21
	Disturbance voltage setting 從 0.4V 變更為 0.3V	
	102A-212052 1. 更新 ITEM 13. Loop/Gain 測試作業規範 圖片說明。	
	2. ITEM 6.Function test (ATS) procedure: (15VDC)	
02	Test Item: Sync Dynamic(only for 15V), 增加 CPK 不計算。	02/17'21
	3. ITEM 7.Function test (ATS) procedure : (9VDC)	
	Test Item: Sync Dynamic(only for 9V), 增加 CPK 不計算。	
02	102A-213123	02/17/21
03	ADD MODEL: ADP-65JW X2A, ADP-65JW Z2A	03/17'21
04	102A-215085	05/14'21
	新增 ITEM 14.0VP 測試作業說明	00/11/21
05	102A-21B098 ITEM 14.OVP 測試作業說明 change to 14. Stress OVP 測試作業說明	11/12'21
03	更改串聯電阻 to 220 歐姆	11/12 21
06	102A-222047	02/15'21
00	新增 ITEM 3.i EMI 測試已 under 6db 做判定。	02/13/21
07	102A-235337	06/01'23
	ADD MODEL: ADP-65JW Y2C 102A-238054	
08	ITEM 9.1 Hi-POT test:	08/07'23
	"Cut off current: Hi-Limit 10mA, Lo-Limit 0.02A" change to "Cut off current: 10mA"	
09	102A-241328 ADD MODEL: ADP-65JW Y2B	02/19'24
	102A-244163	
	1. ITEM 3. 測試注意事項	
10	add j. 噪音測試熱機,以該輸出電壓熱機做熱機測試 (FOR ADP-65JW Y2B)	04/17204
10	2. ITEM 4. 手調測試站 e.OVP test: add	04/17'24
	測試 5V OVP 時,從輸出外灌 7.3V 電壓測試 OVP (FOR ADP-65JW Y2B)	
	測試 9V OVP 時, 從輸出外灌 13V 電壓測試 OVP (FOR ADP-65JW Y2B)	
11	102A-245164 ADD MODEL: ADP-65JW Y2D, ADP-65JW Z2C	05/15'24
	A 法 塚 ス エ 米 駅 少 去 間 八 ヨ DESCRIPTION .	

A NE		達電子工業股 LTA ELECTR	•	DESCRIPTION: 測試注意事項 (Test Specification	on)
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WITHOUT PE		LOR SELL OF APPARA	TUSES OR DEVICES	ADP-65JW X2X SERIE	S
Date	Drawn	Design (EE)	Design (ME)	DOCUMENT NAME. :	REV.
05/15'24	王玉玲	陳俊宇	陳俊豪/張伯毅	TS-65JW X2X SERIES	11

FRAME NAME: DF-PSLA4V-2R01.DOC

SHEET <u>1</u> OF <u>15</u>

MODEL LIST

MODEL NAME	ТҮРЕ
ADP-65JW Y2A/Y2B/ Y2C/Y2D	US
ADP-65JW X2A	CN
ADP-65JW Z2A/ Z2C	EU

1. 測試注意事項內容,未經工程師許可,不可任意變更。

Test Notice contents shall not be changed or revised without engineer permission.

2. 此測試規格用於主線測試,所有項目均需被測試,因設備或線速限制無法全數測試時, 需測試 worst case, QC 需按抽樣標準測試所有 Item 不可只測試主線測試項目.

The production line shall perform all or worst test items/conditions, and QC shall follow the sampling plan to perform all items/conditions not just the worst condition as production did.

3. 測試注意事項:

- a. 功能測試時,電子負載需設定 Von 點為 3V.
- b. 所有 ATS 測試時,須偵測 CONNECTOR 端之電壓。
- c. 在測試及崩應時,治具上各組輸出須有加系統電容。
- d. All function test 輸出並聯電容 100uF/25V。
- e. Open frame 或是 Case 未組裝前的各項測試,於測試完成後須對 BULK CAP 放電
- f. No Load 測試,輸出端不接測試治具且只測試輸出 5V 的條件
- g. 手機干擾測試以 5cm 條件測試與判定。
- h. AC on/off 負載設定為 CR mode.
- i. EMI 測試已 under 6db 做判定。
- j. 噪音測試熱機, 以該輸出電壓熱機做熱機測試 (FOR ADP-65JW Y2B)

		達電子工業股	:份有限公司	DESCRIPTION :	
A DE	LTA DE	LTA ELECTR	ONICS, INC.	測試注意事項 (Test Specificatio	n)
		CATIONS ARE THE PE L NOT BE REPRODUCE	MODEL NO. :		
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Date	Drawn	Design (EE)	Design (ME)	DOCUMENT NAME. :	REV.

FRAME NAME: DF-PSLA4V-2R01.DOC

SHEET <u>2</u> OF <u>15</u>

4. 手調測試站:(以下為範例寫法請依據產品特性自行修正)

a. VR 調整測試條件如下: N/A

b. Full Load Test:檢查滿載輸出是否符合規格

c. Min. Load Test:檢查輕載輸出是否符合規格

d. OTP Test:

Load Condition: 20V/3.25A 15V/3A 9V/3A 5V/3A

測試方法:NTC131 並聯 4.99Kohm 電阻,檢查輸出電壓是否 Latch off。

e. OVP Test:

Load Condition: 0A

短路 R134, OVP 動作模式為 Latch off.

Vout	OVP
5	7.5V
9	13.5V
15	20.25V
20	27V

測試 5V OVP 時, 從輸出外灌 7.3V 電壓測試 OVP (FOR ADP-65JW Y2B) 測試 9V OVP 時, 從輸出外灌 13V 電壓測試 OVP (FOR ADP-65JW Y2B)

f. AC On/Off:

Power supply 連續開關機 On= 5 秒, Off= 5 秒, 5 次後, 必須無損壞情形。(必加項目)

		達電子工業股	份有限公司	DESCRIPTION:	
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WITHOUT PEI				ADP-05JW AZA SEKIE	•
		Design (EE)	Design (ME)	DOCUMENT NAME.:	REV.

FRAME NAME: DF-PSLA4V-2R01.DOC

SHEET <u>3</u> OF <u>15</u>

5. Function test (ATS) procedure: (20VDC)

Input Specification Table:

INPUT VOLTAGE	MINIMUM	MAXIMUM	NOMINAL(RATED)
LOW RANGE	90 VAC	132 VAC	100 VAC
HIGH RANGE	180V AC	264V AC	240V AC

Output Specification Table:

20V/3.25A on-off transient Vo no damage

OUTPUT	MINIMUM	MAXIMUM	NOMINAL(RATED)
Voltage (Vdc)	19	21	20
Loading (Amp)	0	3.25	3.25

Test Item	Vin	Load	Spec	Remark
Hold up Time	100V/50Hz	3.25A	≥5ms	
Power saving requirement	115V/60Hz 230V/50Hz	18W 11W 5W~6.5W 3W 1.65W 1.5W 1W 0.25W	<21W <14W Eff.>80% <5W <3W <2.2W <1.6W <0.48W	
Line Regulation	90/264V 47/63Hz	3.25A	19~21V	
Line Regulation	90/264V 47/63Hz	0A	19~21V	
Ripple & Noise	90V/47Hz 264V/63Hz	20V/3.25A	≤300mVp-p	0.1uF//10uF Oscilloscope at 20MHz bandwidth.25°C
Surge Load (only for 20V)	100V/50Hz 240V/50Hz	Output 3.25A(1s) to 3.9A(1s)	Vo >18.5V	At 25℃.

A NE		達電子工業股 LTA ELECTR	•	DESCRIPTION: 測試注意事項 (Test Specification	on)
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Date	Drawn	Design (EE)	Design (ME)	DOCUMENT NAME. :	REV.
05/15'24	王玉玲	陳俊宇	陳俊豪/張伯毅	TS-65JW X2X SERIES	11

Test Item	Vin	Load	Spec	Remark
Sync Dynamic (only for 20V)	90V/47Hz 264V/63Hz	Output 0.05A to 3.25A Slew rate is 2.5A/us. Frequency is 100Hz~100KHz.	19~21V	
Short Circuit Protection	90V/47Hz 264V/63Hz	Min. Load Turn on then short	Latch	重啟方式 Plug or CC re-plug or ATE 控制板同時送入 2 組 CC 訊號可 reset PD IC
Over Current Protection	90V/47Hz 264V/63Hz	20V/ 3.25A	OCP is 3.9A~5.0A Latch	重啟方式 Plug or CC re-plug or ATE 控制板同時送入 2 組 CC 訊號可 reset PD IC
Input Current	100V /50Hz	20V/ 3.25A	Iin, max <1.5A	
Full Load Efficiency	100V/50Hz 240V /50Hz	20V/ 3.25A	>84.0%	Cold
Average Efficiency	115V/60Hz 230V/50Hz	25%, 50%, 75% & 100% Load	>85% for 20V	Cold
10% Load	115V/60Hz 230V/50Hz	20V / 0.325A	>77.85%	Cold
Full Load Efficiency	100V/50Hz 240V /50Hz	20V/ 3.25A	>86.0%	Hot
Average Efficiency	115V/60Hz 230V/50Hz	25%, 50%, 75% & 100% Load	>89.00% for 20V	Hot
10% Load	115V/60Hz 230V/50Hz	20V / 0.325A	>78.85%	Hot
Capacitive Load	100V/50Hz	20V / 3.25A		Parallel 1000uF Cap at output
Output change and discharge time	100V/50Hz 240V/50Hz	No load Full load	0~275mS	
Peak Load	100V/50Hz 240V/50Hz	Output 2.925A to 7.000A 18ms/2ms	>17.8V	
Peak Load	100V/50Hz 240V/50Hz	Output 2.844A to 7.313A 2.25ms/0.250ms	>17.8V	

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Date	Drawn	Design (EE)	Design (ME)	DOCUMENT NAME. :	REV.
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6. Function test (ATS) procedure: (15VDC)

Input Specification Table:

INPUT VOLTAGE	MINIMUM	MAXIMUM	NOMINAL(RATED)
LOW RANGE	90 VAC	132 VAC	100 VAC
HIGH RANGE	180V AC	264V AC	240V AC

Output Specification Table:

15V/3A on-off transient Vo no damage

OUTPUT	MINIMUM	MAXIMUM	NOMINAL(RATED)
Voltage (Vdc)	14.25	15.75	15
Loading (Amp)	0	3	3

Test Item	Vin	Load	Spec	Remark
Line Regulation	90/264V 47/63Hz	3A	14.25~15.75V	
Line Regulation	90/264V 47/63Hz	0A	14.25~15.75V	
Ripple & Noise	90V/47Hz 264V/63Hz	15V/3A	≤300mVp-p	0.1uF//10uF Oscilloscope at 20MHz bandwidth 25°C.
Surge Load (only for 15V)	100V/50Hz 240V/50Hz	Output 3A(1s) to 3.6A(1s).	Vo >13.7V	
Sync Dynamic (only for 15V)	90V/47Hz 264V/63Hz	Output 0.05A to 3A. Slew rate is 2.5A/us. Frequency is 100Hz~100KHz. 50% duty.	14.25~15.75V	CPK 不計算。
Short Circuit Protection	90V/47Hz 264V/63Hz	Min. Load Turn on then short	Latch	重啟方式 Plug or CC re-plug or ATE 控制板同時送入 2 組 CC 訊號可 reset PDIC

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FRAME NAME: DF-PSLA4V-2R01.DOC

SHEET <u>6</u> OF <u>15</u>

Test Item	Vin	Load	Spec	Remark
Over Current Protection	90V/47Hz 264V/63Hz	15V / 3A	OCP is 3.9~5.0A Latch	重啟方式 Plug or CC re-plug or ATE 控制板同時送入 2 組 CC 訊號可 reset PDIC
Input Current	100V /50Hz	15V / 3A	Iin, max <1.5A	
Full Load Efficiency	100V/50Hz 240V /50Hz	15V / 3A	>84.0%	Cold
Average Efficiency	115V/60Hz 230V/50Hz	25%, 50%, 75% & 100% Load	>85% for 15V	Cold
10% Load	115V/60Hz 230V/50Hz	15V / 0.3A	>77.85%	Cold
Full Load Efficiency	100V/50Hz 240V /50Hz	15V / 3A	>86.0%	Hot
Average Efficiency	115V/60Hz 230V/50Hz	25%, 50%, 75% & 100% Load	>88.85% for 15V	Hot
10% Load	115V/60Hz 230V/50Hz	15V / 0.3A	>78.85%	Hot
Capacitive Load	100V/50Hz	15V / 3A		Parallel 1000uF Cap at output
Output change and discharge time	100V/50Hz 240V/50Hz	No load Full load	0~275mS	
Peak Load	100V/50Hz 240V/50Hz	Output 2.700A to 6.000A 18ms/2ms	>13V	
Peak Load	100V/50Hz 240V/50Hz	Output 2.625A to 6.750A 2.25ms/0.250ms	>13V	

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Date	Drawn	Design (EE)	Design (ME)	DOCUMENT NAME. :	REV.
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FRAME NAME: DF-PSLA4V-2R01.DOC

SHEET <u>7</u> OF <u>15</u>

7. Function test (ATS) procedure: (9VDC)

Input Specification Table:

INPUT VOLTAGE	MINIMUM	MAXIMUM	NOMINAL(RATED)
LOW RANGE	90 VAC	132 VAC	100 VAC
HIGH RANGE	180V AC	264V AC	240V AC

Output Specification Table:

9V/3A on-off transient Vo no damage

OUTPUT	MINIMUM	MAXIMUM	NOMINAL(RATED)
Voltage (Vdc)	8.55	9.45	9
Loading (Amp)	0	3	3

Test Item	Vin	Load	Spec	Remark
Line Regulation	90/264V 47/63Hz	3A	8.55~9.45V	
Line Regulation	90/264V 47/63Hz	0A	8.55~9.45V	
Ripple & Noise	90V/47Hz 264V/63Hz	9V/3A	≤200mVp-p	0.1uF//10uF Oscilloscope at 20MHz bandwidth.25°C 不計算 CPK。
Sync Dynamic (only for 9V)	90V/47Hz 264V/63Hz	Output 0A to 1.5A, 295ms/5ms Output 1.5A to 3A, 25ms/5ms	8.55~9.45V	1A/us slew rate CPK 不計算。
Short Circuit Protection	90V/60Hz 264V/50Hz	Min. Load Turn on then short	Latch	重啟方式 Plug or CC re-plug or ATE 控制板同時送入 2 組 CC 訊號可 reset PDIC

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WITHOUT PEI	RMISSION.			ADP-05JW AZA SERIE	3
Date	Drawn	Design (EE)	Design (ME)	DOCUMENT NAME. :	REV.
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FRAME NAME: DF-PSLA4V-2R01.DOC

SHEET <u>8</u> OF <u>15</u>

Test Item	Vin	Load	Spec	Remark
Over Current Protection	90V/60Hz 264V/50Hz	9V / 3A	OCP is 3.1A~3.6A Latch	重啟方式 Plug or CC re-plug or ATE 控制板同時送入 2 組 CC 訊號可 reset PDIC
Full Load Efficiency	100V/50Hz 240V /50Hz	9V / 3A	>83%	Cold
Average Efficiency	115V/60Hz 230V/50Hz	25%, 50%, 75% & 100% Load	>85% for 9V	Cold
10% Load	115V/60Hz 230V/50Hz	9V / 0.3A	>76.3%	Cold
Full Load Efficiency	100V/50Hz 240V /50Hz	9V / 3A	>84%	Hot
Average Efficiency	115V/60Hz 230V/50Hz	25%, 50%, 75% & 100% Load	>87.3% for 9V	Hot
10% Load	115V/60Hz 230V/50Hz	9V / 0.3A	>77.29%	Hot
Capacitive Load	100V/50Hz	9V / 3A		Parallel 100uF Cap at output
Output change and discharge time	100V/50Hz 240V/50Hz	No load Full load	0~275mS	

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8. Function test (ATS) procedure: (5VDC)

Input Specification Table:

INPUT VOLTAGE	MINIMUM	MAXIMUM	NOMINAL(RATED)
LOW RANGE	90 VAC	132 VAC	100 VAC
HIGH RANGE	180V AC	264V AC	240V AC

Output Specification Table:

5V/3A on-off transient Vo no damage

OUTPUT	MINIMUM	MAXIMUM	NOMINAL(RATED)
Voltage (Vdc)	4.85	5.5	5
Loading (Amp)	0	3	3

Test Item	Vin	Load	Spec	Remark
Inrush Current	264V/50Hz;	3.0A	No damage	Cold /Hot start
Turn On Time	100V/50Hz 240V/50Hz	3.0A	≤ 3s.	
Rise Time	100V/50Hz 240V/50Hz	3.0A	<40ms	From 10 to 90% voltage, monotonic
Line Regulation	90/264V 47/63Hz	3A	4.85~5.5V	
Line Regulation	90/264V 47/63Hz	0A	4.85~5.5V	
Ripple & Noise	90V/47Hz 264V/63Hz	5V/3A	≤180mVp-p	0.1uF//10uF Oscilloscope at 20MHz bandwidth.25°C 不計算 CPK。
Sync Dynamic (only for 5V)	90V/47Hz 264V/63Hz	Output 0A to 1.5A, 295ms/5ms Output 1.5A to 3A, 25ms/5ms	4.6~5.8V	1A/us slew rate
Short Circuit Protection	90V/47Hz 264V/63Hz	Min. Load Turn on then short	Latch	重啟方式 Plug or CC re-plug or ATE 控制板同時送入 2 組 CC

				AIL 控制极问时达入 2.3	組 CC
△ 台達電子工業股份有限公司			DESCRIPTION:		
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Date	Drawn	Design (EE)	Design (ME)	DOCUMENT NAME. :	REV.
05/15'24	王玉玲	陳俊宇	陳俊豪/張伯毅	TS-65JW X2X SERIES	11

FRAME NAME: DF-PSLA4V-2R01.DOC

SHEET <u>10</u> OF <u>15</u>

Test Item	Vin	Load	Spec	Remark
				訊號可 reset PDIC
Over Current Protection	90V/47Hz 264V/63Hz	5V / 3A	OCP is 3.1A~3.6A Latch	重啟方式 Plug or CC re-plug or ATE 控制板同時送入 2 組 CC 訊號可 reset PDIC
Full Load Efficiency	100V/50Hz 240V /50Hz	5V / 3A	>77%	Cold
Average Efficiency	115V/60Hz 230V/50Hz	25%, 50%, 75% & 100% Load	>79.4% for 5V	Cold
10% Load	115V/60Hz 230V/50Hz	5V / 0.3A	>71.48%	Cold
Full Load Efficiency	100V/50Hz 240V /50Hz	5V / 3A	>78%	Hot
Average Efficiency	115V/60Hz 230V/50Hz	25%, 50%, 75% & 100% Load	>81.84% for 5V	Hot
10% Load	115V/60Hz 230V/50Hz	5V / 0.3A	>72.48%	Hot
Pin at No Load	115V/60Hz 230V/50Hz	No Load	≤0.075W	輸出端不可接到負載
Capacitive Load	100V/50Hz	5V / 3A		Parallel 100uF Cap at output

Note 1: After completes required DVT test matrix, identifies and selects the worst case condition for the Production MTR. It is not required that all test conditions be tested. Example: If worst case condition for Output Ripple is minimum input voltage and maximum dc load, then that is the test condition to be used.

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05/15'24	王玉玲	陳俊宇	陳俊豪/張伯毅	TS-65JW X2X SERIES	11

SHEET <u>11</u> OF <u>15</u>

FRAME NAME: DF-PSLA4V-2R01.DOC

9. Safety

9.1Hi-POT test:

Primary to Secondary use 3000+10% Vac. (Rise time: DC=1Sec, AC=0.1Sec)

Cut off current: 10mA

Note: Testing time for production line is 1 minute at EVT/DVT stage and 1 Second at PVT/MP stage. Following

is Arcing sense setting at each stage: EVT1: 5mA, EVT2/DVT: 8mA, PVT/MP: 10mA

9.2Insulation Resistance (IR) test:

The insulation resistance shall be not less than 30M ohms after application of 500Vdc/10mA for 1 minute.

9.3Earth Grounding test: N/A

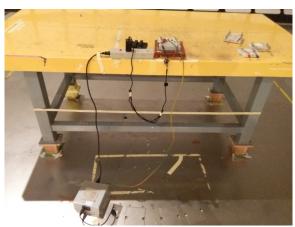
9.4Leakage current:

Leakage current no more than 20uA(max) at 240Vac/50Hz.for delta product line.

9.5EMI and RFI:

RFI Set up:

- 1. Wall mount 用插座測試, DC 線不可與 AC 線接觸
- 2. 依下圖所示使用 1m 長 AC 延長線, AC 線按法規規章自然下垂於地板
- 3. 詳細擺設如下圖示意



		A TO THE			
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CA NE	LTA DE	LTA ELECTR	ONICS, INC.	測試注意事項 (Test Specificat	ion)
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BASIS FOR THE MANUFACTURE OR SELL OF APPARATUSES OR DEVICES WITHOUT PERMISSION.			ADP-65JW X2X SERI	ES	
Date	Drawn	Design (EE)	Design (ME)	DOCUMENT NAME. :	REV.
05/15'24	王玉玲	陳俊宇	陳俊豪/張伯毅	TS-65JW X2X SERIES	11

FRAME NAME: DF-PSLA4V-2R01.DOC

SHEET <u>12</u> OF <u>15</u>

9.6Thermal Test:

Wall mount 用插座站立測試.

10. Burn-in 測試作業規範

5V 6 Hrs

9V 6 Hr

15V 6 Hr

20V 6 Hrs

11. I2C 測試作業規範: N/A

12. FRU Data Barcode Read/Write 測試作業規範: N/A

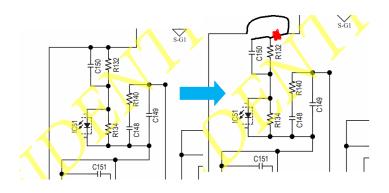
13. Loop/Gain 測試作業規範

Disturbance voltage setting 0.3V

Phase margin > 45deg.

Gain margin > 6db

R132 紅色區域斷開,串接 20ohm 再接回 Vout,如右下圖所示



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Date	Drawn	Design (EE)	Design (ME)
05/15'24	王玉玲	陳俊宇	陳俊豪/張伯毅

DESCRIPTION:

測試注意事項 (Test Specification)

MODEL NO.:

ADP-65JW X2X SERIES

DOCUMENT NAME.:

TS-65JW X2X SERIES

REV.

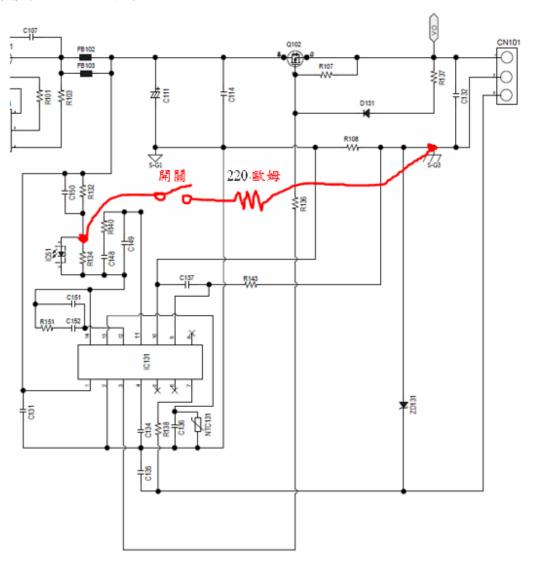
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FRAME NAME: DF-PSLA4V-2R01.DOC

SHEET <u>13</u> OF <u>15</u>

14. Stress OVP 測試作業說明

OVP 測試方式,從 photo coupler 第 1 隻腳拉出並串聯一開關與一 220 歐姆電阻,至二次測接地,並用開涮試 OVP,如下圖。



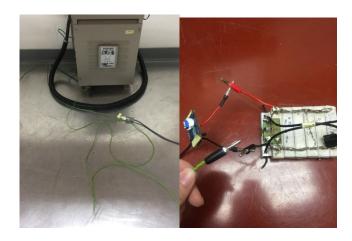


FRAME NAME: DF-PSLA4V-2R01.DOC

SHEET <u>14</u> OF <u>15</u>

15. ESD 測試作業規範

- ±15KV air discharge performance criterion B.
- ±12KV air discharge performance criterion A.
- $\pm 8 \text{KV}$ contact discharge performance criterion A.



ESD 槍每次對負載釋放能量時,負載的地(Vo-)都必須與電源系統的設備地接觸一次

16. Pin assignment

Type C conn. side	PCBA	Power co <mark>rd wir</mark> e side
VBUS A4/A9 B4/B9 o	──── ∨BUS PIN ○──	———— WHITE (18AWG)
CC 1 A5 ○	○ CC PIN ⊙	BLUE (24AWG)
D+ A6 SHORT		
D- A7 SHOKI		
GND A1/A12 B1/B12 0		———— BLACK (18AWG)
SHELL —		



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SHEET <u>15</u> OF <u>15</u>