REV.	Description					Date	e
00	SPEC ISSU		ODEL)			12/10'	'21
	ADP-65VE	BA					
01	2. Item 4.c. OV 3. ITEM 5. Dy 4. Add ITEM 6 5. ITEM 5. OV 6. ITEM 5. add 7. ITEM 5. u	P test update namic Load s 4.4 Surface te ershoot updat I line cycle di update Hold c Load/Over	pec update, 5V=4.5V imperature. te. ropout. up time/Line Regu Current Protection/In	/~6V.	nbine Regulation/Overshoot/Ripple & ge Efficiency; Load condition.	01/28*	'22
02	102A-221179 1. Item.3-g:Add photo. 2. Item.3-i:Revise 系統電容 1000uF. 3. Add Item.3-k: Add 專用 DC cable 型號: 4. Item.3-a:Revise AC turn on 時輸出電流設定. 5. Item.5 Revise Line Regulation 5V=4.5~5.25V 6. Item.5 Revise Load/Combine Regulation 5v=4.5~5.25V 7. Item.5 Revise Dynamic Load 5V=4.25V~6V. 8. Item.5 Revise Peak Load1~3 5V=3.5V~6V. 9. Item.5 AC Line cycle dropout 5V=4.5~5.25V. 10. Item.5 overshoot 5V=5.6v for 產線測試.					02/17'	'22
03	102A-222167 1. Item 4.c OVP 5V spec revise to 8V;ovp test setup revise to "7.4V". 2. Item 5. Test item: Peak load 1-3, 5V standard revise to "3V~6V". 3. Item 5. Test item: OCP standard revise to "full load+0.1A~8A".				03/04'	'22	
04	102A-22500 Section5 item		d1"/"peak load2 <mark>"</mark> /	("peak load3" re	move 5V peak load required.	05/06'	'22
05	102A-226003 1. Revise item 3.g AC cable 使用 1.8m,不加阻抗匹配.接地線靠近 LOAD 處需加 core				06/09'	'22	
06	102A-226151 ITEM 5. Average efficiency add Remark"Vo 須由 adapter 端取樣" ADD ITEM 3.1 Acoustic noise 須使用市電做測試並於輸出加掛 1000uF 系統電容.				06/24'	'22	
		台達智	電子工業股份	有限公司	DESCRIPTION:		
	NELTA	DELT	A ELECTRO	NICS, INC.	測試規格(Test Specificat	tion)	
ELEC BASI	THESE DRAWINGS AND SPECIFICATIONS ARE THE PROPERTY OF DELTA ELECTRONICS, INC. AND SHALL NOT BE REPRODUCED OR USED AS THE			` -	•		
Dat	te [)rawn	Design (EE)	Design (ME)	DOCUMENT NAME. :	I	REV.
03/20)'24 │ ∃	玉玲	陳新淵	陳威堯	TS-65VE B SERIE	S	14

REV.	Description	Date
07	102A-228072 UPDATE ITEM 3.i 測試 ATS/PLD/ESD/EFT 時,治具板須掛 1000uF/25V 之系統電容.	08/10'22
08	102A-229023 1. Section5. "Pin at standby Load" Remark revise:"1. Only for 20V;2. 0.25W cpk 不判定." 2. Section3.g revise to :"接地線靠近插座處需加 core 並纏繞 3ts". 3. Seciton3.l "acoustic noise test" add below description:"另測試冷機時須測試 0%,10%,20%,50%,100%load 之噪音,熱機時只需測試 50%,100%load 之噪音." 4. Add Section3.m "低溫測試只需滿足客戶規格 0 degC,不需加嚴." 5. Add Section3.n "因客戶的 5V/9V 系統不支援有線網路卡,故 5V/9V 輸出時不需測試 ISN."	09/06'22
09	102A-229194 ADD MODEL: ADP-65VE BA9 102A-229212 ADD MODEL: ADP-65VE BA77	10/03'22
10	102A-22B191 ADD ITEM 9. 瓦數分配	11/30'22
11	102A-22C156 ADD MODEL: ADP-65VE BB	12/30'22
12	102A-236241 6.1 HI-POT test: 6.1.1 Lo-Limit change from 0.02A to 0.02mA.	07/01'23
13	102A-237224 ITEM 3. 測試注意事項 l. "Acoustic noise 須使用市電做測試並於輸出加掛 1000uF 系統電容" change to "Acoustic noise 須使用自耦變壓器做測試並於輸出加掛 1000uF 系統電容"	07/20°23
14	102A-242111 ADD MODEL: ADP-65VE BC	03/20'24

	台達智	電子工業股份	有限公司	DESCRIPTION:	
A VEI	TA DELT	A ELECTRO	NICS, INC.	測試規格(Test Specification)	
	VINGS AND SPECIFICA CS, INC. AND SHALL N		MODEL NO.:		
	HÉ MANUFACTURE O		ADP-65VE B SERIES	S	
Date	Drawn	Design (EE)	Design (ME)	DOCUMENT NAME. :	REV.
03/20'24	干干玲	陳新淵	陳威堯	TS-65VE B SERIES	14

MODEL LIST: ADP-65VE BA/BA9/BA77/BB/BC

1 測試注意事項內容,未經工程師許可,不可任意變更。

Test Notice contents shall not be changed or revised without engineer permission.

2 此測試規格用於主線測試,所有項目均需被測試,因設備或線速限制無法全數測試時, 需測試 worst case, QC 需按抽樣標準做抽樣測試.

The production line shall perform all or worst test items/conditions, and QC shall follow the sampling plan to perform the sampling test.

3 測試注意事項:

- 功能測試時,電子負載需設定 3V Von 點.AC turn on 時輸出電流設定需<=0.5A a.
- Common Mode Noise 測試只需滿足客戶規格。 b.

The common mode noise when measure in accordance with IEC 62684 shall not exceed follow below requirement (Test condition following with Full load (per step) by each 10% load)

- o AC Input Voltage: 90Vac/60Hz & 264Vac/50Hz.
- The peak-to-peak voltage measured in the frequency range of 10KHz to 400KHz shall not exceed 150mV peak-to-peak.
- C. Loop gain

測試規格:Gain<-10db,Phase 大於 45deg,Bandwidth>1kHz。 測試時輸出端須加掛 1000uf 系統電容



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Design (EE) Design (ME) Date Drawn 03/20'24 陳新淵 王玉玲 陳威堯

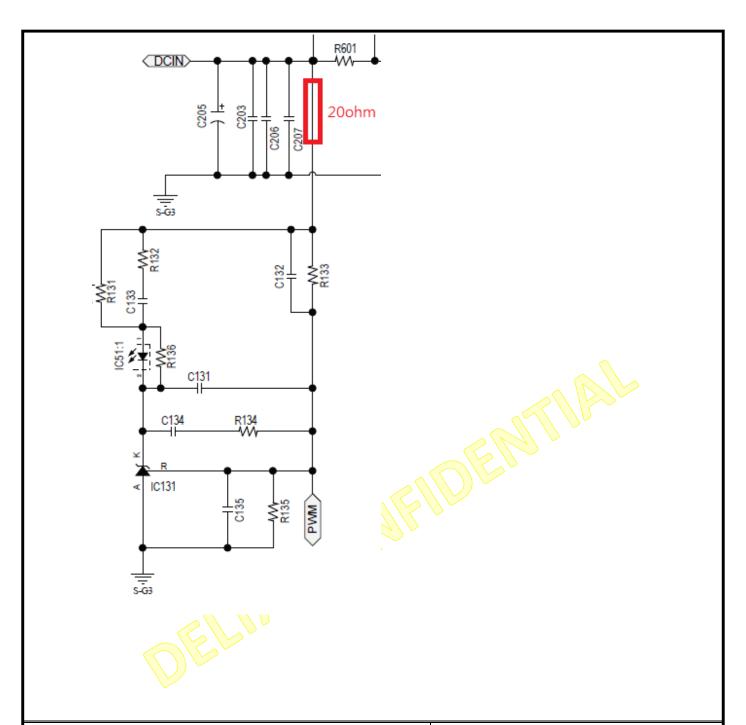
DESCRIPTION:

測試規格(Test Specification)

MODEL NO.:

ADP-65VE B SERIES

DOCUMENT NAME.: TS-65VE B SERIES





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DESCRIPTION:

測試規格(Test Specification)

MODEL NO.:

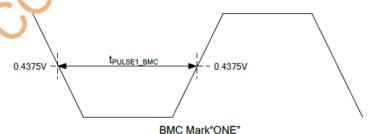
ADP-65VE B SERIES

DOCUMENT NAME.:

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- d. No Load 測試,輸出端不接測試治具.
- e. AC ON-OFF 測試時, 5V 設定 Von=3V, 9V/12V/15V/20V 設定 Von=6V.
- f. CC pin pulse width 測試:此 tpulse1_bmc於 0.4375V level 時需符合 1.4uS ~ 1.8uS 範圍內。

*(1) Pulse width of transmitted BMC "ONE" signal



g. RFI 與 EMI 測試架設擺放方式如下,熱機需用 110Vac 20V3.25A,Burn-in 20min 後測試。 AC cable 使用 1.8m,不加阻抗匹配.接地線靠近插座處需加 core 並纏繞 3ts,core 型號 C0900B-1





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- **h.** 表面溫度測試條件,電木貼鐵架,輸入電壓 100V/60Hz,輸出負載 Thermal Load,溫度線須使用 #30 號線、溫度須滿足 Δ 50 度。
- i. 測試 ATS/PLD/ESD/EFT 時,治具板須掛 1000uF/25V 之系統電容.
- j. 測試 PLD/EFT 時 dummy load 需接地。
- k. 所以測試均須使用 1m DC cable(Vender:JVE, Vender P/N: 1U-01108WA, 品名: USB-C 3.0 GEN1 male-male Cable)
- I. Acoustic noise 須使用自耦變壓器做測試並於輸出加掛 1000uF 系統電容 另測試冷機時須測試 0%,10%,20%,50%,100%load 之噪音,熱機時只需測試 50%,100%load 之噪音.
- m. 低溫測試只需滿足客戶規格 0 degC,不需加嚴.
- n. 因客戶的 5V/9V 系統不支援有線網路卡,故 5V/9V 輸出時不需測試 ISN.

4. 手調測試站:

- a. Full Load Test:檢查滿載輸出是否符合規格。b. Min Load Test:檢查輕載輸出是否符合規格。
- c. OVP Test:(量產後不需測試)

測試方法: 由輸出外灌 OVP test setup 電壓(如下表)給 Adapter, Adapter 需保護, OVP 動作模式 為 Latch off。如測試條件為兩組輸出時,任一組過電壓後兩組輸出必須同時保護.

NOMINAL OUTPUT	OVER VOLTAGE(spec)	OVP test setup
VOLTAGE (V)	MAXIMUM	Voltage(V)
5V	8V	7.4V
9V	13.05V	11.48V
12V	15.80V	15.14V
15V	21.75V	19.7V
20V	29.00V	25V

d. OTP Test:

測試方法:NTC701 並聯 6K ohm 電阻,檢查輸出電壓是否 Latch off。

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e. AC On/Off:

Power supply 連續開關機 On= 5 秒; Off= 5 秒各 5 次後, 必須無損壞情形。

f. 抽載測試輸出: Connector 需掛 10uF & 1uF 的輸出電容做為測試。





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MODEL NO.:

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DOCUMENT NAME.: **TS-65VE B SERIES**

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5. Function test (ATS) procedure:

Input Specification Table:

Input Voltage	Minimum	Maximum	Nominal(Rated)
90Vac~265Vac	90Vac	265Vac	120Vac

Output Specification Table:

P1 / P2	0V	(0)	5V	(1)	9V	(2)	12V	/(3)	15V	7(4)	20V	7(5)
0 / 0		0 /	65	0 / 65		0 / 65		0 / 65		0 / 65		
0V(0)			X	5V/3A	X	9V/3A	X	12V/5A	X	15V/4.33 A	X	20V/3.25 A
	65	/ 0	30 /	30	30 /	/ 30	30	/ 30	20 /	45	20	45
5V(1)	5V/3A	X	5V/3A	5V/3A	5V/3A	9V/3A	5V/3A	12V/2.5A	5V/3A	15V/3A	5V/3A	20V/2.25 A
	65	/ 0	30 /	30	30 /	30	30	/ 30	20 /	45	20	45
9V(2)	9V/3A	X	9V/3A	5V/3A	9V/3A	9V/3A	9V/3A	12V/2.5A	9V/2.22A	15V/3A	9V/2.22A	20V/2.25 A
	65	/ 0	30 /	30	30 /	30	30	/ 30	20 /	45	20	45
12V(3)	12V/5A	X	12V/2.5A	5V/3A	12V/2.5A	9V/3A	12V/2.5A	12V/2.5A	12V/1.66 A	15V/3A	12V/1.66 A	20V/2.25 A
	65	/ 0	45 /	20	45 /	20	45 /	/ 20	30 /	30	30 /	30
15V(4)	15V/4.33 A	X	15V/3A	5V/3A	15V/3A	9V/2.22A	15V/3A	12V/1.66 A	15V/2A	15V/2A	15V/2A	20V/1.5A
	65	/ 0	45 /	20	45 /	/ 20	45 /	/ 20	30 /	30	30 /	′ 30
20V(5)	20V/3.25 A	X	20V/2.25 A	5V/3A	20V/2.25 A	9V/2.22A	20V/2.25 A	12V/1.66 A	20V/1.5A	15V/2A	20V/1.5A	20V/1.5A

Test Plan:

icst i iaii.		
	P1	P2
1	х	20V/3.25A
2	х	15V/ <mark>4.33A</mark>
3	9V/2.22A	20V/2.25A
4	15V/2A	<mark>15V/</mark> 2A
5	12V/1.66A	15V/3A
6	5V/3A	5V/3A

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Test Item	Vin	Load	Spec	Remark
Inrush Current	265V/63Hz; Phase 90°	No load	shall be limited to a 29% margin of the I ² T rating of the input fuse and bridge rectifier.	
Turn On Time	90V/47Hz	5V/3A	< 5Sec	Only output 5V Only test C2 port
Hold up Time	115V/60Hz	NA+20V/3.25A NA+15V/4.33A 9V/2.22A+20V/2.25A 15V/2A+15V/2A 12V/1.66A+15V/3A 5V/3A+5V/3A	>5mSec	
Rise Time	90V/47Hz& 265V/63Hz	0V to 5V 5V to 9V 5V to 12V 5V to 15V 5V to 20V	< 275mSes	Max Load Only test C2 port
Fall Time	90V/47Hz& 265V/63Hz	5V/3A	N/A	Only output 5V
Line Regulation	90/115/230/265V 47/60/50/63Hz	NA+20V/3.25A NA+15V/4.33A 9V/2.22A+20V/2.25A 15V/2A+15V/2A 12V/1.66A+15V/3A 5V/3A+5V/3A	19V ~ 21V(20V) 14.25V ~ 15.75V(15V) 11.4V ~ 12.6V(12V) 8.55V ~ 9.45V(9V) 4.5V ~ 5.25V(5V)	
Load/Combine Regulation	90/115/230/265V 47/60/50/63Hz	NA+20V/3.25A NA+15V/4.33A 9V/2.22A+20V/2.25A 15V/2A+15V/2A 12V/1.66A+15V/3A 5V/3A+5V/3A	19V ~ 21V(20V) 14.25V ~ 15.75V(15V) 11.4V ~ 12.6V(12V) 8.55V ~ 9.45V(9V) 4.5V ~ 5.25V(5V)	
Overshoot	90/115/230/265V 47/60/50/63Hz	NA+20V/3.25A NA+15V/4.33A 9V/2.22A+20V/2.25A 15V/2A+15V/2A 12V/1.66A+15V/3A 5V/3A+5V/3A	21 volts peak(20V) 15.75 volts peak(15V) 12.60 volts peak(12V) 9.45 volts peak(9V) 5.25 volts peak(5V)	During power-on or power-off, the output voltage shall be monotonically increasing or decreasing with respect to the overshoot which shall neither each output volts peak nor be outside the regulation requirements for more than 10ms.
			5.6 volts peak(5V)	For 產線測試用

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DOCUMENT NAME.: TS-65VE B SERIES

		NA+20V/3.25A		
'	'	NA+15V/4.33A	1	1uF/10uF/100uF(PD
Diania 9 Maiga	400)//501/17	9V/2.22A+20V/2.25A		guideline)
Ripple & Noise	100V/50Hz	15V/2A+15V/2A	< 380mvp-p	Oscilloscope at 10KHZ to
'	'	12V/1.66A+15V/3A	'	20MHz bandwidth
'	'	5V/3A+5V/3A	'	
,		NA+20V/3.25A	,	
•		NA+15V/4.33A	1	
ļ		9V/2.22A+20V/2.25A	1	
ļ	•	15V/2A+15V/2A	18.0V~22.0V(20V)	slew rate is 1A/us,
ļ	00//4711- 0	12V/1.66A+15V/3A	` ,	Setting Time is 1Hz&5KHz
II IVnamic i nad	90V/47Hz &	5V/3A+5V/3A	10.8V ~ 13.2V(12V)	Duty Cycle 50%.
-',	265V/63Hz			system capacitance
!	'		4.25V ~ 6V(5V)	1000uF/50V
·		0.1A~50%LOAD	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	
·		50%~100%LOAD	1	
<u>'</u>		0.1A~90%LOAD	'	
,		0A & 5V/3A	,	
'		9V/3A	'	
Short Circuit	90V/47Hz &	12V/5A	Latch off After 3sec	
Protection	265V/63Hz	15V/4.33A		
'		20V/3.25A	'	
		Turn on then short		
,		NA+20V/3.25A		
<u>'</u>		NA+15V/4.33A		
Protection	265Vac/60Hz		off)	Remark:不須計算 CPK
<u>'</u>	'	12V/1.66A+15V/3A		
		5V/3A+5V/3A		
'		NA+20V/3.25A		
'		NA+15V/4.33A		
Input Current	90V/47Hz	9V/2.22A+20V/2.25A	< 1.6A	
Imput Garrent	00 1/7/11/2	15V/2A+15 <mark>V/2A</mark>	1.0/	
<u>'</u>	'	12V/1.66A+15V/3A	'	
		5V/3A+5V/3A	<u> </u>	
•			>89%	Cold/Hot
•			- 00 /0	
IAVARAGE ETTICIENCV I			0070	Remark:不須計算 CPK
,	230V/50Hz			Remark:Vo 須由 adapter
•			>86%	端取樣
		5V/3A+5V/3A	>81.7%	<u> </u>
	11 <mark>5</mark> V/60Hz&	No Load	< 100mW	Only output 5V
	230V/50HZ			
			0.5W	1. Only for 20V;
Pili at Standby Load	230V/50Hz	0.5W	1.0W	2. 0.25W cpk 不判定.
	230V/50Hz	0.5W		

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		1.0W 1.5W	1.7W 2.4W	
Peak Load 1	100V/50Hz	1mS, 5%Duty cycle	17.0V~22.0V(20V) 12.5V~16.5V(15V) 9.8V ~ 13.2V(12V) 7.1V ~ 9.9V(9V)	For cable END measurement. (low current equals 95% loc for 19ms) Remark:不須計算 CPK
Peak Load 2	100V/50Hz	2mS, 10%Duty cycle	17.0V~22.0V(20V) 12.5V~16.5V(15V) 9.8V ~ 13.2V(12V) 7.1V ~ 9.9V(9V)	For cable END measurement. (low current equals 92% loc for 18ms) Remark:不須計算 CPK
Peak Load 3	100V/50Hz	150% Load loc for 10mS, 50%Duty cycle	17.0V~22.0V(20V) 12.5V~16.5V(15V) 9.8V ~ 13.2V(12V) 7.1V ~ 9.9V(9V)	For cable END measurement. (low current equals 50% loc for 10ms) Remark:不須計算 CPK
AC Line cycle dropout	115V/60Hz		19V ~ 21V(20V) 14.25V ~ 15.75V(15V) 11.4V ~ 12.6V(12V) 8.55V ~ 9.45V(9V) 4.5V ~ 5.25V(5V)	

Note 1: After completes required DVT test matrix, identifies and selects the worst case condition for the Production MTR. It is not required that all test conditions be tested. Example: If worst case condition for Output Ripple is minimum input voltage and maximum dc load, then that is the test condition to be used.

6. Safety

6.1 Hi-POT test:

6.1.1 Primary to Secondary use 3000+10% Vac. (Rise time: DC=1Sec, AC=0.1Sec) Cut off current: Hi-Limit 10mA, Lo-Limit 0.02mA.

Note: Testing time for production line is 1 minute at EVT/DVT stage and 1 Second at PVT/MP stage. Following is Arcing sense setting at each stage: EVT1: 8mA, EVT2/DVT: 10mA, PVT/MP: 12mA

6.2 Insulation Resistance (IR)test:

Primary to Secondary use 500Vdc test, Insulation resistance limit >100Mohm

6.3 Leakage Current test :

250Vac/50Hz <= 40uA ∘

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6.4 Surface temperature :

測試條件:100Vac/50Hz Amb=35C,表面溫升需<= 50degC。

7. Burn-in 測試作業規範

- 7-1. Ambient is 35° C, Vin = 220Vac, 80% rated load \circ
- 7-2. Burn-in 時間定義
 - 7-2-1. P/R 階段 B/I 時間 24 hours,每 2 hours 循環一次,輸出電壓與 B/I 時間分配如下:
 - (1).輸出電壓 5V, B/I 時間 0.125 hours。
 - (2).輸出電壓 9V, B/I 時間 0.125 hours。
 - (3).輸出電壓 12V, B/I 時間 0.125 hours。
 - (4).輸出電壓 15V, B/I 時間 0.125 hours。
 - (5).輸出電壓 20V, B/I 時間 1.5 hours。

7-2-2. MP 階段 B/I 時間根據產品的品質穩定性調整 B/I 時間。



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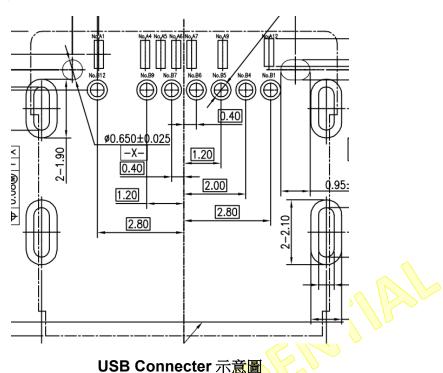
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8. USB Connecter Pin 定義與相關測試

8-1. Pin 定義與描述:



USB Type-C Pin Assignments

No.	Pin Number	Signal Name
1	A1	GND
2	A4	Vaus
3	A5	CC1
4	A6	Dp1
5	A7	Dn1
6	A9	VBUS
7	A12	GND

No.	Pin Number	Signal Name
8	B12	GND
9	B9	VBUS
10	B7	Dn2
11	B6	Dp2
12	B5	CC2
13	B4	VBUS
14	B1	GND

USB Connecter Pin 說明.



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8-2 :相關測試:

(1). 各 PIN 短路開路定義

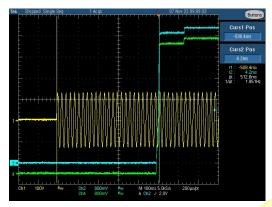
GND Pin: A1, B1, A12, B12 需短路。VBUS Pin: A4, B4, A9, B9 需短路。

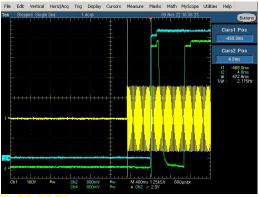
CC Pin: A5, B5。其餘未定義的各 Pin 開路。

9. 瓦數分配

因兩組電壓同時輸出時,在以下條件時需瓦數分配(設計為 error recovery).

1. 開機時, 兩 port type C 同時接著. (第一組會由單 port 65W, 重新定義為 20W or 45W) 因開機 CPU 有機率沒讀到第一組 port 宣告"單 port 65W", 故有可能不重啟 以下為開機時波形





- 2. 開機後, 兩 port type C 分別插入. (第一組會由單 port 65W, 重新定義為 30W)
- 3. 開機後, 兩 port type C 拔除任 紅輸出 (剩餘 port 重新定義為 65W)
- 4. 開機後, 兩 port type C 任一組輸出切電壓.(5V/9V 為 20W, 12V/15V/20V 為 45W)



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