REV.	Description	Date
00	102A-239264   增加 ADP-200JB KA,ADP-200JB KB 與 ADP-200JB HA,HB,HA88,HD,HC 合併發行	10/02'23
01	102A-23A168 FOR ADP-200JB KA/KB Update 12. Loop/Gain 測試作業規範	10/27°23
02	102A-23B281 Update 13.EMI/RFI Setup	11/30°23
03	102A-23C159 Update 7.Function test (ATS) procedure/ Pin at standby Load	12/18'23
04	102A-242146 Update 6.d OVP test	03/06'24
05	102A-243304 FOR ADP-200JB KA/KB ADD 14.DC Plug OTP	03/29'24
06	102A-245210 ADD model ADP-200JB KA-2,ADP-200JB KA-3 102A-245211 ADP-200JB KA1W	05/22'24

台達電子工業股份有限公司 DELTA ELECTRONICS, INC.				DESCRIPTION : 測試規格( <b>Test Specificat</b>	tion)
THESE DRAWINGS AND SPECIFICATIONS ARE THE PROPERTY OF DELTA ELECTRONICS, INC. AND SHALL NOT BE REPRODUCED OR USED AS THE BASIS FOR THE MANUFACTURE OR SELL OF APPARATUSES OR DE VICES WITHOUT PERMISSION.				MODEL NO. : ADP-200JB SERIES	
Date	Drawn	Design (EE)	Design (ME)	DOCUMENT NAME. :	REV.
05/22'24	邱美淳	顏偉任/孔維良	廖明運/陳俊豪 /張伯毅	TS-200JB SERIES	06

Frame Name: DF-PSLA4V-2R01.DOC SHEET 1 OF 11

#### **MODEL LIST**

ADP-200JB HA	ADP-200JB HB	ADP-200JB HA88	ADP-200JB HD	ADP-200JB HC
ADP-200JB KA	ADP-200JB KB	ADP-200JK KA-2	ADP-200JK KA-3	ADP-200JK KA1W

1 測試注意事項內容,未經工程師許可,不可任意變更。

Test Notice contents shall not be changed or revised without engineer permission.

2 此測試規格用於主線測試,所有項目均需被測試,因設備或線速限制無法全數測試時, 需測試 worst case, QC 需按抽樣標準做抽樣測試.

The production line shall perform all or worst test items/conditions, and QC shall follow the sampling plan to perform the sampling test.

#### 3 測試注意事項:

- a. 所有 ATS 測試時,須偵測 CONNECTOR 端之電壓。
- b. Thermal 測試環境:用電木測試
- c. Acoustic noise 測試時須使用 AC source 6530
- d. Acoustic noise 測試高壓時用 254VAC
- e. Power Saving 皆須使用積分 5 分鐘的方式測試
- f. Hi-Pot 測試時 AC cable 須使用兩芯線
- g. 所有測試外掛系統電容(2000uF 日系電容)需直接加在治具端上,不可使用電容盒聯接
- h. 測試 PLD 時,需先滿載 B\I 十分鐘後在測試,電阻負載須接地。
- i. AC on/off 測試必須設 Von 點為 15V
- j. EMI/RFI margin 6dB(以母機種 ADP-200JB BA 能力值判定)



台達電子工業股份有限公司 NELTA DELTA ELECTRONICS, INC.				DESCRIPTION : 測試規格(Test Specificat	tion)
THESE DRAWINGS AND SPECIFICATIONS ARE THE PROPERTY OF DELTA ELECTRONICS, INC. AND SHALL NOT BE REPRODUCED OR USED AS THE BASIS FOR THE MANUFACTURE OR SELL OF APPARATUSES OR DE VICES WITHOUT PERMISSION.				MODEL NO. : ADP-200JB SERIES	
Date	Drawn	Design (EE)	Design (ME)	DOCUMENT NAME. :	REV.
05/22'24	邱美淳	顏偉任/孔維良	廖明運/陳俊豪 /張伯毅	TS-200JB SERIES	06

Frame Name: DF-PSLA4V-2R01.DOC

SHEET <u>2</u> OF <u>11</u>

#### 4 燒錄 IC:

無

5 小板(小板名稱)動態測試:

無

#### 6 手調測試站:

a. Full Load Test: 檢查滿載輸出是否符合規格 b. Min. Load Test: 檢查輕載載輸出是否符合規格

c. OTP Test:

Load Condition: 10A

ADP-200JB HA\HB\HC\HD\HA88

敘述測試方法: NTC31 並聯 2KF,檢查輸出電壓是否 shutdown and Latch off.

ADP-200JB KA\KB

敘述測試方法: NTC31 並聯 2KF,檢查輸出電壓是否 shutdown and Latch off.

#### d. OVP Test:

Load Condition: 0A or 10A

ADP-200JB HA\HB\HC\HD\HA88

敘述測試方法,例如: 持續短路 R134 大於 5sec,檢查輸出電壓是否小於 27V, OVP 動作模式

為 Latch off.

ADP-200JB KA\KB

敘述測試方法,例如: turn on 後輸出外加 22V 的 DC 電壓,檢查輸出電壓是否小於 27V, OVP

動作模式為 Latch off.

#### e. AC On/Off:

Power supply 連續開關機 On=3 秒, Off=3 秒, 5 次後, 必須無損壞情形。

台達電子工業股份有限公司 NELT4 DELTA ELECTRONICS, INC.				DESCRIPTION: 測試規格(Test Specificat	tion)
ELECTRONICS, I	NC. AND SHALL NOT MANUFACTURE OR S	ONS ARE THE PROPI TBE REPRODUCED O SELL OF APPARATUS	MODEL NO.: ADP-200JB SERIES		
Date	Drawn	Design (EE)	Design (ME)	DOCUMENT NAME. :	REV.
05/22'24	邱美淳	顏偉任/孔維良	廖明運/陳俊豪 /張伯毅	TS-200JB SERIES	06

Frame Name: DF-PSLA4V-2R01.DOC SHEET 3 OF 11

# 7 Function test (ATS) procedure:

# **Input Specification Table:**

INPUT VOLTAGE	MINIMUM	MAXIMUM	NOMINAL(RATED)
LOW RANGE	90 VAC	132 VAC	100 VAC
HIGH RANGE	180V AC	264V AC	240 VAC

# **Output Specification Table:**

OUTPUT	MINIMUM	MAXIMUM	NOMINAL(RATED)
Voltage (Vdc)	19	21	20
Loading (Amp)	0A	10A	0~10A

Test Item	Vin	Load	Spec	Remark
Inrush Current	264V/63Hz; Phase 90°	10A	No damage	
Turn On Time	100V/50Hz 240V/50Hz	10A	<3Sec	該項 CPK 以 Bench 為
Hold up Time	100V/50Hz	10A	>16mS	
Rise Time	90V/47Hz 264V/63Hz	10A	<40mSec	
Overshoot	90V/47Hz 264V/63Hz	0A, 10A	<21V	
Line Regulation	90/115/230/264V 47/63Hz	0A, 10A	19~21V	
Load/Combine Regulation	120V/60Hz	0A, 10A	19~21V	
Capacitor Load	90V/47Hz 264V/63Hz	10A	Shall not cause the adapter to shut down	2000uF
Ripple & Noise	90V/47Hz 264V/63Hz	0A, 10A	<350mVp-p	0.1uF//10uF BW : 20MHz
Sync Dynamic	90V/47Hz 264V/63Hz	0.05A~100%Load	18.8~21.2V	S/R: 2.5A/uS, 100Hz~100 KHz
Peak Load	100V/50Hz 240V/50Hz	a) 9A~20A b) 8.75A~22.5A	>18.3V	a) L(18ms),H(2ms) b) L(13.5ms),H(1ms)
				S/R: 2.5A/uS,
Surge Load	100V/50Hz 240V/50Hz	10A(1s) to 12A(1s)	>18.5V	S/R: 2.5A/uS,

台達電子工業股份有限公司 DELTA ELECTRONICS, INC.				DESCRIPTION : 測試規格( <b>Test Specificat</b>	tion)
THESE DRAWINGS AND SPECIFICATIONS ARE THE PROPERTY OF DELTA ELECTRONICS, INC. AND SHALL NOT BE REPRODUCED OR USED AS THE BASIS FOR THE MANUFACTURE OR SELL OF APPARATUSES OR DE'VICES WITHOUT PERMISSION.				MODEL NO. : ADP-200JB SERIES	
Date	Drawn	Design (EE)	Design (ME)	DOCUMENT NAME. :	REV.
05/22'24	邱美淳	顏偉任/孔維良	廖明運/陳俊豪 /張伯毅	TS-200JB SERIES	06

Frame Name: DF-PSLA4V-2R01.DOC SHEET 4 OF 11

Short Circuit Protection	90V/47Hz 264V/63Hz	10A		latch
Over Current Protection	90/115/230/264Vac	10A-16A	12~16A Debounce time 400ms	latch
Input Current	100V/50Hz	10A	<2.5A	
Harmonic Current Power Factor	230V/50Hz	Pin = 75W 100% Load	EN-61000-3-2	
Power factor	100V/50Hz 240V/50Hz	100% Load	PF >0.9	
10% Load Efficiency	115V/60Hz 230V/50Hz	10% Load	76% 79%	Cold Hot
Average Efficiency	230V/50Hz	100% Load	>86%	Cold
Average Efficiency	115V/60Hz 230V/50Hz	25%, 50%, 75% & 100% Load	>89%	Hot
Pin at No Load	115V/60Hz 230V/50Hz	No Load	<0.15W	輸出端不可接到負載 請以積分測試,該項 CPK以Bench為準
Pin at standby Load	115V/60Hz 230V/50Hz	_		請以積分測試,該項 CPK 以 Bench 為準 不考慮 CPK

Note 1: After completes required DVT test matrix, identifies and selects the worst case condition for the Production MTR. It is not required that all test conditions be tested. Example: If worst case condition for Output Ripple is minimum input voltage and maximum dc load, then that is the test condition to be used.

		電子工業股份	DESCRIPTION:		
CA VE	DELT DELT	A ELECTRO	測試規格(Test Specificat	tion)	
ELECTRONICS, I	NC. AND SHALL NOT MANUFACTURE OR S	ONS ARE THE PROPI T BE REPRODUCED O SELL OF APPARATUS	MODEL NO.: ADP-200JB SERIES		
Date	Drawn	Design (EE)	Design (ME)	DOCUMENT NAME. :	REV.
05/22'24	邱美淳	顏偉任/孔維良	廖明運/陳俊豪 /張伯毅	TS-200JB SERIES	06

Frame Name: DF-PSLA4V-2R01.DOC SHEET <u>5</u> OF <u>11</u>

# 8. Safety

#### 8.1 Hi-POT test:

8.1.1 PRIMARY to SECONDARY use 3000+10% Vac. (上昇時間: DC=1Sec, AC=0.1Sec)。
Test time=1sec。Arcing current=Level 8(EVT1: 5mA, EVT2, DVT: 8mA, PVT/MP: 10mA)
Hi-Limit current=10mA。Lo-Limit current=0.01mA。

Primary to FG:1.5KVac for 1minute

#### 8.2 Insulation Resistance (IR) test:

3.2.1 PRIMARY to SECONDARY use 500Vdc test; Insulation resistance limit: >30M ohm •

#### 8.3 Leakage current

8.3.1 The power supply leakage current shall be less than 100 uA by 240Vac/50Hz
Test with AC cable 80cm

### 9. Burn-in 測試作業規範

Follow Delta Standard Burn-in Condition

## 10. I2C 測試作業規範

N.A.

## 11. FRU Data Barcode Read/Write 測試作業規範

N.A.

		電子工業股份	分有限公司	DESCRIPTION:	
CA DE	LTA DELT	A ELECTRO	NICS, INC.	測試規格(Test Specificat	tion)
THESE DRAWINGS AND SPECIFICATIONS ARE THE PROPERTY OF DELTA ELECTRONICS, INC. AND SHALL NOT BE REPRODUCED OR USED AS THE BASIS FOR THE MANUFACTURE OR SELL OF APPARATUSES OR DE'VICES WITHOUT PERMISSION.				MODEL NO.: ADP-200JB SERIES	
Date	Drawn	Design (EE)	Design (ME)	DOCUMENT NAME. :	REV.
05/22'24	邱美淳	顏偉任/孔維良	廖明運/陳俊豪 /張伯毅	TS-200JB SERIES	06

Frame Name: DF-PSLA4V-2R01.DOC SHEET 6 OF 11

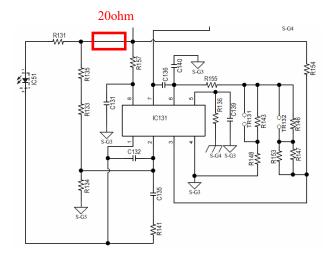
# 12. Loop/Gain 測試作業規範

Disturbance voltage setting 1.77V

線路如下所示:

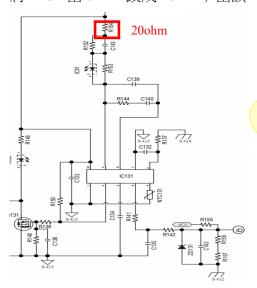
FOR ADP-200JB HA/HB/HA88/HD/HC

將 R131/R135 與 Vo 間的 trace 斷開串入 20ohm, 由該 20ohm 電阻進行 loop gain 之量測



FOR ADP-200JB KA/KB

將 R154 由 0ohm 改成 20ohm, 由該 20ohm 電阻進行 loop gain 之量測



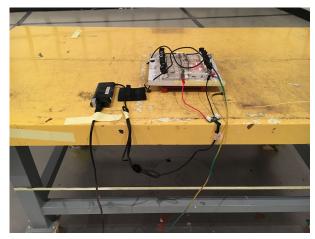
台達電子工業股份有限公司 DELTA ELECTRONICS, INC.				DESCRIPTION : 測試規格(Test Specificat	tion)
THESE DRAWINGS AND SPECIFICATIONS ARE THE PROPERTY OF DELTA ELECTRONICS, INC. AND SHALL NOT BE REPRODUCED OR USED AS THE BASIS FOR THE MANUFACTURE OR SELL OF APPARATUSES OR DE'VICES WITHOUT PERMISSION.				MODEL NO. : ADP-200JB SERIES	
Date	Drawn	Design (EE)	Design (ME)	DOCUMENT NAME.: TS-200JB SERIES	REV.
05/22'24	邱美淳	顏偉任/孔維良	廖明運/陳俊豪 /張伯毅		06

Frame Name: DF-PSLA4V-2R01.DOC SHEET 7 OF 11

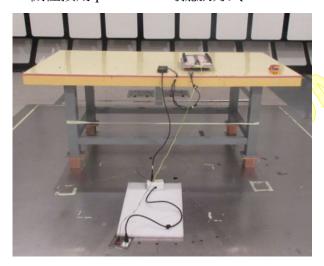
## 13. EMI/RFI Setup

- 1. AC power cord 使用 1M 線
- 2. 樣品 DC cable 放在樣品與 dummy load 之間 (不能跨到 AC power cord 及接地線)
- 3. Dummy load 放桌内, 治具與桌面切齊
- 4. 判定方式以原始機種擺放方式測試結果判定.

原始機種的擺放方式



Asus 機種接用 power box 的擺放方式



台達電子工業股份有限公司 **DESCRIPTION: DELTA ELECTRONICS, INC.** 測試規格(Test Specification) THESE DRAWINGS AND SPECIFICATIONS ARE THE PROPERTY OF DELTA MODEL NO.: ELECTRONICS, INC. AND SHALL NOT BE REPRODUCED OR USED AS THE BASIS FOR THE MANUFACTURE OR SELL OF APPARATUSES OR DE'VICES ADP-200JB SERIES WITHOUT PERMISSION. Drawn Design (EE) Design (ME) REV. Date DOCUMENT NAME.: 廖明運/陳俊豪 **TS-200JB SERIES** 05/22'24 邱美淳 顏偉任/孔維良 **06** /張伯毅

Frame Name: DF-PSLA4V-2R01.DOC SHEET 8 OF 11

#### 14. DC Plug OTP(FOR ADP-230JB KA/KB)

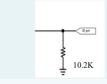
#### Adapter 使用PD IC

系統使用類比方式偵測 CC pin 分壓 Between 1.8V-2.4V, 使用ADC方式動作

> 系統使用PDIC 偵測CC PIN分壓1.1V~1.7V, 使用BMC方式動作

#### System Side ID pin Resister

CC PIN With Analogy Circuit



CC PIN With PD IC



ADC Mode

BMC	)

ID Level	Adapted Behavior	
1.8V~2.4V	Normal Out	
< 0.67V	Latch off	
	(Dehounce time 300ms)	

Follow Item 13





# 台達電子工業股份有限公司

**DELTA ELECTRONICS, INC.** 

THESE DRAWINGS AND SPECIFICATIONS ARE THE PROPERTY OF DELTA ELECTRONICS, INC. AND SHALL NOT BE REPRODUCED OR USED AS THE BASIS FOR THE MANUFACTURE OR SELL OF APPARATUSES OR DE'VICES WITHOUT PERMISSION.

Date	Drawn	Design (EE)	Design (ME)
05/22'24	邱美淳	顏偉任/孔維良	廖明運/陳俊豪 /張伯毅

**DESCRIPTION:** 

測試規格(Test Specification)

MODEL NO.:

ADP-200JB SERIES

REV. **DOCUMENT NAME.: TS-200JB SERIES 06** 

Frame Name: DF-PSLA4V-2R01.DOC

SHEET <u>9</u> OF <u>11</u>

## 15. Mechanical 包裝測試條件: 請參照台達規範: 10000-0089

- (1) Drop Test
  - a. 條件

Carton weight

~25kg, 高度 60cm

26~50, 高度 45cm

51~75, 高度 35cm

76~100, 高度 30cm

b. 紙箱測試順序

以紙箱之1個稜角/3個稜線/6個面,每次落下試驗可取任一稜角(傾斜角不得超過10度)

- c. 試驗步驟如下
  - Step1. 垂直落下此角 (Corner 2-3-5)
  - Step2. 由此角引申之最小稜線 (Edge 3-5)
  - Step3. 由此角引申之次長稜線 (Edge 2-5)
  - Step4. 由此角引申之最長稜線 (Edge 2-3)
  - Step5. 最小的面 (Front 5)
  - Step6. 相對的最小面 (Rear 6)
  - Step7. 次小的面 (Right 2)
  - Step8. 相對的次小面 (Left 4)
  - Step9. 最大的面 (Bottom 3)
  - Step10. 相對的最大面 (Top 1)
- (2) Vibration Test
  - a. 條件

頻率 5 Hz, 振幅 20 mm, 時間 5 Min.

頻率 10 Hz, 振幅 5 mm, 時間 5 Min.

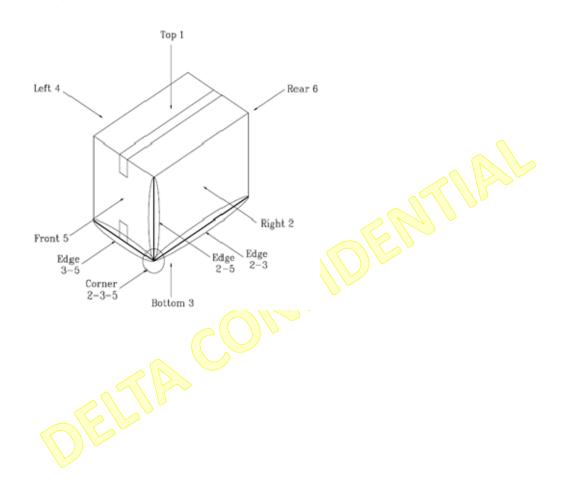
台達電子工業股份有限公司 DELTA ELECTRONICS, INC.				DESCRIPTION : 測試規格(Test Specificat	tion)
THESE DRAWINGS AND SPECIFICATIONS ARE THE PROPERTY OF DELTA ELECTRONICS, INC. AND SHALL NOT BE REPRODUCED OR USED AS THE BASIS FOR THE MANUFACTURE OR SELL OF APPARATUSES OR DE'VICES WITHOUT PERMISSION.				MODEL NO. : ADP-200JB SERIES	
Date	Drawn	Design (EE)	Design (ME)	DOCUMENT NAME.: TS-200JB SERIES	REV.
05/22'24	邱美淳	顏偉任/孔維良	廖明運/陳俊豪 /張伯毅		06

Frame Name: DF-PSLA4V-2R01.DOC

SHEET <u>10</u> OF <u>11</u>

頻率 15 Hz, 振幅 2.2 mm, 時間 5 Min. 頻率 20 Hz, 振幅 1.25 mm, 時間 5 Min.

- \* 包裝測試後判定標準:
  - (1) Drop Test --- 產品 --- 外觀無損壞, 輸出正常, Hi-Pot 測試無不良.
    - --- 包材 --- 外箱可變形,隔板潰縮移位不可大於同方向紙箱內尺寸之 4%, 產品自身之單體包裝 (PE Bag, 彩盒,吸塑盒......) 不得有變形及破損.
  - (2) Vibration Test --- 產品 --- 外觀無損壞,輸出正常, Hi-Pot 測試無不良,包裝材料無損壞.
- \* 如果參考機種已完成包裝測試,則不需重新測試.



台達電子工業股份有限公司 DELTA ELECTRONICS, INC.				DESCRIPTION: 測試規格(Test Specificat	tion)
THESE DRAWINGS AND SPECIFICATIONS ARE THE PROPERTY OF DELTA ELECTRONICS, INC. AND SHALL NOT BE REPRODUCED OR USED AS THE BASIS FOR THE MANUFACTURE OR SELL OF APPARATUSES OR DE'VICES WITHOUT PERMISSION.				MODEL NO.: ADP-200JB SERIES	
Date	Drawn	Design (EE)	Design (ME)	DOCUMENT NAME. :	REV.
05/22'24	邱美淳	顏偉任/孔維良	廖明運/陳俊豪 /張伯毅	TS-200JB SERIES	06

Frame Name: DF-PSLA4V-2R01.DOC

SHEET <u>11</u> OF <u>11</u>