Design Target Specification

Product No.	NAU83G60
Function	Stereo Class-D Amplifier 30W per channel , DSP & I/V-sense

Items:

1. General Description
2. Features
3. Pin Configuration
4. Pin Description
5. System Diagram
6. Block Diagram
7. Functional Description
8. Control and Status Registers
9. Electrical Characteristics
10. Package Specification
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- Software product design target specification should contain Item 1, 2, 5, 6, 7, 11 and others.

Manager:	Prepared By: Alan Huang

Table No.:

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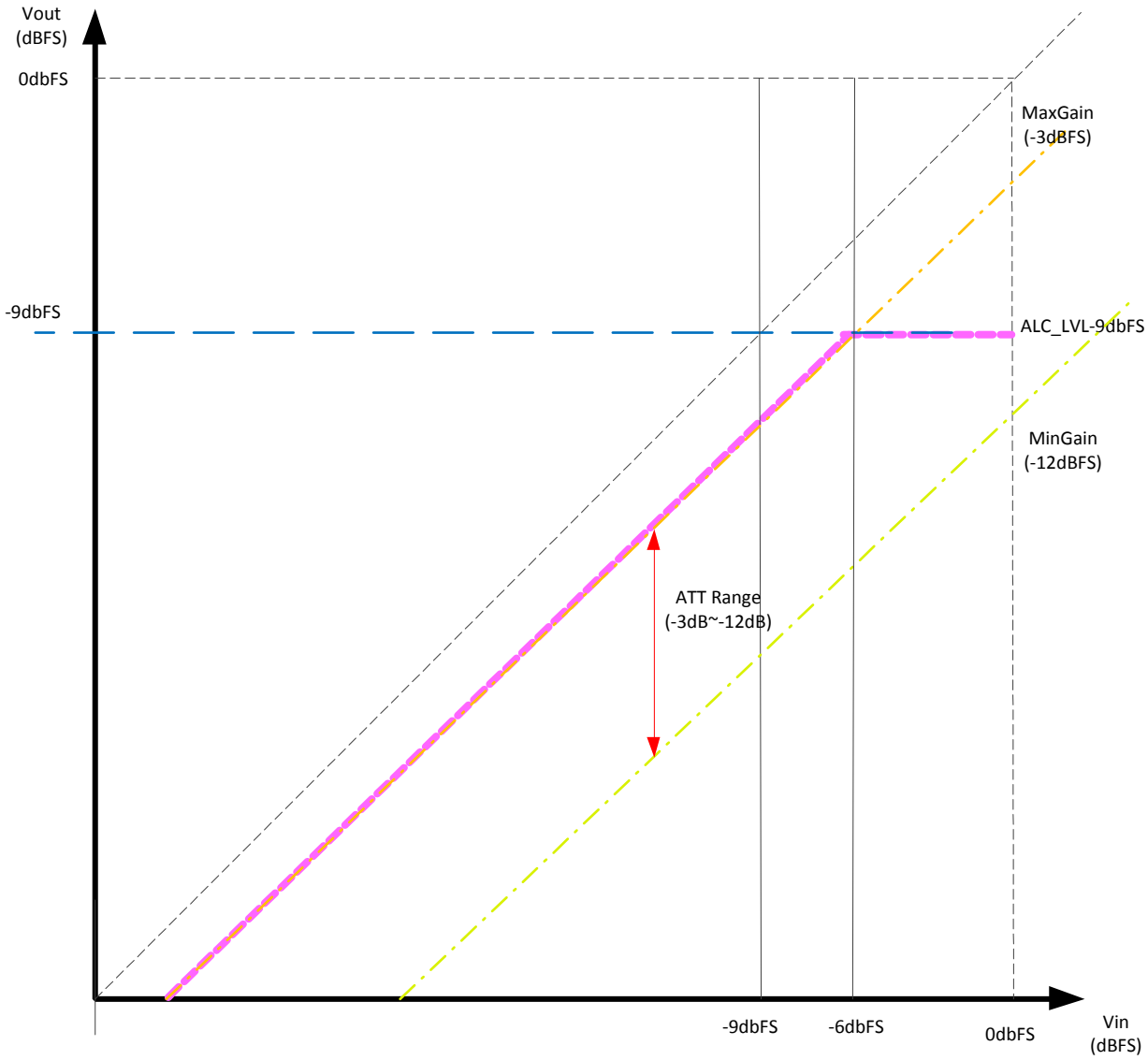

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1 GENERAL DESCRIPTION

1.1 Overview

The NAU83G60 is a Stereo amp device with DSP and V/I sense. The DSP ROM is programmed with a speaker excursion control algorithm. The target application for this device is car audio system,TV, laptop and subwoofer market. Compared to traditional Class D amp, the NAU83G60 has 4 ADCs integrated such that speaker voltage and current can be sensed and sent back to the DSP for speaker excursion control. This speaker excursion control along with boost amp technology can prevent the speaker membrane excursion from exceeding its rated limit and provide ample headroom for overall loudness and sound quality.

1.2 Features

The NAU83G60 Amplifier with DSP and I/V Sense. It has a powerful Class-D Amplifier. The chip features high output power capability, low-output noise in Receiver Mode, low-current shutdown mode, and click-and-pop suppression. Numerous types of device protection schemes are supported, as well as speaker protection schemes. The temperature monitoring in the NAU83G60 protects both the chip from overheating. The chip is available in a 56pin QFN Package (WLCSP TBDS).

Key Feature List

- Powerful Class-D Amplifier: (TBD)
  - 1 x 60W, PBTL mode (2ohm, 20V, THD+N=1%), peak power
  - 1 x 60W, PBTL mode (2ohm, 19V, THD+N=10%),peak power
  - 2 x 30W, Stereo mode (4ohm, 19V, THD+N=1%),peak power
  - 2 x 30W, Stereo mode (4ohm, 18V, THD+N=10%),peak power
  - 2 x 1W, Stereo mode(4ohm,12~20V, THD+N=0.03%)
- Low Output Noise: (TBD)
- ≥ 70 dB Power Supply Rejection Ratio (PSRR)
- Low Current Shutdown Mode (TBD)
- IRQ to HOST
- Programmable Serial Interfaces:
  - I2C Interface:
    - Clock up to Max 1MHz to reduce the initial time
  - I2S Interface:
    - supports 16,32,44.1,48,88.2,96,192KHz sample rates
    - I2S, LJ,RJ, TDM, for audio monitoring, echo cancellation reference.
  - PCM Interface
- Digital IO driving capacity: four level adjustments
- 15-Band PEQ: to provide flexible frequency response and real time adjustment for each band & update with zero crossing
- 3-Band DRC for bass enhancement
- Automatic Level Control (ALC), Under Voltage Lockout Prevention (UVLOP)
- Segment control: to improve the efficiency for low output power
- Low latency path: provide a direct ANC with 0.5ms latency@48KHz
- E-fuse: to trim the internal clock to be more accurate
- 12bit SAR ADC:
- Device Protection:
  - Over Current Protection (OCP),
  - Over Voltage Protection (OVP)
  - Under Voltage Lock Out (UVLO)
  - Over Temperature Protection (OTP)
  - Clock Termination Protection (CTP)
- Speaker Protection:
  - Current & Voltage Sensing
- Tone Generator
- ROM:128KB, RAM:24KB
- Dual Hi-Fi Fusion Core
  - DSP Max clock:122.88MHz/48KHz, 124.1856MHz/44.1KHz
  - KCS algorithm to optimize the audio performance and speaker protection
  - Support Stereo Amp or mono PBTL mode
  - Embedded Multi-band DRC multi-band
  - Support write the same command to both DSP in the same time.
- Filter-less Electro Magnetic Interference (EMI) mitigation
  - QFN56 7x7 package

Applications

- DTV,HDTV,UHD and multi-purpose monitors
- Soundbars and subwoofers, notebooks,pc speakers
- Wireless, Bluetooth speakers
- Smart Speakers (with voice assistant)
- Car Audio System(with ANC)

2 PIN CONFIGURATIONS

2.1 Pin Diagrams

The NAU83G60 Boosted Class-D Amplifier with DSP and I/V-Sense is available in a QFN56 package as shown below

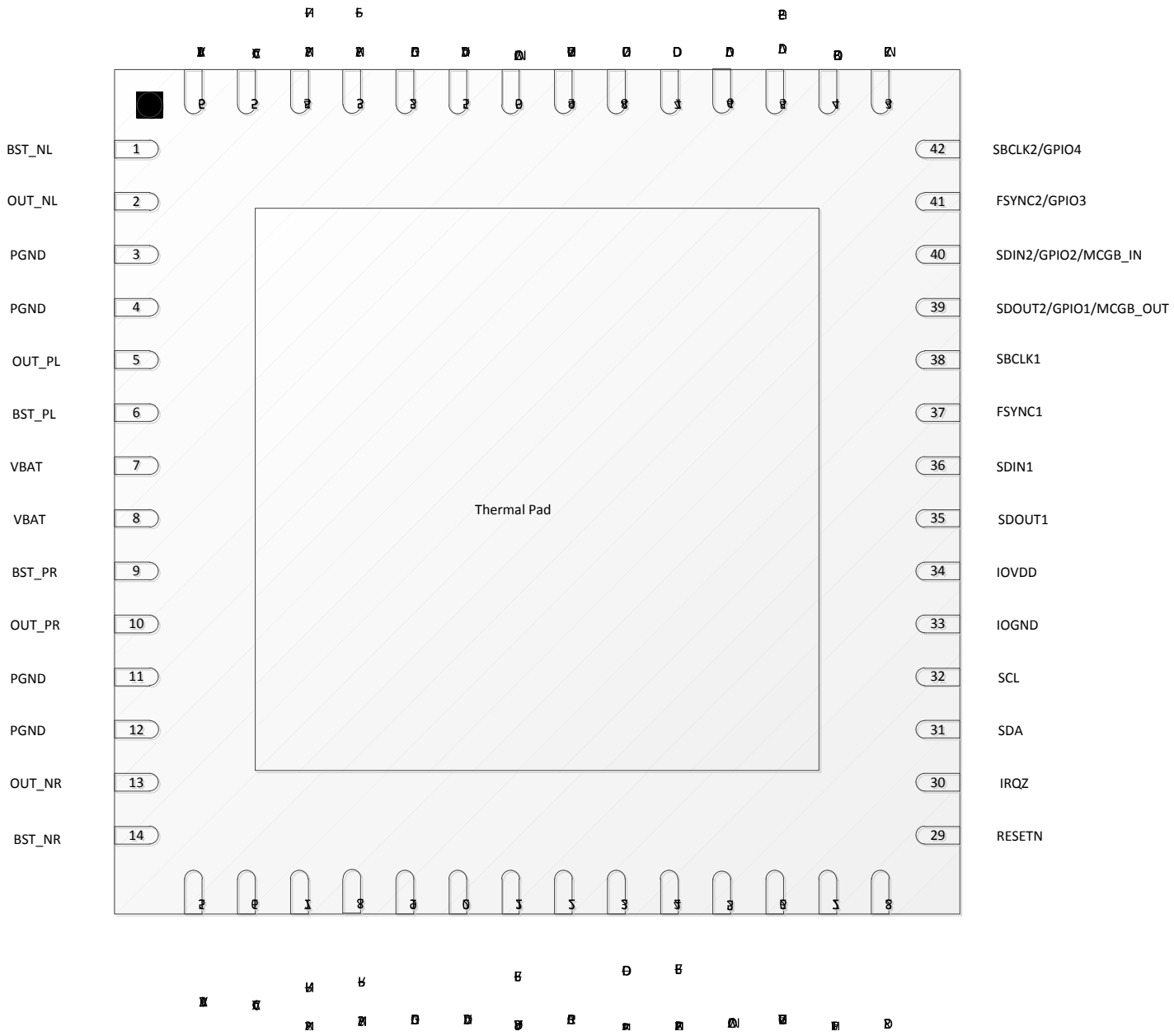


Figure 1 Pin Diagram of NAU83G60 (Top View)

2.2 PIN DESCRIPTIONS

Pin descriptions for the NAU83G60 Boosted Mono Class-D Amplifier with DSP and I/V Sense are provided in **Table 1.**

Table 1 Pin Descriptions for the NAU83G60

Pin #	Name	Type (Supply Domain)	Description
1	BST_NL	I	Left channel bootstrap I/O, negative high-side FET.
2	OUT_NL	O	Left channel negative power stage output .
3	PGND	P	Power stage ground.
4	PGND	P	Power stage ground.
5	OUT_PL	O	Left channel positive power stage output .
6	BST_PL	I	Left channel bootstrap I/O, positive high-side FET
7	VBAT	P	Class D power supply
8	VBAT	P	Class D power supply
9	BST_PR	I	Right channel bootstrap I/O, positive high-side FET
10	OUT_PR	O	Right channel positive power stage output .
11	PGND	P	Power stage ground.
12	PGND	P	Power stage ground.
13	OUT_NR	O	Right channel negative power stage output .
14	BST_NR	I	Right channel bootstrap I/O, negative high-side FET.
15	VBAT	P	Class D power supply
16	AVCC	P	Class D power supply for GVDD REG from 5V to 20V.
17	VSNS_NR	I	Right channel voltage sense negative input. Connect to class D negative output after ferrite bead filter
18	VSNS_PR	I	Right channel voltage sense positive input. Connect to class D positive output after ferrite bead filter
19	GVDD	O	High side FET Gate drive voltage regulator output (Typ 4.5V). Decouple with cap to GND.
20	AVDD	P	Analog power supply of class D analog loop.provided by internal LDO,Decouple a cap to GND.
21	SARAD_REF	O	Reference voltage output of SAR-ADC. Connect a decoupling cap to AGND.
22	VBG	O	Reference voltage output of Bandgap. Connect a decoupling cap to AGND.
23	IVSENSE_LDO	O	voltage regulator output for IVSENSE
24	IVSENSE_REF	O	Reference voltage output of IVSENSE. Connect a decoupling cap to AGND.
25	VCOM	O	Mid voltage of DAC common mode. Decouple with cap to AGND_DAC.
26	AGND	P	Analog GND of class D analog loop

Pin #	Name	Type (Supply Domain)	Description
27	FAULT	O	Fault pin inform.
28	SDZ	I	Active low hardware shutdown. 0V: chip shut down. IOVDD: chip enable
29	RESETN	I	Chip low reset. 0V: reset. IOVDD: release reset
30	IRQZ	O	Open drain, active low interrupt pin JTAG (JTDI)
31	SDA	I	I2C data pin. Pull up to IOVDD with a resistor.
32	SCL	I	I2C clock pin. Pull up to IOVDD with a resistor.
33	IOGND	P	Digital IO GND.
34	IOVDD	P	Digital IO supply. Connect a supply between 1.7~5.5V. Decouple a cap to IOGND.
35	SDOUT1	O	TDM0 serial data output in TDM mode. JTAG (JTDO)
36	SDIN1	I	TDM0 serial data input.
37	FSYNC1	I	TDM0 frame sync.
38	SBCLK1	I	TDM0 serial bit clock output in TDM mode.
39	SDOUT2/ MCGB_IN/ GPIO1	I/O	TDM1 serial data output. MCGB output GPIO1 (I2C Address selection) JTAG (JTRST) TestMode
40	SDIN2/ MCGB_OUT/ GPIO2	I/O	TDM1 serial data input. MCGB input GPIO2 (I2C Address selection) JTAG (JTMS) Testmode
41	FSYNC2/ GPIO3/ TestMode	I/O	TDM1 frame sync GPIO3. JTAG (JTDOEn) CLKOUT
42	SBCLK2/ GPIO4/ Testmode	I/O	TDM1 serial bit clock input. GPIO4 JTAG (JTCK)
43	MCLK	I	External clock input pin
44	FSOURCE	I/O	EFUSE SOURCE pin
45	IOVDD_EFUSE	P	Power supply of Efuse IP
46	DVDD	P	Power supply input of internal DREG regulator. Decouple with cap to DGND.
47	DLDO	O	Digital core voltage regulator output (1.5V). Decouple with cap to

Pin #	Name	Type (Supply Domain)	Description
			DGND.
48	DGND	P	Digital GND.
49	AGND	P	Analog GND of class D analog loop
50	VCOM	O	Mid voltage of DAC common mode. Decouple with cap to AGND_DAC.
51	AVDD	P	Analog power supply of class D analog loop from Internal LDO. Decouple a cap to GND.
52	GVDD	O	High side FET Gate drive voltage regulator output (Typ 4.5V). Decouple with cap to GND.
53	VSNS_PL	I	Left channel voltage sense positive input. Connect to class D positive output after ferrite bead filter
54	VSEN_NL	I	Left channel voltage sense negative input. Connect to class D negative output after ferrite bead filter
55	AVCC	P	Class D power supply from VBAT.
56	VBAT	P	Class D power supply

3 BLOCK DIAGRAM

A Block Diagram for the NAU83G60 is provided in

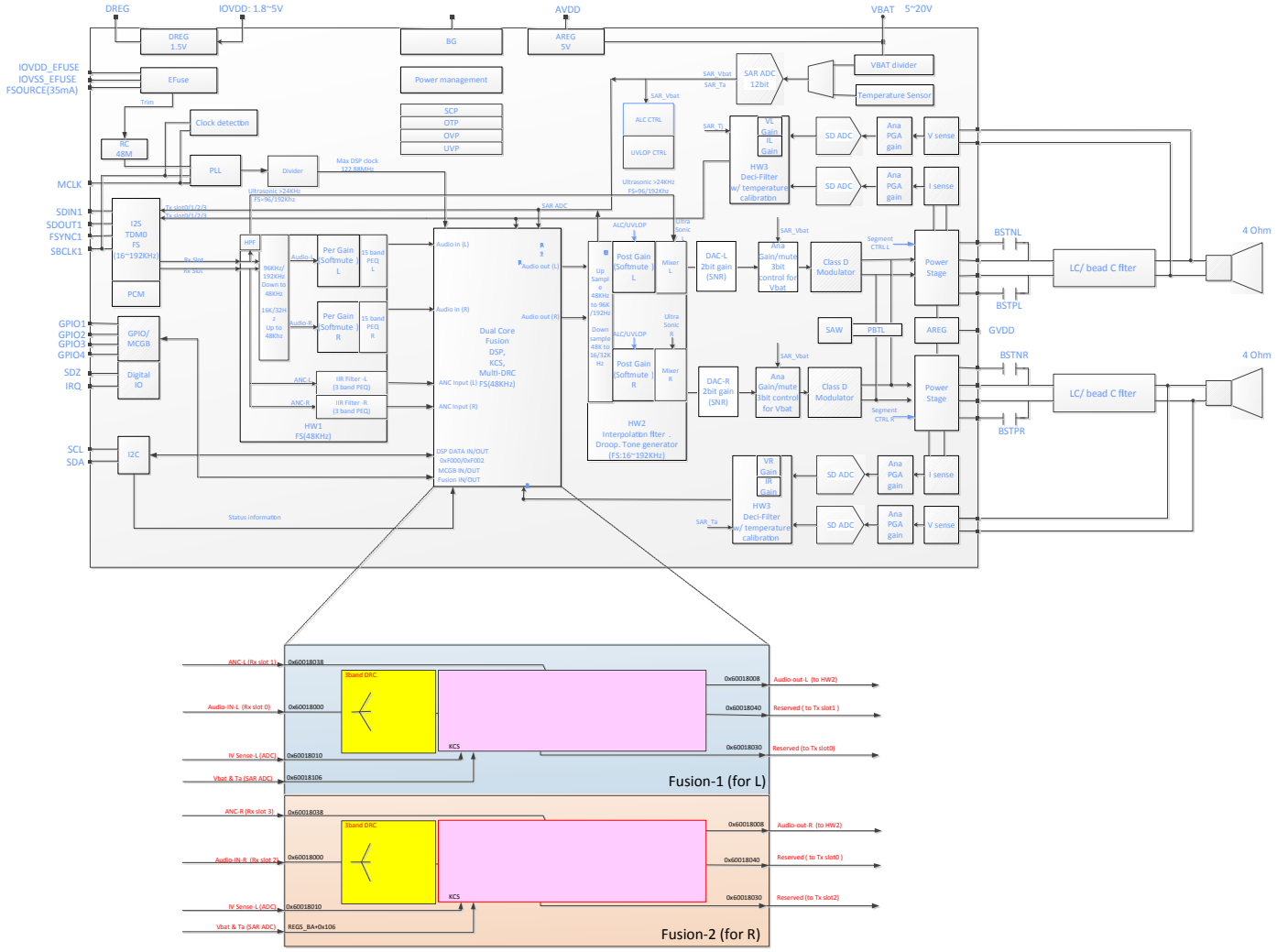


Figure 2 NAU83G60 Block Diagram

4 ELECTRICAL CHARACTERISTICS

The tables in this chapter provide the various electrical parameters for the NAU83G60 and their values.

4.1 Absolute Maximum Ratings

Table 2 Absolute Maximum Ratings

Parameter	Min	Max	Units
IOVDD Digital I/O Supply Range	-0.3	6	V
DVDD Digital supply Range	-0.3	6	V
VBAT Battery Supply Range	-0.3	22	V
AVCC Analog Supply Range	-0.3	22	V
Voltage Input I/O Range	DGND - 0.3	IOVDD + 0.3	V
Junction Temperature, T_J	-40	+150	°C
Storage Temperature	-65	+150	°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely influence product reliability and result in failures not covered by the warranty.

4.2 Operating Conditions

Table 3 Recommended Operating Conditions for the NAU83G60

Condition	Symbol	Min	Typical	Max	Units
Battery Supply Range	VBAT/AVCC	5.0	18	20	V
Digital I/O Supply Range	IOVDD/DVDD	1.70	3.3	5.2	V
Ground	DGND		0		V
Industrial Operating Temperature		-40		+85	°C

4.3 Electrical Parameters

Table 4 Electrical Characteristics

Conditions: IOVDD = 3.3V; V_{BAT}= 18V. R_L = 8 Ω + 33 µH, f = 1kHz, 48kHz sample rate, MCLK=12.88MHz, Boost Inductor = 1 µH , unless otherwise specified. Limits apply for T_A = 25°C

Symbol	Parameter	Conditions	Typical	Limit	Units
ISD	Stutdown Supply Current	IOVDD, clocks off	TBD		µA
		$V_{BAT,}$ clocks off	TBD		µA
ISB	Standby Mode Supply Current	IOVDD, clocks off, clock gating on	TBD		µA
		$V_{BAT,}$ clocks off, clock gating on	TBD		µA
IDD	Operating Mode Supply Current	IOVDD, idle Channel,DSP off	TBD		mA
		$V_{BAT,}$ idle Channel,DSP off	TBD		mA
Class-D Channel					
P_O	Output Power	RL = 8 Ohm + 33 µH and Total Harmonic Distortion+Noise (THD+N) = 1%	TBD		W
		RL = 8 Ohm + 33 µH and Total Harmonic Distortion+Noise (THD+N) = 10% VBAT=18V	TBD		W
		RL = 4 Ohm + 33 µH and Total Harmonic Distortion+Noise (THD+N) = 1%	TBD		W
		RL = 4 Ohm + 33 µH and Total Harmonic Distortion+Noise (THD+N) = 10% VBAT=18V	30		W
THD+N	Total Harmonic Distortion + Noise	R_L = 8 Ω + 33 µH, f=1kHz, P_O = 1W	0.03		%
e_{OS}	Output Noise	A-Weighted, 20Hz-20kHz, Receiver mode or Auto attenuate, no DAC input signal, gain = 0dB	TBD		µVrms
		A-Weighted, 20Hz-20kHz, no DAC input signal, gain = 17.5dB	TBD		µVrms
PSRR	Power Supply Rejection Ratio	DC, V_{BAT} = 2.9V – 5.5V, GAIN = 17.5dB	70		dB
		f_{RIPPLE} = 217Hz, V_{RIPPLE} = 200mV_{P_P} GAIN = 17.5dB	70		dB
		f_{RIPPLE} = 1020Hz, V_{RIPPLE} = 200mV_{P_P} GAIN = 17.5dB	70		dB
		f_{RIPPLE} = 4kHz, V_{RIPPLE} = 200mV_{P_P} GAIN = 17.5dB	70		dB
Fres	Frequency Response	F = 20Hz ~ 20KHz, 1Watt, R_L = 8 Ω + 33 µH	+-0.8		dB
V_{OS}	Output Offset Voltage	Idle Channel, Gain= 0dB	±0.7	±5	mV
Kpop	Pop and Click Noise	A-weighted, Idle DAC input, Clock Gating, toggling clocks on/off	TBD		mVrms
		A-weighted, Idle DAC input, toggling between -120dBFs DAC In & 2048 zero samples	TBD		mVrms
Rdson-P	Driver P Side MOS-FET ON-resistance	V_{BAT}= 18V. R_L = 8 Ω + 33 µH, DC Output Clipping	0.18		Ohm
Rdson-N	Driver N Side MOS-FET ON- resistance	V_{BAT}= 18V. R_L = 8 Ω + 33 µH, DC Output Clipping	0.18		Ohm
Fsw	Switching Frequency	Average	TBD		kHz
Voltage Sense ADC					
THD+N	ADC Total Harmonic Distortion + Noise	VBAT = 18V, +10dBVrms, Class-D off	TBD		%

Symbol	Parameter	Conditions	Typical	Limit	Units
SNR	Signal to Noise Ratio	Flat, 20Hz – 20kHz	TBD		dB
FS_{ADC}	ADC Full Scale Input Level		TBD		V_{PK}
Current Sense ADC					
THD+N	ADC Total Harmonic Distortion + Noise		TBD		%
SNR	Signal to Noise Ratio	Flat, 20Hz – 20kHz	TBD		dB
FS_{ADC}	ADC Full Scale Input Level		TBD		A_{PK}
Battery Sense ADC					
INL	Integrated Non-Linearity	V_{BAT}= 5V-30V (gain & offset compensated)	TBD		LSB
DNL	Differential Non-Linearity	V_{BAT}= 5V-30V	TBD		LSB
PLL					
Fin	Input Frequency Range		TBD		
Fout	output Frequency Range		TBD		
SARADC					
VBAT	Voltage Battery input Range			4.5~26	V
Tj	Junction temperature input range			-40~120	℃

4.4 Digital I/O Parameters

Table 5 Digital I/O Characteristics

Parameter	Symbol	Comments/Conditions		Min	Max	Units
Input LOW level	V_{IL}	IOVDD = 1.8V			0.33*IOVDD	V
		IOVDD = 3.3V			0.37*IOVDD	
Input HIGH level	V_{IH}	IOVDD = 1.8V		(1.7V) 0.94*IOVDD		V
		IOVDD = 3.3V		0.63*IOVDD		
Output HIGH level	V_{OH}	I_{Load}= 1mA	IOVDD=1.8V	(1.7V) 0.94*IOVDD		V
			IOVDD = 3.3V	0.95*IOVDD		
Output LOW level	V_{OL}	I_{Load}= 1mA	IOVDD = 1.8V		0.1*IOVDD	V
			IOVDD=3.3V		0.05*IOVDD	

Parameter	Symbol	Comments/Conditions	Min	Max	Units
MCLK dutycycle	D_{MCLK}	PLL (TBD)	48	52	%
MCLK jitter	j_{MCLK}	PLL (TBD)	-	0.1	nsec rms
MCLK Frequency	MCLK	1.8V IO voltage	-	24.576	(MHz)
BCLK Frequency	SBCLK1	1.8V IO voltage		24.576	(MHz)

4.5 THD+N Plots

Figure 3 NAU83G60 THDN Plot examples

4.6 PSRR Plots

Figure 4 NAU83G60 PSRR Plot examples

4.7 Frequency Response Plots

Figure 5 NAU83G60 Frequency Response Plot examples

4.8 Power Plots

Figure 6 NAU83G60 Output Power Plot examples

5 FUNCTIONAL DESCRIPTION

This chapter provides detailed descriptions of the major functions of the NAU83G60 Stereo Amplifier.

5.1 Inputs

The NAU83G60 provides digital inputs to acquire and process audio signals with high fidelity and flexibility. There is an input path from I2S/PCM/TDM Interface to receive the Audio/ANC data from the Host in the same Frame.

5.2 Outputs

The NAU83G60 Amplifier has a Class-D PWM driver that can drive an 8 Ohm speaker up a peak voltage of 20V.The Class-D output voltage and current sensing data are provided at the I2S/PCM Interface output. There is an output path from I2S/PCM/TDM Interface to output the AEC reference data to the Host in the same Frame.

5.3 ADC, DAC

The NAU83G60 has four independent, high-quality Analog-to-Digital Converters (ADCs) and two Digital-to-Analog Converter (DAC). These are high-performance, 24-bit sigma-delta converters, which are suitable for a very wide range of applications.

5.4 Digital Signal Processing

There are three hardware engine for the advanced Digital Signal Processing (DSP) subsystems that enable a very wide range of programmable signal conditioning and signal optimizing functions. All digital processing is done with 24-bit precision to minimize processing artifacts and to maximize the audio dynamic range supported by the NAU83G60.

HW engine1 supports Up/Down sample rate converter, high-pass filters to separate ultra-sonic data over 24KHz, soft mute/unmute to avoid the pop noise and gain adjustment. Sample rate converter will transfer the 16KHz/32KHz sample rate to 48KHz sample rate, 96/192KHz sample rate to 48KHz sample rate.

HW Engine2 supports up sample rate converter, ALC gain control, ultra-sonic mixer. Ups sample rate to transfer 48KHz sample rate to 96/192KHz sample rate. The ALC Gain will depend on the voltage of Battery to adjust the digital signal level to avoid the clipping if the voltage of battery drops largely.

HW Engine3 supports the digital gain adjustment for the Voltage/Current Sense data from Class-D amplifier. The current Sense data will be corrected with temperature compensation to get better performance.

5.5 Digital Interfaces

The I2C control interface provides a flexible, 2-wire Serial Control Interface and its Max clock is up to 1MHz to reduce the initial time during the system power on. the NAU83G60 will provide the different I2C address selection which depends on the status of GPIO1/GPIO2

5.6 Power Supply

The NAU83G60 only needs two external power source to operate. The VBAT and AVCC is designed to connect with the external power supply or battery cells which the voltage range is 5V~20V as the analog domain power source. The IOVDD and DVDD is designed to connect with the external supply or PMIC which the voltage range is 1.8V/3.3V/5V as the digital domain power source. There are three internal LDO (DLDO/ALDO/IVSENSE_LDO) to provide the excellent PSRR performance with low noise and low quiescent current.

However, the Electro Static Detection (ESD) protection diodes between the supplies impact the application of the supplies. Because of these diodes, the following conditions need to be met to avoid current leakage: (TBD)

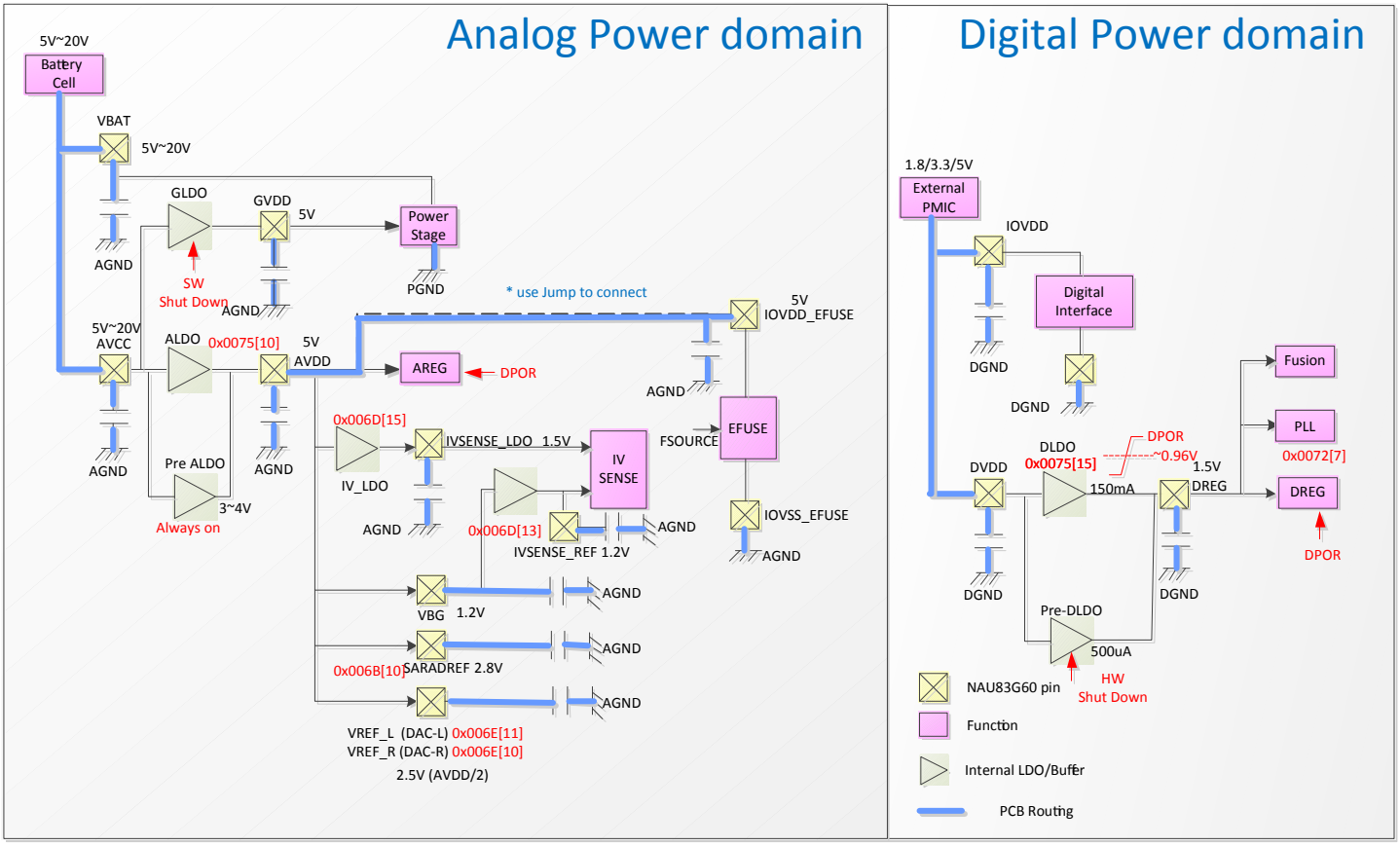


Figure 7 NAU83G60 Power Tree

5.7 Power-On-and-Off Reset

The NAU83G60 includes a Power-On-and-Off Reset circuit on-chip. This circuit resets the internal logic control at DVDD supply power-up and this reset function (DPOR) is automatically generated internally. Both the digital and analog logic control register will be reset to default value. Reset thresholds are around 0.96V of DVDD during a poweron ramp. It should be noted that these values are much lower than the required voltage for normal operation of the chip and AVDD is earlier than the DVDD when the system power up.

5.8 Voltage Reference (VREF)

The NAU83G60 includes Four voltage reference, VREF_L, VREF_R, SARADREF and IOSENSE_REF. The VREF_L and VREF_R is the mid-supply, reference circuit that produces voltage close to AVDD/2 that is decoupled to VSS through the VREF pin by means of an external bypass capacitor. Because VREF_L and VREF_R are used as a reference voltage for the majority of the NAU83G60 of DAC, a large capacitance is required to achieve good power supply rejection at low frequency, typically 4.7 µF is used.

The SARAD_REF and IOSENSE_REF are used as the reference voltage for the majority of the NAU83G60 of SARADC and IV Sense, a large capacitance is required to achieve good power supply rejection at low frequency, typically 4.7 µF is used.

APPLICATION NOTES:

- Larger capacitances can be used but increase the rise time of VREF and delay the line output signal.
- Due to the high impedance of the VREF pin, it is important to use a low-leakage capacitor.
- A pre-charge circuit has been implemented to reduce the VREF rise time.

5.9 DAC Soft Mute

The Hardware Engine 1 and 2 are embedded programmable digital gain with soft mute function. it ramps down the DAC digital volume to zero. When disabled, the volume increases to the register-specified volume level for each channel. This function is beneficial for using the DAC without introducing pop-and-click sounds.

5.10 Hardware and Software Reset

The NAU83G60 and all of its control registers can be reset to initial default power-up conditions by writing any value to **REG0X00** ***once*** using any of the control interface modes. Writing to any other valid register address terminates the reset condition, but all registers will be set to their power-on default values. This is typically done during hardware reset.

The NAU83G60 can be reset to initialized power-up conditions by writing any value to **REG0X01** ***twice*** using any of the control interface modes. Writing to **REG0X01** will reset the NAU83G60, but all registers values will be unaffected. This is typically done during operation to quickly force NAU83G60 in the known initialized startup state.

<HW/SW Reset Register 0x0000/0x0001>

0	HARDWARE_RST	RESET_N1																	Write this register ***once*** to reset all the registers.
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
1	SOFTWARE_RST	RESET_N_ SOFT_PRE																	Write this register ***twice*** to reset all internal stated machines without resetting the registers.
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000

5.11 SAR ADC

The SAR ADC is an 12-bit Analog-to-Digital Converter (ADC) used to detect the voltage level on the VBAT supply voltage, the junction temperature sensor.

<SAR ADC Register 0x00 & 0x00>

006A	SARADC_CFG0	ADC_EN																	1: Enable SAR ADC (default) 0: Disable SAR ADC
		RESETB_SARADC																	ResetB of SAR ADC 0: reset the ADC
		ADC_CAL																	Auto-calibration 0:disable calibration
		ADC_CLKDIV																	CLK divider 0:CLK_ADC = CLK (default)
		ADC_CALSEL[2:0]																	3'd0 calibrate offset(coarse+fine) 3'd1 calibrate offset + MSB 3'd2 calibrate offset+ MSB+MSB-1 ...f
		Reserved																	Reserved
		CH[1:0]																	Manual setting of Input channel select bit <00>:channel 0: (default) VBAT <01>:channel 1: Temperature sensor <10>:channel 2: null <11>:channel 3: Test mode analog input
		TRIMSMPL[2:0]																	Trim sample time (48Mhz CLK) <000> 20.83ns (for test mode) <001> 666.667ns (default) <010> 1.333us ..... <111> 4.667us
		SAR_Input_Ch_Sel_Mode??(RTL select?)																	1: Manual mode 0: Auto-mode
		VBAT_AVG_EN																	Enable of extra average filter of SAR_ADC VBAT output for better SNR and lower speed. 0: Disable average filter (default) 1: Enable average filter
		VTEMP_AVG_EN																	Enable of extra average filter of SAR_ADC temperature sensor output for better SNR and lower speed. 0: Disable average filter 1: Enable average filter (default)
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000

006B	SARADC_CFG1	VTEMP_EN																	1: Enable temperature sensor 0: Disable temperature sensor output is "low state"
		VBATDIV_EN																	1: Enable VBATDIV 0: Disable VBATDIV
		VBATDIV_TRIM[2:0]																	VBAT trim: default 3'b000
		VRF_EN																	VRF enable bit ; 1'b1 : enable; 1'b0: VRF_OUT=FLOATING. Note: Bandgap must be turned on before VRF
		PRELOAD_VRF_EN																	Pre-load enable bit, default=1'b0 1'b0 : pre-load disable ; 1'b1 : pre-load enable
		Reserved																	Reserved
		VRF_TRIM[6:0]																	Trim VRF_OUT, default= 7'b1000000 Output MAX=7'b1111111; Output MIN=7'b0000000
		Reserved																	Reserved
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000

5.11.1 SAR ADC Functions

The SAR ADC is enabled by **0x006A[15].** Setting this bit to 1 enables the SAR ADC; setting the bit to 0 disables the function. After the SAR ADC has been enabled using **SAR_ENA**, the SAR ADC enters a sampling phase. During this phase, the voltage level on the input is sampled at a speed determined by **0x006A[12]**.

5.11.2 SAR ADC Control

The NAU83G60 needs to process and monitor two inputs: Battery Supply Voltage (VBAT), Junction Temperature (Tj),as shown in **Figure 8**.

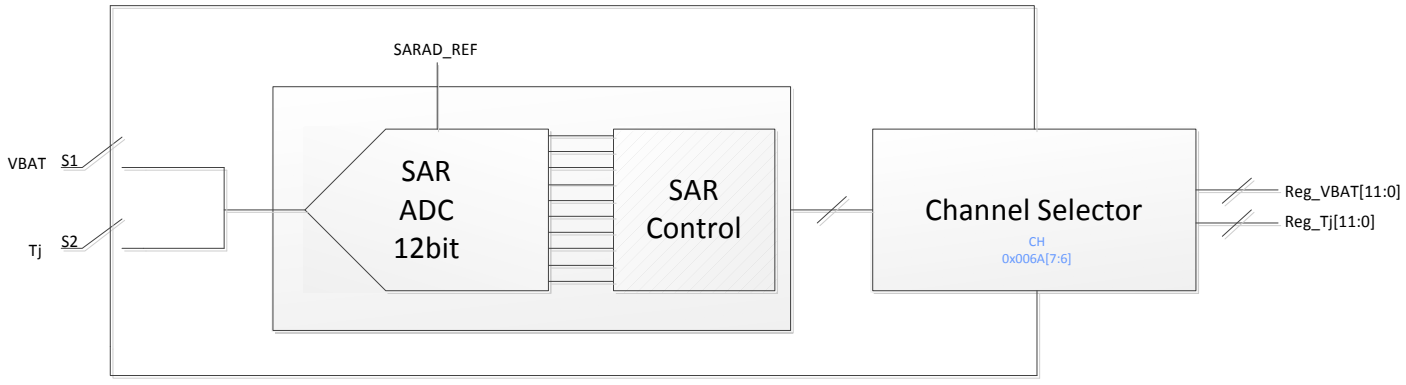


Figure 8 SAR ADC Control

The SAR ADC reads a full scale of 26V on VBAT. Below is a table of the VBAT voltage and the SAR reading

Vbat	SarADC (0xXXXX)	Tj	SarADC (0xXXXX)
4.5		-40	
5		-30	
6		-20	
7		-10	
8		0	
9		10	
10		20	
11		30	
12		40	
13		50	
14		60	
15		70	
16		80	
17		90	
18		100	
19		110	
20		120	
21			
22			
23			
24			
25			
26			

5.12 Clock Tree

The block diagram of the clock tree of NAU83G60 is shown in **Figure 9**.The digital/analog system clock can be generated from MCLK/PLLOUT/BCLK0/RC48M.It is noted that some device can't provide the MCLK output but the Nau83G60 can still generate the system clock from the BCLK. The internal RC48M is another system clock source if the Host works abnormally and stops the MCLK/BCLK without following the driver behavior. By this way, we can make sure that the function still works and protect the system. The NAU83G60 includes the Fraction-N PLL to provide wide input/output clock range. The Max operation speed of Fusion and Hardware engine is 122.88MHz.

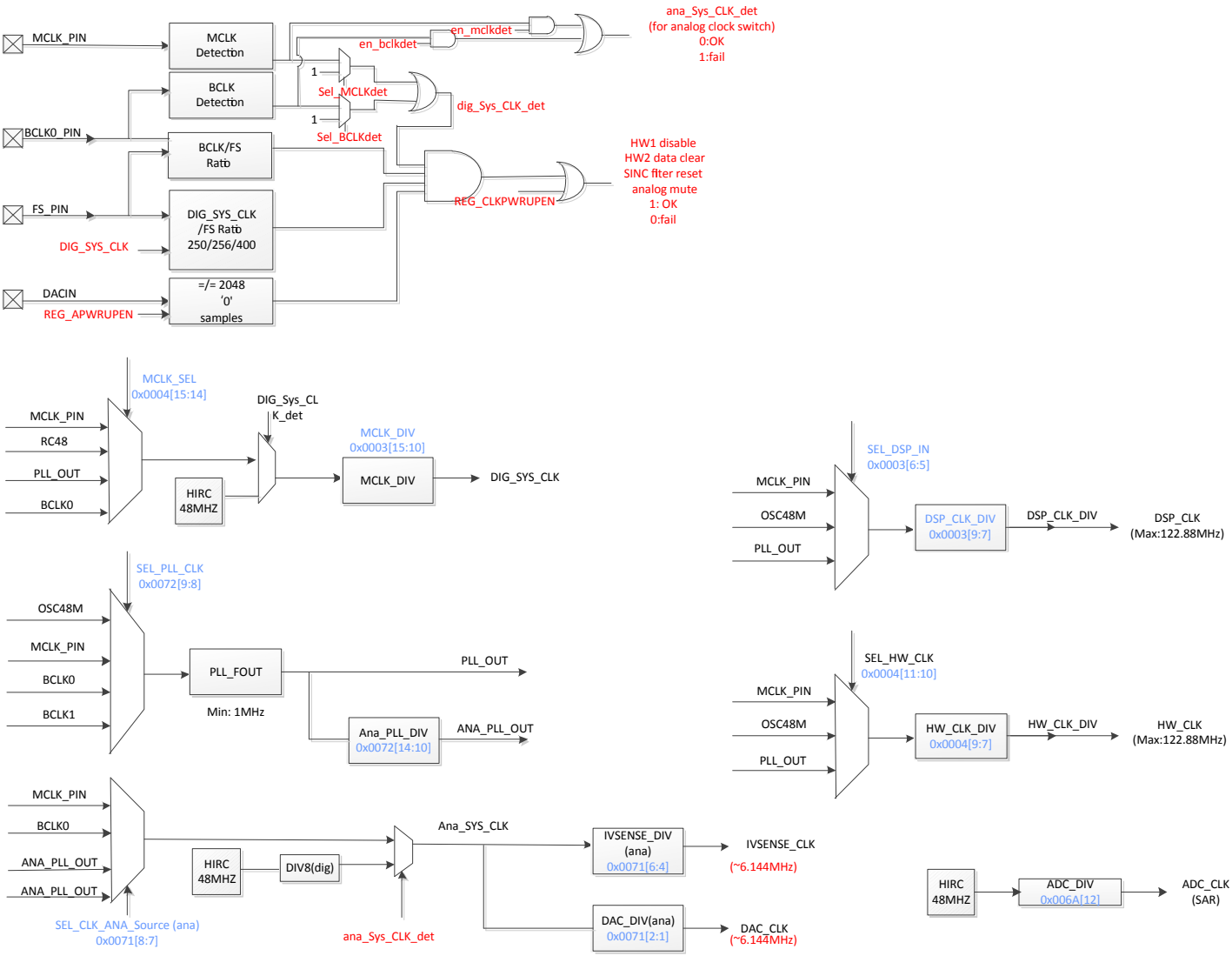


Figure 9 NAU83G60 Clock Tree

5.12.1 Clock Detection

The NAU83G60 includes a Clock Detection circuit that can sense the external clock MCLK,FS and BCLK. It also computes the ratio of MCLK/FS and BCLK/FS to configure prepare clock setting. The clock detection works with BCLK in 32bits or more than 32bits Fs format. The engineer needs to depends on the external MCLK and FS to write the correct information into 0x0040[12:10] and 0x0040[9:7]. If external MCLK is failed to output to the NAU83G60 when the abnormal system operation, the clock detection will auto switch the system clock source from MCLK to internal RC48M clock.

40	CLK_DET1	APWRUPEN	1															default:1 1: enable zero data function 0: disable
		CLKPWRUPEN		0														default:0 1: disable clock dtection funcion 0: enable
		PWRUP_DFT			0													default:0 when user disable clock dtection funcion, user can set PWRUP_DFT to control clock detection signal
		REG_SRATE				0	0	1										usre need to set the correct sampling rate by setting this register 000: 16K 001: 32K 010: 48K 011: 96K 100: 192K
		MCLK_RATE							1	0	0							usre need to set the correct MCLK rate by setting this register 000: 12MHz 001: 12.288MHz 010: 19.2MHz 011: 24MHz 100: 24.576MHz
		reserved																reserved
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000

Conditions for enabling clock detection:

1) If **REG_APWRUPEN (0x0040[15])** is set to 1, clock detection will require non-zero samples to enable output of a power-up signal. Any non-zero sample will be sufficient. After power-up, if 2048 zero samples are detected, the **PWRUPEN** signal is asserted to 0. If **REG_APWRUPEN** is set to 0, this function does not control the **PWRUPEN** signal.
2) Clock detection in the NAU83G60 is disabled by setting **REG_CLKPWRUPEN(0x0040[13])** to 1. In this state, **PWRUPEN** is no longer controlled by the enabling conditions listed above, but is set to 1. However, the MCLKDET and clock dividers are still active.

The range of the input clocks is shown in **Table 6**.

Table 6 Range of Input Clocks

Signal	Min	Max
Frame Synch (FS) (kHz)	16	192
Master Clock MCLK (MHz)	12	24.576

5.12.2 Sample and Over Sampling Rates

Possible Sample Rate and DIG_SYS_CLK selections are shown in **Table 7**.

DIG_SYS_CLK(MHz)	OSR
6.144	128
11.2896	256
12	250
12.288	256
19.2	400
24	250
24.576	256

Table 7 Sampling and Over Sampling Rates

DSP clock & Hardware Engine clock

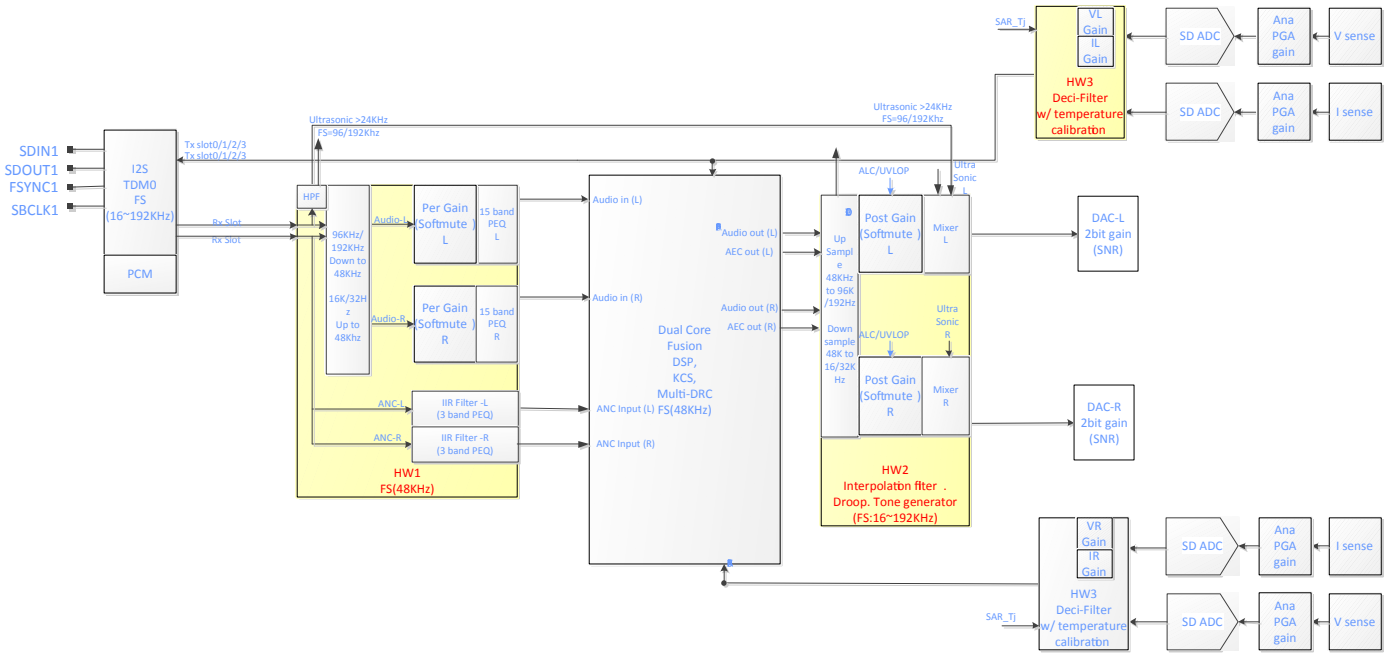
The clock for the DSP and hareware engine are generated from external MCLK, internal RC clock or embedded PLL block. The Max frequency of this clock is 122.88MHz.

5.12.3 MCLK/BCLK Clock Divider

The NAU83G60 includes several dividers: MCLK_DIV, BCLK_DIV and DSP_CLK_DIV…etc. it depending on the sample rate setting and the MCLK/FS and BCLK/FS ratio, the user needs to depends on the application to configure the register properly.

5.13 HW Engine

For NAU83G60, there are three embedded hardware engine (HW1,HW2 and HW3). These engines provide the up/down sample converter, PEQ, Soft mute, gain adjustment, temperature compensation, low latency ANC path to cover kinds of different application and scenario.



5.13.1 Hardware Engine 1(HW1)

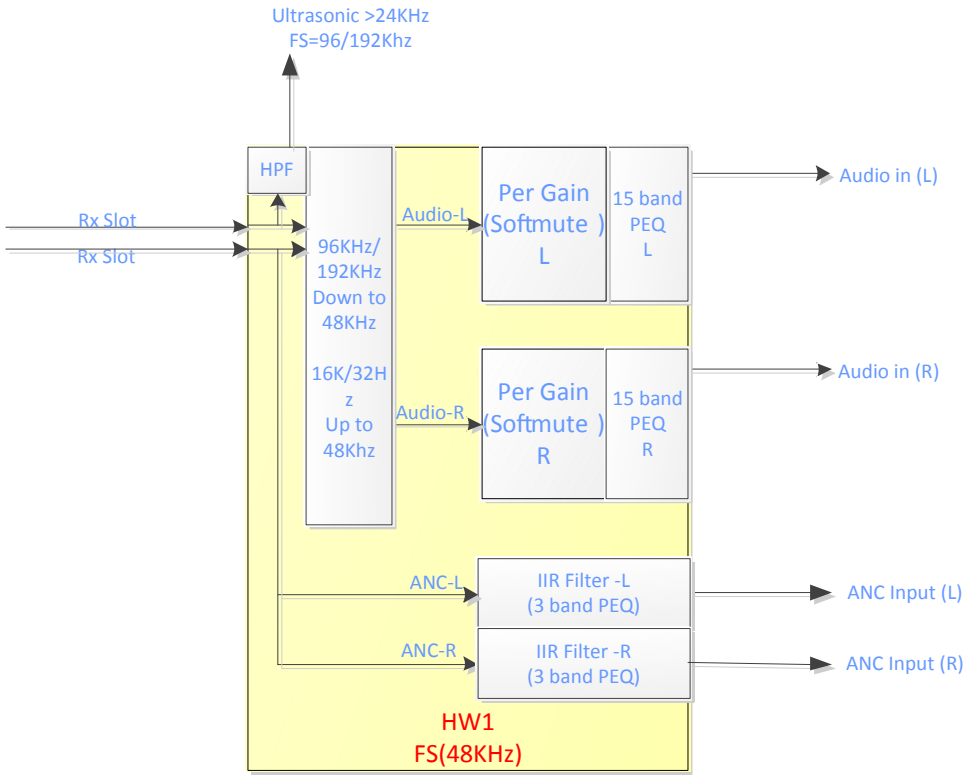


Table 8 HW1 block diagram

HW1 is placed between TDM0 and Fusion-L/Fusion-R. it plays the key role as crossover filter of ultra-sonic, sample rate converter, digital gain adjustment with soft mute, crossover filter of multi-band DRC and low latency ANC path.

Crossover filter of ultra-sonic will separate TDM RX signal to two Frequency band by HPF. The cutoff frequency of HPF is 24KHz.

The ultrasonic data is available after HPF and will be mixed with the processed audio data in the HW2 block.

HW1 also transfers different input sample rate to compatible with DSP algorithm. If the sample rate is 16/32KHz from TDM0, it will up-sample to 48KHz. It the sample rate is 96KHz or 192KHz from TDM0, it will down-sample to 48KHz.if the sample rate is 44.1/48KHz, the up/down sample is not active.

9A	HW1_CTL0	VOL_L																	Interpolator volume gain Left channel
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
9B	HW1_CTL1	VOL_R																	Interpolator volume gain Right channel
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
9C	HW1_CTL2	reserved																	
		VSR																	
		HW1_CH_MUTE								1									
		Zero_THD									1	0	0	0	0	0	0	0	
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
9D	PEQ_CTL	PEQ_band	1	0	0	0													
		mem_test																	set 1 : write coeficient, set 0 : normal run
		mem_clear																	set 1 : clear DRAM, set 0 : normal run
		PRQ_stall																	set 1 : stall PEQ HW, set 0 : normal run
		Default	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0x0000

After up/down sample, the signal level can be adjusted by per-gain 0x009A[15:0] & 0x009B[15:0]

The Soft mute/unmute can avoid the pop noise during mute/unmute 0x009C[8]. This attacking/recover time can be adjusted by the register 0x009C[10:9] to have better hearing. When the soft unmute/unmute is active, the gain will be changed only if the zero cross happens. If there is any DC offset in the path, the register 0x009D[7:0] can be adjusted.

HW1 also embedded 15-band high precision PEQ to provide more flexible Frequency response. The register 0x009D[15:12] is controlled the band numbers is enable.

	L	R
BIQ0	0100~010b	0200~020b
BIQ1	010c~0117	020c~0217
BIQ2	0118~0123	0218~0223
BIQ3	0124~012F	0224~022F
BIQ4	0130~013B	0230~023B
BIQ5	013C~0147	023C~0247
BIQ6	0148~0153	0248~0253
BIQ7	0154~015F	0254~025F
BIQ8	0160~016B	0260~026B
BIQ9	016C~0177	026C~0277
BIQ10	0178~0183	0278~0283
BIQ11	0184~018F	0284~028F
BIQ12	0190~019B	0290~029B
BIQ13	019C~01A7	029C~02A7
BIQ14	01A8~01B3	02A8~02B3

The coefficient of each band is placed in the register table as below. when the user writes the coefficient in to the HW1, it needs to follow the sequence as below

PEQ setup flow:

Step1: set PEQ_stall 0x009D[0]= 1

Step2: set_mem_test 0x009D[2]= 1

Step3: set mem_clear 0x009D[1]= 1

Step4: wait mem_clear 0x009D[1]= 1

Step5: set mem_clear 0x009D[2]= 0

Step6: write coefficient (L:0x0100~01B3, R:0x0200~02B3)

Step7: set mem_test 0x009D[2]= 0

Step8: set PEQ_stall 0x009D[0]= 0

The path of ANC signal is required with low latency(<0.5ms). when the ANC is enable, the Band13/14/15 of PEQ can be transferred as 3rd IIR Filter in the ANC path. After processing, the ANC signal will be mixed with Audio stream inside the DSP.

5.13.2 Hardware Engine 2 (HW2)

HW2 is placed between Fusion-L/Fusion-R and DAC. it plays the key role as sample rate converter, digital gain adjustment with soft mute, mixer to combine ultrasonic and audio data. It receives the data from the output buffer which is processed by KCS and already combine the ANC and audio data. After DSP processing, the sample rate is 44.1KHz or 48KHz.

Since the signal of AEC reference is required for the Host, it needs to keep the same sample rate for the TDM0 Tx/Rx.

If the up/down sample converter of HW1 is active, it means the down/up sample converter of HW2 is also active.

By this way, the data of TDM0 Tx/Rx will operate the same sample rate without extra processing.

For ultra-sonic application, the TDM0 operates as 192KHz and HW1 will down sample from 192KHz to 48KHz before DSP processing. Then HW2 will up sample from 48KHz to 192KHz.

For narrow band application,

The digital post gain is controlled by the ALC function which depends on the voltage of VBAT to adjust. Since the post gain is one of the factor for KCS algorithm, the gain information is relative with the KCS calibration and can be access directly from the memory.

The Final stage is the mixer to combine processed audio data and the ultra-sonic data.

The HW2 also includes the tone generator which is active as beeper during the system power on.

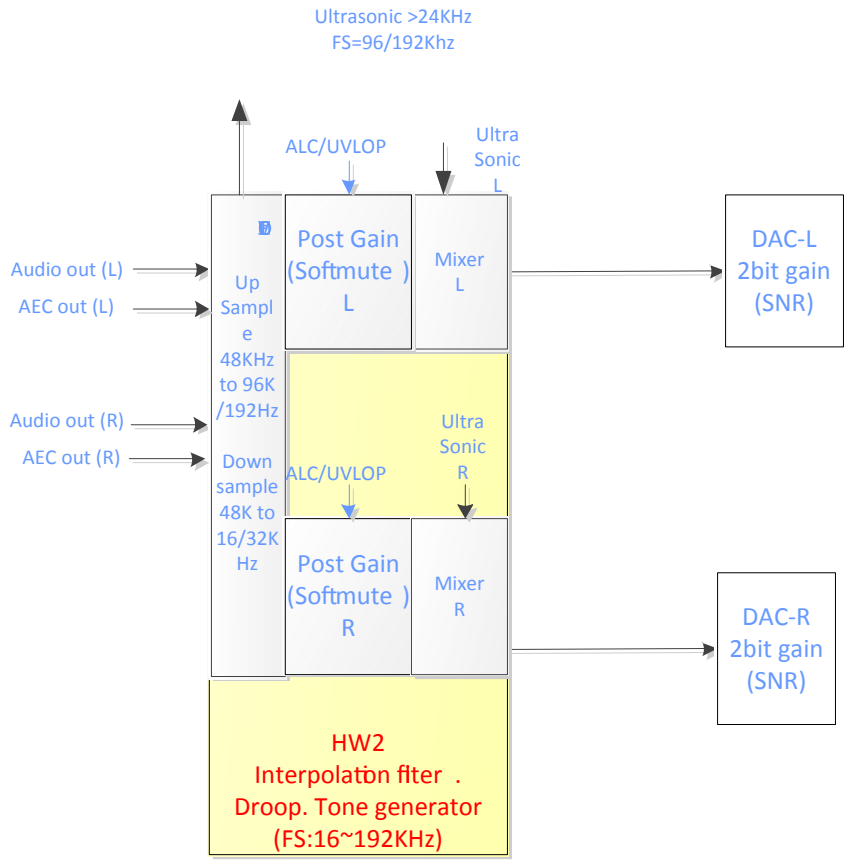


Table 9 HW2 block diagram

5.13.3 Hardware Engine 3 (HW3)

HW3 is placed between analog gain of voltage sense(V-Gain)/current sense(I-Gain) and Fusion-L/Fusion-R. it receives the processed V-Sense/I-Sense Data and can adjust the digital level by the V-Gain/I-Gain. Since the performance of I Sense is influenced by the

temperature. The HW3 will refer the Tj(junction temperature) from SARADC to compensate the I-Gain and output to Fusion-L/Fustion-R or the TDM0 for debug usage.

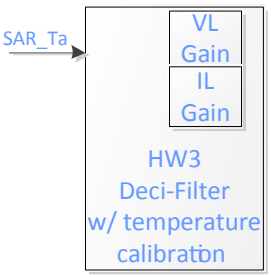


Table 10 HW3 block diagram

5.14 Automatic Level Control

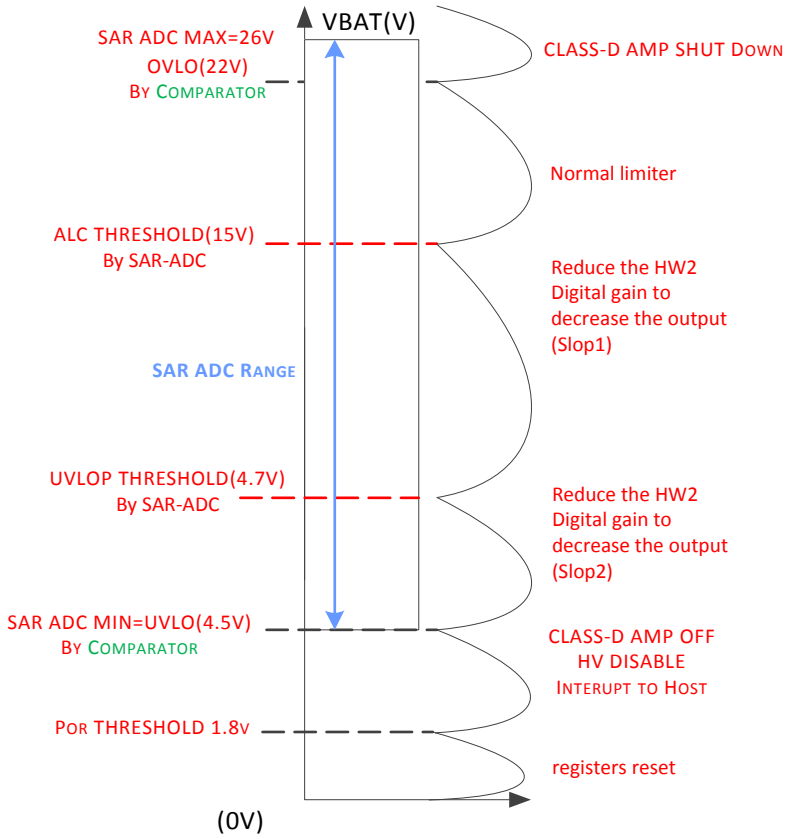


Table 11 NAU83G60 VBAT Threshold

The NAU83G60 employs several limit thresholds on the battery voltage VBAT. This limit threshold can be used to program gain changes in order to protect the system from shutting down or to prevent excessive current draw. On VBAT an ALC threshold between UVLO(4.5V) and OVLO(22V)can be programmed in order to adjust the digital gain when the battery voltage drops due to discharge. The ALC can reduce the output level in order to reduce the power consumed from the battery supply. See the NAU83G60 ALC section below

for more details. When the battery voltage drops further down an Under Voltage Lockout Prevention (UVLOP) threshold can be set between UVLO(4.5V) and ALCThreshold in order to limit the input current. This will prevent large currents from being drawn at low battery voltages as the device tries to supply the load and allow for the battery voltage to recover such that it does not approach the Under Voltage Lockout Threshold (UVLO). In addition, a second gain limiter can be activated to reduce the gain even further at a faster attack rate. The operation of this limiter will be described in this specification.

When the battery drops even further down despite the gain and current limiters, the class-D driver will shut down at the Under Voltage Lockout Threshold (UVLO) threshold of about 4.5V. If the VBAT drops even further below 1.8V then the device control and registers will reset.

On the VBST output, the NAU83G60 employs only two limits. The NAU83G60 VBST has an Over Voltage LockOut (OVLO) voltage of about 22V. If VBST reaches above this voltage, the class-D driver will shut down and the outputs will remain at ground until the VBST reaches below the OVLO threshold.

This section describes the various level control options based on the thresholds outlined above.

The digital Automatic Level Control (ALC) supports the input digital audio path of the NAU83G60 by providing an optimized signal level at the output of the Class-D Amplifier. This is achieved by automatically decreasing the amplitude of the input signal according to the user's set amplitude or low battery voltage, and restoring amplitude when conditions are lifted. Figure 10 illustrates the basic relationship of the ALC to other major functions of the NAU83G60. Since the VBAT may drop and recover suddenly by the content of music, NAU83G60 will provides several periods of de-bounce time to adjust additionally.

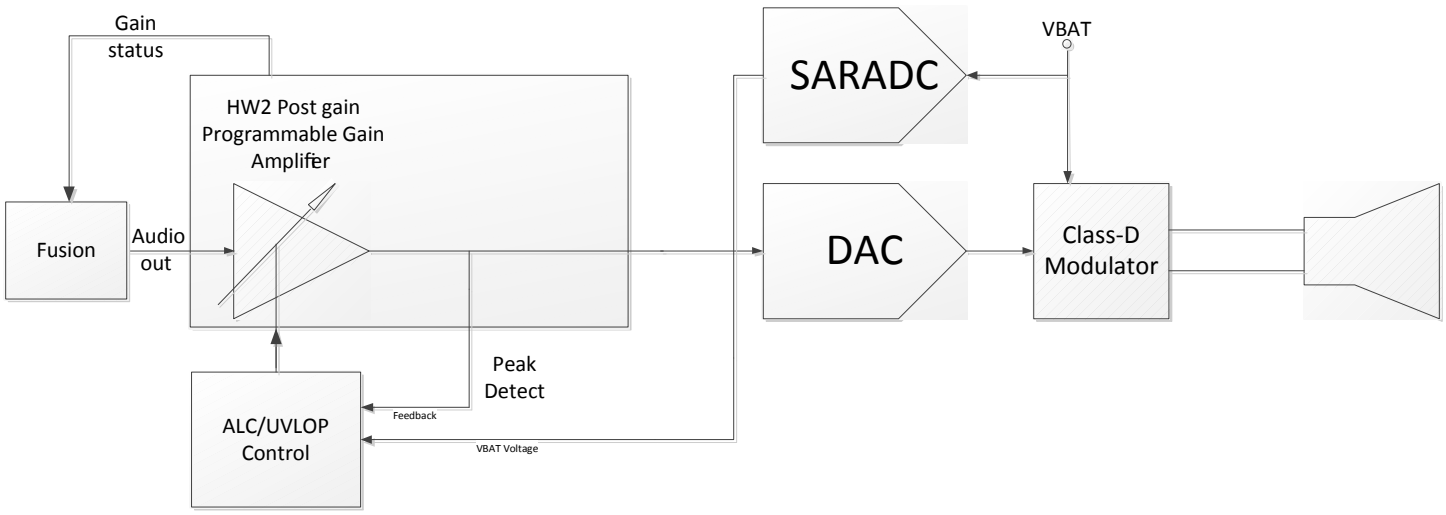


Figure 10 ALC / UVLOP Block Diagram

5.14.1 ALC Operation (TBD)

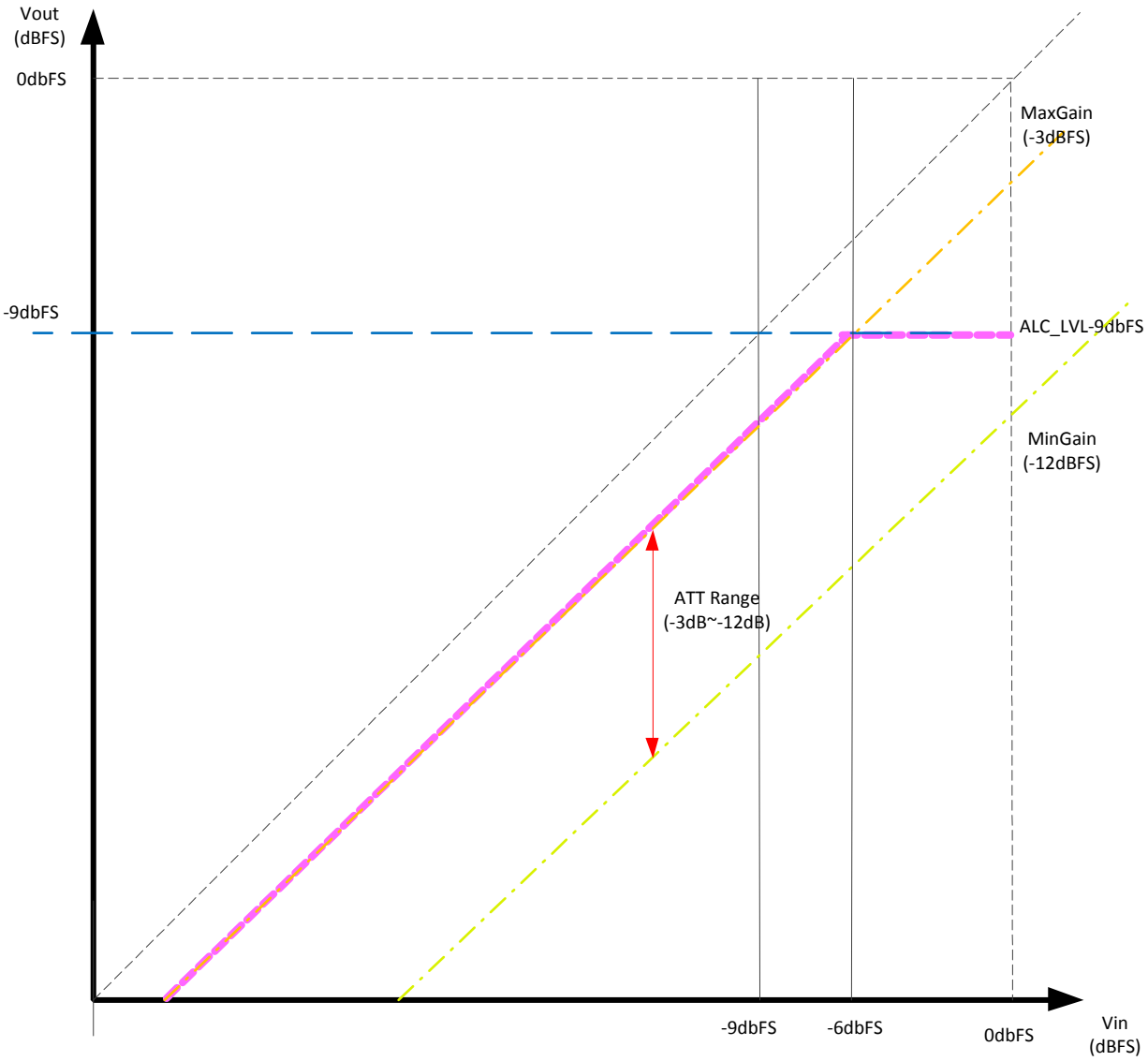


Figure 11 ALC / UVLOP Operation

The ALC is enabled by ALC_CTRL3.ALC_EN_REG0X2E[15] and operates according to the Limiter Mode register ERROR: REFERENCE SOURCE NOT FOUND.ERROR: REFERENCE SOURCE NOT FOUND REG0X2E[14:12]. It uses feedback to detect the signal output level from either the output of the digital Programmable Gain Amplifier (**dPGA**) or output of the soft mute gain compensation through a Peak Detector, set by ALC_CTRL4.PEAK_SEL_REG0X2F[13]. Using the output of the **dPGA** provides a direct feedback for control while using the output of the soft mute gain compensation allows for the ALC to adjust based on the activation of the soft mute, deactivating when the soft-mute function drops the signal below the user's set amplitude or reactivating when disabling the soft mute when signal rises above the set amplitude and/or clipping. More information can be read about the soft mute in Section 5.9.

The Peak Detector can be configured by either using a full-wave rectification peak, ensuring equal ALC operation on both positive and negative signals, or absolute value calculated peak, which updates at every peak and degrades until a new peak is detected. This is set in ALC_CTRL1.ALCPKSEL_REG0X2C[11]. Additionally, the ALC can update either from the zero crossing point of the signal or immediately upon triggering. This is determined by the register ALC_CTRL1.ALC_ZC_REG0X2C[14] and when enabled also overrides the register ALC_CTRL4.LPGAZC_REG0X2F[14] to ensure zero crossing point reference consistency. ALC updating on

the zero crossing point ensures that if the ALC responds faster than the signal degrades, the ALC will wait until the signal reaches close to zero before changing the gain on the **dPGA**, or input signal gain. This may be helpful depending on the application and can reduce popping on speakers. If immediate action is needed for input signal attenuation then **ALC_ZC** can be disabled. The ALC has three operational states: ALC *Attack*, ALC *Release*, and ALC *Hold*. In the ALC *Attack* state, the ALC decreases the **dPGA** gain at a single dB decrement at a time, gradually based on the **ALCATK** register; in the ALC *Release* state, the ALC increases the **dPGA** gain at a single dB increment at a time gradually based on the **ALCDCY** register; in the ALC *Hold* state, the ALC holds constant the **dPGA** gain for a specified time determined by the **ALCHLD** register. While the attack state is immediate upon meeting conditions, the ALC will enter the hold state before releasing the signal. This is to account for any noise or fluctuations that may occur on the input signal.

The registers below are used in every ALC operational mode that are defined in ERROR: REFERENCE SOURCE NOT FOUND.ERROR: REFERENCE SOURCE NOT FOUND_REG0X2E[14:12] .

- ALC_CTRL3.ALC_EN_REG0X2E[15] – ALC Enable Register, enables the ALC for operation.
- ALC_CTRL4.PEAK_SEL_REG0X2F[13] – Selects the feedback for peak detection from the output of the **dPGA** of which the ALC controls (1) or the soft mute gain compensation (0).
- ALC_CTRL1.ALCPKSEL_REG0X2C[11] – Selects between full-wave rectification peak (0) or absolute value calculated peak (1).
- ALC_CTRL1.ALC_ZC_REG0X2C[14] – Selects whether the ALC should update immediately at peak detection or at the zero crossing point of the signal. This is recommended as it prevents sudden changes that may occur.
- ALC_CTRL1.ALCMAXGAIN_REG0X2C[7:5] – The maximum gain level allowed to be set by the ALC on the **dPGA** when enabled. This is applied automatically when ALC is enabled and acts as the upper limit the input signal is allowed until ALC is disabled.
- ALC_CTRL1.ALCMINGAIN_REG0X2C[3:1] – The minimum gain level allowed to be set by the ALC on the **dPGA** when enabled. This acts as the lowest limit the input signal is allowed until the ALC is disabled.
- ALC_CTRL2.ALCDCY_REG0X2D[15:12] – The rate at which the ALC will *release*, or increase the gain of, the signal determined by step time doubling its increment from 2µs to 4196µs at 0.1875dB per step. Typically, the decay time is much slower than the attack time. When the DAC output level is below the ALC Target value by at least 1.5 dB, the gain increases at a rate determined by this parameter. In Limiter Mode, the time constants are faster than in ALC mode.
- ALC_CTRL2.ALCATK_REG0X2D[11:8] – The rate at which the ALC will *attack*, or attenuate, the signal determined by step time doubling its increment from 2µs to 4196µs at 0.1875dB per step. Typically, the attack time is much faster than the decay time. In the NAU83G60, when the absolute value of the DAC output exceeds the ALC Target Value **ALCLVL**, the gain will be reduced at a step-size and rate determined by this parameter. When the peak DAC output is at least 1.5 dB lower than the **ALCLVL**, the stepped gain reduction will halt.
- ALC_CTRL2.ALCHLD_REG0X2D[7:4] – The length of time at which the ALC will hold the signal for, ranging from 0ms to 512ms. Hold time refers to the duration of time when no action is taken. This is typically used to avoid undesirable sounds that can happen when an ALC responds too quickly to a changing input signal. In the NAU83G60, the hold time value is the duration of time that the ADC output peak value must be less than the target value, **ALCLVL**, before there is an actual gain increase.
- ALC_CTRL2.ALCLVL_REG0X2D[3:1] – A requirement for the input signal level to hold at after clearing the conditions specified in each of the ALC operational mode for the amount of time set in the **ALCHLD** register before entering the ALC Release state, or increase the gain of the **dPGA** at the rate specified by the **ALCDCY** register. This value is expressed as a fraction of Full Scale (FS) output from the DAC. Depending on the logic conditions, the output value used in the comparison may be either the instantaneous value of the DAC ***or*** a time weighted average of the DAC peak output level.

NOTE: See **Chapter 6 Control and Status Registers**: Registers 0x2C to 0x2F for more information regarding settings for ALC functions.

The following are different operational modes allowed by the **LIM_MDE** control register:

- Normal Limiting Mode
- Low-Battery Limiting Mode

- Low-Battery Limiting Mode with Preprogrammed VBAT Ratio

***NOTE*:** The gain range for the **dPGA** is restricted between **ALCMAXGAIN** and **ALCMINGAIN**. Upon enabling of the ALC, the **dPGA** is automatically set to the **ALCMAXGAIN** and when an ALC event triggers, the gain is adjusted according to the conditions as long as the target attenuation level is below the **ALCMAXGAIN** and above the **ALCMINGAIN** restrictions.

5.14.1.1 Normal Limiting Mode

Registers used in Normal Limiting Mode:

- **ALC_CTRL3.LIM_MDE_REG0X2E[14:12]=010** – ALC limiter mode set to **010** for operation based on user's set amplitude.

Description:

In **Normal Limiting Mode**, **ERROR: REFERENCE SOURCE NOT FOUND.ERROR: REFERENCE SOURCE NOT FOUND REG0X2E[14:12] =010,** a maximum DAC output level is programmed to limit the full scale output level. Immediately upon enable, the ALC will set the **dPGA** gain according to the **ALCMAXGAIN** value without delay or decay. The signal peak is read continuously until the level reaches above the user's set amplitude in the **ALCLVL** register. Upon overstepping the set amplitude, the ALC will enter the *Attack* state, lowering the **dPGA** gain at the pre-programmed rate specified in the **ALCATK** register until the peak detector returns a lower level than the **ALCLVL** register. When the input signal level becomes 1.5dBFS below the ALC target level (**ALCLVL** register), then the ALC enters *Hold* state, holding the **dPGA** gain for a specified time determined by the **ALCHLD** register. The ALC then goes into the *Release* state, increasing the **dPGA** gain at the pre-programmed rate specified in the **ALCDCY** register until the **dPGA** gain is at maximum or until the peak returns a level above the **ALCLVL** register, in which the ALC will be triggered and enter the *Attack* state again.

Example Problem Set: Limit maximum output to not exceed -3dBFS limit and update on the zero crossing point to prevent any spontaneous change in the signal. Limit the attenuation and release rate by a manageable amount to prevent any audible change.

Register Settings for problem set:

- **ALC_CTRL1.REG0X2C** = 0x***68E0***
  - [14] **ALC_ZC** set to update the ALC on the zero crossing point of the signal, so there is no instantaneous changes on the signal when ALC adjusts.
  - [11] **ALCPK_SEL** set to update Peak Detection on a calculated absolute value.
  - [7:5] **ALCMAXGAIN** set to 0dB. The absolute maximum gain that the **dPGA** is allowed. Upon enable, the ALC will immediately set the **dPGA** to this level and will restrict the *Release* state from going beyond this level.
  - [3:1] **ALCMINGAIN** set to -6dB. The absolute minimum gain that the **dPGA** is allowed. Upon enable, the ALC will restrict the *Attack* state from going beyond this level.
  - The rest is left at default.
- **ALC_CTRL2.REG0X2D** = 0x***5350***
  - [15:12] **ALCDCY** set to 16ms/step at 0.1875dB ***increase*** per step. Main occurrence in the ALC *Release* state. After each step the signal peak level is compared to the **ALCLVL** register. If the signal peak is ***lower***, then the ALC takes another step. If the signal peak is ***higher***, then the ALC enters the ALC *Attack* state. This setting is the recommended rate but can be adjusted to be faster or slower depending on user design.
  - [11:8] **ALCATK** set to 16us/step at 0.1875dB ***decrease*** per step. Main occurrence in the ALC *Attack* state. After each step the signal peak level is compared to the **ALCLVL** register. If the signal peak is higher, then the ALC takes another step. If the signal peak is lower, then the ALC enters the ALC *Hold* state. This setting is the recommended rate but can be adjusted to be faster or slower depending on user design.
  - [7:4] **ALCHLD** set to 32ms pause that occurs after the ALC *Attack* state where the ALC attenuates the signal based on the rate set in the **ALCATK** register. After occurring, the ALC will enter the ALC *Release* state. This setting is the recommended delay but can be adjusted to be faster or slower depending on user design.
  - [3:1] **ALCLVL** set to -3dBFS. The main component for ALC Normal Limiting Mode. This is the comparison level which triggers the state of the ALC to go into Attack, Release, or Hold as mentioned above.
  - The rest is left at default.
- **ALC_CTRL3.REG0X2E** = 0x***A010***
  - [15] **ALC_EN** is set to 1. This is the ALC Enable bit and should be the last register to write to ensure proper setup.

- [14:12] **LIM_MDE** is set to 010. This is set to Normal Limiting mode and follows the operation explained in the description portion of this section.
- The rest is left at default.

- ALC_CTRL4.REG0X2F = 0x***0020***
  - Left at default settings

The register settings above should be implemented as either part of or after the desired ON-sequence. To ensure proper sequence control, use I²C to write to each of the addresses in the following sequence from first to last: ***0x2C***, ***0x2D***, ***0x2E***. The register ***0x2E*** is written to last as it holds the enable bit and will ensure proper activation of the ALC.

5.14.1.2 Low Battery Limiting Mode

Registers used in Low Battery Limiting Mode:

- ALC_CTRL3.LIM_MDE_REG0X2E[14:12]=011 – ALC limiter mode set to **011** for operation based on low battery mode.
- ALC_CTRL3.VBAT_THRESHOLD_REG0X2E[9:5] – VBAT threshold value as the condition for ALC activation within **LIM_MDE** = 011 and 100. The available values range from 3.14V (1111) to 4.61V (0000) at ~0.10V to 0.11V steps. For exact values, please refer to the Section 6.5, the Control Register List.

Description:

In **Low-Battery Limiting Mode**, ALC_CTRL3.LIM_MDE_REG0X2E[14:12]=011, a maximum DAC output level is programmed to limit the full scale output level with the additional constraint of low-battery activation. Immediately upon enable, the ALC will set the **dPGA** gain according to the **ALCMAXGAIN** value without delay or decay.

The ALC activates when the VBAT voltage declines below the set value in the **VBAT_THRESHOLD** register. The signal peak is read continuously until the level reaches above the user's set amplitude in the **ALCLVL** register. Upon overstepping the set amplitude, the ALC will enter the *Attack* state, lowering the **dPGA** gain at the pre-programmed rate specified in the **ALCATK** register until the peak detector returns a lower level than the **ALCLVL** register.

When the input signal level becomes 1.5dBFS below the ALC target level (**ALCLVL** register), then the ALC enters *Hold* state, holding the **dPGA** gain for a specified time determined by the **ALCHLD** register. The ALC then goes into the *Release* state, increasing the **dPGA** gain at the pre-programmed rate specified in the **ALCDCY** register until the **dPGA** gain is at maximum or until the peak returns a level above the **ALCLVL** register, in which the ALC will be triggered and enter the *Attack* state again.

If VBAT were to be recharged at any given moment, the ALC will cease triggering and return to an idle state until VBAT lowers its level below the **VBAT_THRESHOLD** register again.

Example Problem Set: When battery becomes discharged lower than 3.53V, limit maximum output to not exceed -3dBFS limit to lessen battery discharge. Additionally, update on the zero crossing point to prevent any spontaneous change in the signal. Limit the attenuation and release rate by a manageable amount to prevent any audible change.

Register Settings for problem set:

- ALC_CTRL1.REG0X2C = 0x***68E0***
  - [14] **ALC_ZC** set to update the ALC on the zero crossing point of the signal, so there is no instantaneous changes on the signal when ALC adjusts.
  - [11] **ALCPK_SEL** set to update Peak Detection on a calculated absolute value.
  - [7:5] **ALCMAXGAIN** set to 0dB. The absolute maximum gain that the **dPGA** is allowed. Upon enable, the ALC will immediately set the **dPGA** to this level and will restrict the *Release* state from going beyond this level.
  - [3:1] **ALCMINGAIN** set to -6dB. The absolute minimum gain that the **dPGA** is allowed. Upon enable, the ALC will restrict the *Attack* state from going beyond this level.
  - The rest is left at default.
- ALC_CTRL2.REG0X2D = 0x***5350***
  - [15:12] **ALCDCY** set to 16ms/step at 0.1875dB ***increase*** per step. Main occurrence in the ALC *Release* state. After each step the signal peak level is compared to the **ALCLVL** register. If the signal peak is ***lower***, then the ALC takes

another step. If the signal peak is ***higher***, then the ALC enters the ALC *Attack* state. This setting is the recommended rate but can be adjusted to be faster or slower depending on user design.

- [11:8] **ALCATK** set to 16us/step at 0.1875dB ***decrease*** per step. Main occurrence in the ALC *Attack* state. After each step the signal peak level is compared to the **ALCLVL** register. If the signal peak is higher, then the ALC takes another step. If the signal peak is lower, then the ALC enters the ALC *Hold* state. This setting is the recommended rate but can be adjusted to be faster or slower depending on user design.
- [7:4] **ALCHLD** set to 32ms pause that occurs after the ALC *Attack* state where the ALC attenuates the signal based on the rate set in the **ALCATK** register. After occurring, the ALC will enter the ALC *Release* state. This setting is the recommended delay but can be adjusted to be faster or slower depending on user design.
- [3:1] **ALCLVL** set to -3dBFS. The main component for ALC Normal Limiting Mode. This is the comparison level which triggers the state of the ALC to go into Attack, Release, or Hold as mentioned above.
- The rest is left at default.

- ALC_CTRL3.REG0X2E = 0x***B2D0***
  - [15] **ALC_EN** is set to 1. This is the ALC Enable bit and should be the last register to write to ensure proper setup.
  - [14:12] **LIM_MDE** is set to 011. This is set to Low Battery Limiting mode and follows the operation explained in the description portion of this section.
  - [9:5] **VBAT_THRESHOLD** is set to 3.53V for ALC activation at this voltage.
  - The rest is left at default.
- ALC_CTRL4.REG0X2F = 0x***0020***
  - Left at default settings

The register settings above should be implemented as either part of or after the desired ON-sequence. To ensure proper sequence control, use I^2C to write to each of the addresses in the following sequence from first to last: ***0x2C***, ***0x2D***, ***0x2E***. The register ***0x2E*** is written to last as it holds the enable bit and will ensure proper activation of the ALC.

5.14.1.3 Low Battery Limiting Mode with Pre-programmed VBAT Ratio

Registers used in Low Battery Limiting Mode with Pre-programmed VBAT Ratio:

- ALC_CTRL3.LIM_MDE_REG0X2E[14:12]=100 – ALC limiter mode set to **100** for operation based on a split operation, #1 or #2, between above or below VBAT threshold, respectively. Operation 1: Normal Limiting Mode as specified in 5.14.1.1. Operation 2: ALC Target Level follows a ratio of the sense VBAT voltage. More information of the two modes can be found in the description of this section.
- ALC_CTRL3.VBAT_THRESHOLD_REG0X2E[9:5] – VBAT threshold value as the condition for ALC activation within **LIM_MDE** = 011 and 100. The available values range from 3.14V (1111) to 4.61V (0000) at ~0.10V to 0.11V steps. For exact values, please refer to the Section 6.5, the Control Register List.
- ALC_CTRL3.VBAT_RATIO_REG0X2E[11:10] – VBAT ratio, an additional setting only used for LIM_MDE=100. This changes the ALC output level based on the sensed VBAT voltage.

Description:

In **Low-Battery Limiting Mode with Preprogrammed VBAT Ratio,** ALC_CTRL3.LIM_MDE_REG0X2E[14:12]=100**,** there are two modes within its operation, one above the VBAT Threshold and another below the VBAT Threshold, in which the threshold can be set in the **VBAT_THRESHOLD** register. Above the VBAT Threshold (Operation 1), the ALC functions the same as Normal Limiting Mode as specified in 5.14.1.1. Below the VBAT Threshold (Operation 2), the maximum DAC output level is programmed to attenuate the full scale output level based on the ratio, specified in the **VBAT_RATIO** register, of the **VBAT_THRESHOLD,** also in its own register, minus the sensed VBAT voltage. The equation describing this operation is shown below:

$$V_{out} = V_{out\,(VBAT > VBAT_{threshold})} - \left[RATIO_{VBAT} * \left(VBAT_{threshold} - V_{BAT} \right) \right]$$

The output voltage, V_{rms}, is determined by the VBAT acquired when VBAT is greater than the threshold voltage, minus by the ratio multiplied by the difference of threshold voltage and current VBAT voltage. The ALC activates when the VBAT voltage declines below the set value in the **VBAT_THRESHOLD** register. Before the activation, the peak voltage of the output is recorded from the peak detector and used for the variable $V_{out(VBAT>VBATthreshold)}$ in the equation above. Immediately upon activation, the ALC will enter the *Attack* state, lowering the **dPGA** gain by the pre-programmed rate specified in the **ALCATK** register until the peak detector returns a level lower

or equal to the *Vout* described in the equation above where *Vout* is the representation of the output ALC level. This level can be calculated from the equation below and is rounded to the nearest whole number:

$$ALC\ Attenuation\ Level = 20\log\left(\frac{V_{out}}{V_{out\,(VBAT>VBAT_{threshold})}}\right)$$

Take note that the ALC attenuation occurs at incremental steps of 1dB and thus the steps can be accurately calculated if the V_{out} is known. If the input signal extends beyond *Vout* while the VBAT voltage is lower than the VBAT Threshold, the ALC enters the ALC *Attack* state, lowering the **dPGA** gain at the pre-programmed rate set in the **ALCATK** register. This continues until the DAC output level has been reduced to below the limit threshold. This limits DAC clipping if there is a sudden increase in the input signal level. During the whole of Operation 2, while the VBAT is charging and the ALC has been activated, the ALC will remain at its current gain level until VBAT has increased above **VBAT_Threshold**. An example of this is when VBAT starts at 3.6V, while **VBAT_Threshold** is 3.4V, and drops to 2.7V, this is theoretically enough make the ALC gain at -1dB when there's constant input, i.e. music or a wave. When the VBAT is being charged, the ALC gain will remain at -1dB until the VBAT is above 3.4V.

NOTE: The maximum gain at full scale input is set by the ALC Target Level, **ALCLVL**.

Example Problem Set: When battery becomes discharged lower than 3.93V, limit maximum output to not exceed -3dBFS limit to lessen battery discharge. Additionally, update on the zero crossing point to prevent any spontaneous change in the signal. Limit the attenuation and release rate by a manageable amount to prevent any audible change.

Register Settings for problem set:

- **ALC_CTRL1.REG0X2C** = 0x***68E0***
  - [14] **ALC_ZC** set to update the ALC on the zero crossing point of the signal, so there is no instantaneous changes on the signal when ALC adjusts.
  - [11] **ALCPK_SEL** set to update Peak Detection on a calculated absolute value.
  - [7:5] **ALCMAXGAIN** set to 0dB. The absolute maximum gain that the **dPGA** is allowed. Upon enable, the ALC will immediately set the **dPGA** to this level and will restrict the *Release* state from going beyond this level.
  - [3:1] **ALCMINGAIN** set to -6dB. The absolute minimum gain that the **dPGA** is allowed. Upon enable, the ALC will restrict the *Attack* state from going beyond this level.
  - The rest is left at default.
- **ALC_CTRL2.REG0X2D** = 0x***5350***
  - [15:12] **ALCDCY** set to 16ms/step at 0.1875dB ***increase*** per step. Main occurrence in the ALC *Release* state. After each step the signal peak level is compared to the **ALCLVL** register. If the signal peak is ***lower***, then the ALC takes another step. If the signal peak is ***higher***, then the ALC enters the ALC *Attack* state. This setting is the recommended rate but can be adjusted to be faster or slower depending on user design.
  - [11:8] **ALCATK** set to 16us/step at 0.1875dB ***decrease*** per step. Main occurrence in the ALC *Attack* state. After each step the signal peak level is compared to the **ALCLVL** register. If the signal peak is higher, then the ALC takes another step. If the signal peak is lower, then the ALC enters the ALC *Hold* state. This setting is the recommended rate but can be adjusted to be faster or slower depending on user design.
  - [7:4] **ALCHLD** set to 32ms pause that occurs after the ALC *Attack* state where the ALC attenuates the signal based on the rate set in the **ALCATK** register. After occurring, the ALC will enter the ALC *Release* state. This setting is the recommended delay but can be adjusted to be faster or slower depending on user design.
  - [3:1] **ALCLVL** set to -3dBFS. The main component for ALC Normal Limiting Mode. This is the comparison level which triggers the state of the ALC to go into Attack, Release, or Hold as mentioned above.
  - The rest is left at default.
- **ALC_CTRL3.REG0X2E** = 0x***B5D0***
  - [15] **ALC_EN** is set to 1. This is the ALC Enable bit and should be the last register to write to ensure proper setup.
  - [14:12] **LIM_MDE** is set to 011. This is set to Low Battery Limiting mode and follows the operation explained in the description portion of this section.
  - [11:10] **VBAT_RATIO** is set to 2:1 to lower the input signal gain following this linear pattern based on VBAT. As VBAT lowers, the input signal gain will also lower by this amount in 1dB increments.
  - [9:5] **VBAT_THRESHOLD** is set to 3.93V for ALC activation at this voltage.

- The rest is left at default.

- ALC_CTRL4.REG0X2F = 0x***0020***
  - Left at default settings

The register settings above should be implemented as either part of or after the desired ON-sequence. To ensure proper sequence control, use I²C to write to each of the addresses in the following sequence from first to last: ***0x2C***, ***0x2D***, ***0x2E***. The register ***0x2E*** is written to last as it holds the enable bit and will ensure proper activation of the ALC.

The input and output waveforms for ALC during limiter operation are shown in **Figure 12** and **Figure 13.** The waveforms during ALC limiter operation as the gain is reduced are shown in **Figure 12**, while the input and output waveforms during ALC limiter operation as the gain is released are shown in **Figure 13**.

MEASURED WAVEFORM TBD

Figure 12 ALC Limiter Waveforms (Gain Reduced)

MEASURED WAVEFORM TBD

Figure 13 ALC Limiter Waveforms (Gain Released)

5.14.1.4 Under Voltage Lock Out Prevention Limiter

The NAU83G60 incorporates another battery voltage dependent gain limiter, which can be used independently from the digital ALC described above. It does share the same VBAT threshold setting as the boost current limiter. This additional limiter can be used to prevent the system from reaching the Under Voltage Lock Out threshold of 2.4V. Hence, this limiter is referred to as the Under Voltage Lock Out Prevention limiter (UVLOP limiter). The UVLOP limiter provides an attenuation directly at the modulator inputs, allowing for minimal group delay. The gain can be attenuated from 0 to -15.5dB in 0.5dB steps. However, up to 2 dB attack steps can be chosen. The block diagram of the UVLOP Gain Limiter is shown below.
The UVLOP limiter is enabled by setting UVLO_CTRL0[11] (ENABLE_UVLOP) to 1. When the battery voltage VBAT goes below the threshold set in ANALOG_CTRL_8[7:4], the UVLOP limiter will start to attenuate the output signal at the attack rate set in UVLO_CTRL0.UVLOP_ATK and the gain step set in UVLO_CTRL0.UVLOP_STEP. The UVLOP limiter attenuations stops at the minimum gains set in UVLO_CTRL1.UVLOP_ATTN. Once the battery voltage recovers above the threshold, the UVLOP limiter will gain up the signal back to 0dB after a hold time UVLO_CTRL0.UVLOP_HLD and using a release step time of UVLO_CTRL0.UVLOP_RLS.

Figure 14 UVLOP Gain Limiter

5.14.2 Example ALC Values ALC Hold Time

Input signals with different characteristics (such as voice vs. music) may require different settings of the ALC Hold Time parameter for optimum performance. A shorter Hold Time may be useful in voice applications where a faster reaction time helps adjust the volume setting for speakers with different volumes. **Figure 15** shows ALC Input and Output waveforms when no Hold Time is set.

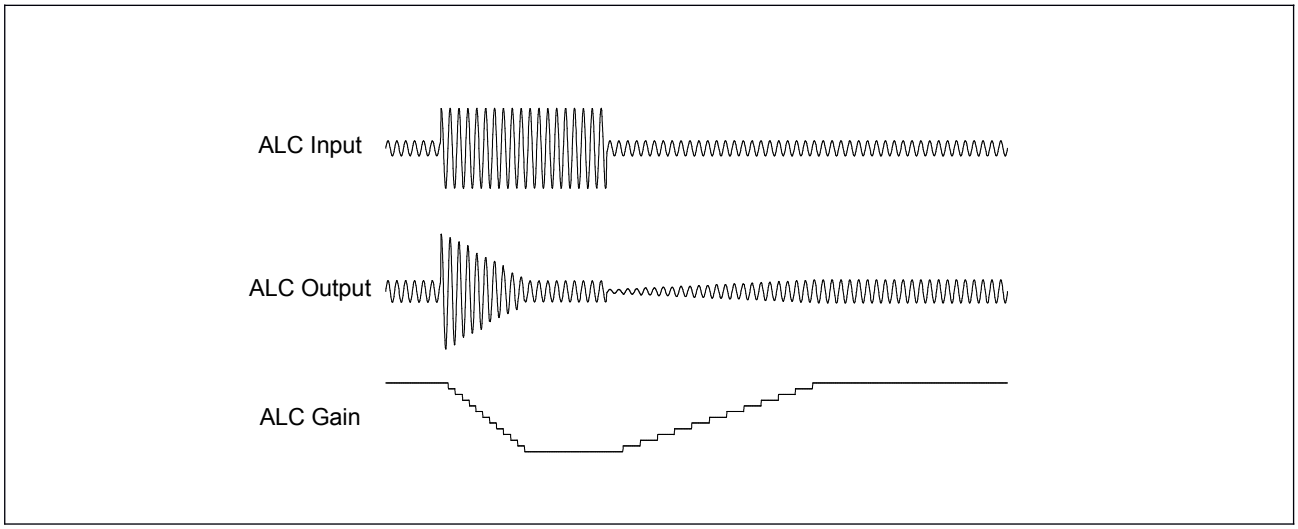


Figure 15 ALC Operation without Hold Time

Increasing the ALC Hold Time prevents the ALC from reacting too quickly to brief periods of silence such as those that may occur in music recordings. ***Figure 16*** shows ALC Input and Output waveforms when a Hold Time has been set. The Hold Time parameter is set in the **Error: Reference source not found Error: Reference source not found REG0x2D[7:4]**. In the example, a Hold Time of 16 msec has been set.

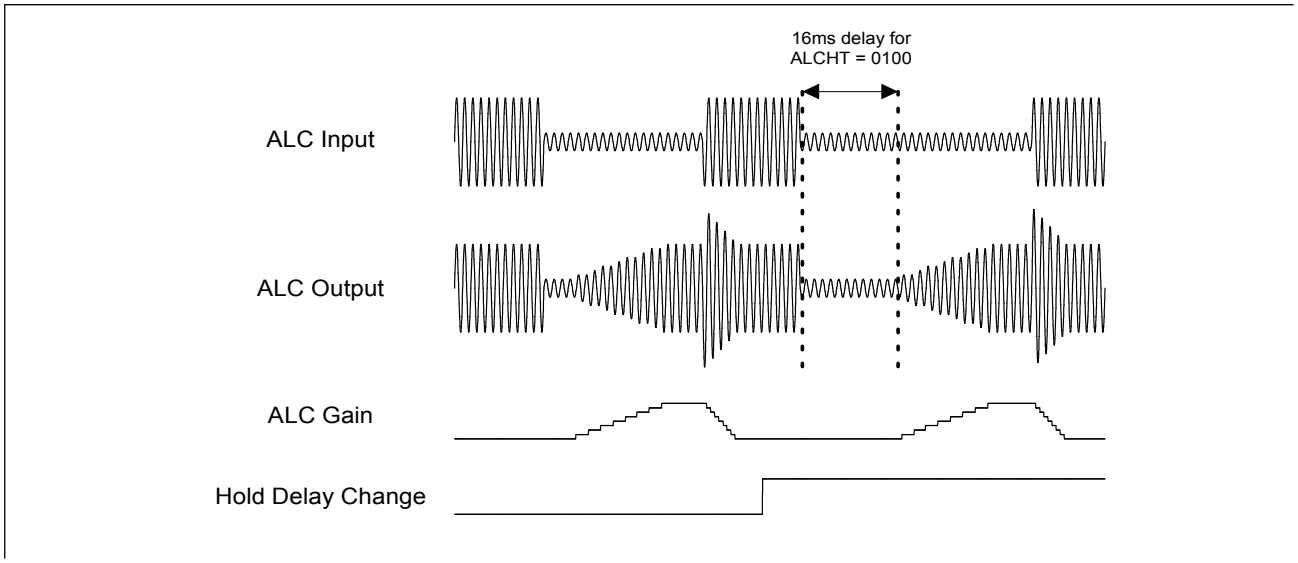


Figure 16 ALC Operation with Hold Time

5.15 Device Protection

The NAU83G60 includes the following types of device protection:

- Over Current Protection (OCP)
- Supply Over Voltage Protection (OVLP)
- Under Voltage Lock Out (UVLO)
- Over Temperature Protection (OTP)
- Clock Termination Protection (CTP)

Over Current Protection is provided in the NAU83G60. If a short circuit is detected on any of the pull-up or pull-down devices on the output drivers for at least 16.7 µsec, the output drivers will be disabled for 100 msec. The output drivers will then be enabled again and checked for the short circuit. If the short circuit is still present, the output drivers are disabled after 16.7 µsec. This cycle will continue until the short circuit is removed. The short circuit threshold is 4.0 A at 3.6 V.

Supply Over Voltage Protection (OVLP) is provided in the NAU83G60. If the VBAT supply voltage reaches 22V, the output drivers will be set to pull down to ground while the NAU83G60 control circuitry continues to operate. If the supply drops below 20V, the output drivers are re-enabled.

Under Voltage Lock Out (UVLO) provides Supply Under Voltage Protection in the NAU83G60. If the VBAT supply voltage drops below 4.7V, the output drivers will be disabled while the NAU83G60 control circuitry continues to operate. This will prevent the battery supply from going too low before the host processor can safely shut down the devices on the system. If the supply goes back up, the drivers will be enabled again at 4.9V. If the supply drops further (below 4.5 V), the internal power-on reset is activated and puts the entire device into the power-down state.

Over Temperature Protection (OTP) is provided in the event of thermal overload. When the internal junction temperature of the device reaches 135°C, the NAU83G60 will disable the output drivers. When the device cools down and a safe operating temperature of 120°C has been achieved for at least 100 usec, the output drivers will be enabled again.

Clock Termination Protection (CTP) is provided in the NAU83G60. If the clock stops running, the NAU83G60 automatically shuts down the Class-D driver and Boost converter if Clock Detection is enabled (see clock detection section).

5.16 Power-up and Power-Down Control

When the supply voltage ramps up, the internal power on reset circuit is triggered. At this time, all internal circuits will be set to the power-down state. The device can be enabled by initializing the registers and starting the clocks. Upon starting the clocks, the device will go through an internal power-up sequence in order to minimize 'pops' on the speaker output. The complete power-up sequence requires about 4 msec. The device will power down in about 30 µsec, when the clocks are stopped.

NOTE: It is important to keep the input signal at zero amplitude or enable the mute condition in order to minimize the 'pops' when the clocks are stopped.

5.17 Bypass Capacitors

Bypass capacitors are required to remove the AC ripple on the VDD pins. The value of these capacitors depends on the length of the VDD trace. In most cases, 10 µF and 0.1 µF are sufficient to achieve good performance.

5.18 Printed Circuit Board Layout Considerations

Good Printed Circuit Board (PCB) layout and grounding techniques are essential to achieve good audio performance. It is better to use low-resistance traces as these devices are driving low impedance loads. The resistance of the traces has a significant effect on the output power delivered to the load. In order to dissipate more heat, use wide traces for the power and ground lines.

5.18.1 Recommended PCB Footprint (TBD)

The recommended footprint for the PCB layout for the NAU83G60 is provided in **Figure 17**, as viewed from the top of the pcb.

Figure 17 Recommended PCB Footprint

5.18.2 PCB Layout Notes

Given the efficiency of the Boost Converter and the Class-D Amplifier, this requires up to 6 Amperes of peak current through the boost converter inductor. The Boost Converter and the Class-D Amplifier are both high power switching circuits that can cause Electro Magnetic Interference (EMI) when they are poorly connected. Therefore, care must be taken to design the PCB eliminate Electro Magnetic Interference (EMI), reduce IR drops, and maximize heat dissipation.

The following notes are provided to assist product design and enhance product performance:

- Use a VSS plane, preferably on both sides, to shield clocks and reduce EMI
- Maximize the copper to the VSS balls and have solid connections to the plane
- Planes on VBAT&AVCC, IOVDD & DVDD are optional
- The VBAT connection needs to be a solid piece of copper
- Use thick copper options on the supply layers if cost permits
- Use 2Mil copper or plated copper on the top layer
- Place the VBAT decoupling capacitor close to the other side of the inductor
- Use a big VIA outside the NAU83G60 to connect the VBAT balls in parallel with the inner trace
- Keep the speaker connections short and thick. Do not use VIAs
- Use a small speaker connector like a wire terminal block (Phoenix Contact)
- Keep the VREF capacitor close to the ball and shielded from the inductor
- For better heat dissipation, use ball VIAs to conduct heat to the other side of the PCB
- Do not use VIA's to connect L1, C1, C2, C3, SPK+ & SPK- to U1. Use a direct top layer copper connection to the balls. Thick copper is preferred.
- Use large or multiple parallel VIAs to decoupling capacitors when connecting to a ground plane
- The digital IO lines can be shielded between power planes
- The ground return of D0 should run separately back to the NAU83G60
- For the traces that run between the balls, follow the guidelines listed in **Figure 17** and see the example illustrated in **Figure 18.**

Figure 18 Layout Traces Example

5.19 Filters

The NAU83G60 is designed for use without any filter on the output line. However, the NAU83G60 may be used with or without various types of filters, depending on the needs of the application.

5.19.1 Class D without Filters

The NAU83G60 is designed for use without any filter on the output line. That means the outputs can be directly connected to the speaker in the simplest configuration. This type of filter-less design is suitable for portable applications where the speaker is very close to the amplifier. In other words, this is preferable in applications where the length of the traces between the speaker and amplifier is short. **Figure 19** illustrates this simple configuration.

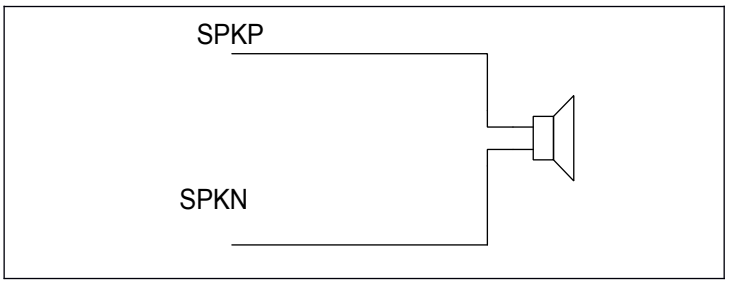


Figure 19 NAU83G60 Speaker Connections without Filter

5.19.2 Class D with Filters

In some applications, shorter trace lengths are not possible because of speaker size limitations and other layout reasons. In these applications, long traces will cause EMI issues. Several types of filter circuits are available to reduce the EMI effects. These are Ferrite Bead Filters, LC filters, Low-Pass LCR Filters, and High-Pass Filters.

Ferrite Bead Filters are used to reduce high-frequency emissions. The characteristic of a Ferrite Bead Filter is such that it offers higher impedance at high frequencies. For better EMI performance, select a Ferrite Bead Filter which offers the highest impedance at high frequencies, so that it will attenuate the signals at higher frequencies. The typical circuit diagram using a Ferrite Bead Filter for each output to the speaker is shown **Figure 20**.

NOTE: Usually, the ferrite beads have low impedance in the audio range, so they will act as pass-through filters in the audio frequency range.

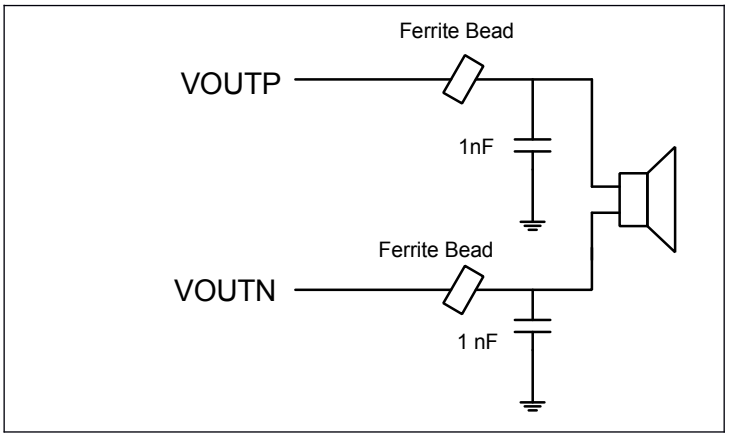


Figure 20 NAU83G60 Speaker Connections with Ferrite Bead Filters

LC Filters are used to suppress low-frequency emissions. The diagram in **Figure 21** shows the NAU83G60 outputs connected to the speaker with an LC Filter circuit. R_L is the resistance of the speaker coil.

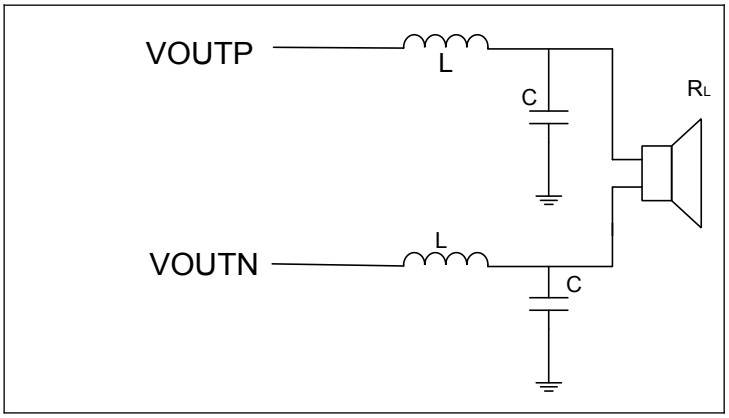


Figure 21 NAU83G60 Speaker Connections with LC Filters

Low-Pass LCR Filters may also be useful in some applications where long traces or wires to the speakers are used. **Figure 22** shows the speaker connections using standard Low-Pass LCR Filters.

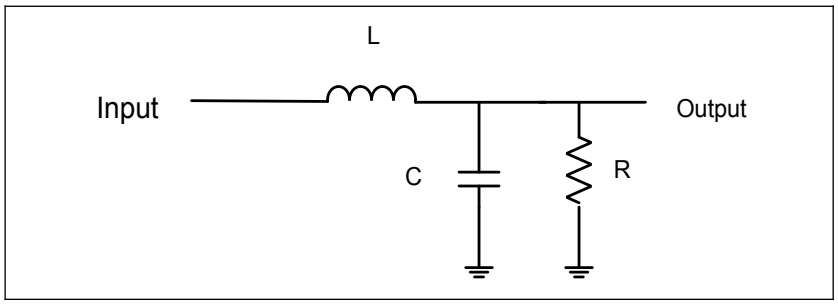


Figure 22 NAU83G60 Speaker Connections with Low-Pass Filters

The following equations apply for critically damped (ζ = 0.707) standard Low-Pass LCR Filters:

$$2\pi f c = \frac{1}{\sqrt{(LC)}} \quad f c \text{ is the cut-off frequency}$$

$$\zeta = 0.707 = \frac{1}{2R} * \sqrt{\frac{L}{C}}$$

NOTE: The L and C values for differential configuration can be calculated by duplicating the single-ended configuration values and substituting RL = 2R.

High-Pass Filters may also be useful in some applications. There is a High-Pass Filter for each ADC Channel and each DAC Channel. The High-Pass Filters may be enabled by setting **HPF_EN REG0X12[15}, [13],** and **[5].** The High-Pass Filter has two operation modes that apply to both channels simultaneously. In the Audio Mode, the filter is a simple first-order DC blocking filter, with a cut-off frequency of 3.7 Hz. In the Application-Specific Mode, the filter is a second-order audio frequency filter, with a programmable cut-off frequency. The programmable filter mode may be enabled by setting **HPF_APP REG0X12[14], [9],** and **[4].**

Table 12 identifies the cut-off frequencies with different sample rates.

Table 12 High-Pass Filter Cut-Off Frequencies

HPFCUT	Sample Rate in KHz (FS)							
	REG_SRATE= 3'b000		REG_SRATE= 3'b001		REG_SRATE= 3'b010		REG_SRATE= 3'b011	
	8	12	16	24	32	48	64	96
000	87	130	87	130	87	130	87	130
001	103	155	103	155	103	155	103	155
010	132	198	132	198	132	198	132	198
011	165	248	165	248	165	248	165	248
100	207	311	207	311	207	311	207	311
101	265	398	265	398	265	398	265	398
110	335	503	335	503	335	503	335	503
111	409	614	409	614	409	614	409	614

6 Control and Status Registers (TBD)

The NAU83G60 includes an I2C Control Interface as well as two I2S/PCM Audio Interface. The following sections describe the Control and Audio Interfaces and registers.

6.1 Digital Control Interface

The NAU83G60 uses two I2C/SPI Interface with pin programmable (GPIO1, GPIO2) addresses. The I2C address = 0x1A, 0x1B, 0x4A, 0x4B.

6.2 Digital Audio Interface

The NAU83G60 can be configured as either the Master or the Slave, by setting register Error: Reference source not found Error: Reference source not found **REG0XE[3]** to 1 for Master Mode or setting it to 0 for Slave Mode. Slave Mode is the default if this bit is not written. In Master Mode, NAU83G60 outputs both Frame Sync (FS) and the audio data Bit Clock (BCLK) and has full control of the data transfer. In Slave Mode, an external controller supplies BCLK and FS. Data is latched on the rising edge of BCLK; and ADCOUT clocks out ADC data, while DACIN clocks in data for the DACs.

When not transmitting data, ADCOUT pulls LOW in the default state. Depending on the application, the output can be configured to pull up or pull down. When the Time Slot function is enabled, there are additional output state modes, including controlled tri-state capability (see **Section 9.2.9**).

The NAU83G60 has two DAC channel and four ADC channels. The ADC left and right channel data could be swapped in the I2S Interface by setting register **Error: Reference source not found Error: Reference source not found** **REG0XD[5]** to 1.

WHEN Error: Reference source not found Error: Reference source not found **REG0X28[15]** or Error: Reference source not found Error: Reference source not found **REG0X28[7]** is set to 1, the I2S Interface ADC path will transmit normal audio data . If both of them are set to 0, the ADC path will transmit I/V Sense data and SAR ADC data, which could be in either signed or unsigned format by setting **Error: Reference source not found Error: Reference source not found REG0XC[9]** to be 0 or 1, respectively. The I2S Interface DAC path will transmit normal audio data at any situation.

The NAU83G60 supports four port data lengths: 16, 20, 24, and 32 bits by setting **Error: Reference source not found Error: Reference source not found REG0XD[3:2]** The chip also supports 8-bit word length for Compounding Mode operation by setting **Error: Reference source not found Error: Reference source not found REG0XD** to 1.

The NAU83G60 supports ten audio formats: I2S, Right Justified, Left Justified, TDM I2S, TDM Right Justified, TDM Left Justified, PCM A, PCM B, PCM Offset, and PCM Time Slot.

When operated in the TDM I2S, TDM Right Justified, or TDM Left Justified mode and in all PCM modes, the NAU83G60 supports 8-channel data transmission on both ADC and DAC paths simultaneously. **Error: Reference source not found Error: Reference source not found REG0XC[15]** should be set = 1 if using TDM I2S, TDM Right Justified, or TDM Left Justified modes.

Table 13 Digital Audio Interface Mode Settings

PCM Mode	Error: Reference source not found ERROR: REFERENCE SOURCE NOT FOUND REG0XD[1:0]	Error: Reference source not found ERROR: REFERENCE SOURCE NOT FOUND REG0XD[6]	Error: Reference source not found ERROR: REFERENCE SOURCE NOT FOUND REG0XE[10]	Error: Reference source not found ERROR: REFERENCE SOURCE NOT FOUND REG0XC[14]
Right Justified	00	0	0	0
Left Justified	01	0	0	0
I2S	10	0	0	0
PCM A	11	0	0	0
PCM B	11	1	0	0
PCM Offset	11	Don't care	0	1
PCM Time Slot	11	Don't care	1	0

6.2.1 Left-Justified Audio Data

In Left-Justified Mode, the MSB is clocked on the first BCLK rising edge after the FS transitions. When FS is HIGH, Channel 0 data are transmitted; when FS is LOW, Channel 1 data are transmitted. This can be seen in **Figure 23**.

Figure 23 Left-Justified Audio Data

6.2.2 I2S Audio Data

In I2S Mode, the MSB is clocked on the second BCLK rising edge after the FS transitions. When FS is LOW, Left Channel data are transmitted; when FS is HIGH, Right Channel data are transmitted. This can be seen in **Figure 24.** Note: In standard I2S mode the V-sense channel has one sample delay with respect to the I-sense channel.

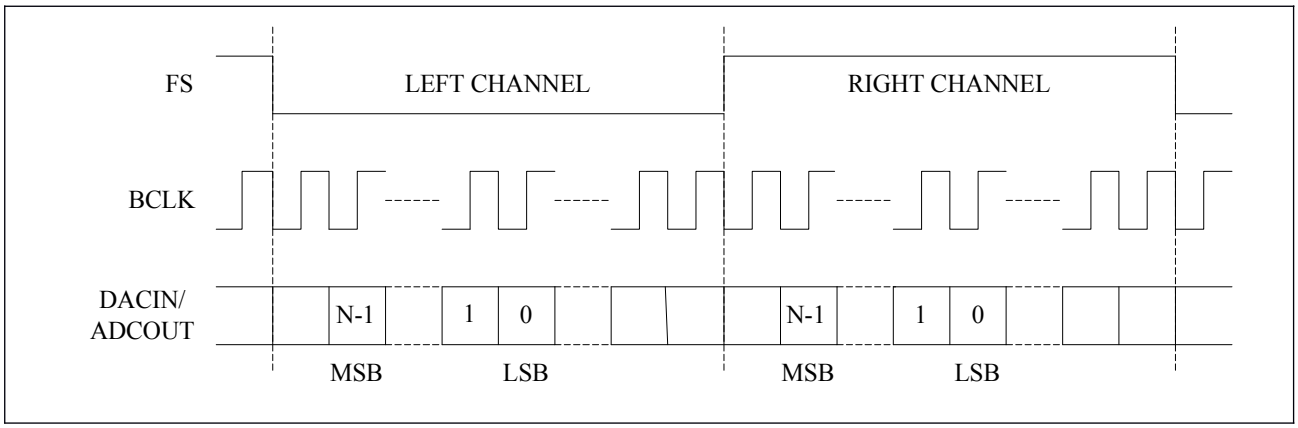


Figure 24 I2S Audio Data

6.2.3 TDM Left-Justified Audio Data

In TDM Left-Justified Mode, the MSB is clocked on the first BCLK rising edge after the FS transitions. When FS is LOW, Channel 1 data are transmitted, then Channel 3, 5, and 7 data are transmitted; when FS is HIGH, Channel 0 data are transmitted, then Channel 2, 4, and 6 data are transmitted. This is shown in **Figure 25**.

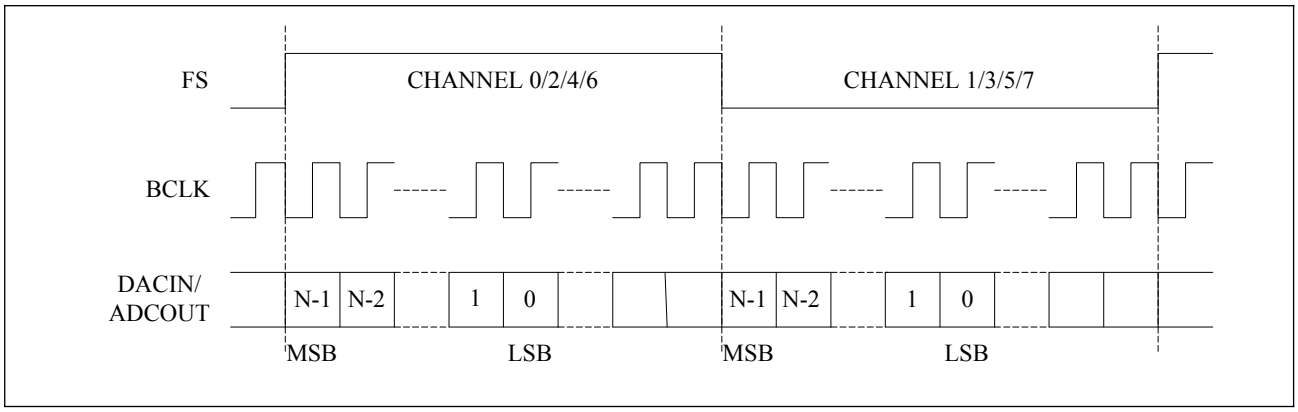


Figure 25 TDM Left-Justified Audio Data

6.2.4 TDM I2S Audio Data

In I2S Mode, the MSB is clocked on the second BCLK rising edge after the FS transitions. When FS is LOW, Channel 0 data are transmitted, then Channel 2, 4, and 6 data are transmitted; when FS is HIGH, Channel 1 data are transmitted, then Channel 3, 5, and 7 data are transmitted. This is shown in **Figure 26.**

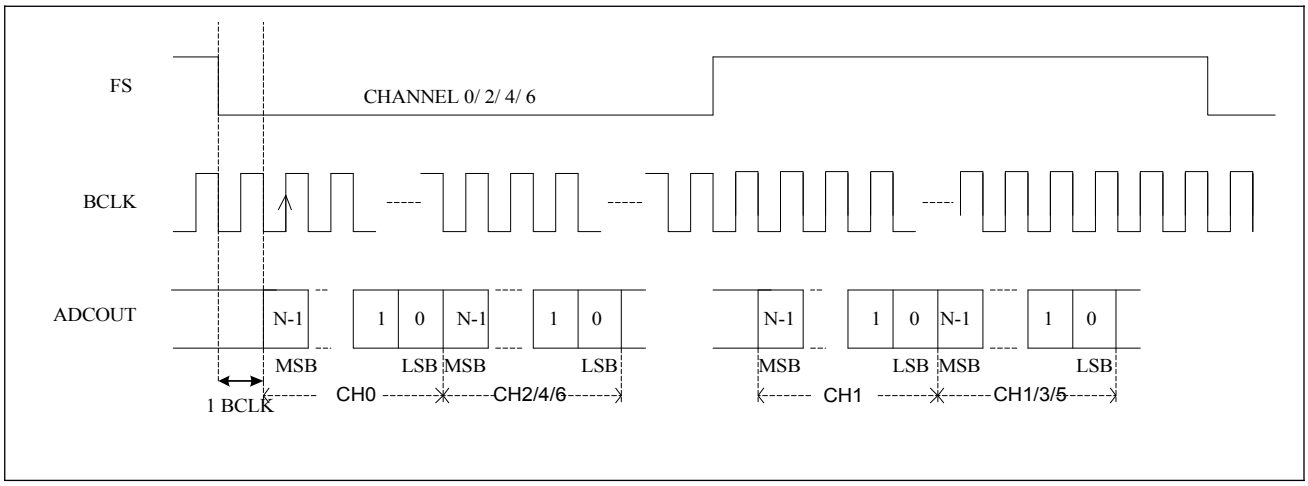


Figure 26 TDM I2S Audio Data

6.2.5 PCM A Audio Data

In PCM A Mode, Channel 0 data are transmitted first, followed sequentially by Channel 1, 2, and 3, 4, 5, 6, and 7 data immediately after. The Channel 0 MSB is clocked on the second BCLK rising edge after the FS pulse rising edge, and the subsequent channel's MSB is clocked on the next BCLK after the previous channel's LSB. This is shown in **Figure 27.** Note that this supports only 8 channels as shown here.

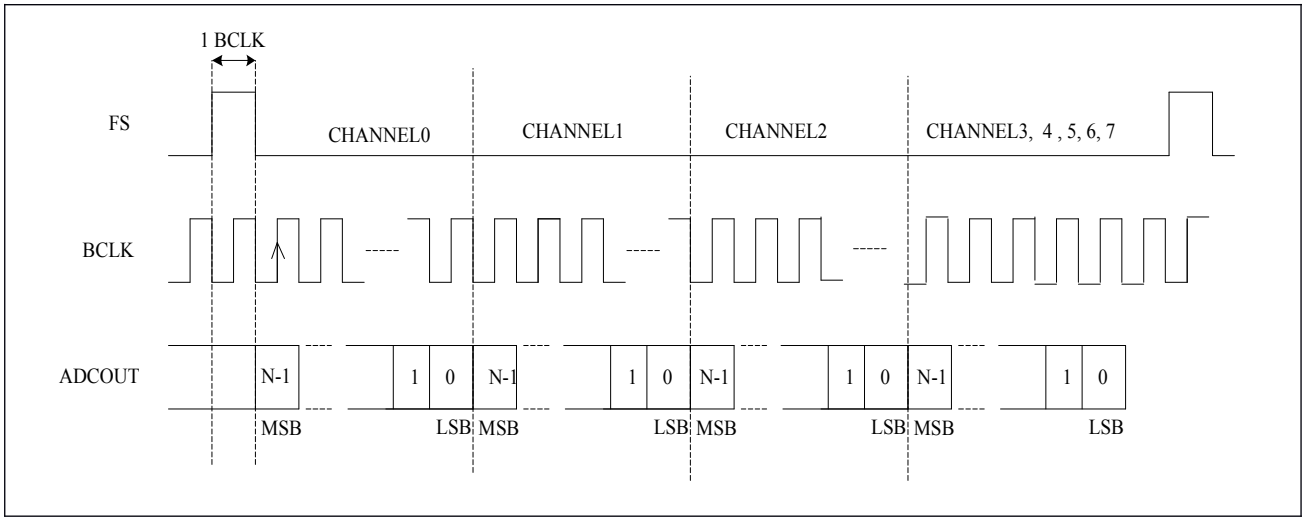


Figure 27 PCM A Audio Data

6.2.6 PCM B Audio Data

In PCM B Mode, Channel 0 data are transmitted first, followed immediately by Channel 1, 2, and 3, 4, 5, 6, and 7 data immediately after. The Channel 0 MSB is clocked on the first BCLK rising edge after the FS pulse rising edge, and the Channel 1 MSB is clocked on the next SCLK after the Channel 0 LSB. This is shown in **Figure 28**.

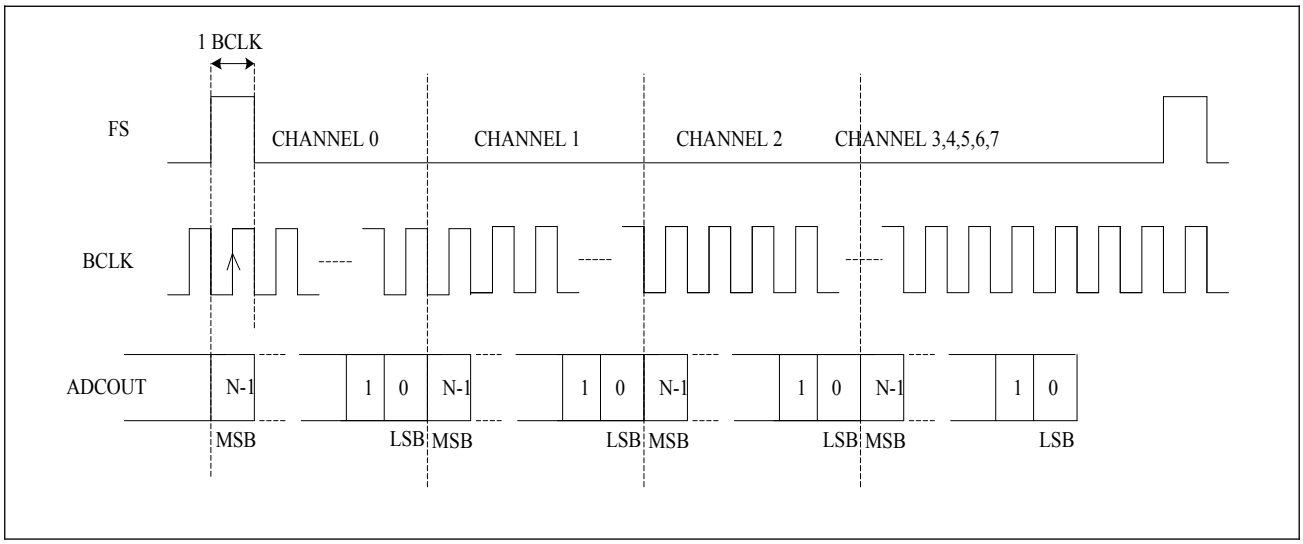


Figure 28 PCM B Audio Data

6.2.7 PCM Time Slot Audio Data

PCM Time Slot Mode is used to delay the time at which the DAC and/or ADC data are clocked. This can be useful when multiple NAU83G60 chips or other devices share the same audio bus. This will allow the audio from the chips to be delayed around each other without interference.

Normally, the DAC and ADC data are clocked immediately after the Frame Sync (FS); however, in PCM Time Slot Mode, the audio data can be delayed by setting **Error: Reference source not found Error: Reference source not found REG0XF[9:0]** and **Error: Reference source not found Error: Reference source not found REG0X10[9:0]** for the left and right channels, respectively. **Error: Reference source not found Error: Reference source not found REG0XE[10**] needs to be set to 1. These delays can be seen before the MSB in **Figure 29**.

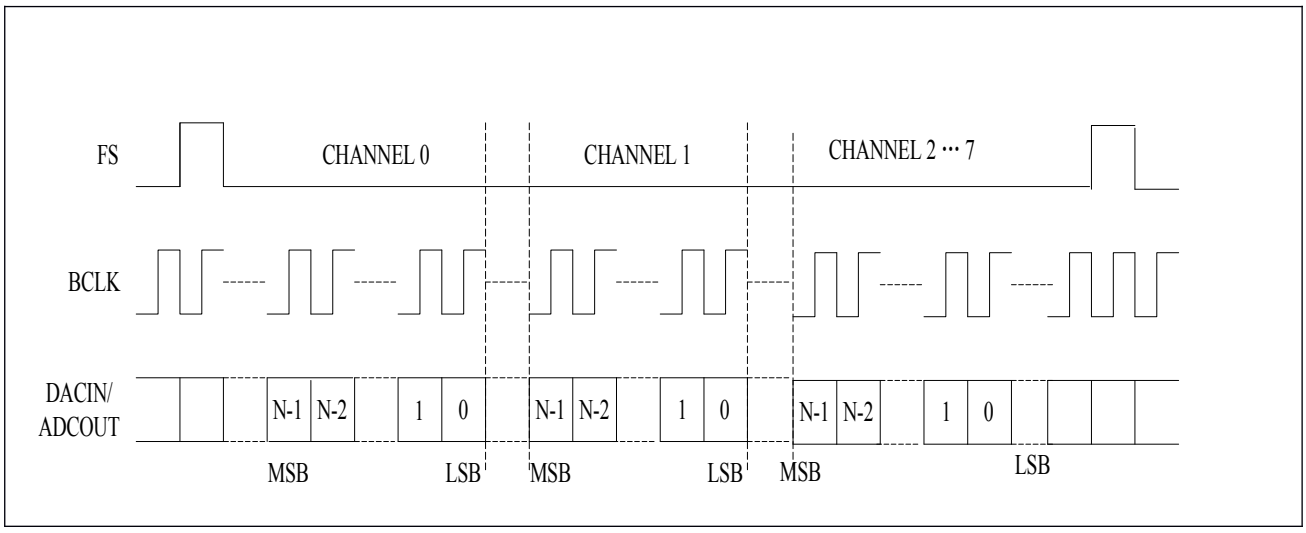


Figure 29 PCM Time Slot Audio Data

APPLICATION NOTES:

- When using the NAU83G60 with other driver chips, the ADCOUT pin can be set to pull up or pull down by enabling Error: Reference source not found Error: Reference source not found **REG0XE[6]** and selecting up or down **with** Error: Reference source not found Error: Reference source not found **REG0XE[5]**. This allows for wired-OR type bus sharing. If both are set to 0, ADCOUT is high impedance, except when transmitting channel audio data. Tri-stating on the negative edge allows the transmission of data by multiple sources in adjacent time slots with reduced risk of bus- driver contention.
- **BY DEFAULT,** Error: Reference source not found Error: Reference source not found **REG0XE[4]** sets the ADCOUT pin in high impedance state. This condition needs to be disabled in order to drive the data line.

6.2.8 PCM Time Offset Audio Data

PCM Time Offset Mode is used to delay the time at which the DAC and/or ADC data are clocked. This increases the flexibility of the NAU83G60 for use in a wide range of system designs. One key application of this feature is to enable multiple NAU83G60 chips or other devices to share the audio data bus, thus enabling more than four channels of audio. This feature may also be used to swap channel data, or to cause multiple channels to use the same data. **ERROR: REFERENCE SOURCE NOT FOUND ERROR: REFERENCE SOURCE NOT FOUND REG0XC[14]** must be set to 1 for this application.

Normally, the DAC and ADC data are clocked immediately after the Frame Sync (FS). In this mode, audio data are delayed by a delay count specified in the device control registers. The Channel 0 MSB is clocked on the BCLK rising edge defined by the delay count set in **Error: Reference source not found Error: Reference source not found REG0XF[9:0]**. The subsequent channel's MSB is clocked on the next BCLK after the LSB of the previous channel. This can be seen in **Figure 30**.

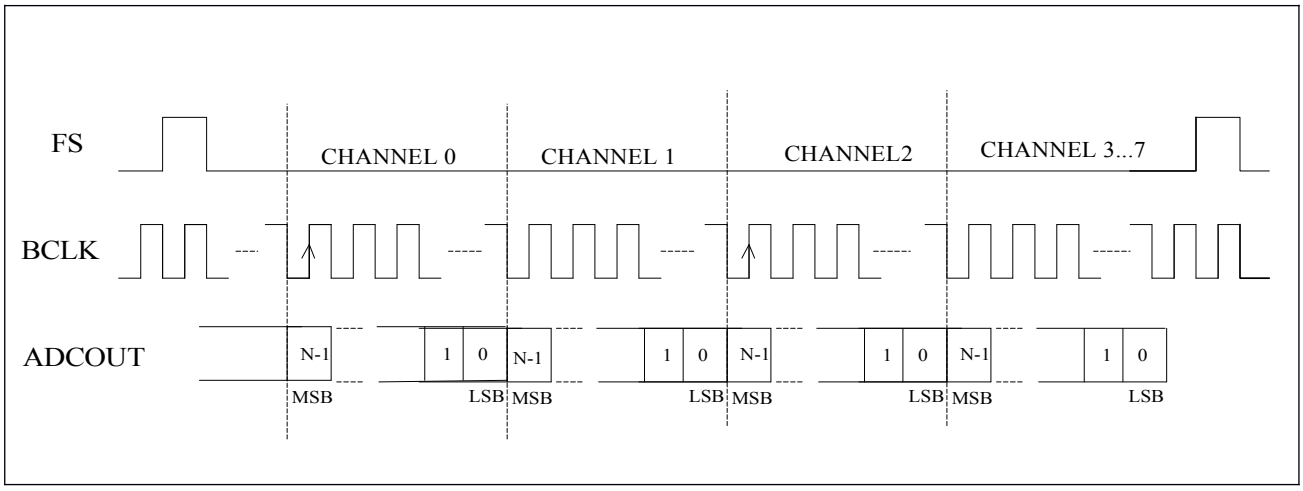


Figure 30 PCM Time Offset Audio Data

6.2.9 I/V Sense Data Stereo Mode (TBD)

	Data Type	Descriptions
1	AL	16bit AEC Reference Signal from Left Channel
2	AR	16bit AEC Reference Signal from Right Channel
3	VL	16bit V Sense Data from Left Channel
4	VR	16bit V Sense Data from Right Channel
5	IL	16bit I Sense Data from Left Channel
6	IR	16bit I Sense Data from Right Channel

~~7~~	~~DL1~~	~~First 16bit Diagnostic Data from Left channel~~
~~8~~	~~DL2~~	~~Second 16bit Diagnostic Data from Left channel~~
~~9~~	~~DR1~~	~~First 16bit Diagnostic Data from Right channel~~
~~10~~	~~DR2~~	~~Second 16bit Diagnostic Data from Right channel~~
11	Emp	Empty Channel
12	VL+IL	16bit Vsense + 16bit Isense data from Left Channel
13	VR+IR	16bit Vsense + 16bit Isense data from Right Channel
14	~~DL1+DL2~~	~~32bit Diagnostic data from Left channel~~
15	~~DR1+DR2~~	~~32bit Diagnostic data from Right channel~~
16	AL+DL1	16bit AEC Reference + first 16bit Diagnostic Data from Left Channel
17	AR+DR1	16bit AEC Reference + first 16bit Diagnostic Data from Right Channel

Sampling Rate	Audio Format	Ch 1	Ch 2	Ch 3	Ch 4	Ch 5	Ch 6	Ch 7	Ch 8
Up to 192KHz	32bit I2S	AL	AR						
Up to 192KHz	24bit I2S	AL	AR						
Up to 192KHz	16bit I2S	AL	AR						
Up to 192KHz	32Bit TDM 4-Ch	AL	DL1+DL2	AR	DL1+DL2				
Up to 192KHz	24Bit TDM 4-Ch	AL	DL1	AR	DR1				
Up to 192KHz	16Bit TDM 4-Ch	AL	DL1	AR	DR1				
Up to 96KHz	32Bit TDM 8-Ch	AL	Emp	AR	Emp	DL1+DL2	Emp	DR1+DR2	Emp
Up to 96KHz	24Bit TDM 8-Ch	AL	Emp	AR	Emp	DL1	Emp	DR1	Emp
Up to 96KHz	16Bit TDM 8-Ch	AL	Emp	AR	Emp	DL1	Emp	DR1	Emp

6.3 Interrupt Request (TBD)

Interrupt Request is a useful error checking feature that can indicate problems on the amplifier during use. Below is the registers used to control the nature of the request. Please refer to the corresponding register for more information.

- INTERRUPT_CTRL_REG0X05
- INT_CLR_STATUS_REG0X06
- IO_CTRL_REG0X0A[15:11]

A brief overview of the feature is that the physical IRQ pin [30] Figure 1 goes to active logic when one of the bits in INT_CLR_STATUS become activated. The IRQ pin can be configured in IO_CTRL_REG0X0A[15:11], in which we will be assuming that it is using active high logic (meaning the register will become one when triggered) set in IO_CTRL_REG0X0A[15]. Additionally, this IRQ pin **[30]** should be connected to the external interrupt of its controller, of which the controller will activate its Interrupt Service Routine (ISR) when IRQ pin goes high. The ISR should then read INT_CLR_STATUS register, reset the same register by sending a single bit 1 to the activated bit in that register, and trigger a flag to fix what may have happened depending on the interrupt status shown in INT_CLR_STATUS. NOTE: Only one bit can be reset at a time.

What shows in the IRQ pin [30] and the status register is controlled by the INTERRUPT_CTRL register. The top bits (disable) [14:8] control whether the conditions would show up in both the INT_CLR_STATUS register and IRQ pin while the lower bits (mask) [7:0] will let it show on the INT_CLR_STATUS register but not on the IRQ pin. In short, the IRQ pin is latched to all of the triggering bits in the INT_CLR_STATUS register and will go low when all bits in the INT_CLR_STATUS register is reset.

An example of this is when Over Voltage Protection (OVP) occurs during activation of output. On initial register loading, we set IO_CTRL to 0x8800 meaning IRQ logic is active high and output is enable. Additionally we want to set the INTERRUPT_CTRL to 0x6070 which enables the current/temperature protection, clipping, low/over voltage protection, and power detection and masks the interrupt detecting clipping on the output.

Interrupt Triggers:

- INT_CLR_STATUS_REG0X06[0] – Power Interrupt Status: Triggered by providing supply power, activating ENA_CTRL_REG0X04, and based on the **PWRUPEN** signal.
- INT_CLR_STATUS_REG0X06[1]– Over Voltage Protection (OVP) Detection: Triggered by VBAT reaching 20V

Activating output by triggering ENA_CTRL, INT_CLR_STATUS bit 0 becomes activated and the IRQ pin latches causing a trigger on the external interrupt on the controller. The controller can then acknowledge this in its check on the status register and reset both the IRQ pin and status register by writing 0x0001 to INT_CLR_STATUS. However, the IRQ pin is still active, indicating there is something wrong with the NAU83G60. The controller must then invoke a check on INT_CLR_STATUS again in which it sees INT_CLR_STATUS bit 1 is still high. From this we can deduce that after a short time after resetting the status register, the OVP detection interrupt triggered meaning the VBST voltage ramped up after setting output but slow enough to occur right after resetting the status register. The controller must realize this and take appropriate steps to fix this occurrence.

NOTE: When activating the Class-D Driver output either manually through registers or through the **PWRUPEN** signal, OVP may trigger and will require reset.

NOTE: Because the on/off trigger is based on the **PWRUPEN** signal and when inducing the **PWRUPEN** signal through the clock detection circuit (Section ERROR: REFERENCE SOURCE NOT FOUND) using the I^2S communication protocol, if any of the incoming signals are stopped, specifically DACIN, then the **PWRUPEN** signal is set to 0 and awaits the signal is present again. When present again, the **PWRUPEN** signal will trigger and the on/off interrupt will also trigger.

6.4 FusionF1 DSP core

NAU83G60 consist of two Cadence Tensilica LX7 Core, with Fusion F1 core package.

The DSP core is equipped with 128KB Instruction ROM (IROM0), and 24KB Data RAM (DRAM0). In addition, a 1KB memory mapped IO is available for register access, Audio/Sense data communication, and further communication interface with the host.

DSP Core Clock can be up to 120(MHz), provided by an in-chip MCLK PLL.

NAU83G60 DSP Core runs Klippel's Non-Linear Speaker Protection Algorithm (KCS).

Figure 31 describes the different interfaces connected to the DSP Core.

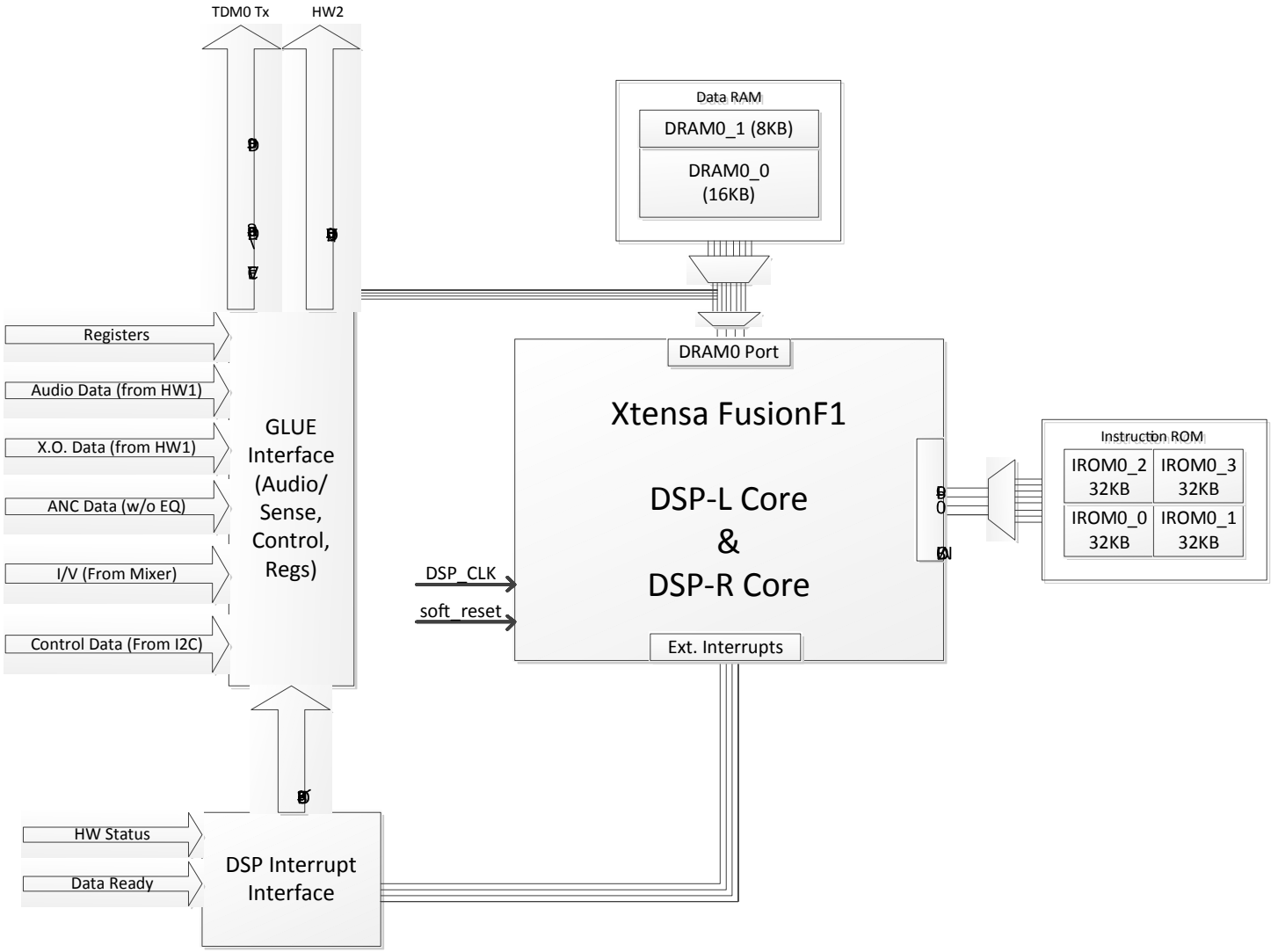


Figure 31 DSP Connection Diagram

6.4.1 Reset and Clocks

NAU83G60 DSP Core is released from reset after either a Hardware(0x0000) or a Software reset (0x0001). Whenever the DSP is reset, the protection algorithm will be reinitialized, and the host processor should re-communicate with the KCS library and reinstate speaker parameters (see below).

NAU83G60 DSP Core Clock is derived from the provided MCLK, OSC48MHz and PLL.

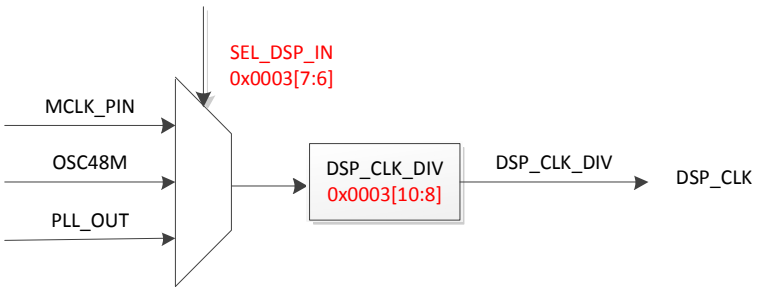


Figure 32 DSP Clock Diagram

6.4.2 Memory Map

DSP Memory map is detailed in Table 14 DSP Core Memory Map.

The DSP Memory architecture is Harvard architecture, i.e. Instruction memory and Data memory are two separate buses in the system, and has two different access attributes. Instruction memory can only be accessed in 32 bit aligned accesses. Data memory can be accessed in 8 bit aligned accesses. NAU83G60 DSP Core Instruction memory is a 128KB ROM (IROM0), partitioned to 4 32KB ROM instances. Data memory is a 24KB SRAM (DRAM0), partitioned ta a 8KB and 16KB block. In addition to memory instances, DSP Core memory interface provides access to IO mapped devices, in order to communicate to and from the DSP Core.

Table 14 DSP Core Memory Map

Address Space	Token	Modules
Core Local Memories		
0x6002_0000– 0x6003_FFFF	IROM0	Instruction ROM Memory 0
0x6001_0000– 0x6001_8000	DRAM0	Data RAM Memory 0
Memory Mapped IO Space (0x6001_8000– 0x6001_8D7F)		
0x6001_8000-0x6001_8007	DATA_FLOW_BA	Audio Data Input Full band
0x6001_8008-0x6001_800F	DATA_FLOW_BA	TDM0 TX Slot0/2
0x6001_8010-0x6001_8017	DATA_FLOW_BA	I/V Sense Data Input Value
0x6001_8018-0x6001_801F	DATA_FLOW_BA	Host input data by I2c
0x6001_8020-0x6001_8027	DATA_FLOW_BA	DSP output data to I2C
0x6001_8028-0x6001_802F	DATA_FLOW_BA	DSP latch I2C data
0x6001_8030-0x6001_8037	DATA_FLOW_BA	TDM0 TX Slot1/3
0x6001_8038-0x6001_803F	DATA_FLOW_BA	ANC data Input
0x6001_8040-0x6001_8047	DATA_FLOW_BA	Audio Data Output Value
0x6001_8048-0x6001_804F	DATA_FLOW_BA	Audio Data Input High Band
0x6001_8050-0x6001_8057	DATA_FLOW_BA	Audio Data Input Middle Band
0x6001_8058-0x6001_805F	DATA_FLOW_BA	Audio Data Input Low Band
0x6001_8100-0x6001_8107	~~CHIP_BA~~	I2C control register1
0x6001_8108-0x6001_810F	~~CHIP_BA~~	I2C control register1
0x6001_8110-0x6001_811F	~~CHIP_BA~~	I2C control register1
0x6001_8120-0x6001_812F	~~CHIP_BA~~	DSP Interrupt Control

6.4.3 Interrupts

NAU83G60 DSP Core has 1 general purpose timer, and up to 11 interrupt sources. A total of 9 interrupts (8 to 0) are external interrupts used to notify DSP of system events. An additional two interrupts, Software and Timer0 interrupts are also provided for software usage.

Interrupts are divided to three level groups. Higher the interrupt level, higher its priority. Interrupts with higher priority will preempt interrupts with lower priority. Level 1 interrupts are prioritize by the XTOS frame (Tensilica provided HAL), according to the interrupt number (higher interrupt gets higher priority). The interrupts priorities are in place to give higher priorities to input audio and sensor data buffering, before next samples arrives.

Interrupt #	Interrupt Type	Interrupt Level	Description
INT0	Edge	LEVEL 3	Audio Sample Ready Interrupt (also DRC High/Middle/Low band Data Ready interupt) ANC Sample Ready Interrupt Sense Sample Ready Interrupt
INT1	Edge	LEVEL 2	IV debug
INT2	Edge	LEVEL 1	I2C: Inbound control data in DSP_IN_DATA is ready for DSP to process
INT3	Edge	LEVEL 1	I2C: DSP_OUT_DATA for outbound data is ready for new data
INT4	Edge	LEVEL 1	I2C: communication error with host
INT5	Edge	LEVEL 1	ALC Change Interrupt
INT6	Edge	LEVEL 1	Combined HW Indications
INT7	Edge	LEVEL 1	ANC debug
INT8	Edge	LEVEL 1	
INT9	Software	LEVEL 1	General porpuse SW-triggered interrupt (Used for KCS processing)
INT10	Timer	LEVEL 1	General porpuse core timer interrupt

6.4.4 Hardware-Software Interface

The hardware/software interface implements the following paths for data to be collected and communicated to and from the DSP Core:

- Audio/Sense data path – audio/ANC data from the host (DAC data), IV sense data from the in-chip ADC. Both data streams are real time PCM.
- Audio data is available on AUDIO_DATA_IN register, and is a signed 32 bit word. Once output data is ready, it can be written as 32 bit word to AUDIO_DATA_OUT register.
- Sensor data is available on SENSE_DATA_IN register. This register contains two fields –
- ANC data is available on ANC_DATA_IN register, and is a signed 32 bit word. Once output data is ready, it can be written as 32 bit word to AUDIO_DATA_OUT register.
- Hardware state information – a read only access to the in-chip registers that provides the status of different HW components
- Control and diagnostics information – a HW/SW layer that provides a way for the host to get information to in from the DSP

1.1.1.1 Audio and Sense Data Path Interface

Figure 33illustrates the audio and sensor data paths to the DSP in NAU83G60.

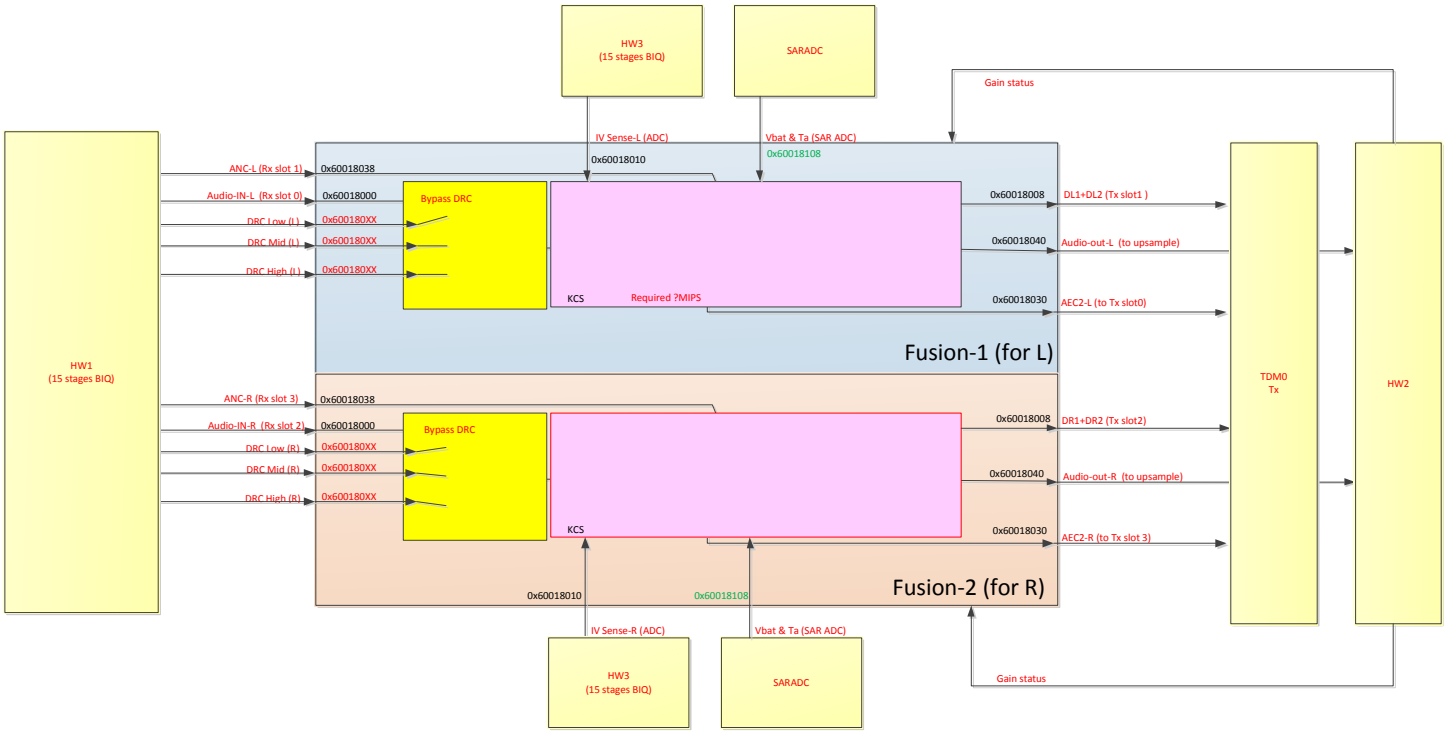


Figure 33 Audio and Sensor Paths Components

Audio IN Data is a two channel (stereo) PCM stream originated at the host via I2S bus. Host PCM word width may be 8, 16, 24 or 32 bit.. After an I2S transceiver, the audio data goes through a configurable System Equalizer (15 stages BIQ filter), and a configurable HPF. Once HPF data out is ready, NAU83G60 stores the data as a 32 bit signed word into a shared register,

DRC IN Data is separated as three frequence band as DRC_Low,DRC_MIDDLE and DRC_High and each of them is a two channel (stereo) PCM stream from HW1. It is an optional function.

Case1: Bypass DRC

ERROR: REFERENCE SOURCE NOT FOUND.(0X60018000)

After registering the data, NAU83G60 raises an interrupt to the DSP (IINT0). Then the DSP can read the data from this register and process it.

After data was processed, the DSP ROM Code writes output audio word, a 32 bit signed PCM word, into

(0x60018040). NAU83G60 samples this register at each frame sync, unless the DSP is bypassed (see CFG_REGXXXX[X]). When the DSP is bypassed, the data is taken from the DSP Input.

Case2: Multi-band DRC

ERROR: REFERENCE SOURCE NOT FOUND.(0X60018048)

ERROR: REFERENCE SOURCE NOT FOUND.(0X60018050)

ERROR: REFERENCE SOURCE NOT FOUND.(0X60018058)

After registering three DRC data, NAU83G60 will raises an interrupt to the DSP (INT0). The INT0 is also shared as Audio IN Data.

Then the DSP can read the data from this register and process it.

ANC data is a two channel (stereo) PCM stream originated at the host via I2S bus. Host PCM word width may be 8, 16, 24 or 32 bit. After an I2S transceiver, the ANC data should bypass by a configurable System Equalizer (three stages BIQ filter), and a configurable HPF. Once HPF data out is ready, NAU83G60 stores the data as a 32 bit signed word into a shared register,

ERROR: REFERENCE SOURCE NOT FOUND.(0X6001_8038)

After registering the data, NAU83G60 raises an interrupt to the DSP (INT7). Then the DSP can read the data from this register and process it.

Sensor data is originated from NAU83G60 sensor SDADC.

The SDADC produces two 16 bits words, Current measurement (ISENSE) and Voltage measurement (VSENSE). Both ISENSE and VSENSE go through a configurable HPF. Then ISENSE data is fed into a temperature compensation block, which amplifies the signal (digitally) according to temperature. Once both ISENSE and VSENSE are ready, NAU83G60 stores them as a 32 bit word in

.(0x60018010)

Then, an interrupt is generated to the DSP Core (INT1). After the DSP gets the interrupt, it can read the data from this register, parse it back to ISENSE/VSENSE, and process it.

NAU83G60 ROM Code supports the following sampling rates pairs[1].

Table 15 Supported Audio/Sense Rates

Audio Sampling Rate	Sense Sampling Rate	Minimum DSP_CLK
16kHz	16KHz	TBD
32kHz	32kHz	TBD
44.1kHz	44.1kHz	TBD
48kHz	48Khz	96MHz
96KHz	48KHz	96MHz
192KHz	48KHz	96MHz

Audio sampling rate is obtained by the DSP by reading mirrored register ERROR: REFERENCE SOURCE NOT FOUND (CFG_REG40).
Sensor sampling rate is obtained by reading the mirrored value of CLK_CTRL[12:11], (CFG_REG03).

Note: CFG_REG03[12:11] bits are reflected as read only on bits on ERROR: REFERENCE SOURCE NOT FOUND[1:0], which is mirrored to the DSP Core.

1.1.1.2 Control Flow

Control Flow is the interface that allows I2C communication between the DSP and the outside world (i.e. Host processor).

Figure 34 describes the hardware implementation of the control interface. Both inbound (to DSP) and outbound (from DSP) data paths contains two 32 bit registers (one for DSP and one for I2C), to hold the data to be communicated. These registers are called: I2C_REG_IN, DSP_IN_DATA (for inbound data), and I2C_REG_OUT, DSP_OUT_DATA (for outbound data).

[1] For ROM Code revision 00, only 48kHz/12kHz is supported

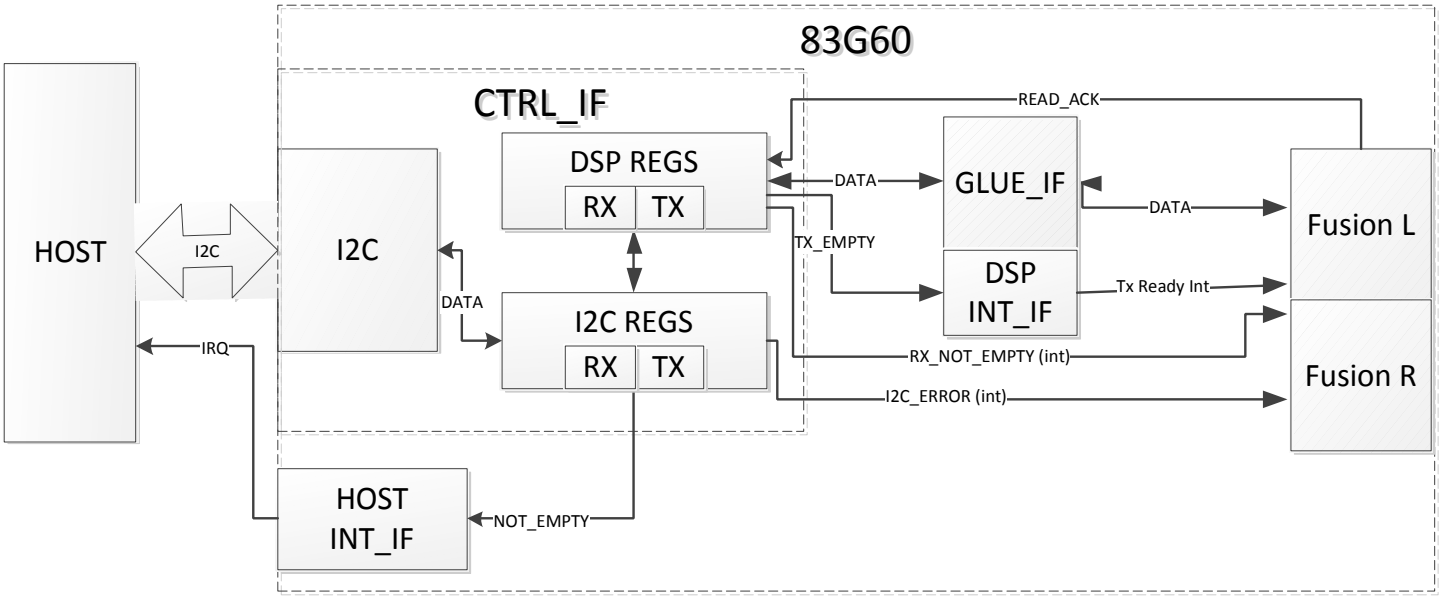


Figure 34 Control Interface Block Diagram

For **Inbound Path (Host Writes to DSP)**, the following flow describes the low level HW implementation of the communication protocol.

- Host initiating an I2C write transaction to NAU83G60, addressed to the DSP register (using register address 0xF000 for Fusion –L/ 0xF002 for Fustion -R), with 4 bytes of data.
- If I2C_REG_IN is empty, NAU83G60 will store the received 4 bytes in I2C_REG_IN
- If I2C_REG_IN is not empty (i.e. contains data that was not consumed by the DSP), NAU83G60 will NACK the first byte of data (right after the DSP register address), and generates a data error interrupt to the DSP Core (INT4)
- Once **INBOUND CONTROL DATA REGISTER (DSP_IN_DATA)** is empty (i.e. ready for new data), NAU83G60 will:
- Store I2C_REG_IN data to DSP_IN_DATA, and marks I2C_REG_IN empty.
- Raise an interrupt (INT2 – I2C Inbound Data Ready) to the DSP Core
- Mark DSP_IN_DATA as not-empty
- After getting the Data Ready Interrupt, DSP ROM Code:
- Reads the data from DSP_IN_DATA
- Acknowledge that data was read by writing any value to

- __.
- NAU83G60 will then mark DSP_IN_DATA as empty.

For **Outbound Path (Host reads from DSP)**[2]:

- Whenever **OUTBOUND CONTROL DATA REGISTER (DSP_OUT_DATA)** becomes empty, NAU83G60 generates an interrupt to the DSP (INT3).
- If the DSP has data to write, it writes to DSP_OUT_DATA. If the DSP does not have data to write, it will write an idle pattern to DSP_OUT_DATA. (0xF1 0xF2 0xF3 0xF4).
- If I2C_REG_OUT is empty, NAU83G60 moves the data from DSP_OUT_DATA to I2C_REG_OUT, and marks DSP_OUT_DATA as empty.
- Host initiating an I2C read transaction to NAU83G60, addressed to the DSP register (using register address 0xF000 for Fusion-L/0xF002 for Fusion-R), and reads 4 bytes.
- Then NAU83G60 Marks I2C_REG_OUT empty
- Next time DSP_OUT_DATA becomes not empty, NAU83G60 moves the data from DSP_REG_OUT to I2C_REG_OUT.

6.4.5 Audio Path Initialization

6.4.5.1 Host Processor POR Procedure

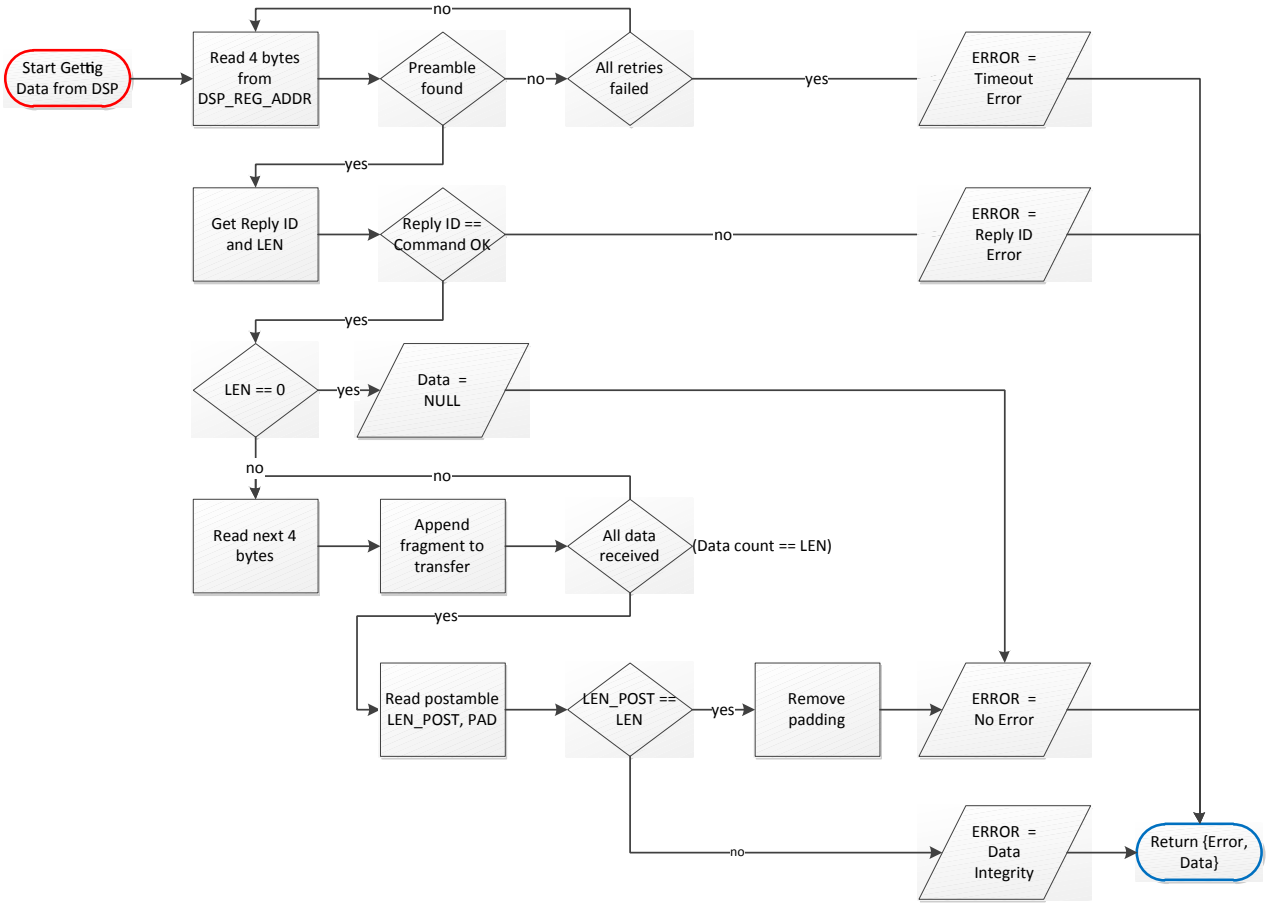
At power up Host Processor is expected to set initial configuration of NAU83G60, and then configure the DSP and its protection algorithm. NAU83G60 DAC and ADC sampling rate must be set before the DSP initialization sequence.

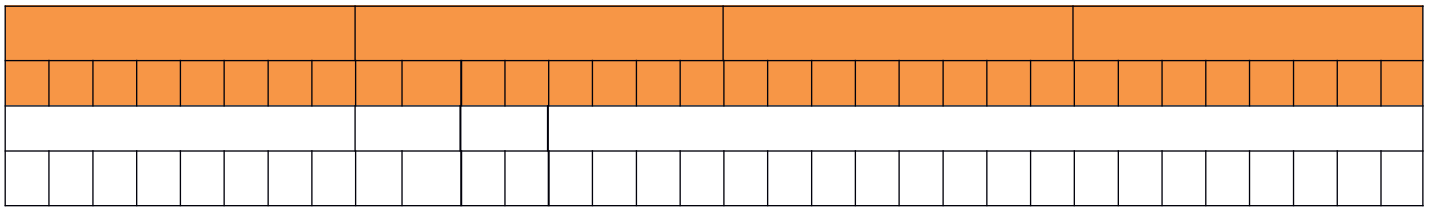
Figure 35 describes the procedure that should take place in order to release NAU83G60 DSP from reset and configure it.

In order to properly configure DSP, MCLK and DSP_CLK must be provided and set to a correct frequency according to TABLE 15 SUPPORTED AUDIO/SENSE RATES. Host Processor then configures NAU83G60 for the required sampling rate of both the audio input and sensor data. This configuration sequence can be part of the normal NAU83G60 initialization sequence that includes all the subsystems (filters, ALC, etc.). Once CODEC configuration is done, Host processor issues a Soft Reset. DSP is then re-initialized according to the flow that is described in section 6.4.5.2. DSP initialization sequence can take up to TBD ms.

[2] NAU83G60 also implements outbound host IRQ to notify Host processor whenever I2C_REG_OUT is not empty. However, this feature is not in use and data flow control is maintained by SW protocol.

Then, while still providing MCLK, Host Processor sends CMD_GET_FRAME_STATUS (see





) and checks that the protection algorithm was initialization was successful. After getting this confirmation, Host will updated speaker parameters by issuing CMD_SET_KCS_SETUP commands. Once speaker parameters were updated successfully, Host Processor will remove DSP Bypass by writing to CFG_REG1A[5].

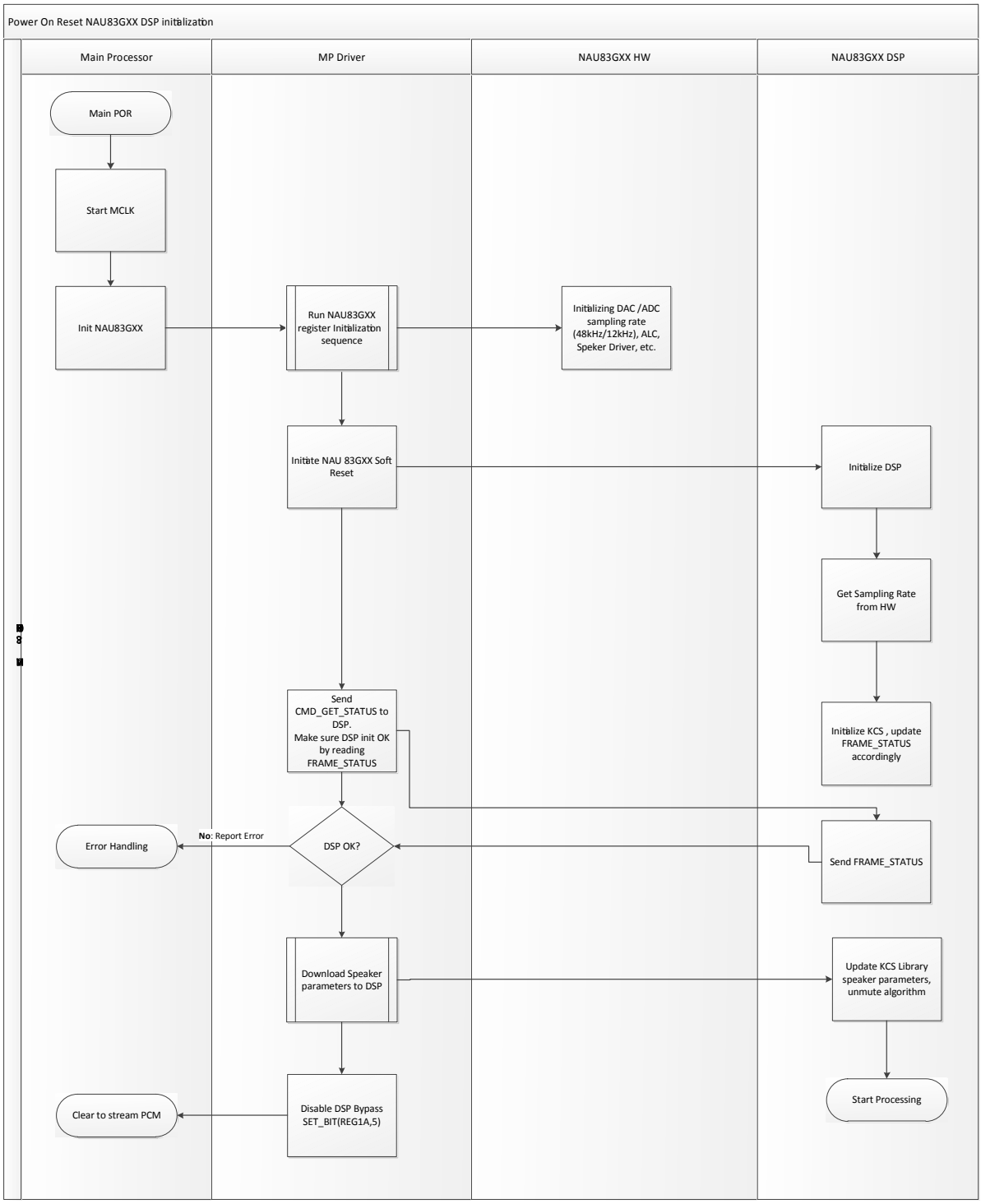


Figure 35 Host to DSP POR Procedure

6.4.5.2 DSP Initialization

NAU83G60 DSP is released from reset after power up, assuming that its clock is enabled, or after a soft reset as described before. After DSP released from reset, the DSP ROM Code will initialize DSP and Protection algorithm library.

Upon DSP reset, ROM Code initializes internal DSP registers, disables and clears all interrupts, and unpacks variables to Instruction RAM. The DSP core initialization process is based on XTOS library – Tensilica's HAL package.

Sampling rate calculation is done after this basic DSP core initialization. ROM Code will initialize internal audio, VSENSE and ISENSE buffers, and obtain the configured Audio and Sensor sampling rate, by reading mirrored registers.

In order to obtain the configured Audio and Sensor sampling, DSP reads the following registers:

- CFG_REG40[12:10] – REG_SRATE
- CFG_REG40[9] – REG_ALT_SRATE
- CFG_REG40[0] – REG_MINMAX
- CFG_REG22[1:0], which mirrors the value of CFG_REG3[12:11] – [ADC_DIV2, ADC_DIV4]

Then, the rate is calculated according to the following table[3]:

REG_SRATE	REG_MINMAX	REG_ALT_SRATE	ADC_DIV	Audio Rate	Sensor Rate
~~000~~	~~0~~	~~X~~	~~00~~	~~8kHz~~	~~8kHz~~
001	0	X	00	16kHz	16kHz
~~001~~	~~1~~	~~X~~	~~10~~	~~24kHz~~	~~12kHz~~
010	0	X	10	32kHz	32kHz
010	1	1	01	44.1kHz	44.1kHz
010	1	3) 0	01	4) 48kHz	5) 48kHz

Table 16 Sample Rate Selection (TBD)

For any other register configuration, ROM Code sets the audio path to behave in "Feed Through" mode. In this mode the ROM Code bypass the algorithm and does not perform any processing on input data. Instead, output audio data will be equal to input audio data.

KCS Library Initialization is the next step, after obtaining a valid audio and sensor sampling rates. At this stage ROM Code initializes the protection algorithm library (KCS library). If any error was encountered while initializing KCS library structures, ROM Code enables "Feed Through" mode, and updates FRAME_STATUS accordingly.

NAU83G60 DSP uses interrupts in order to handle both control and data (audio/sense) communication flow from the Host processor and NAU83G60.

In order to properly latch HW Indication events, DSP enables certain HW events (UVLO, OVP, OCP_OTP) to be latched in HW_INT_STS, by setting corresponding bits in HW_INT_EN. For audio and sensor processing purposes, DSP ROM Code installs handlers for INT0 (audio data sync) and INT1 (sensor data ready) and enables these interrupts. For Control processing, ROM Code installs handler for INT3 (Inbound control data ready) and INT4 (outbound control buffer ready). Once initialization is done, ROM Code starts the Main loop.

Figure 36 describes the initialization sequence that takes place inside the DSP.

[3] For ROM Code revision 00, only 48kHz/12kHz is supported

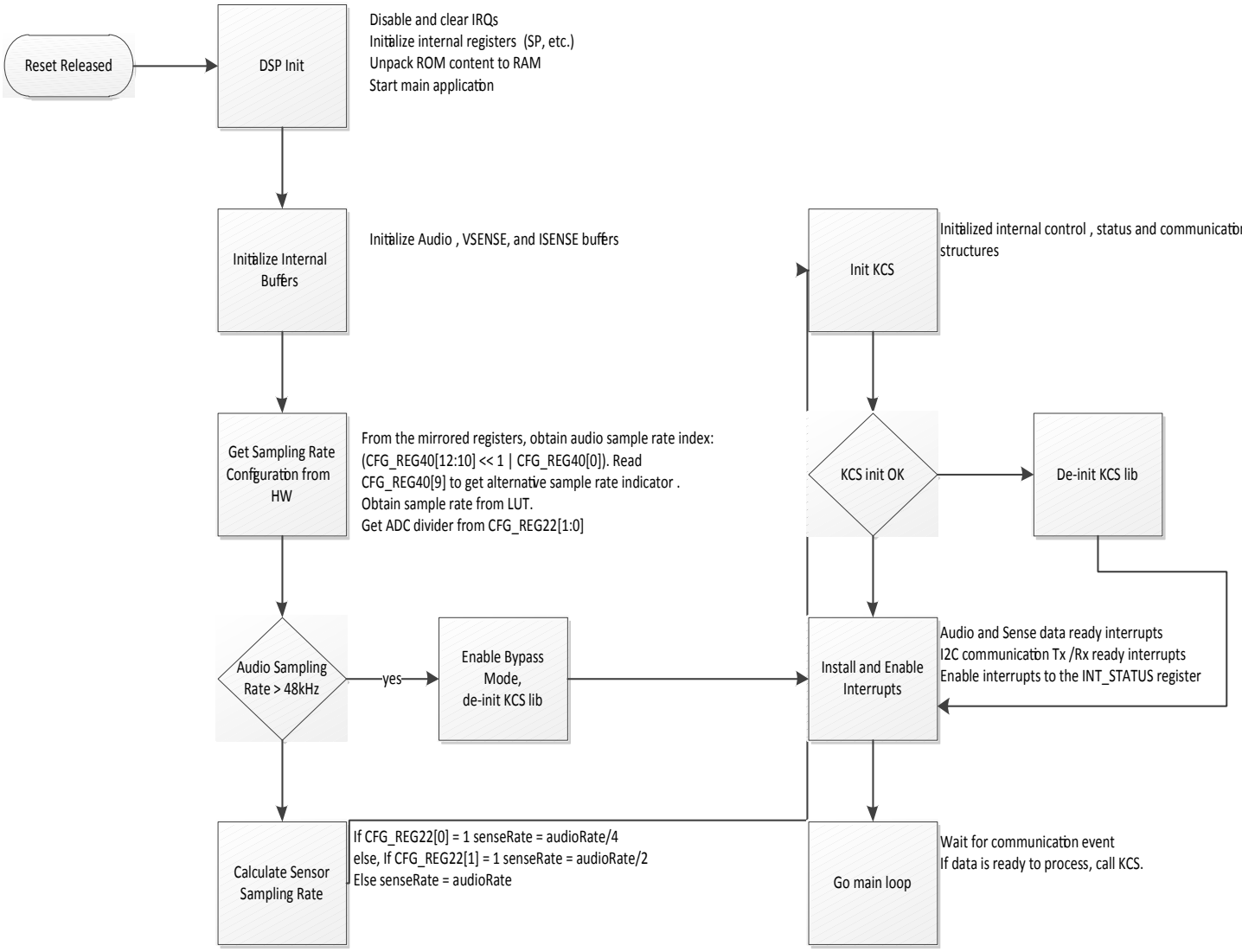


Figure 36 ROM Code Initialization Flow Chart

6.4.6 Communication Protocol

In order to control and configure KCS Library and ROM Code settings, The NAU83G60 DSP ROM Code uses the control flow interface described in section above.

The ROM Code implements a communication protocol that provides:

- Interface to send commands to the DSP
- Interface to read and write control and status structures from the DSP memory
- Basic error detection mechanism.

The communication protocol is a Master-Slave type protocol where the Host Processor is the master and the DSP is the slave. The Master initiates the communication and can either write or read back from the Slave. Transactions from the Master are called “Messages”, and read-back data from the Slave is called a “Reply”.

The communication protocol is divided to three layers: Application, Transport and Physical layers. Both the Host Processor and the DSP implement this protocol.

6.4.6.1 Host to DSP

Figure 37 describes how data is treated and organized by the host before it is being transmitted.

Host Application Layer:

- Prepares a *Message* that consist of:
  - Command ID – 5 bit command (see Table 22 DSP Supported Commands)
  - Data to be send – array of bytes, with maximum length of 128 bytes.
- Send the Message to Transport Layer

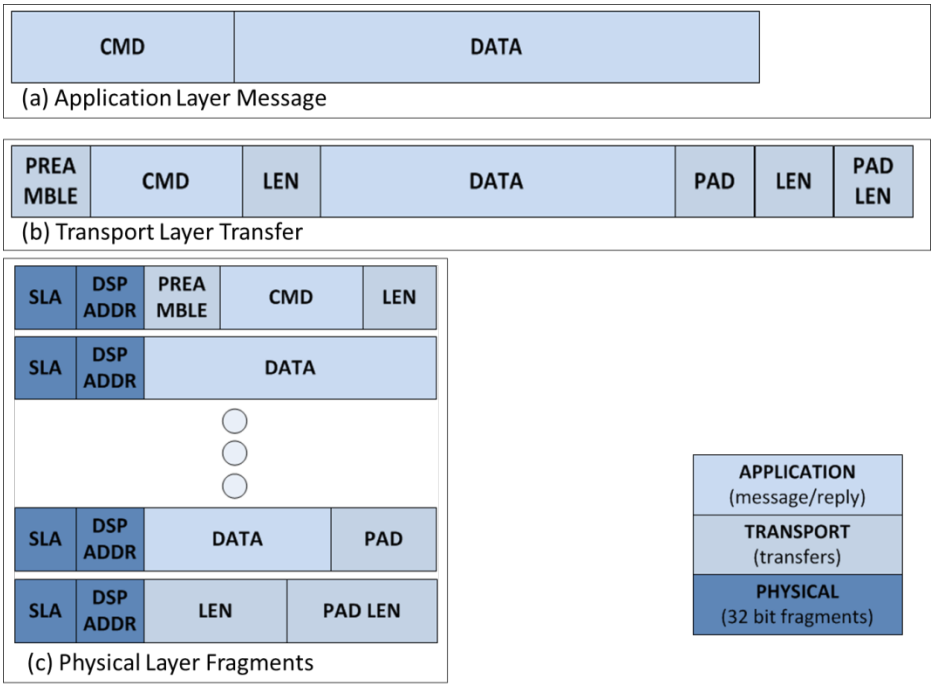


Figure 37 Protocol Layer Breakdown (Host)

Host Transport Layer prepares a *Transfer*:

1) Stores transfer length (in quotes of 32 bit) in a variable LEN
2) Adds a preamble to the message
   a. Set leading fragment BYTE0[7:0] to 0xA1
   b. Set leading fragment BYTE1[7:0] to 0xB2
3) Organize Command ID and Transfer length as follows:
   a. Set leading fragment BYTE2[7:2] to Command ID
   b. Set leading fragment BYTE2[1:0] to LEN[1:0]
   c. Set leading fragment BYTE3[7:0] to LEN[9:7]
4) Pad the end of the message to with zeros so it will be 32-bit aligned,
5) If length of message is not zero, adds a post amble to the message:
   a. Set trailing fragment BYTE0[7:0] to LEN[7:0]
   b. Set trailing fragment BYTE1[7:6] to LEN[9:8]
   c. Set trailing fragment BYTE1[5:4] to number of bytes padded
6) Breaks the transfer into 32-bit *fragments*.
7) Send fragments to lower level I2C driver

Table 17 is an example of a leading fragment for a transfer of command ID 0x7, that has 10 fragments of 32-bit words to transfer.

Table 17 Host To DSP Leading Fragment

BYTE0								BYTE1								BYTE2								BYTE3							
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Preamble (0xA1 0xB2)																CMD_ID (e.g. 0x07)						LEN[1:0]		LEN[9:2] (e.g. 10)							
1	0	1	0	0	0	0	1	1	0	1	1	0	0	1	0	0	0	0	1	1	1	1	0	0	0	1	0	0	0	0	0

Table 18 is an example of a trailing fragment for a transfer that had 10 fragments of 32-bit words to transfer, and that the last payload fragment had 1 byte of padding.

Table 18 Host To DSP Trailing Fragment

BYTE0								BYTE1								BYTE2								BYTE3							
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
LEN [7:0]								LEN[9:8]		PAD		Reserved																			
0	0	1	0	0	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Host Physical Layer:

1) Adds DSP register address (0xF000/0xF002) to each fragments
2) Sends fragments in I2C to NAU83GXX slave address.

Host transmit flow is described in Figure 38.

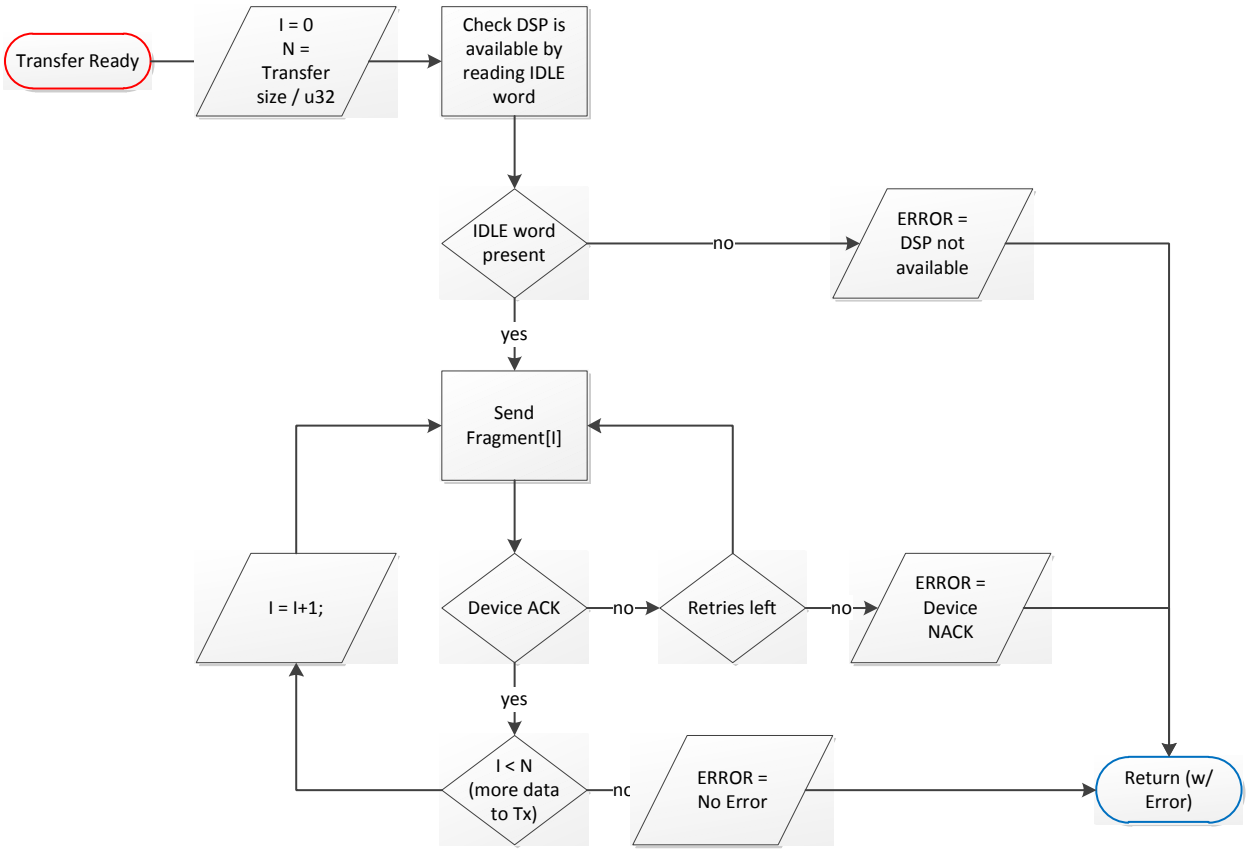


Figure 38 Host Control Tx Flow

On the receiver side, the DSP receives the fragments, and recover the entire message. Then, if the message is valid it will execute the command, and send back a reply. The DSP receive flow consists of two parts, data gathering, and command handling, as described in figures below. (detailed description TBD).

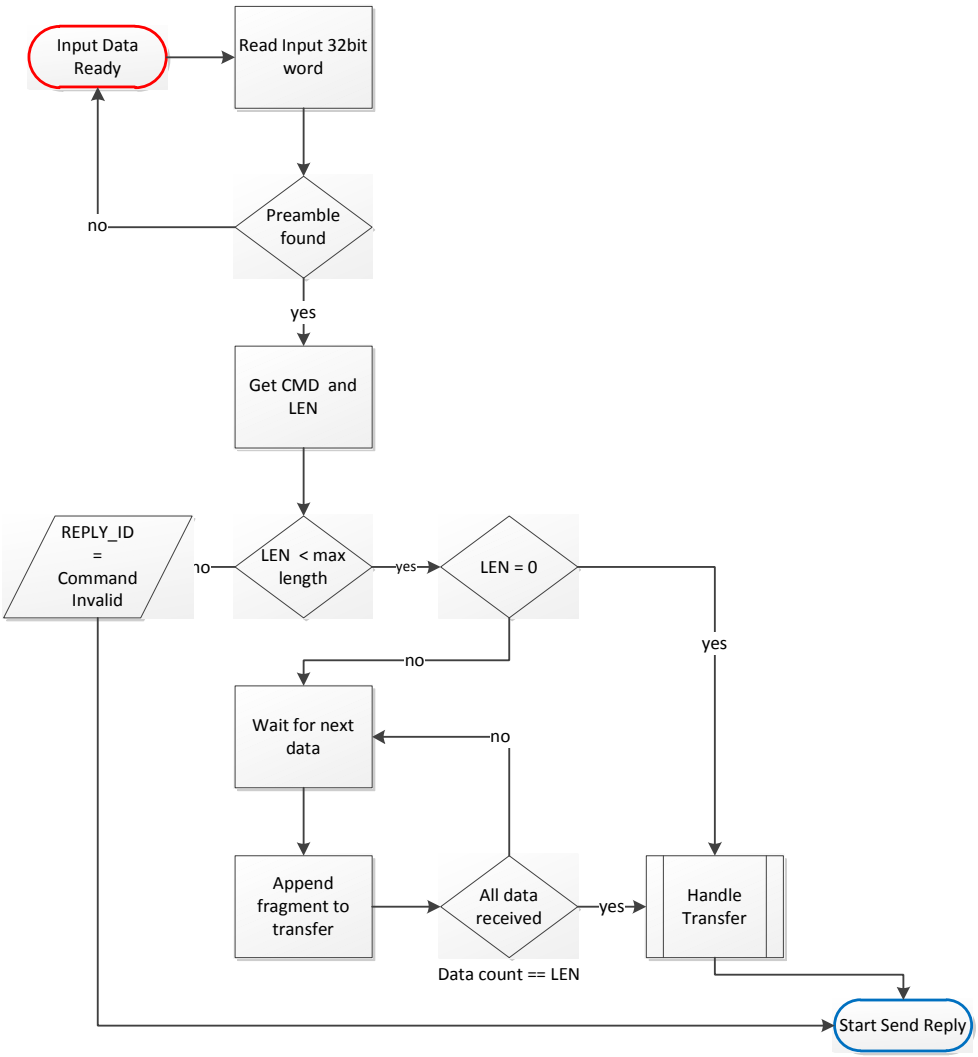


Figure 39 DSP Control Rx flow I

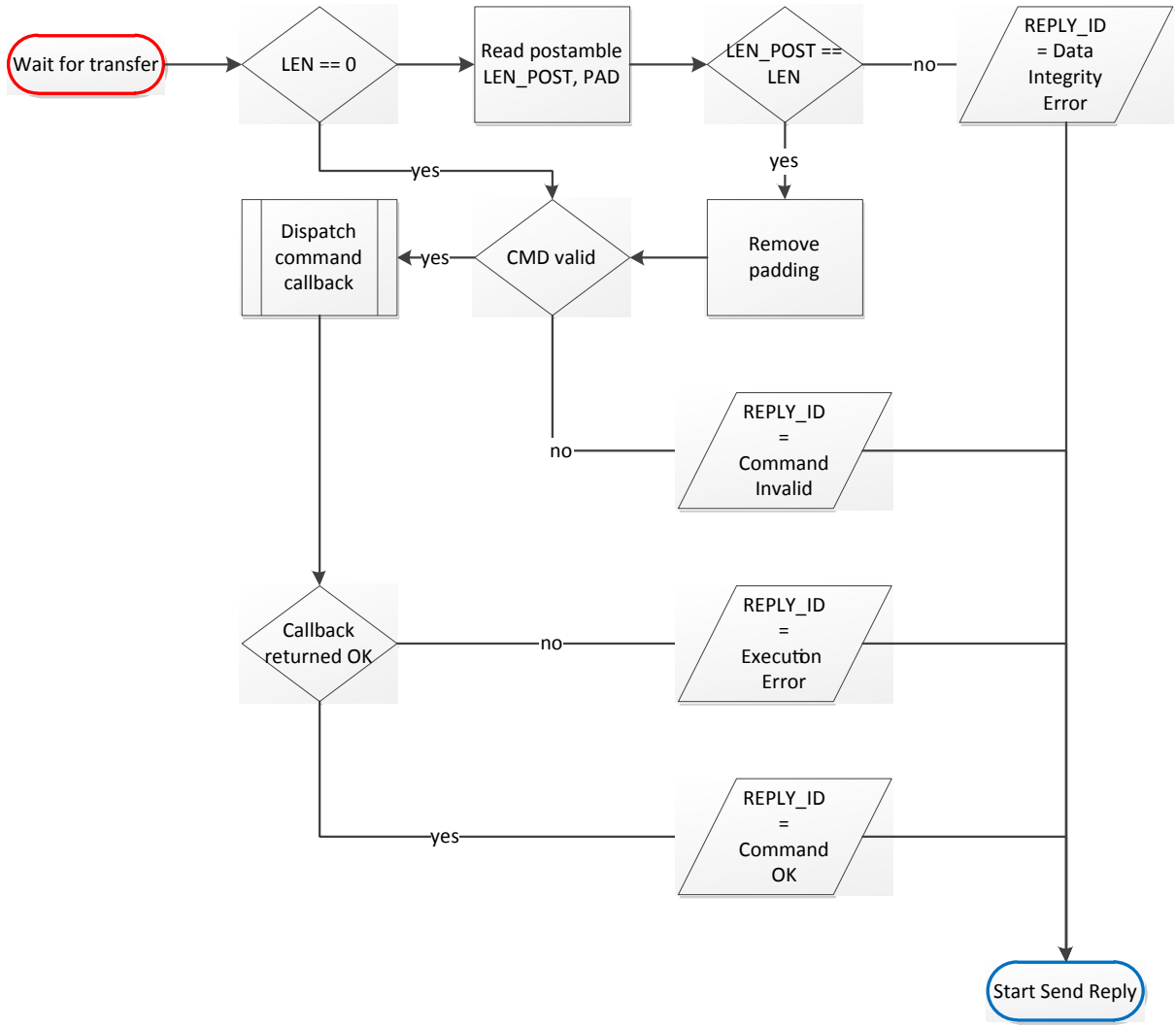


Figure 40 DSP Control Rx Flow II

6.4.6.2 DSP to Host (Reply)

Once DSP as a reply ready to send, it will start putting in on DSP_OUT_DATA register, for the host to read back.

DSP transport layer orders output data in similar way to the message path.

1) Stores transfer length (in quotes of 32 bit) in a variable LEN
2) Adds a preamble to the message
    a. Set leading fragment BYTE0[7:0] to 0xA1
    b. Set leading fragment BYTE1[7:0] to 0xB2
3) Organize Command ID and Transfer length as follows:
    a. Set leading fragment BYTE2[7:2] to Reply ID (see Table 19).
    b. Set leading fragment BYTE2[1:0] to LEN[9:8]
    c. Set leading fragment BYTE3[7:0] to LEN[7:0]
4) Pad the end of the message to with zeros so it will be 32-bit aligned,
5) If length of message is not zero, adds a post amble to the message:

a. Set trailing fragment BYTE0[7:0] to LEN[9:2]
b. Set trailing fragment BYTE1[7:6] to LEN[1:0]
c. Set trailing fragment BYTE1[5:4] to number of bytes padded

6) Breaks the transfer into 32-bit *fragments*.
7) Write fragments to lower level DSP_OUT_DATA

Table 19 DSP Control Flow Reply IDs

REPLY_ID	Name
0x00	REPLY_OK
0x01	REPLY_MSG_INTEGRETY_ERR
0x02	REPLY_EXECUTION_ERR
0x03	REPLY_COMMAND_DOESNT_EXISTS_ERR
0x04	REPLY_UNKNOWN_ERR
0x05	REPLY_MSG_TOO_LONG

Figure 41 Host Control Reply Flow describes the procedure Host Processor should take in order to gather data from the DSP.

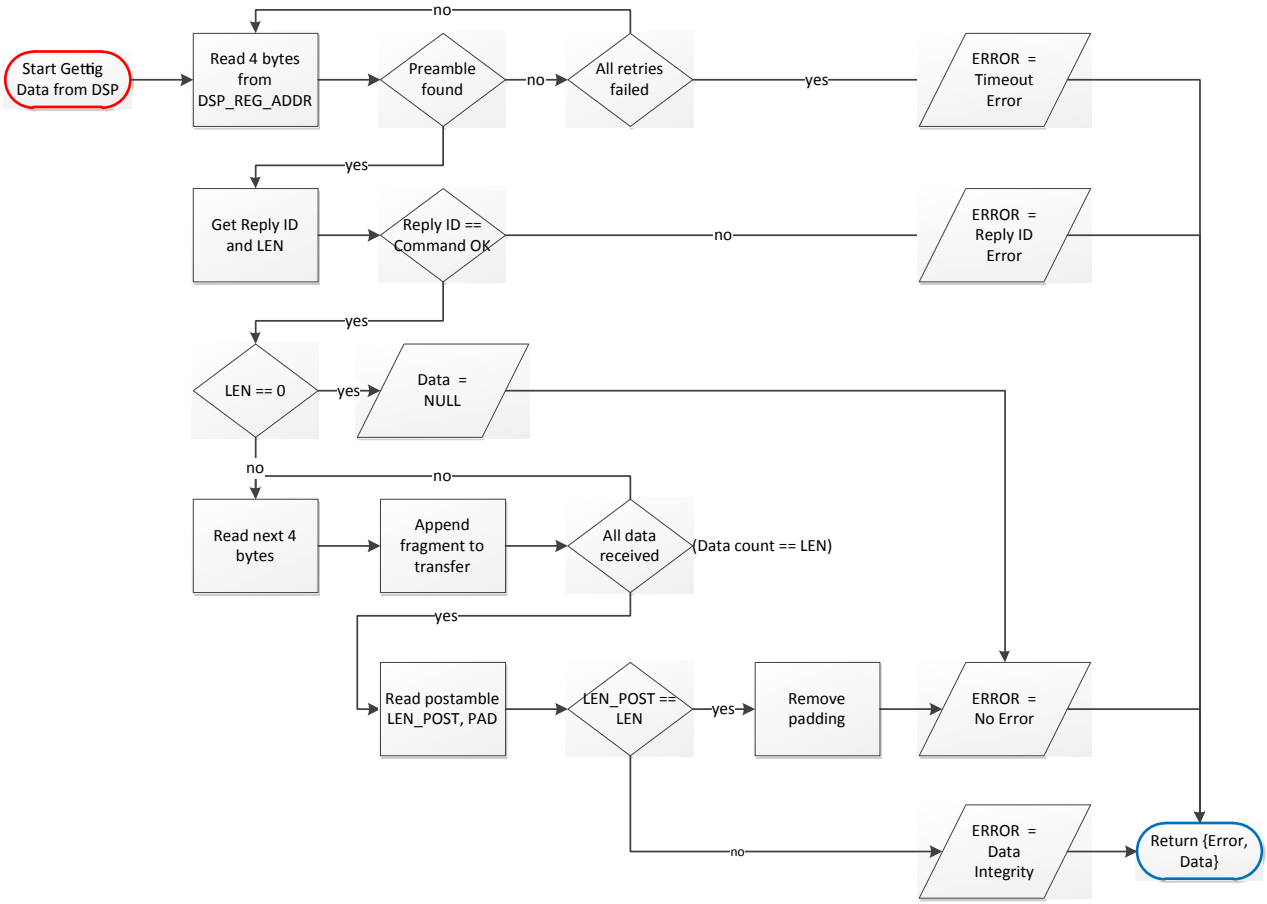


Figure 41 Host Control Reply Flow

After sending data to the DSP host will start reading back 32bit fragments from the DSP register (0xF000). If a preamble was not found in the incoming word after few retries, host will report error, and may try to send the message later.

If the preamble (0xA1 0xB1) was found, it means that the Host got a leading fragment. The host parses Reply ID and Length of the incoming fragment.

If Reply ID is not REPLY_OK, host should handle the error accordingly.

If the message has data (LEN != 0), Host will continue to read fragments until it read LEN fragments. When host reaches the trailing fragment, it reads back the LEN from it and make sure that LEN field in trailing fragment and leading fragment are the same (if not, it should handle the error). finally the host will check how many bytes were padded in the last payload fragment, by parsing PAD_LEN field from the trailing fragment.

Table 20 is an example of a leading fragment for a reply that was OK, and has 10 fragments of 32-bit words to transfer.

Table 20 DSP To Host Leading Fragment

BYTE0								BYTE1								BYTE2								BYTE3							
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Preamble (0xA1 0xB2)																Reply_ID (e.g. 0x00)						LEN[1:0]		LEN[9:2]							
1	0	1	0	0	0	0	1	1	0	1	1	0	0	1	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	0	0

Table 21 is an example of a trailing fragment for a transfer that had 10 fragments of 32-bit words to transfer, and that the last payload fragment had 1 byte of padding.

Table 21 DSP To Host Trailing Fragment

BYTE0								BYTE1								BYTE2								BYTE3							
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
LEN[7:0]								LEN[9:8]		PAD		Reserved																			
0	0	1	0	0	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

6.4.6.3 Supported Commands

Table 22 DSP Supported Commands

CMD_ID	Pnemonic	Parameters	Description
0x01	CMD_GET_COUNTER	None	Returns an increasing counter each time the command is called, can be used as a heartbeat to see that DSP is alive.
0x09	CMD_GET_FRAME_STATUS	None	Returns FRAME_STATUS 32bit word that contains the current KCS init, audio/sense sampling rates, and HW indication
0x0A	CMD_GET_REVISION	None	Retruns the ROM Code revision and KCS

			revision.
0x04	CMD_GET_KCS_RSLTS	Offset, Length	Gets Data from internal algorithm results structure. Returns *Length* bytes from address *Offset* relative to KCS start
0x06	CMD_GET_KCS_SETUP	Offset, Length	Gets Data from internal algorithm configuration structure. Returns *Length* bytes from address *Offset* relative to KCS start
0x07	CMD_SET_KCS_SETUP	Offset, Length, Data	Sets *Data* to internal algorithm configuration structure. Write *Length* bytes of *Data*, starting at address *Offset*. Returns Execution status only

DSP ROM Code Frame Status (FRMAE_STATUS)

The following table describes the 32 bit word that the DSP returns after issuing CMD_ID 0x09 (CMD_GET_FRAME_STATUS).

31	30	29	28	27	26	25	24
SNS_OVF	AUD_UVF	AUD_OVF	ALC_STS	HW_IND_STS [7:4]			
23	22	21	20	19	18	17	16
HW_IND_STS [3:0]				SNSR_RATE [7:4]			
15	14	13	12	11	10	9	8
SNSR_RATE [3:0]				AUDIO_RATE [7:4]			
7	6	5	4	3	2	1	0
AUDIO_RATE [3:0]				Reserved		FEED_TRU	ALGO_OK

Bits	Description	
[31]	SNS_OVF	**Sensor Data Overflow** This bit indicates that the sensor data input buffer overflowed and some sensor samples were ommited and not buffered to the protection algorithm. This may happen at power up, and if clock configuration is incorrect. After reading FRAME_STATUS, DSP sets this bit to 0.
[30]	AUD_UVF	**Audio Data Underflow** This bit indicates that the audio data underflowed, meaning was no new processed samples to transmit on frame sync. After reading FRAME_STATUS, DSP sets this bit to 0.
[29]	AUD_OVF	**Audio Data Overflow** This bit indicates that the audio data input buffer overflowed and some sensor samples were ommited and not buffered to the protection algorithm. This may happen at power up, and if clock configuration is incorrect. After reading FRAME_STATUS, DSP sets this bit to 0.

[28]	**ALC_STS**	**ALC Status** This bit represents the latest ALC Change indication the DSP ROM Code used for the protection algorithm. It is set to 1 whenever the DSP detects ALC gain is different from zero.
[27:20]	**HW_IND_STS**	**HW Indication Status** This field is a reflection of the latest status the DSP read from RD_INT_STATUS before calling the protection algorithm
[19:12]	**SNSR_RATE**	**Sensor Data Rate** This field contains the sensor sampling rate the DSP calculated according to the chip registers, divided by 1000 (e.g. for sensor rate of 12kHz, this field will have 12).
[11:4]	**AUDIO_RATE**	**Audio Data Rate** This field contains the audio sampling rate the DSP calculated according to the chip registers, divided by 1000 (e.g. for audio rate of 48kHz, this field will be 48)
[3:2]	**Reserved**	
[1]	**FEED_TRU**	**Feed Through Mode** This bit indicates that the DSP is in feed through mode. In this mode DSP discards sensors samples, and bypass the audio samples (i.e. audio out equals to audio in).
[0]	**ALGO_OK**	**Algorithm Initilazition OK** This bit indicates that the audio protection algorithm was initialized successfully.

6.4.7 DSP Registers (TBD)

A memory mapped IO space provides access from the DSP core to HW registers. This memory mapped area allows the DSP to get audio/ sense data, information as of the state of the chip, and control information from the host. In addition to control and data, DSP Core has access to mirrored register set from which the ROM Code can get system status and current configuration.
R: read only, **W**: write only, **R/W**: both read and write

Register	Offset	NAU83G60 Register	R/ W	Description	Reset Value
REGS_BA = 0x6001_FC00					
AUDIO_DATA_IN	REGS_BA+0x000		R	Inbound Audio Data Register	0x00000000
AUDIO_DATA_OUT	REGS_BA+0x008		W	Outbound Audio Data Register	0x0000_0000
SENSE_DATA_IN	REGS_BA+0x010		R	Inbound I/V sense data from speaker ADC	0x0000_0000
DSP_IN_DATA	REGS_BA+0x018		R	Inbound control data from host	0x0000_0000
DSP_OUT_DATA	REGS_BA+0x020		W	Outbound control data to host	0x0000_0000
DSP_CTL_ACK	REGS_BA+0x024		W	Control Data Read Ack	0x0000
TX_SLOT13_OUT	REGS_BA+0x030		W	Outbound Data Register to TX Slot	0x0000_0000
ANC_DATA_IN	REGS_BA+0x038		R	Inbound I/V sense data from speaker ADC	0x0000_0000
TX_SLOT0/2_OUT	REGS_BA+0x040		W	Outbound Data Register to TX Slot	0x0000_0000
Fustion output to GPIO	REGS_BA+0x048		W	Fustion output to GPIO	0x0000_0000
GPIO input to Fustion	REGS_BA+0x050		R	GPIO to Fusion input	0x0000_0000

Register	Offset	NAU83G60 Register	R/W	Description	Reset Value
MCGB IN	REGS_BA+0x070		R	MCGB input	0x0000_0000
MCGB OUT	REGS_BA+0x078		R	MCGB ouput	0x0000_0000
KCS Read status	REGS_BA+0x080		R	Direct KCS status read	0x0000_0000
KCS Write status	REGS_BA+0x088		W	Direct KCS status Write	0x0000_0000
RD_INT_STATUS	REGS_BA+0x100	0x0006	R	System Interrupt Status Readback	0xXXXX
BOOST_ CTRL_O	REGS_BA+0x102	0x001C	R	Boost Control Target Value	0xXXXX
GENERAL_STATUS1	REGS_BA+0x104	0x001E	R	General Status Register 1	0xXXXX
SAR_ADC_OUT_01	REGS_BA+0x106	0x0020	R	In-Chip SAR ADC outputs 0, 1	0xXXXX
SAR_ADC_OUT_23	REGS_BA+0x108	0x0021	R	In-Chip SAR ADC outputs 2, 3	0xXXXX
ALC_READOUT1	REGS_BA+0x10A	0x0022	R	ALC Status Register 1	0xXXXX
ALC_READOUT2	REGS_BA+0x10C	0x0023	R	ALC Status Register 2	0xXXXX
CLK_DET_ CTRL	REGS_BA+0x10E	0x0040	R	Clock Detection Readback	0xa801
SOFTWARE_ID	REGS_BA+0x110	0x0045	R	Software ID	0x????
I2C_DEVICE_ID	REGS_BA+0x112	0x46	R	Device ID	0xXXXX
ANALOG_READ	REGS_BA+0x114	0x4A	R	Analog Status Register	0xXXXX
ANALOG_CONTROL_3	REGS_BA+0x116	0x64	R	Analog Control 3 Readback	0xXXXX
DSP_INT_MASK	REGS_BA+0x120		W	DSP Host Interrupts Mask	0x00
DSP_INT_CLR	REGS_BA+0x121		W	DSP Host Interrupts Clear	0x00
L_EQ over flow status		1bit	R	15band cascade overflow status for left channel	
R_EQ over flow status		1bit	R	15band cascade overflow status for right channel	
Stereo/BPTL mono Mode		1bit	R	external pull high/down of GPIO1 to settle the PCBa as Stereo mode or PBTL mode	
L/R Fustion status		1bit	R	distinguish between L fusion and R Fusion	
L_3band XO		32*3=96Byte=768bit	R	to access the multi-band DRC parameters	
L_3band DRC		32*3=96Byte=768bit	R	to access the multi-band DRC parameters	
R_3band XO		32*3=96Byte=768bit	R	to access the multi-band DRC parameters	
R_3band DRC		32*3=96Byte=768bit	R	to access the multi-band DRC parameters	

Register	Offset	NAU83G60 Register	R/W	Description	Reset Value
L_post gain		?? bit	R	Left channel digital post gain	
R_post_gain		?? bit	R	Right channel digital post gain	
L_DAC gain		2bit	R	Left channel analog DAC gain for the performance	
R_DAC_gain		2bit	R	Right channel analog DAC gain for the performance	
L/R_Ratio_gain		3bit	R	Ratio gain depends on the VBAT	
L_V_ana_gain		2bit	R	Left channel voltage sense gain	
L_I_ana_gain		2bit	R	Left channel current sense gain	
R_V_ana_gain		2bit	R	Right channel voltage sense gain	
R_I_ana_gain		2bit	R	Right channel current sense gain	
KCS status		?? bit	R	direct KCS status read	

Inbound Audio Data Register (AUDIO_DATA_IN)

Register	Offset	83G01 index	R/W	Description	Reset Value
AUDIO_DATA_IN	REGS_BA+0x000		R	Inbound Audio Data Register	0x00000000

31	30	29	28	27	26	25	24
AUDIO_DAT [31:24]							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
AUDIO_DAT [23:16]							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
AUDIO_DAT [15:8]							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
AUDIO_DAT [7:0]							

Bits	Description	
[31:0]	**AUDIO_DAT**	**Inbound Audio Data from Host** This register is updated automatically every frame sync with new audio sample. SW must read this value before next frame sync cycle, otherwise the sample would be lost. Note: AUDIO_DAT[7:0] is always zero

Outbound Audio Data Register (AUDIO_DATA_OUT)

Register	Offset	83G01 index	R/W	Description	Reset Value
AUDIO_DATA_OUT	REGS_BA+0x008		W	Outbound Audio Data Register	0x0000_0000

31	30	29	28	27	26	25	24
AUDIO_DAT [31:24]							
23	22	21	20	19	18	17	16
AUDIO_DAT [23:16]							
15	14	13	12	11	10	9	8
AUDIO_DAT [15:8]							
7	6	5	4	3	2	1	0
AUDIO_DAT [7:0]							

Bits	Description	
[31:0]	AUDIO_DAT	**Outbound Audio Data to Speaker** This register should be written by the SW with new outbound data, between each frame cycle. At the start of each frame, HW will use take the data in this register and drive it to the audio path. The SW must place new data in this register before frame starts. Note: HW takes AUDIO_DAT[31:8]

Inbound Sense Data Register (SENSE_DATA_IN)

Register	Offset	83G01 index	R/W	Description	Reset Value
SENSE_DATA_IN	REGS_BA+0x010		R	Inbound I/V sense data from speaker ADC	0x0000_0000

31	30	29	28	27	26	25	24
I_SENSE_DAT [15:8]							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
I_SENSE_DAT[7:0]							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
V_SENSE_DAT [15:8]							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
V_SENSE_DAT [7:0]							

Bits	Description	
[31:16]	**I_SENSE_DAT**	**Inbound Current Sense Data** This register is updated automatically every sense frame sync with new current sense sample. SW must read this value before next frame sync, otherwise the sample would be lost.
[15:0]	**V_SENSE_DAT**	**Inbound Voltage Sense Data** This register is updated automatically every sense frame sync with new voltage sense sample. SW must read this value before next frame sync, otherwise the sample would be lost.

Inbound Control Data Register (DSP_IN_DATA)

Register	Offset	83G01 index	R/W	Description	Reset Value
DSP_IN_DATA	REGS_BA+0x018		R	Inbound control data from host	0x0000_0000

31	30	29	28	27	26	25	24
CTL_DAT [31:24]							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CTL_DAT [23:16]							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CTL_DAT [15:8]							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CTL_DAT [7:0]							

Bits	Description	
[31:0]	**CTL_DAT**	**Inbound Control Data from Host** This register is the input portion of the host to DSP communication protocol. After the Host writes a 32 bit to this I2C mapped register, the HW generates an interrupt to the DSP core and the SW may access it and read from it. (See Error: Reference source not foundError: Reference source not found)

Outbound Control Data Register (DSP_OUT_DATA)

Register	Offset	83G01 index	R/W	Description	Reset Value
DSP_OUT_DATA	REGS_BA+0x020		W	Outbound control data to host	0x0000_0000

31	30	29	28	27	26	25	24
CTL_DAT [31:24]							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CTL_DAT [23:16]							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CTL_DAT [15:8]							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CTL_DAT [7:0]							

Bits	Description	
[31:0]	**CTL_DAT**	**Outbound Control Data to Host** This register is the output portion of the host to DSP communication protocol. DSP SW may write to this register when it is empty (indicated by DSP_REG_OUT_EMPTY interrupt). After the SW writes a 32 bit word to this register, the HW generates an interrupt to the Host which in turn may access it via I2C and read from it. (See Error: Reference source not foundError: Reference source not found)

Control Data Read Ack Register (DSP_CTL_ACK)

Register	Offset	83G01 index	R/W	Description	Reset Value
DSP_CTL_ACK	REGS_BA+0x020		W	Control Data Read Ack	0x0000_0000

31	30	29	28	27	26	25	24
CTL_ACK [31:24]							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CTL_ACK [23:16]							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CTL_ACK [15:8]							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CTL_ACK [7:0]							

Bits	Description	
[31:0]	**CTL_ACK**	**Inbound Control Data Read Acknowledgment** This register should be written with any value after the DSP consumed the data in DSP_IN_DAT. (See Error: Reference source not foundError: Reference source not found)

Outbound AEC Data Register (AEC_DATA_OUT)

Register	Offset	83G01 index	R/W	Description	Reset Value
TX_SLOT13_OUT	REGS_BA+0x030		W	Outbound Audio Data Register	0x0000_0000

31	30	29	28	27	26	25	24
AEC_DAT [31:24]							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
AEC_DAT [23:16]							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
AEC_DAT [15:8]							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
AEC_DAT [7:0]							

Bits	Description	
[31:0]	**TX_SLOT13_DAT**	**Outbound Audio Data to Speaker** This register should be written by the SW with new outbound data, between each frame cycle. At the start of each frame, HW will use take the data in this register and drive it to the audio path. The SW must place new data in this register before frame starts.

Inbound ANC Data Register (ANC_DATA_IN)

Register	Offset	83G01 index	R/W	Description	Reset Value
ANC_DATA_IN	REGS_BA+0x038		R	Inbound ANC Data Register	0x00000000

31	30	29	28	27	26	25	24
ANC_DAT [31:24]							
23	22	21	20	19	18	17	16
ANC_DAT [23:16]							
15	14	13	12	11	10	9	8
ANC_DAT [15:8]							
7	6	5	4	3	2	1	0
ANC_DAT [7:0]							

Bits	Description	
[31:0]	ANC_DAT	**Inbound Audio Data from Host** This register is updated automatically every frame sync with new audio sample. SW must read this value before next frame sync cycle, otherwise the sample would be lost. Note: ANC_DAT[7:0] is always zero

System Interrupt Status (HW_INT_STS)

Register	Offset	R/W	Description	Reset Value
HW_INT_STS	REGS_BA+0x100	RO	System Interrupt Status	0xXXXX

15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved SW_HARD_RST			OCP	CLIP	LVD	OVP	Reserved

Bits	Description	
[15:5]	Resreved	
[4]	OCP_OTP	**Over Current / Over Temperature Shutdown** Reflect the state of Over Current or Over Temperature indication coming from the HW. An OCP or OTP event sets this bit to 1, if the corresponing bit in HW_INT_EN is also set to 1. This bit is cleared by writing 1 to the correspoding bit in HW_INT_CLR.
[3]	CLIP	**System Clipping** Reflect the state of Clipping indication coming from the HW (CLIP detector) A clipping event sets this bit to 1, if the corresponing bit in HW_INT_EN is also set to 1. This bit is cleared by writing 1 to the correspoding bit in HW_INT_CLR.
[2]	LVD	**Low Voltage Detection** Reflect the state of Under Voltage Lock Out indication coming from the HW (UVLO) A UVLO event sets this bit to 1, if the corresponing bit in HW_INT_EN is also set to 1. This bit is cleared by writing 1 to the correspoding bit in HW_INT_CLR.
[1]	OVP	**Over Voltage Protection** Reflect the state of Over Voltage indication coming from the HW. An OVP event sets this bit to 1, if the corresponing bit in HW_INT_EN is also set to 1. This bit is cleared by writing 1 to the correspoding bit in HW_INT_CLR.
[0]	Reserved	

System Interrupt Mask (HW_INT_MSK)

Register	Offset	R/W	Description	Reset Value
HW_INT_MASK	REGS_BA+0x120	WO	System Interrupt Mask	0x00

7	6	5	4	3	2	1	0
Reserved SW_HARD_RST			**OCP**	**CLIP**	**LVD**	**OVP**	**Reserved**

Bits	Description	
[7:5]	**Resreved**	
[4]	**OCP_OTP**	**Over Current / Over Temperature Shutdown** This bit enables OCP_OTP event to generate Combined HW Indications interrupt (INT6). When this bit is set to 1, INT6 will be generated to the DSP Core whenever the corresponding bit in HW_INT_STS becomes 1. The DSP should usualy set/clear this bit at initial configuration.
[3]	**CLIP**	**System Clipping** This bit enables CLIP event to generate Combined HW Indications interrupt (INT6). When this bit is set to 1, INT6 will be generated to the DSP Core whenever the corresponding bit in HW_INT_STS becomes 1. The DSP should usualy set/clear this bit at initial configuration.
[2]	**LVD**	**Low Voltage Detection** This bit enables UVLO event to generate Combined HW Indications interrupt (INT6). When this bit is set to 1, INT6 will be generated to the DSP Core whenever the corresponding bit in HW_INT_STS becomes 1. The DSP should usualy set/clear this bit at initial configuration.
[1]	**OVP**	**Over Voltage Protection** This bit enables OVP event to generate Combined HW Indications interrupt (INT6). When this bit is set to 1, INT6 will be generated to the DSP Core whenever the corresponding bit in HW_INT_STS becomes 1. The DSP should usualy set/clear this bit at initial configuration.
[0]	**Reserved**	

System Interrupt Enable (HW_INT_EN)

Register	Offset	R/W	Description	Reset Value
HW_INT_EN	REGS_BA+0x121	WO	System Interrupt Enable	0xXX

7	6	5	4	3	2	1	0
Reserved SW_HARD_RST			OCP	CLIP	LVD	OVP	Reserved

Bits	Description	
[7:5]	Resreved	
[4]	OCP_OTP	**Over Current / Over Temperature Shutdown** This bit enables the corresponding bit in HW_INT_STS register to latch an OCP_OTP event. When this bit is set to 1, OCP_OTP events will be latched by HW_INT_STS. The DSP should usualy set/clear this bit at initial configuration.
[3]	CLIP	**System Clipping** This bit enables the corresponding bit in HW_INT_STS register to latch a CLIP event. When this bit is set to 1, CLIP events will be latched by HW_INT_STS. The DSP should usualy set/clear this bit at initial configuration.
[2]	LVD	**Low Voltage Detection** This bit enables the corresponding bit in HW_INT_STS register to latch a UVLO event. When this bit is set to 1, UVLO events will be latched by HW_INT_STS. The DSP should usualy set/clear this bit at initial configuration.
[1]	OVP	**Over Voltage Protection** This bit enables the corresponding bit in HW_INT_STS register to latch a OVP event. When this bit is set to 1, OVP events will be latched by HW_INT_STS. The DSP should usualy set/clear this bit at initial configuration.
[0]	Reserved	

System Interrupt Clear (HW_INT_CLR)

Register	Offset	R/W	Description	Reset Value
HW_INT_MASK	REGS_BA+0x122	WO	System Interrupt Clear	0xXX

7	6	5	4	3	2	1	0
Reserved SW_HARD_RST			OCP	CLIP	LVD	OVP	Reserved

Bits	Description	
[7:5]	Resreved	
[4]	OCP	Over Current / Over Temperature Shutdown
[3]	CLIP	System Clipping
[2]	LVD	Low Voltage Detection
[1]	OVP	Over Voltage Protection
[0]	Reserved	

6.5 Control Registers (TBD)

Error: Reference source not found provides detailed information for the NAU83G60 Control Registers. Note that all registers marked as 'Reserved' should not be overwritten, unless it is requested to do so by Nuvoton Technology Corporation.

REG	Function	same as G20	TC9205	New
0	HARDWARE_RST			
1	SOFTWARE_RST			
2	I2C_ADDR			
3	CLK_CTRL			
4	ENA_CTRL			
5	INTERRUPT_CTRL			
6	INT_CLR_STATUS			
7	SAR_CTRL1			
8	GPIO124_CTRL			
9	GPIOOUT			
A	IO_CTRL			
B	I2S0_PCM_CTRL1		V	
C	I2S0_PCM_CTRL2		V	
D	I2S0_PCM_CTRL3		V	
E	I2S0_DATA_CTRL1		V	
F	I2S0_DATA_CTRL2		V	
10	I2S0_DATA_CTRL3		V	
11	I2S0_DATA_CTRL4			V
12	HPF_CTRL			
13	MUTE_CTRL			
14	ADC_VOL_CTRL			
15	LRCK_DIV_CTRL			V
16	BCLK_DIV_CTRL			V
17	I2S0_DATA_CTRL5			V
18	CTRL2			
19	DSP_CORE_CTRL1			
1A	DSP_CORE_CTRL2			
1B	CLK_DOUBLER_O			
1C	RESERVED			
1D	GENERAL_STATUS0			
1E	GENERAL_STATUS1			
1F	GENERAL_STATUS2			

20	SAR_ADC_OUT_01			
21	SAR_ADC_OUT_23			
22	ALC_READOUT1			
23	ALC_READOUT2			
24	ALC_READOUT3			
25	DSP_STATUS_0			
26	DSP_STATUS_1			
27	DSP_STATUS_2			
28	ADC_RATE			
29	DAC_CTRL1			
2A	DAC_CTRL2			
2C	ALC_CTRL1			
2D	ALC_CTRL2			
2E	ALC_CTRL3			
2F	ALC_CTRL4			
30	TEMP_COMP_CTRL			
31	UVLO_CTRL0			
32	UVLO_CTRL1			
33	LPF_CTRL			
38	I2S1_PCM_CTRL1			V
39	I2S1_PCM_CTRL2			V
3A	I2S1_PCM_CTRL3			V
3B	I2S1_DATA_CTRL1			V
3C	I2S1_DATA_CTRL2			V
3D	I2S1_DATA_CTRL3			V
3E	I2S1_DATA_CTRL4			V
3F	I2S1_DATA_CTRL5			V
40	CLK_DET_CTRL			
46	I2C_DEVICE_ID			
4A	ANALOG_READ			

55	MISC_CTRL			
58	I2S2_PCM_CTRL1			V
59	I2S2_PCM_CTRL2			V
5A	I2S2_PCM_CTRL3			V
5B	I2S2_DATA_CTRL1			V
5C	I2S2_DATA_CTRL2			V
5D	I2S2_DATA_CTRL3			V
5E	I2S2_DATA_CTRL4			V
5F	I2S2_DATA_CTRL5			V
60	BIAS_ADJ			
61	ANALOG_CONTROL_1			
62	ANALOG_CONTROL_2			
63	ANALOG_CONTROL_3			
64	ANALOG_CONTROL_4			
65	ANALOG_CONTROL_5			
66	ANALOG_CONTROL_6			
68	ANALOG_CONTROL_7			
69	CLIP_CTRL			
6B	ANALOG_CONTROL_8			
6C	ANALOG_CONTROL_9			
71	ANALOG_ADC_1			
72	ANALOG_ADC_2			
73	RDAC			
76	PGA			
77	FEPGA			
7F	PGA_GAIN			
80-9D	BIQUAD CONTROL			
80-9D	BIQUAD CONTROL			

7 SYSTEM DIAGRAM(TBD)

7.1 Reference System Diagram

A basic system reference diagram is provided in **Figure 42**.

Figure 42 NAU83G60 Simplified System Diagram

7.2 Bill of Materials

A suggested system Bill of Materials (BOM) is provided in **Table 30**.

Table 23 NAU83G60 System Bill of Materials

8 INSTRUCTION SET

To be determined (TBD).

9 Application Reference Circuit (TBD)

Figure 43 provides an example application circuit diagram. **Table 24** provides a suggested Bill of Materials for the example reference circuit.

Figure 43 Application Reference Circuit Diagram

Table 24 NAU83G60 Application Reference Circuit Bill of Materials

10 Package Specification (TBD)

The NAU83G60 stereo Class-D Amplifier with DSP and I/V Sense is available in a small, QFN56 7x7 package, as shown in **Figure 44**.

Figure 44 NAU83G60 Package Specification

11 Ordering Information (TBD)

Nuvoton Part Number Description:

Part Number	Dimension	Package	Package Material
NAU83G60VG	2600mm x 5310mm	WLCSP 50-Balls	Green

NAU83G60xxxVG = Part Name

xxx = Algorithm Option

A00	Waves Audio Enhancement and Speaker Protection algorithm including followings; MaxxEQ, MaxxBass, MaxxVolume, MaxxLeveler, MaxxTreble, MaxxStereo, MaxxDialog, Multiband Compressor.
	Klippel - KCS

V = indicates WLCSP packaging

G = Lead-Free (Green) Packaging

12 Revision History

Version			Description
#	Date	Page(s)	
0.01	11/14/2020	All	Taken from NAU8331 preliminary datasheet Rev 0.01
0.02	12/03/2020	All	Update pin assignment and block diagram
0.03	01/07/2021	All	Update pin assignment and features.
0.04	01/14/2021	All	Update clock tree and and power tree and pin assignment Update the ALC/UVLOP function block Update the level of INT
0.05	03/27/2021	All	Update the pin assignment and block diagram

13 Important Notice

Nuvoton Products are neither intended nor warranted for usage in systems or equipment, any malfunction or failure of which may cause loss of human life, bodily injury or severe property damage. Such applications are deemed, "Insecure Usage".

Insecure usage includes, but is not limited to: equipment for surgical implementation, atomic energy control instruments, airplane or spaceship instruments, the control or operation of dynamic, brake or safety systems designed for vehicular use, traffic signal instruments, all types of safety devices, and other applications intended to support or sustain life.

All Insecure Usage shall be made at customer's risk, and in the event that third parties lay claims to Nuvoton as a result of customer's Insecure Usage, customer shall indemnify the damages and liabilities thus incurred by Nuvoton.