PLL MOSbius Proposal

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Goal and Motivation

- Help facilitate lab experiments for students in IC design learning PLL theory.
- Have different PFD and VCO blocks and programmable Dividers and Charge Pumps to allow students to observe PLL operation at different frequencies and learn trade-offs between various PLL configurations and designs.

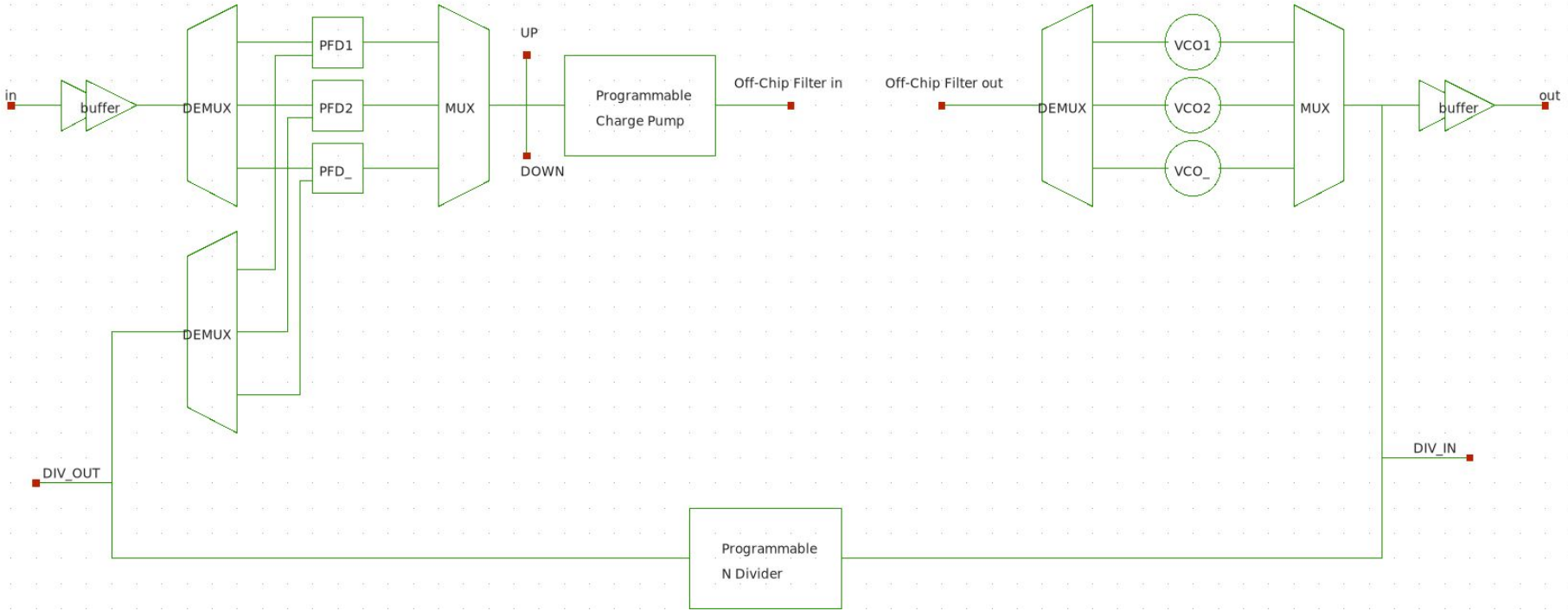
- Goal: Would eventually like to use the PLL MOSbius in a AM and/or FM radio receiver and/or transmitter block which would require a frequency range of around 1MHz to 100MHz.
    - For now, assumption is made that the reference frequency from an off-chip crystal oscillator (put through a reference divider) will be 10kHz.

Brainstorming Ideas

- PFD (Phase-Frequency Detector):
  - DFF / AND Gate PFD,
  - Zero Dead Zone PFD,
  - XOR PFD, …
- Charge Pump:
  - Programmable currents ranging from TBD to TBD
- VCO (Voltage Controlled Oscillator):
  - Current Starved Ring VCO,
  - LC VCO,
  - Relaxation VCO, …
- N Divider:
  - Divide-by-2 DFF Frequency Divider,
  - Dual-Modulus Prescaler, …
  - Integer N ranging from 1 to ~20

- In the future, also need to start thinking about noise.

Block Diagram / Demo



Educational Considerations

- The key unique of our PLL design is “flexibility” (like the 1st MOSbius), by programming the selection of the MUX, students can analyze the differences/results caused by different units in the PLL.

  Example: PD/PFD can be made using an XOR gate, a 2 DFF + AND + Delay configuration, or using Dynamic Logic. Students can connect different circuits as their PD/PFD so they can analyze the trade-offs between each design (like impact of cycle slipping when using an XOR as the PD or when working in lower frequencies using a dynamic PFD)

  In addition, since the filter unit is off-chip, students can connect different values of R-C to analyze the effect it brings to the PLL feedback system (like importance of a zero from RC filter for the whole system’s stability).

  Also, it provides options to link with the 1st generation MOSbius which can perform active filtering, or an LC oscillator function.

On-Chip Analog Measurement MUX and Buffer

- The MUXes are used for selecting different design blocks to construct the PLL with different specifications; the Buffers are used to reduce glitches and spurs, to improve noise behavior, and to adjust the driving strength between different blocks.

  For MUX: need to be designed as an analog MUX, since the input reference clock and VCO output are both sinusoidal waves; transmission gates will be used, so the "on" resistance needs to be carefully considered to avoid affecting the amplitude of the analog signal or noise, etc. First, we need to design the other blocks to confirm the number of channels and the i/o resistance and capacitance of each block.

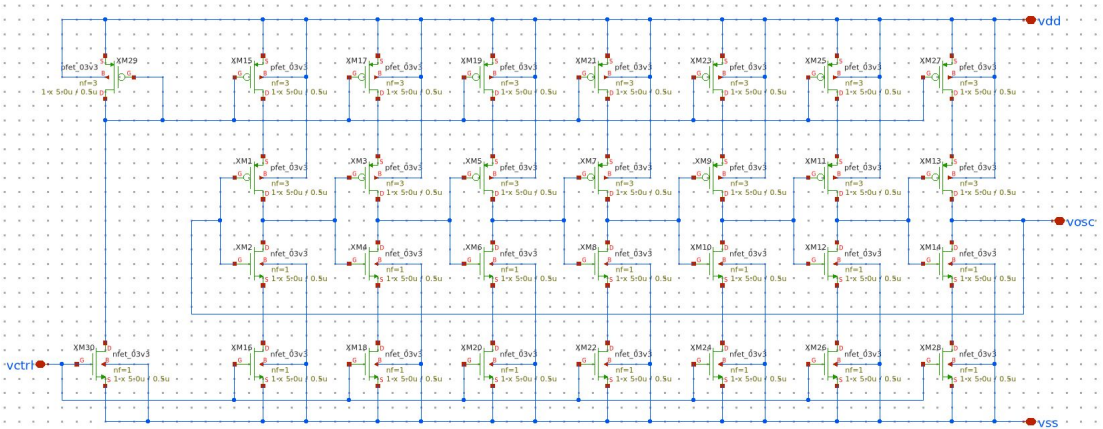
  For Buffer: can use a source follower if we need sinusoidal wave at output of PLL, but we need to consider the output range drop caused by the SF. Otherwise, we can use a Schmitt trigger if we need square wave at the output, since it's better for removing noise and glitches than single inverters, while reducing risks of small parasitic pulses close to rising/falling edges.

Proof of Concept - Overview

- 7-Stage Current-Starved Ring VCO
- DFF Frequency Divider (N = 8)
- PFD - 2 DFF / 1 AND / 1 Delay
- Charge Pump - Basic Charge Pump
- Filter (off-chip) - RC / C Filter

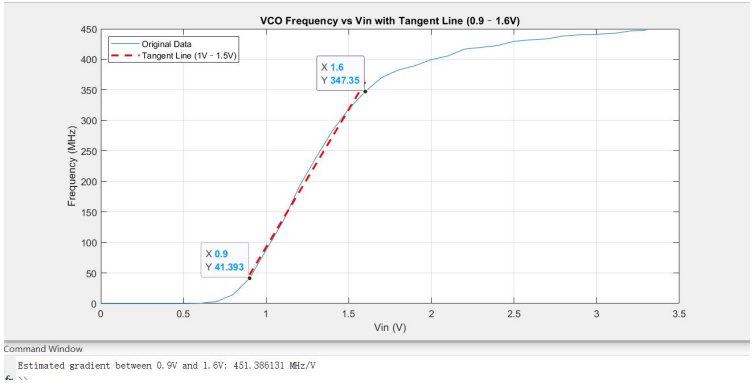
Proof of Concept - 7-Stage Current Starved Ring VCO

Current Starved Ring VCO Schematic

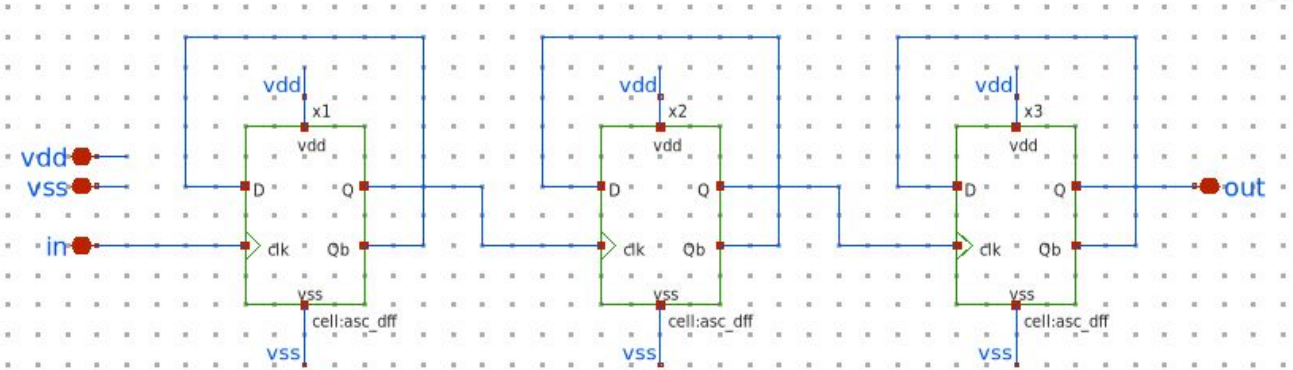


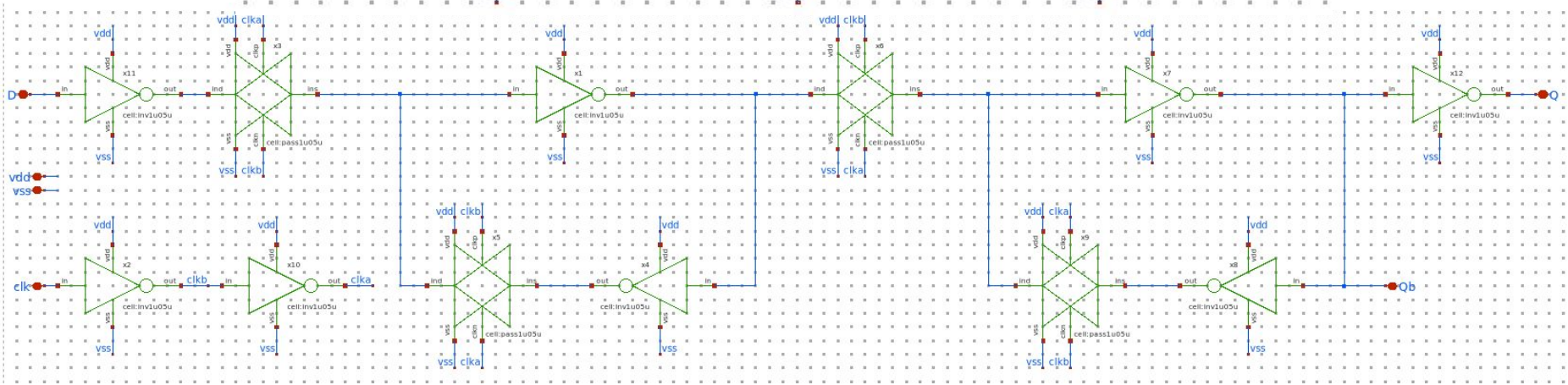
VCO Characteristic
(Gain Curve of Frequency VS Control Voltage)

- VCO Gain (Kv) = 451.386MHz/V

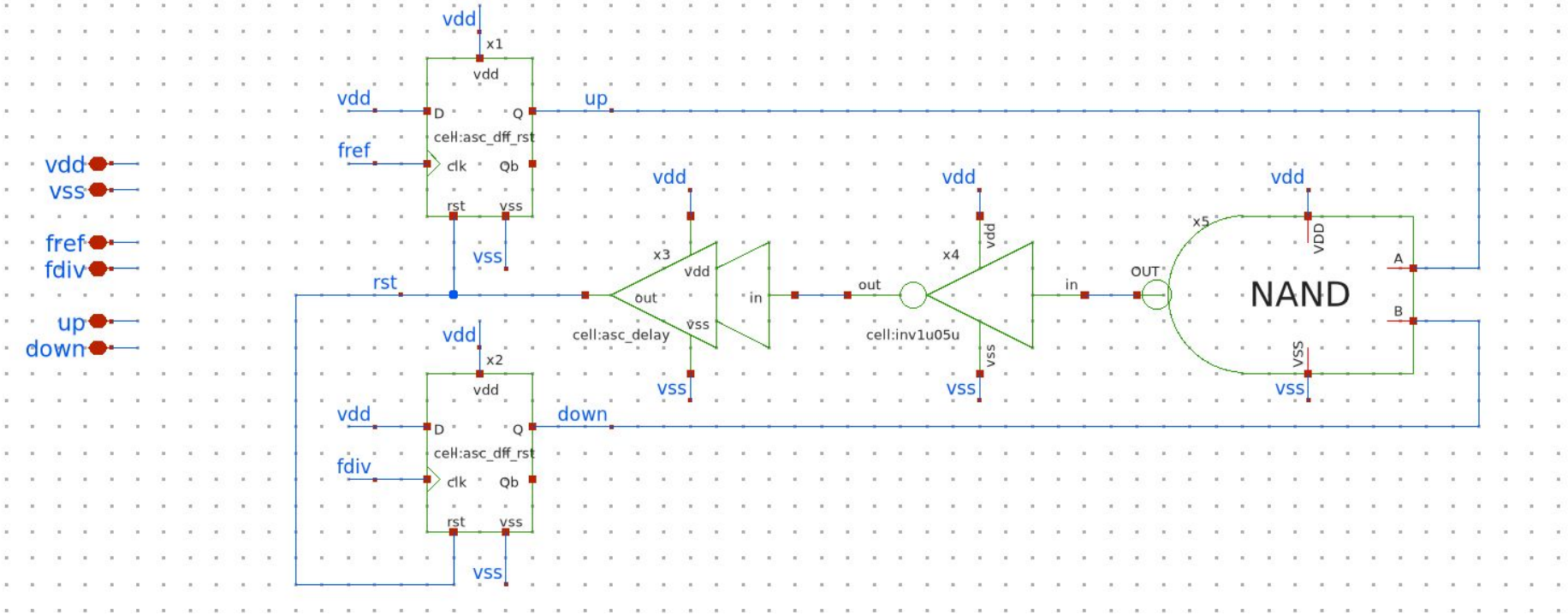


Proof of Concept - DFF Frequency Divider

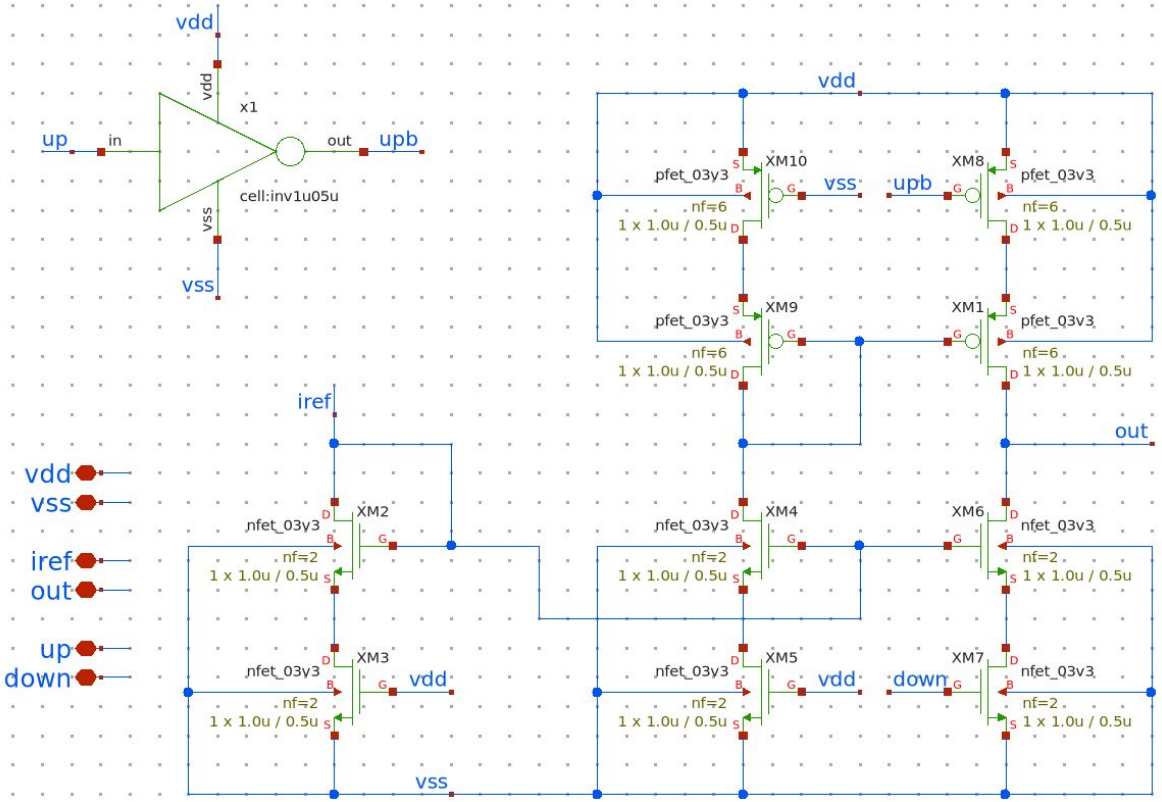




Proof of Concept - DFF / AND Based PFD



Proof of Concept - Basic Charge Pump



Proof of Concept - Off-Chip 2n-order RC Filter

Example of Calculation of R-C Filter Design for PLL system
with 60 degree phase margin and 50 kHz bandwidth

$$\frac{\omega_p}{\omega_z} = \frac{C_1+C_2}{R_1 C_1 C_2} \cdot R_1 C_1 = \frac{C_1+C_2}{C_2} \Rightarrow C_2 = (C_1+C_2)\frac{\omega_z}{\omega_p}$$

$$\therefore \begin{cases} C_2 = \frac{1}{N}\frac{I_p}{2\pi}\frac{K_{VCO}}{\omega_u^2}\sqrt{\frac{\omega_z}{\omega_p}} \\ C_1 = C_2\left(\frac{\omega_p}{\omega_z}-1\right) \\ R_1 = \frac{1}{C_1\omega_z} \end{cases}$$

generally: $\omega_u < \frac{1}{10}\omega_{ref}$

example: $N=8$, $I_p = 100uA$, $K_{VCO} = 451.38\,MHz/V$

$\omega_{ref} = 2\pi \times 500KHz$. $\omega_u = 2\pi \times 50KHz$.

$PM = 60°$.

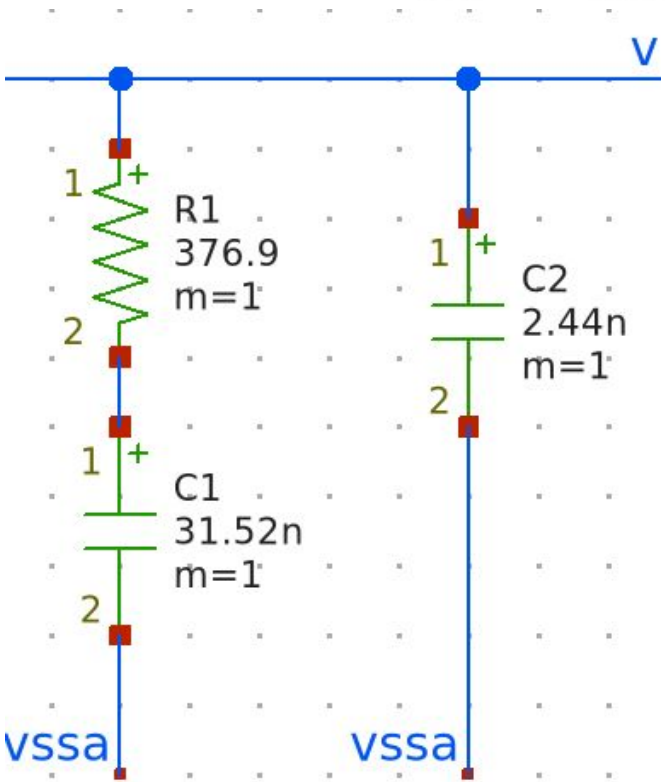
$\omega_p = \omega_u \frac{\cos 60°}{1-\sin 60°}$, $\omega_z = \omega_u \frac{1-\sin 60°}{\cos 60°}$

$C_2 = \frac{1}{8} \times \frac{100uA}{2\pi} \times \frac{451.38\,MHz/V}{2\pi^2 \times 50kHz^2} \times \frac{1-\sin 60°}{\cos 60°}$

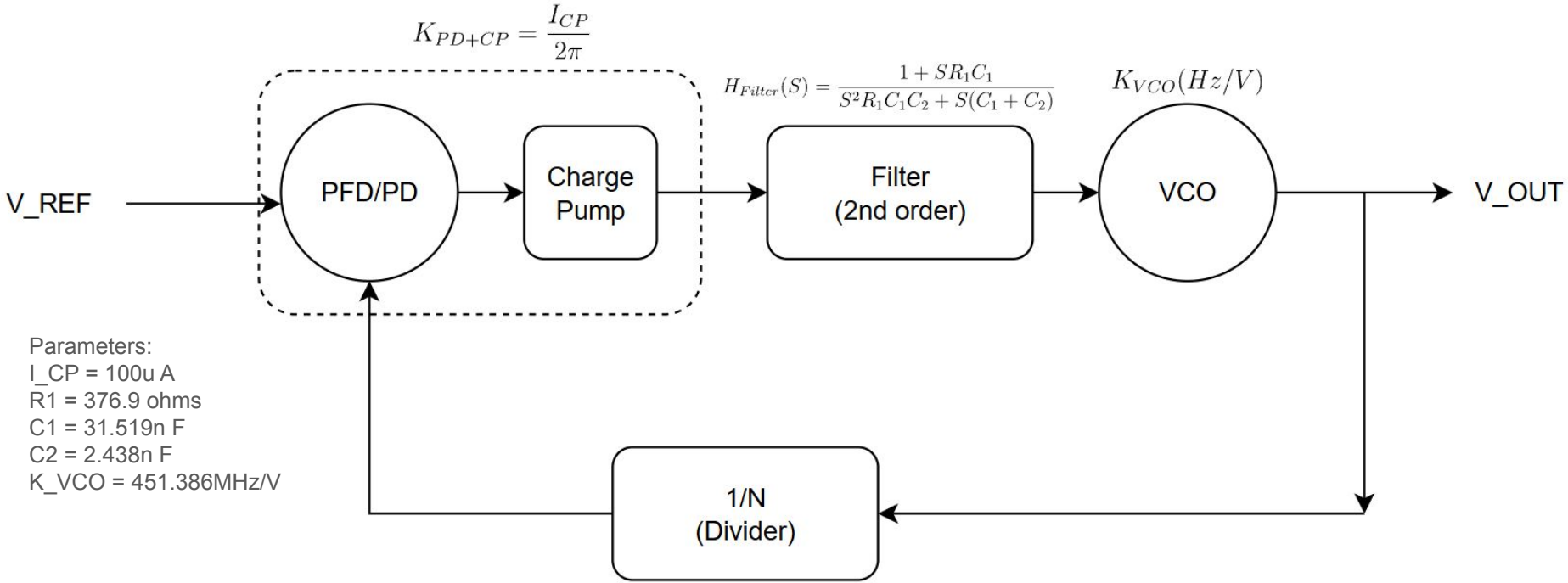
$= 2.438\,nF$

$C_1 = C_2 \times \left[\left(\frac{\cos 60°}{1-\sin 60°}\right)^2 - 1\right] = 12.928\,C_2 = 31.519\,nF$

$R_1 = 376.90\,\Omega$.



Proof of Concept - PLL Behaviour Level Design

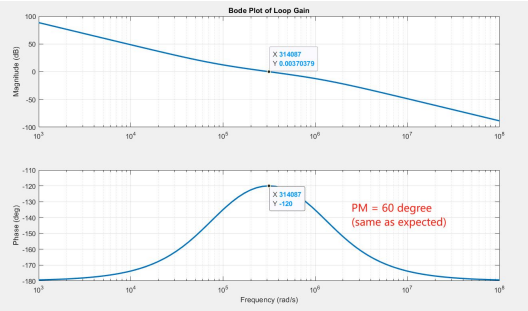


Parameters:
I_CP = 100u A
R1 = 376.9 ohms
C1 = 31.519n F
C2 = 2.438n F
K_VCO = 451.386MHz/V

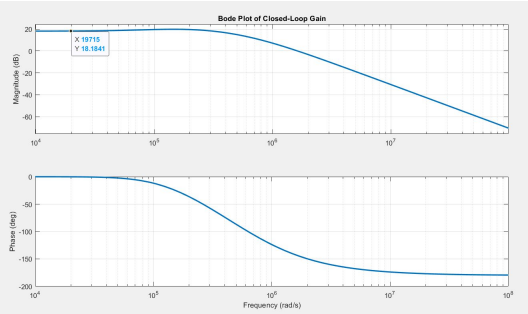
Proof of Concept - PLL Behaviour Level Simulation

1. Loop Gain Simulation

- BW = 314k rad/s ~50kHz
- Phase Margin = 60 degrees

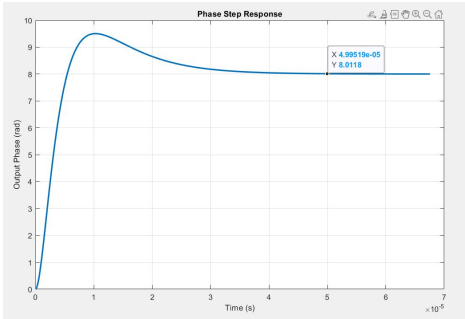


2. Closed-Loop Simulation



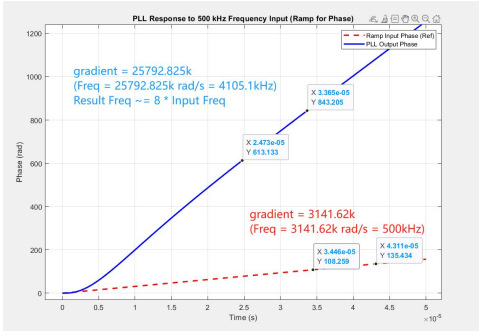
3. Phase Step Response

- Settling Time ~= 50us



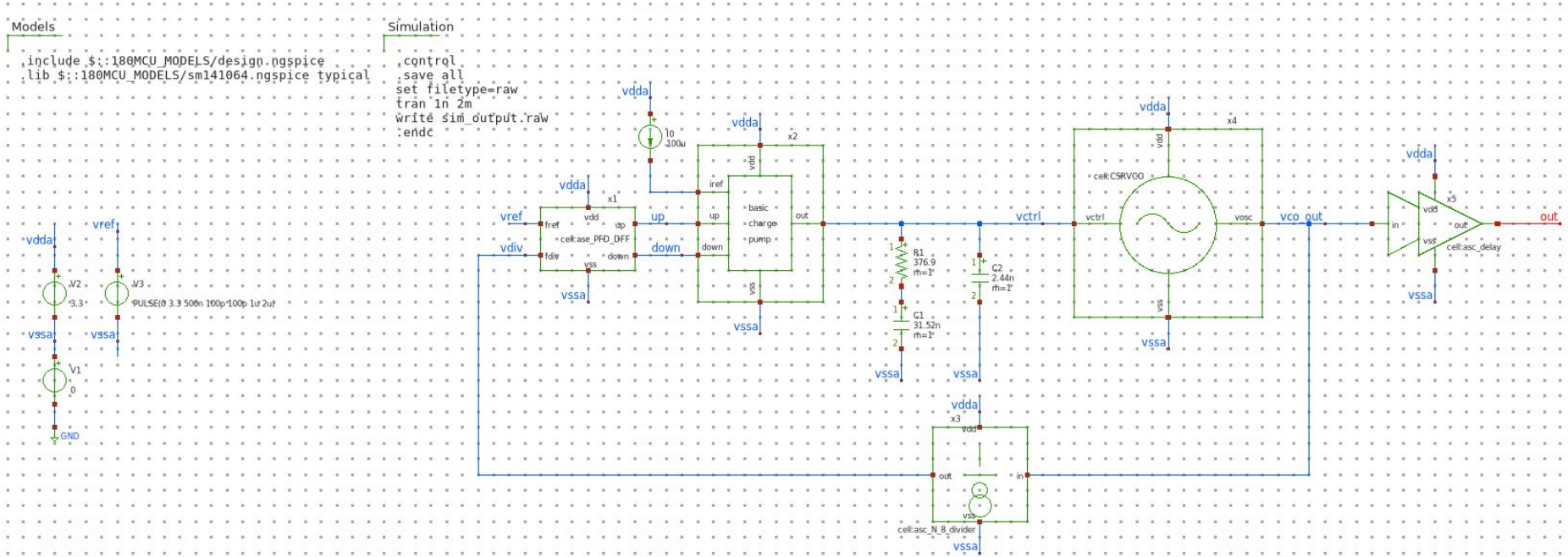
4. Frequency Step Response

(also is the phase ramp response)

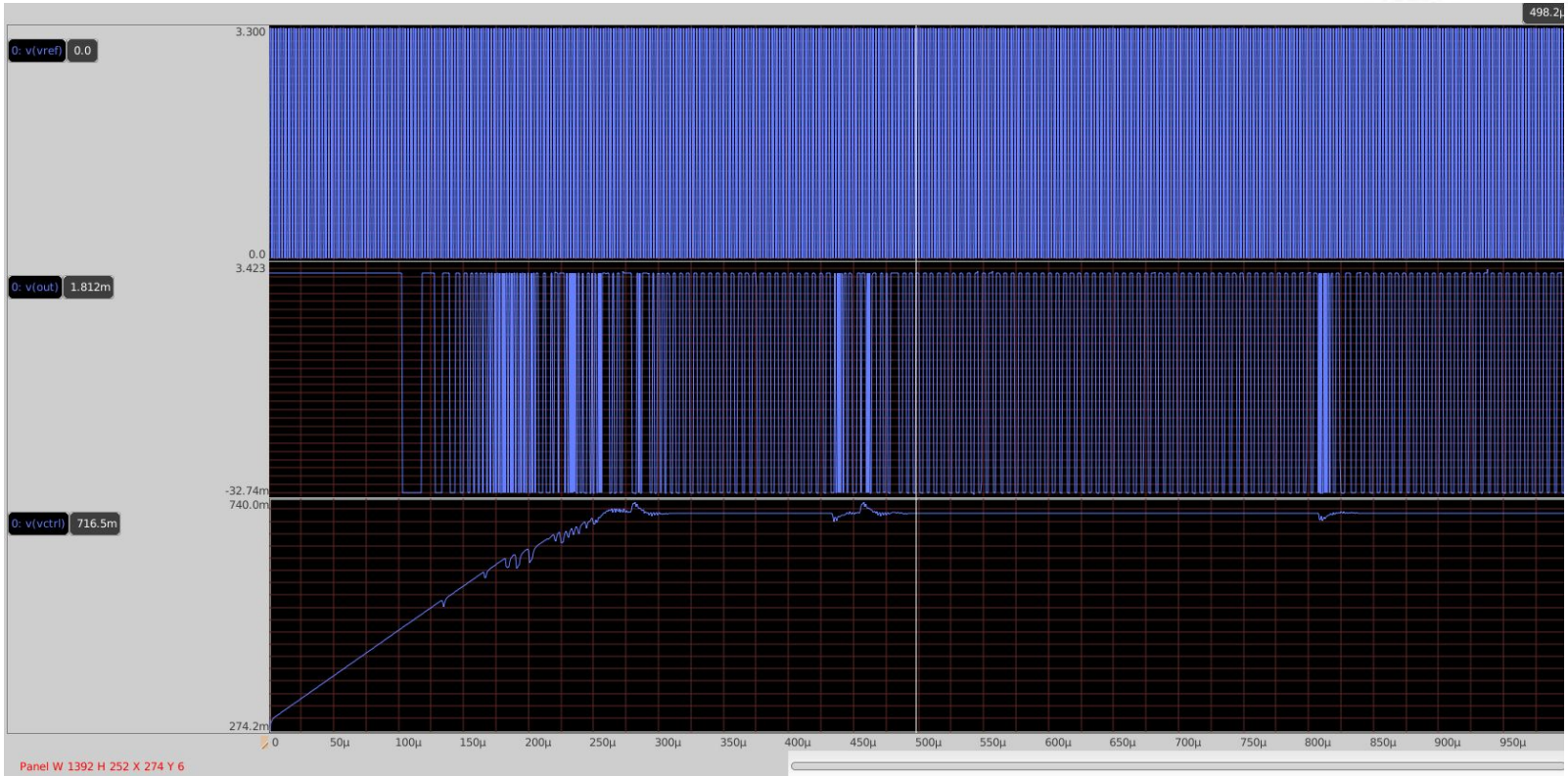


Proof of Concept - PLL Circuit Level Simulation

- 3.3V Supply Voltage
- 100uA Charge Pump Current
- Input Frequency of 500kHz
- Target Output Frequency of 500k * 8 = 4MHz

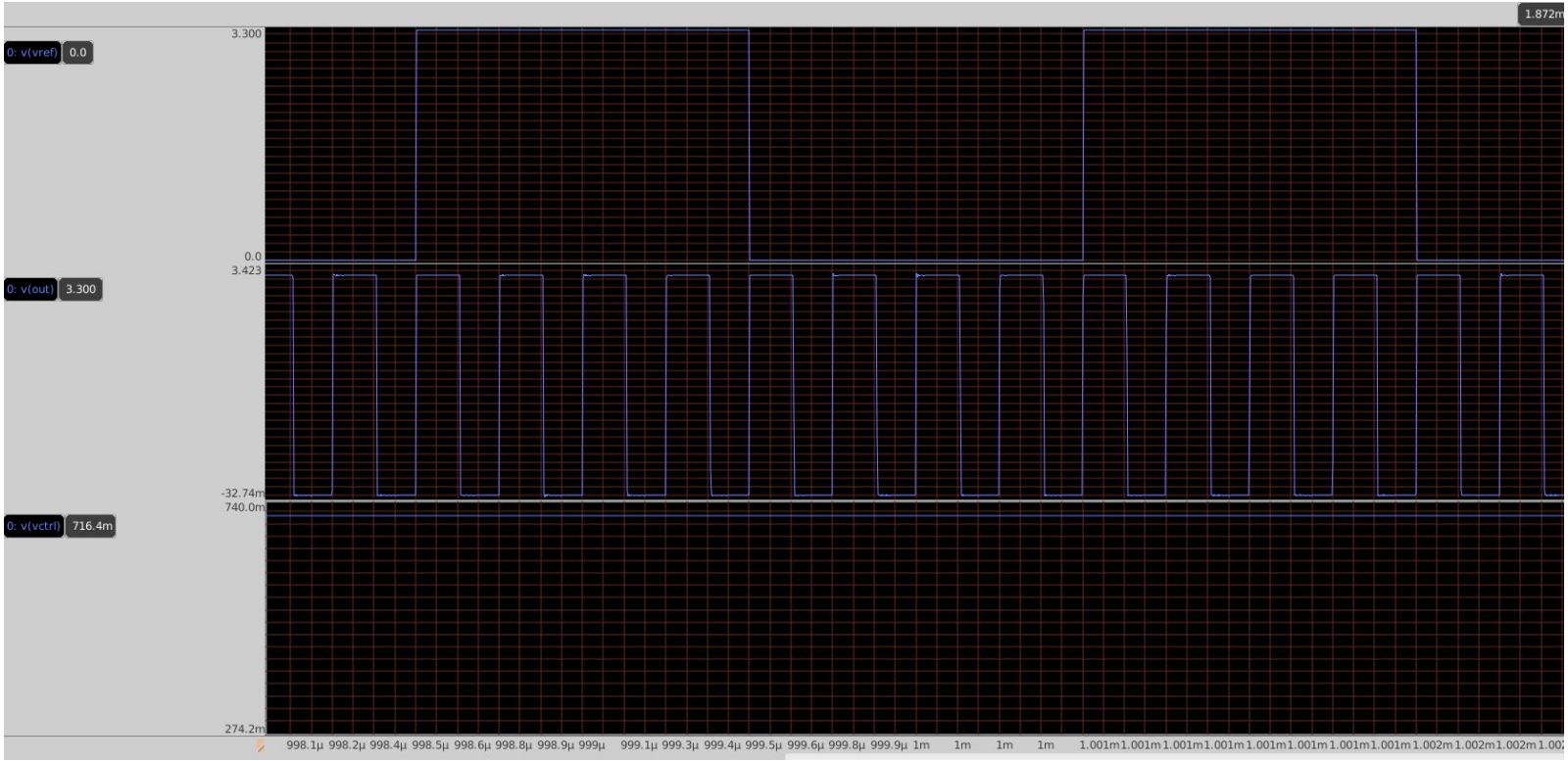


Proof of Concept - Result (1)



Proof of Concept - Result (2)

- Proved that the proposed PLL can achieve target output frequency of 4MHz with 500kHz input



Pin-List

Pin Name	Function
VDD	
VSS	
EN	Enable of Digital Program
CLK	CLK for registers (program CLK)
DATA	register data input
REF_IN	Reference Voltage Input to PLL
PLL_OUT	Output of PLL
PFD_1_IN	Input of DFF PFD
PFD_1_OUT	Output of DFF PFD
PFD_2_IN	Input of XOR PD
PFD_2_OUT	Output of XOR PD
PFD_x_IN	*Input of PFD Option 3 ... TBD (dynamic PFD)*
PFD_x_OUT	*Output of PFD Option 3 ... TBD (dynamic PFD)*
VCO_1_IN	Input of Current Starved VCO
VCO_1_OUT	Output of Current Starved VCO
VCO_2_IN	Input of Relaxation VCO
VCO_2_OUT	Output of Relaxation VCO
VCO_x_IN	*Input of PFD Option 3 ... TBD (Off-CHIP LC VCO)*
VCO_x_OUT	*Output of PFD Option 3 ... TBD (Off-CHIP LC VCO)*
FILTER_IN	Input to the Filter (Off Chip)
Filter_OUT	Output of (Off Chip) Filter
DIV_IN	Input of Divider
DIV_OUT	Output of Divider
CP_IN	Input to Charge Pump (Current Input)
CP_OUT	Output of Charge Pump

Schedule and Timeline

Deadline	**Task**
July 11th	Project Proposal
August 8st	Schematics (Blocks and Top-Level)
September 5th	Layout (DRC, LVS Clean)
September 19th	Verification Simulations (Top-Level w/ PEX)
September 26th	Tape-Out (GDS)

If Time Allows…

- DLL
- Quadrature Output from PLL (-> Local Oscillator for Transceiver)
- Fractional - N
- On-Chip Filter (Biquad, Gm-C, …)
- Mixer

- Which will potentially have additional demos like DLL, and Zero-IF Transceiver