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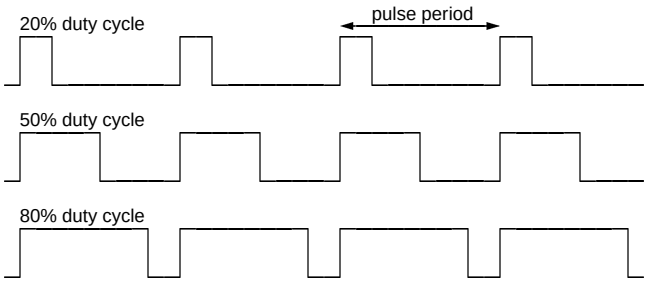
1 PWM

1.1 Introduction

Pulse Width Modulation (PWM) is a pulse width modulated digital signal where a duty cycle is the ratio of high pulse time of the pulse period. Below is a PWM signal with a duty cycle of 20%, 50% and 80% sketched.



1.2 Design constraints

1.3 Features

- 32-bit OPB slave interface.
- Up to 16 PWM driver instances.
- up to 32 bit Frequency divider and 32 bit signed PWM duty width.
- 2 Phase chopping, 1 Phase Chopping and Enable Chopping.

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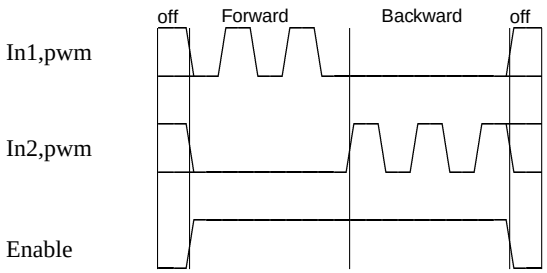
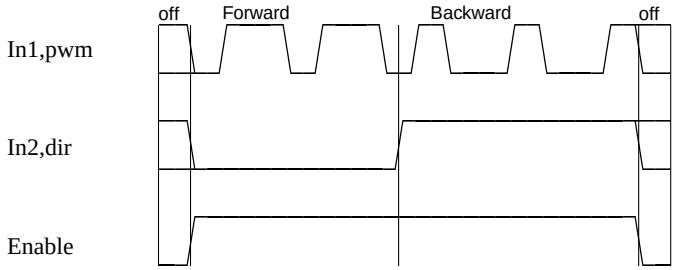
1.4 Design implementation

We have implemented 3 different types of PWM-generators: 2-phase, 1-phase and enable chopping. The types are different in the way they represent the output. The following timing diagrams show this difference.

The **2-phase chopping** outputs a PWM on either out1 or out2. If PWM is on out1 the direction is forward. If on out2 the direction is backward. Enable is used to turn power on and off. This type is chosen with the generic C_PWM_TYPE=0 and is the default.



In **1-Phase chopping** PWM is output on out1. Out2 determines the direction of drive. Notice that when out2 goes high the PWM output on out1 is mirrored. This type is choosen with C_PWM_TYPE=1.



Enable chopping is chosen by setting C_PWM_TYPE = 2. In this mode the PWM signal is routed to the enable pin and out1,out2 chooses the direction.