Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	IO Performance	E144 *(2)*
1A	VREFB1N0	IO	ADC1IN1		DIFFIO_RX_L1n	DIFFOUT_L1n	Low_Speed	6
1A	VREFB1N0	IO	ADC1IN2		DIFFIO_RX_L1p	DIFFOUT_L1p	Low_Speed	7
1A	VREFB1N0	IO	ADC1IN3		DIFFIO_RX_L3n	DIFFOUT_L3n	Low_Speed	8
1A	VREFB1N0	IO	ADC1IN4		DIFFIO_RX_L3p	DIFFOUT_L3p	Low_Speed	10
1A	VREFB1N0	IO	ADC1IN5		DIFFIO_RX_L5n	DIFFOUT_L5n	Low_Speed	11
1A	VREFB1N0	IO	ADC1IN6		DIFFIO_RX_L5p	DIFFOUT_L5p	Low_Speed	12
1A	VREFB1N0	IO	ADC1IN7		DIFFIO_RX_L7n	DIFFOUT_L7n	Low_Speed	13
1A	VREFB1N0	IO	ADC1IN8		DIFFIO_RX_L7p	DIFFOUT_L7p	Low_Speed	14
1B	VREFB1N0	IO		JTAGEN				15
1B	VREFB1N0	IO		TMS	DIFFIO_RX_L11n	DIFFOUT_L11n	Low_Speed	16
1B	VREFB1N0	IO	VREFB1N0					17
1B	VREFB1N0	IO		TCK	DIFFIO_RX_L11p	DIFFOUT_L11p	Low_Speed	18
1B	VREFB1N0	IO		TDI	DIFFIO_RX_L12n	DIFFOUT_L12n	Low_Speed	19
1B	VREFB1N0	IO		TDO	DIFFIO_RX_L12p	DIFFOUT_L12p	Low_Speed	20
1B	VREFB1N0	IO			DIFFIO_RX_L14n	DIFFOUT_L14n	Low_Speed	21
1B	VREFB1N0	IO			DIFFIO_RX_L14p	DIFFOUT_L14p	Low_Speed	22
1B	VREFB1N0	IO			DIFFIO_RX_L16n	DIFFOUT_L16n	Low_Speed	24
1B	VREFB1N0	IO			DIFFIO_RX_L16p	DIFFOUT_L16p	Low_Speed	25
2	VREFB2N0	IO	CLK0n		DIFFIO_RX_L18n	DIFFOUT_L18n	High_Speed	26
2	VREFB2N0	IO	CLK0p		DIFFIO_RX_L18p	DIFFOUT_L18p	High_Speed	27
2	VREFB2N0	IO	CLK1n		DIFFIO_RX_L20n	DIFFOUT_L20n	High_Speed	28
2	VREFB2N0	IO	CLK1p		DIFFIO_RX_L20p	DIFFOUT_L20p	High_Speed	29
2	VREFB2N0	IO	VREFB2N0					30
2	VREFB2N0	IO	PLL_L_CLKOUTn		DIFFIO_RX_L27n	DIFFOUT_L27n	High_Speed	32
2	VREFB2N0	IO	PLL_L_CLKOUTp		DIFFIO_RX_L27p	DIFFOUT_L27p	High_Speed	33
3	VREFB3N0	IO			DIFFIO_TX_RX_B1n	DIFFOUT_B1n	High_Speed	38
3	VREFB3N0	IO			DIFFIO_TX_RX_B1p	DIFFOUT_B1p	High_Speed	39
3	VREFB3N0	IO			DIFFIO_TX_RX_B3n	DIFFOUT_B3n	High_Speed	41
3	VREFB3N0	IO			DIFFIO_TX_RX_B3p	DIFFOUT_B3p	High_Speed	43
3	VREFB3N0	IO			DIFFIO_TX_RX_B5n	DIFFOUT_B5n	High_Speed	44
3	VREFB3N0	IO			DIFFIO_TX_RX_B5p	DIFFOUT_B5p	High_Speed	45
3	VREFB3N0	IO			DIFFIO_TX_RX_B7n	DIFFOUT_B7n	High_Speed	46
3	VREFB3N0	IO			DIFFIO_TX_RX_B7p	DIFFOUT_B7p	High_Speed	47
3	VREFB3N0	IO			DIFFIO_TX_RX_B9n	DIFFOUT_B9n	High_Speed	50
3	VREFB3N0	IO	VREFB3N0					48
3	VREFB3N0	IO			DIFFIO_TX_RX_B9p	DIFFOUT_B9p	High_Speed	52
3	VREFB3N0	IO						54
3	VREFB3N0	IO			DIFFIO_TX_RX_B12n	DIFFOUT_B12n	High_Speed	55
3	VREFB3N0	IO			DIFFIO_TX_RX_B12p	DIFFOUT_B12p	High_Speed	56
3	VREFB3N0	IO			DIFFIO_TX_RX_B14n	DIFFOUT_B14n	High_Speed	57
3	VREFB3N0	IO			DIFFIO_TX_RX_B14p	DIFFOUT_B14p	High_Speed	58
3	VREFB3N0	IO			DIFFIO_TX_RX_B16n	DIFFOUT_B16n	High_Speed	59
3	VREFB3N0	IO			DIFFIO_TX_RX_B16p	DIFFOUT_B16p	High_Speed	60
4	VREFB4N0	IO	VREFB4N0					61
4	VREFB4N0	IO						62
4	VREFB4N0	IO			DIFFIO_TX_RX_B23n	DIFFOUT_B23n	High_Speed	64
4	VREFB4N0	IO			DIFFIO_TX_RX_B23p	DIFFOUT_B23p	High_Speed	65
4	VREFB4N0	IO						66
4	VREFB4N0	IO			DIFFIO_TX_RX_B27n	DIFFOUT_B27n	High_Speed	69
4	VREFB4N0	IO			DIFFIO_TX_RX_B27p	DIFFOUT_B27p	High_Speed	70
5	VREFB5N0	IO			DIFFIO_RX_R1p	DIFFOUT_R1p	High_Speed	75
5	VREFB5N0	IO			DIFFIO_RX_R2p	DIFFOUT_R2p	High_Speed	74
5	VREFB5N0	IO			DIFFIO_RX_R1n	DIFFOUT_R1n	High_Speed	77
5	VREFB5N0	IO			DIFFIO_RX_R2n	DIFFOUT_R2n	High_Speed	76
5	VREFB5N0	IO			DIFFIO_RX_R7p	DIFFOUT_R7p	High_Speed	79
5	VREFB5N0	IO						78
5	VREFB5N0	IO			DIFFIO_RX_R7n	DIFFOUT_R7n	High_Speed	81
5	VREFB5N0	IO	VREFB5N0					80
5	VREFB5N0	IO			DIFFIO_RX_R10p	DIFFOUT_R10p	High_Speed	85
5	VREFB5N0	IO			DIFFIO_RX_R11p	DIFFOUT_R11p	High_Speed	84
5	VREFB5N0	IO			DIFFIO_RX_R10n	DIFFOUT_R10n	High_Speed	87
5	VREFB5N0	IO			DIFFIO_RX_R11n	DIFFOUT_R11n	High_Speed	86
6	VREFB6N0	IO	CLK2p		DIFFIO_RX_R14p	DIFFOUT_R14p	High_Speed	88
6	VREFB6N0	IO	CLK2n		DIFFIO_RX_R14n	DIFFOUT_R14n	High_Speed	89
6	VREFB6N0	IO	CLK3p		DIFFIO_RX_R16p	DIFFOUT_R16p	High_Speed	90
6	VREFB6N0	IO	CLK3n		DIFFIO_RX_R16n	DIFFOUT_R16n	High_Speed	91
6	VREFB6N0	IO			DIFFIO_RX_R18p	DIFFOUT_R18p	High_Speed	92
6	VREFB6N0	IO			DIFFIO_RX_R18n	DIFFOUT_R18n	High_Speed	93
6	VREFB6N0	IO	DPCLK3		DIFFIO_RX_R26p	DIFFOUT_R26p	High_Speed	96
6	VREFB6N0	IO	VREFB6N0					97
6	VREFB6N0	IO	DPCLK2		DIFFIO_RX_R26n	DIFFOUT_R26n	High_Speed	98
6	VREFB6N0	IO			DIFFIO_RX_R27p	DIFFOUT_R27p	High_Speed	99
6	VREFB6N0	IO			DIFFIO_RX_R28p	DIFFOUT_R28p	High_Speed	100
6	VREFB6N0	IO			DIFFIO_RX_R27n	DIFFOUT_R27n	High_Speed	101
6	VREFB6N0	IO			DIFFIO_RX_R28n	DIFFOUT_R28n	High_Speed	102
6	VREFB6N0	IO			DIFFIO_RX_R33p	DIFFOUT_R33p	High_Speed	105
6	VREFB6N0	IO			DIFFIO_RX_R33n	DIFFOUT_R33n	High_Speed	106
7	VREFB7N0	IO			DIFFIO_RX_T1p	DIFFOUT_T1p	High_Speed	110
7	VREFB7N0	IO			DIFFIO_RX_T1n	DIFFOUT_T1n	High_Speed	111
7	VREFB7N0	IO	VREFB7N0					112
7	VREFB7N0	IO						113
7	VREFB7N0	IO						114
7	VREFB7N0	IO			DIFFIO_RX_T10p	DIFFOUT_T10p	High_Speed	118
7	VREFB7N0	IO			DIFFIO_RX_T10n	DIFFOUT_T10n	High_Speed	119
8	VREFB8N0	IO			DIFFIO_RX_T16p	DIFFOUT_T16p	Low_Speed	120
8	VREFB8N0	IO		DEV_CLRn	DIFFIO_RX_T16n	DIFFOUT_T16n	Low_Speed	121
8	VREFB8N0	IO		DEV_OE				122
8	VREFB8N0	IO	VREFB8N0					123
8	VREFB8N0	IO		CONFIG_SEL				126

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	IO Performance	E144 *(2)*
8	VREFB8N0	IO			DIFFIO_RX_T19p	DIFFOUT_T19p	Low_Speed	124
8	VREFB8N0	Input_only		nCONFIG				129
8	VREFB8N0	IO			DIFFIO_RX_T19n	DIFFOUT_T19n	Low_Speed	127
8	VREFB8N0	IO			DIFFIO_RX_T20p	DIFFOUT_T20p	Low_Speed	130
8	VREFB8N0	IO			DIFFIO_RX_T20n	DIFFOUT_T20n	Low_Speed	131
8	VREFB8N0	IO			DIFFIO_RX_T22p	DIFFOUT_T22p	Low_Speed	132
8	VREFB8N0	IO		CRC_ERROR	DIFFIO_RX_T22n	DIFFOUT_T22n	Low_Speed	134
8	VREFB8N0	IO						135
8	VREFB8N0	IO		nSTATUS	DIFFIO_RX_T24p	DIFFOUT_T24p	Low_Speed	136
8	VREFB8N0	IO		CONF_DONE	DIFFIO_RX_T24n	DIFFOUT_T24n	Low_Speed	138
8	VREFB8N0	IO			DIFFIO_RX_T26p	DIFFOUT_T26p	Low_Speed	140
8	VREFB8N0	IO			DIFFIO_RX_T26n	DIFFOUT_T26n	Low_Speed	141
		GND						95
		GND						83
		GND						68
		GND						63
		GND						53
		GND						42
		GND						142
		GND						137
		GND						133
		GND						125
		GND						116
		GND						104
		REFGND						4
		VCCIO1A						9
		VCCIO1B						23
		VCCIO2						31
		VCCIO3						49
		VCCIO3						40
		VCCIO4						67
		VCCIO5						82
		VCCIO6						94
		VCCIO6						103
		VCCIO7						117
		VCCIO8						139
		VCCIO8						128
		VCCA1						35
		VCCA2						34
		VCCA3						107
		VCCA4						143
		VCCA5						71
		VCCA6						2
		VCC_ONE						73
		VCC_ONE						72
		VCC_ONE						51
		VCC_ONE						37
		VCC_ONE						36
		VCC_ONE						144
		VCC_ONE						115
		VCC_ONE						109
		VCC_ONE						108
		VCC_ONE						1
		ADC_VREF						5
		ANAIN1						3

Notes:

(1) For more information about pin definition and pin connection guidelines, refer to the MAX 10 FPGA Device Family Pin Connection Guidelines.

(2) The E144-pin package has an exposed ground pad at the bottom of the package. The exposed ground pad is used for electrical connectivity and not for thermal purposes. You must connect the exposed ground pad to the ground plane of the PCB.

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	IO Performance	M153
1A	VREFB1N0	IO	ADC1IN1		DIFFIO_RX_L1n	DIFFOUT_L1n	Low_Speed	D2
1A	VREFB1N0	IO	ADC1IN2		DIFFIO_RX_L1p	DIFFOUT_L1p	Low_Speed	C2
1A	VREFB1N0	IO	ADC1IN3		DIFFIO_RX_L3n	DIFFOUT_L3n	Low_Speed	F5
1A	VREFB1N0	IO	ADC1IN4		DIFFIO_RX_L3p	DIFFOUT_L3p	Low_Speed	G5
1A	VREFB1N0	IO	ADC1IN5		DIFFIO_RX_L5n	DIFFOUT_L5n	Low_Speed	C1
1A	VREFB1N0	IO	ADC1IN6		DIFFIO_RX_L5p	DIFFOUT_L5p	Low_Speed	B1
1A	VREFB1N0	IO	ADC1IN7		DIFFIO_RX_L7n	DIFFOUT_L7n	Low_Speed	E1
1A	VREFB1N0	IO	ADC1IN8		DIFFIO_RX_L7p	DIFFOUT_L7p	Low_Speed	E2
1B	VREFB1N0	IO		JTAGEN				G7
1B	VREFB1N0	IO		TMS	DIFFIO_RX_L11n	DIFFOUT_L11n	Low_Speed	G1
1B	VREFB1N0	IO	VREFB1N0					G2
1B	VREFB1N0	IO		TCK	DIFFIO_RX_L11p	DIFFOUT_L11p	Low_Speed	J1
1B	VREFB1N0	IO		TDI	DIFFIO_RX_L12n	DIFFOUT_L12n	Low_Speed	H5
1B	VREFB1N0	IO		TDO	DIFFIO_RX_L12p	DIFFOUT_L12p	Low_Speed	H4
1B	VREFB1N0	IO			DIFFIO_RX_L14n	DIFFOUT_L14n	Low_Speed	H3
1B	VREFB1N0	IO			DIFFIO_RX_L14p	DIFFOUT_L14p	Low_Speed	J2
1B	VREFB1N0	IO			DIFFIO_RX_L16n	DIFFOUT_L16n	Low_Speed	L1
1B	VREFB1N0	IO			DIFFIO_RX_L16p	DIFFOUT_L16p	Low_Speed	K2
2	VREFB2N0	IO	CLK0n		DIFFIO_RX_L18n	DIFFOUT_L18n	High_Speed	J4
2	VREFB2N0	IO	CLK0p		DIFFIO_RX_L18p	DIFFOUT_L18p	High_Speed	J5
2	VREFB2N0	IO	CLK1n		DIFFIO_RX_L20n	DIFFOUT_L20n	High_Speed	K5
2	VREFB2N0	IO	CLK1p		DIFFIO_RX_L20p	DIFFOUT_L20p	High_Speed	K4
2	VREFB2N0	IO	DPCLK0		DIFFIO_RX_L22n	DIFFOUT_L22n	High_Speed	L5
2	VREFB2N0	IO	VREFB2N0					P1
2	VREFB2N0	IO	DPCLK1		DIFFIO_RX_L22p	DIFFOUT_L22p	High_Speed	L4
2	VREFB2N0	IO						R2
2	VREFB2N0	IO	PLL_L_CLKOUTn		DIFFIO_RX_L27n	DIFFOUT_L27n	High_Speed	N1
2	VREFB2N0	IO	PLL_L_CLKOUTp		DIFFIO_RX_L27p	DIFFOUT_L27p	High_Speed	P2
3	VREFB3N0	IO			DIFFIO_TX_RX_B1n	DIFFOUT_B1n	High_Speed	M4
3	VREFB3N0	IO			DIFFIO_RX_B2n	DIFFOUT_B2n	High_Speed	P3
3	VREFB3N0	IO			DIFFIO_TX_RX_B1p	DIFFOUT_B1p	High_Speed	M5
3	VREFB3N0	IO			DIFFIO_RX_B2p	DIFFOUT_B2p	High_Speed	R3
3	VREFB3N0	IO			DIFFIO_TX_RX_B3n	DIFFOUT_B3n	High_Speed	L6
3	VREFB3N0	IO			DIFFIO_RX_B4n	DIFFOUT_B4n	High_Speed	P4
3	VREFB3N0	IO			DIFFIO_TX_RX_B3p	DIFFOUT_B3p	High_Speed	L7
3	VREFB3N0	IO			DIFFIO_RX_B4p	DIFFOUT_B4p	High_Speed	R5
3	VREFB3N0	IO			DIFFIO_TX_RX_B5n	DIFFOUT_B5n	High_Speed	P6
3	VREFB3N0	IO			DIFFIO_RX_B6n	DIFFOUT_B6n	High_Speed	R7
3	VREFB3N0	IO			DIFFIO_TX_RX_B5p	DIFFOUT_B5p	High_Speed	P7
3	VREFB3N0	IO			DIFFIO_RX_B6p	DIFFOUT_B6p	High_Speed	P8
3	VREFB3N0	IO			DIFFIO_TX_RX_B7n	DIFFOUT_B7n	High_Speed	L8
3	VREFB3N0	IO			DIFFIO_RX_B8n	DIFFOUT_B8n	High_Speed	P9
3	VREFB3N0	IO			DIFFIO_TX_RX_B7p	DIFFOUT_B7p	High_Speed	M7
3	VREFB3N0	IO			DIFFIO_RX_B8p	DIFFOUT_B8p	High_Speed	R9
3	VREFB3N0	IO			DIFFIO_TX_RX_B9n	DIFFOUT_B9n	High_Speed	M8
3	VREFB3N0	IO	VREFB3N0					R11
3	VREFB3N0	IO			DIFFIO_TX_RX_B9p	DIFFOUT_B9p	High_Speed	N8
3	VREFB3N0	IO						P12
3	VREFB3N0	IO			DIFFIO_TX_RX_B10n	DIFFOUT_B10n	High_Speed	R14
3	VREFB3N0	IO			DIFFIO_TX_RX_B10p	DIFFOUT_B10p	High_Speed	P15
3	VREFB3N0	IO			DIFFIO_TX_RX_B12n	DIFFOUT_B12n	High_Speed	L9
3	VREFB3N0	IO			DIFFIO_TX_RX_B12p	DIFFOUT_B12p	High_Speed	M9
3	VREFB3N0	IO			DIFFIO_TX_RX_B14n	DIFFOUT_B14n	High_Speed	L10
3	VREFB3N0	IO			DIFFIO_TX_RX_B14p	DIFFOUT_B14p	High_Speed	M11
3	VREFB3N0	IO			DIFFIO_TX_RX_B16n	DIFFOUT_B16n	High_Speed	P14
3	VREFB3N0	IO			DIFFIO_TX_RX_B16p	DIFFOUT_B16p	High_Speed	R13
5	VREFB5N0	IO			DIFFIO_RX_R1p	DIFFOUT_R1p	High_Speed	M12
5	VREFB5N0	IO			DIFFIO_RX_R2p	DIFFOUT_R2p	High_Speed	N15
5	VREFB5N0	IO			DIFFIO_RX_R1n	DIFFOUT_R1n	High_Speed	L11
5	VREFB5N0	IO			DIFFIO_RX_R2n	DIFFOUT_R2n	High_Speed	N14
5	VREFB5N0	IO			DIFFIO_RX_R7p	DIFFOUT_R7p	High_Speed	K11
5	VREFB5N0	IO						M14
5	VREFB5N0	IO			DIFFIO_RX_R7n	DIFFOUT_R7n	High_Speed	K12
5	VREFB5N0	IO	VREFB5N0					L15
5	VREFB5N0	IO			DIFFIO_RX_R10p	DIFFOUT_R10p	High_Speed	J9
5	VREFB5N0	IO			DIFFIO_RX_R11p	DIFFOUT_R11p	High_Speed	K14
5	VREFB5N0	IO			DIFFIO_RX_R10n	DIFFOUT_R10n	High_Speed	J11
5	VREFB5N0	IO			DIFFIO_RX_R11n	DIFFOUT_R11n	High_Speed	J14
6	VREFB6N0	IO	CLK2p		DIFFIO_RX_R14p	DIFFOUT_R14p	High_Speed	J12
6	VREFB6N0	IO	CLK2n		DIFFIO_RX_R14n	DIFFOUT_R14n	High_Speed	H11
6	VREFB6N0	IO	CLK3p		DIFFIO_RX_R16p	DIFFOUT_R16p	High_Speed	H12
6	VREFB6N0	IO	CLK3n		DIFFIO_RX_R16n	DIFFOUT_R16n	High_Speed	H13
6	VREFB6N0	IO			DIFFIO_RX_R18p	DIFFOUT_R18p	High_Speed	J15
6	VREFB6N0	IO			DIFFIO_RX_R18n	DIFFOUT_R18n	High_Speed	G15
6	VREFB6N0	IO	DPCLK3		DIFFIO_RX_R26p	DIFFOUT_R26p	High_Speed	G11
6	VREFB6N0	IO	VREFB6N0					E15
6	VREFB6N0	IO	DPCLK2		DIFFIO_RX_R26n	DIFFOUT_R26n	High_Speed	G12
6	VREFB6N0	IO						E14
6	VREFB6N0	IO			DIFFIO_RX_R27p	DIFFOUT_R27p	High_Speed	F11
6	VREFB6N0	IO			DIFFIO_RX_R28p	DIFFOUT_R28p	High_Speed	C15
6	VREFB6N0	IO			DIFFIO_RX_R27n	DIFFOUT_R27n	High_Speed	F12
6	VREFB6N0	IO			DIFFIO_RX_R28n	DIFFOUT_R28n	High_Speed	C14
6	VREFB6N0	IO			DIFFIO_RX_R33p	DIFFOUT_R33p	High_Speed	E11
6	VREFB6N0	IO			DIFFIO_RX_R33n	DIFFOUT_R33n	High_Speed	D12
8	VREFB8N0	IO			DIFFIO_RX_T14p	DIFFOUT_T14p	Low_Speed	D11
8	VREFB8N0	IO			DIFFIO_RX_T15p	DIFFOUT_T15p	Low_Speed	B15
8	VREFB8N0	IO			DIFFIO_RX_T14n	DIFFOUT_T14n	Low_Speed	D10
8	VREFB8N0	IO			DIFFIO_RX_T15n	DIFFOUT_T15n	Low_Speed	B14
8	VREFB8N0	IO			DIFFIO_RX_T16p	DIFFOUT_T16p	Low_Speed	C8

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	IO Performance	M153
8	VREFB8N0	IO			DIFFIO_RX_T17p	DIFFOUT_T17p	Low_Speed	B13
8	VREFB8N0	IO		DEV_CLRn	DIFFIO_RX_T16n	DIFFOUT_T16n	Low_Speed	B8
8	VREFB8N0	IO			DIFFIO_RX_T17n	DIFFOUT_T17n	Low_Speed	A14
8	VREFB8N0	IO		DEV_OE	DIFFIO_RX_T18p	DIFFOUT_T18p	Low_Speed	E10
8	VREFB8N0	IO			DIFFIO_RX_T18n	DIFFOUT_T18n	Low_Speed	E9
8	VREFB8N0	IO	VREFB8N0					A13
8	VREFB8N0	IO		CONFIG_SEL				D8
8	VREFB8N0	IO			DIFFIO_RX_T19p	DIFFOUT_T19p	Low_Speed	B12
8	VREFB8N0	Input_only		nCONFIG				E8
8	VREFB8N0	IO			DIFFIO_RX_T19n	DIFFOUT_T19n	Low_Speed	B11
8	VREFB8N0	IO			DIFFIO_RX_T20p	DIFFOUT_T20p	Low_Speed	B7
8	VREFB8N0	IO			DIFFIO_RX_T21p	DIFFOUT_T21p	Low_Speed	A9
8	VREFB8N0	IO			DIFFIO_RX_T20n	DIFFOUT_T20n	Low_Speed	B6
8	VREFB8N0	IO			DIFFIO_RX_T21n	DIFFOUT_T21n	Low_Speed	A11
8	VREFB8N0	IO			DIFFIO_RX_T22p	DIFFOUT_T22p	Low_Speed	D7
8	VREFB8N0	IO			DIFFIO_RX_T23p	DIFFOUT_T23p	Low_Speed	A7
8	VREFB8N0	IO		CRC_ERROR	DIFFIO_RX_T22n	DIFFOUT_T22n	Low_Speed	E7
8	VREFB8N0	IO			DIFFIO_RX_T23n	DIFFOUT_T23n	Low_Speed	A5
8	VREFB8N0	IO		nSTATUS	DIFFIO_RX_T24p	DIFFOUT_T24p	Low_Speed	D6
8	VREFB8N0	IO						B4
8	VREFB8N0	IO		CONF_DONE	DIFFIO_RX_T24n	DIFFOUT_T24n	Low_Speed	E6
8	VREFB8N0	IO			DIFFIO_RX_T26p	DIFFOUT_T26p	Low_Speed	A2
8	VREFB8N0	IO			DIFFIO_RX_T26n	DIFFOUT_T26n	Low_Speed	A3
		GND						R15
		GND						R1
		GND						M6
		GND						M2
		GND						M10
		GND						L12
		GND						J7
		GND						H8
		GND						H14
		GND						G9
		GND						G4
		GND						E5
		GND						E12
		GND						D9
		GND						D5
		GND						B2
		GND						A15
		GND						A1
		REFGND						E4
		VCCIO1A						F2
		VCCIO1B						H2
		VCCIO2						L2
		VCCIO3						P5
		VCCIO3						P11
		VCCIO3						P10
		VCCIO5						L14
		VCCIO6						G14
		VCCIO6						F14
		VCCIO8						B9
		VCCIO8						B5
		VCCIO8						B10
		VCCA1						N2
		VCCA2						D14
		VCCA3						B3
		VCCA4						P13
		VCC_ONE						J8
		VCC_ONE						H9
		VCC_ONE						H7
		VCC_ONE						G8
		ADC_VREF						F4
		ANAIN1						D4

Note:
(1) For more information about pin definition and pin connection guidelines, refer to the
MAX 10 FPGA Device Family Pin Connection Guidelines.

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	IO Performance	U169
1A	VREFB1N0	IO	ADC1IN1		DIFFIO_RX_L1n	DIFFOUT_L1n	Low Speed	D1
1A	VREFB1N0	IO	ADC1IN2		DIFFIO_RX_L1p	DIFFOUT_L1p	Low Speed	C2
1A	VREFB1N0	IO	ADC1IN3		DIFFIO_RX_L3n	DIFFOUT_L3n	Low Speed	E3
1A	VREFB1N0	IO	ADC1IN4		DIFFIO_RX_L3p	DIFFOUT_L3p	Low Speed	E4
1A	VREFB1N0	IO	ADC1IN5		DIFFIO_RX_L5n	DIFFOUT_L5n	Low Speed	C1
1A	VREFB1N0	IO	ADC1IN6		DIFFIO_RX_L5p	DIFFOUT_L5p	Low Speed	B1
1A	VREFB1N0	IO	ADC1IN7		DIFFIO_RX_L7n	DIFFOUT_L7n	Low Speed	F1
1A	VREFB1N0	IO	ADC1IN8		DIFFIO_RX_L7p	DIFFOUT_L7p	Low Speed	E1
1B	VREFB1N0	IO		JTAGEN				E5
1B	VREFB1N0	IO		TMS	DIFFIO_RX_L11n	DIFFOUT_L11n	Low Speed	G1
1B	VREFB1N0	IO	VREFB1N0					H1
1B	VREFB1N0	IO		TCK	DIFFIO_RX_L11p	DIFFOUT_L11p	Low Speed	G2
1B	VREFB1N0	IO		TDI	DIFFIO_RX_L12n	DIFFOUT_L12n	Low Speed	F5
1B	VREFB1N0	IO		TDO	DIFFIO_RX_L12p	DIFFOUT_L12p	Low Speed	F6
1B	VREFB1N0	IO			DIFFIO_RX_L14n	DIFFOUT_L14n	Low Speed	F4
1B	VREFB1N0	IO			DIFFIO_RX_L14p	DIFFOUT_L14p	Low Speed	G4
1B	VREFB1N0	IO			DIFFIO_RX_L16n	DIFFOUT_L16n	Low Speed	H2
1B	VREFB1N0	IO			DIFFIO_RX_L16p	DIFFOUT_L16p	Low Speed	H3
2	VREFB2N0	IO	CLK0n		DIFFIO_RX_L18n	DIFFOUT_L18n	High Speed	G5
2	VREFB2N0	IO			DIFFIO_RX_L19n	DIFFOUT_L19n	High Speed	J1
2	VREFB2N0	IO	CLK0p		DIFFIO_RX_L18p	DIFFOUT_L18p	High Speed	H6
2	VREFB2N0	IO			DIFFIO_RX_L19p	DIFFOUT_L19p	High Speed	J2
2	VREFB2N0	IO	CLK1n		DIFFIO_RX_L20n	DIFFOUT_L20n	High Speed	H5
2	VREFB2N0	IO			DIFFIO_RX_L21n	DIFFOUT_L21n	High Speed	M1
2	VREFB2N0	IO	CLK1p		DIFFIO_RX_L20p	DIFFOUT_L20p	High Speed	H4
2	VREFB2N0	IO			DIFFIO_RX_L21p	DIFFOUT_L21p	High Speed	M2
2	VREFB2N0	IO	DPCLK0		DIFFIO_RX_L22n	DIFFOUT_L22n	High Speed	N2
2	VREFB2N0	IO	VREFB2N0					L1
2	VREFB2N0	IO	DPCLK1		DIFFIO_RX_L22p	DIFFOUT_L22p	High Speed	N3
2	VREFB2N0	IO						L2
2	VREFB2N0	IO	PLL_L_CLKOUTn		DIFFIO_RX_L27n	DIFFOUT_L27n	High Speed	M3
2	VREFB2N0	IO			DIFFIO_RX_L28n	DIFFOUT_L28n	High Speed	K1
2	VREFB2N0	IO	PLL_L_CLKOUTp		DIFFIO_RX_L27p	DIFFOUT_L27p	High Speed	L3
2	VREFB2N0	IO			DIFFIO_RX_L28p	DIFFOUT_L28p	High Speed	K2
3	VREFB3N0	IO			DIFFIO_TX_RX_B1n	DIFFOUT_B1n	High Speed	L5
3	VREFB3N0	IO			DIFFIO_RX_B2n	DIFFOUT_B2n	High Speed	M4
3	VREFB3N0	IO			DIFFIO_TX_RX_B1p	DIFFOUT_B1p	High Speed	L4
3	VREFB3N0	IO			DIFFIO_RX_B2p	DIFFOUT_B2p	High Speed	M5
3	VREFB3N0	IO			DIFFIO_TX_RX_B3n	DIFFOUT_B3n	High Speed	K5
3	VREFB3N0	IO			DIFFIO_RX_B4n	DIFFOUT_B4n	High Speed	N4
3	VREFB3N0	IO			DIFFIO_TX_RX_B3p	DIFFOUT_B3p	High Speed	J5
3	VREFB3N0	IO			DIFFIO_RX_B4p	DIFFOUT_B4p	High Speed	N5
3	VREFB3N0	IO			DIFFIO_TX_RX_B5n	DIFFOUT_B5n	High Speed	N6
3	VREFB3N0	IO			DIFFIO_RX_B6n	DIFFOUT_B6n	High Speed	N7
3	VREFB3N0	IO			DIFFIO_TX_RX_B5p	DIFFOUT_B5p	High Speed	M7
3	VREFB3N0	IO			DIFFIO_RX_B6p	DIFFOUT_B6p	High Speed	N8
3	VREFB3N0	IO			DIFFIO_TX_RX_B7n	DIFFOUT_B7n	High Speed	J6
3	VREFB3N0	IO			DIFFIO_RX_B8n	DIFFOUT_B8n	High Speed	M8
3	VREFB3N0	IO			DIFFIO_TX_RX_B7p	DIFFOUT_B7p	High Speed	K6
3	VREFB3N0	IO			DIFFIO_RX_B8p	DIFFOUT_B8p	High Speed	M9
3	VREFB3N0	IO			DIFFIO_TX_RX_B9n	DIFFOUT_B9n	High Speed	J7
3	VREFB3N0	IO	VREFB3N0					N11
3	VREFB3N0	IO			DIFFIO_TX_RX_B9p	DIFFOUT_B9p	High Speed	K7
3	VREFB3N0	IO						N12
3	VREFB3N0	IO			DIFFIO_TX_RX_B10n	DIFFOUT_B10n	High Speed	M13
3	VREFB3N0	IO			DIFFIO_RX_B11n	DIFFOUT_B11n	High Speed	N10
3	VREFB3N0	IO			DIFFIO_TX_RX_B10p	DIFFOUT_B10p	High Speed	M12
3	VREFB3N0	IO			DIFFIO_RX_B11p	DIFFOUT_B11p	High Speed	N9
3	VREFB3N0	IO			DIFFIO_TX_RX_B12n	DIFFOUT_B12n	High Speed	M11
3	VREFB3N0	IO			DIFFIO_TX_RX_B12p	DIFFOUT_B12p	High Speed	L11
3	VREFB3N0	IO			DIFFIO_TX_RX_B14n	DIFFOUT_B14n	High Speed	J8
3	VREFB3N0	IO			DIFFIO_TX_RX_B14p	DIFFOUT_B14p	High Speed	K8
3	VREFB3N0	IO			DIFFIO_TX_RX_B16n	DIFFOUT_B16n	High Speed	M10
3	VREFB3N0	IO			DIFFIO_TX_RX_B16p	DIFFOUT_B16p	High Speed	L10
5	VREFB5N0	IO			DIFFIO_RX_R1p	DIFFOUT_R1p	High Speed	K10
5	VREFB5N0	IO			DIFFIO_RX_R2p	DIFFOUT_R2p	High Speed	K11
5	VREFB5N0	IO			DIFFIO_RX_R1n	DIFFOUT_R1n	High Speed	J10
5	VREFB5N0	IO			DIFFIO_RX_R2n	DIFFOUT_R2n	High Speed	L12
5	VREFB5N0	IO			DIFFIO_RX_R7p	DIFFOUT_R7p	High Speed	K12
5	VREFB5N0	IO						L13
5	VREFB5N0	IO			DIFFIO_RX_R7n	DIFFOUT_R7n	High Speed	J12
5	VREFB5N0	IO	VREFB5N0					K13
5	VREFB5N0	IO			DIFFIO_RX_R8p	DIFFOUT_R8p	High Speed	J9
5	VREFB5N0	IO			DIFFIO_RX_R9p	DIFFOUT_R9p	High Speed	J13
5	VREFB5N0	IO			DIFFIO_RX_R8n	DIFFOUT_R8n	High Speed	H10
5	VREFB5N0	IO			DIFFIO_RX_R9n	DIFFOUT_R9n	High Speed	H13
5	VREFB5N0	IO			DIFFIO_RX_R10p	DIFFOUT_R10p	High Speed	H9
5	VREFB5N0	IO			DIFFIO_RX_R11p	DIFFOUT_R11p	High Speed	G13
5	VREFB5N0	IO			DIFFIO_RX_R10n	DIFFOUT_R10n	High Speed	H8
5	VREFB5N0	IO			DIFFIO_RX_R11n	DIFFOUT_R11n	High Speed	G12
6	VREFB6N0	IO	CLK2p		DIFFIO_RX_R14p	DIFFOUT_R14p	High Speed	G9
6	VREFB6N0	IO	CLK2n		DIFFIO_RX_R14n	DIFFOUT_R14n	High Speed	G10
6	VREFB6N0	IO	CLK3p		DIFFIO_RX_R16p	DIFFOUT_R16p	High Speed	F13
6	VREFB6N0	IO	CLK3n		DIFFIO_RX_R16n	DIFFOUT_R16n	High Speed	E13
6	VREFB6N0	IO			DIFFIO_RX_R18p	DIFFOUT_R18p	High Speed	F12
6	VREFB6N0	IO			DIFFIO_RX_R18n	DIFFOUT_R18n	High Speed	E12
6	VREFB6N0	IO	DPCLK3		DIFFIO_RX_R26p	DIFFOUT_R26p	High Speed	F9
6	VREFB6N0	IO	VREFB6N0					D13
6	VREFB6N0	IO	DPCLK2		DIFFIO_RX_R26n	DIFFOUT_R26n	High Speed	F10
6	VREFB6N0	IO						C13
6	VREFB6N0	IO			DIFFIO_RX_R27p	DIFFOUT_R27p	High Speed	F8

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	IO Performance	U169
6	VREFB6N0	IO			DIFFIO_RX_R28p	DIFFOUT_R28p	High Speed	B12
6	VREFB6N0	IO			DIFFIO_RX_R27n	DIFFOUT_R27n	High Speed	E9
6	VREFB6N0	IO			DIFFIO_RX_R28n	DIFFOUT_R28n	High Speed	B11
6	VREFB6N0	IO			DIFFIO_RX_R29p	DIFFOUT_R29p	High Speed	C12
6	VREFB6N0	IO			DIFFIO_RX_R30p	DIFFOUT_R30p	High Speed	B13
6	VREFB6N0	IO			DIFFIO_RX_R29n	DIFFOUT_R29n	High Speed	C11
6	VREFB6N0	IO			DIFFIO_RX_R30n	DIFFOUT_R30n	High Speed	A12
6	VREFB6N0	IO			DIFFIO_RX_R31p	DIFFOUT_R31p	High Speed	E10
6	VREFB6N0	IO			DIFFIO_RX_R31n	DIFFOUT_R31n	High Speed	D9
6	VREFB6N0	IO			DIFFIO_RX_R33p	DIFFOUT_R33p	High Speed	D12
6	VREFB6N0	IO			DIFFIO_RX_R33n	DIFFOUT_R33n	High Speed	D11
8	VREFB8N0	IO			DIFFIO_RX_T14p	DIFFOUT_T14p	Low Speed	C10
8	VREFB8N0	IO			DIFFIO_RX_T15p	DIFFOUT_T15p	Low Speed	A8
8	VREFB8N0	IO			DIFFIO_RX_T14n	DIFFOUT_T14n	Low Speed	C9
8	VREFB8N0	IO			DIFFIO_RX_T15n	DIFFOUT_T15n	Low Speed	A9
8	VREFB8N0	IO			DIFFIO_RX_T16p	DIFFOUT_T16p	Low Speed	B10
8	VREFB8N0	IO			DIFFIO_RX_T17p	DIFFOUT_T17p	Low Speed	A10
8	VREFB8N0	IO		DEV_CLRn	DIFFIO_RX_T16n	DIFFOUT_T16n	Low Speed	B9
8	VREFB8N0	IO			DIFFIO_RX_T17n	DIFFOUT_T17n	Low Speed	A11
8	VREFB8N0	IO		DEV_OE	DIFFIO_RX_T18p	DIFFOUT_T18p	Low Speed	D8
8	VREFB8N0	IO			DIFFIO_RX_T18n	DIFFOUT_T18n	Low Speed	E8
8	VREFB8N0	IO	VREFB8N0					B7
8	VREFB8N0	IO		CONFIG_SEL				D7
8	VREFB8N0	IO			DIFFIO_RX_T19p	DIFFOUT_T19p	Low Speed	A7
8	VREFB8N0	Input_only		nCONFIG				E7
8	VREFB8N0	IO			DIFFIO_RX_T19n	DIFFOUT_T19n	Low Speed	A6
8	VREFB8N0	IO			DIFFIO_RX_T20p	DIFFOUT_T20p	Low Speed	B6
8	VREFB8N0	IO			DIFFIO_RX_T21p	DIFFOUT_T21p	Low Speed	A4
8	VREFB8N0	IO			DIFFIO_RX_T20n	DIFFOUT_T20n	Low Speed	B5
8	VREFB8N0	IO			DIFFIO_RX_T21n	DIFFOUT_T21n	Low Speed	A3
8	VREFB8N0	IO			DIFFIO_RX_T22p	DIFFOUT_T22p	Low Speed	E6
8	VREFB8N0	IO			DIFFIO_RX_T23p	DIFFOUT_T23p	Low Speed	B3
8	VREFB8N0	IO		CRC_ERROR	DIFFIO_RX_T22n	DIFFOUT_T22n	Low Speed	D6
8	VREFB8N0	IO			DIFFIO_RX_T23n	DIFFOUT_T23n	Low Speed	B4
8	VREFB8N0	IO		nSTATUS	DIFFIO_RX_T24p	DIFFOUT_T24p	Low Speed	C4
8	VREFB8N0	IO						A5
8	VREFB8N0	IO		CONF_DONE	DIFFIO_RX_T24n	DIFFOUT_T24n	Low Speed	C5
8	VREFB8N0	IO			DIFFIO_RX_T26p	DIFFOUT_T26p	Low Speed	A2
8	VREFB8N0	IO			DIFFIO_RX_T26n	DIFFOUT_T26n	Low Speed	B2
		GND						N13
		GND						N1
		GND						M6
		GND						L9
		GND						J4
		GND						H12
		GND						G7
		GND						F3
		GND						E11
		GND						D5
		GND						C3
		GND						B8
		GND						A13
		GND						A1
		REFGND						E2
		VCCIO1A						F2
		VCCIO1B						G3
		VCCIO2						K3
		VCCIO2						J3
		VCCIO3						L8
		VCCIO3						L7
		VCCIO3						L6
		VCCIO5						J11
		VCCIO5						H11
		VCCIO6						G11
		VCCIO6						F11
		VCCIO8						C8
		VCCIO8						C7
		VCCIO8						C6
		VCCA1						K4
		VCCA2						D10
		VCCA3						D4
		VCCA4						K9
		VCC_ONE						H7
		VCC_ONE						G8
		VCC_ONE						G6
		VCC_ONE						F7
		ADC_VREF						D3
		ANAIN1						D2

Note:
(1) For more information about pin definition and pin connection guidelines, refer to the MAX 10 FPGA Device Family Pin Connection Guidelines.

Date	Version	Changes Made
September 2014	2014.09.22	Initial release.
December 2014	2014.12.15	-Updated the BOOT_SEL pin name to CONFIG_SEL pin name. -Removed differential pair pins for non-differential function support.
May 2015	2015.05.08	Added note (2) to Pin List E144.
December 2016	2016.12.23	Removed I/O performance for single-ended pins.