

Bank Number Pin Name/Function Optional Function(s) Configuration Function Dedicated Tx/Rx Channel Emulated LVDS Output Channel IO Performance E144 (2) /REFB1N0 DIFFIO RX L1n DIFFOUT_L1n Low_Speed ADC1IN2 IFFIO RX L1p DIFFOLIT I 1n Low_Speed DIFFOUT L3n 1A VREFB1N0 ADC1IN3 DIFFIO RX L3n Low Speed REFB1N0 IFFIO RX L3p ADC1IN4 Low Speed Low_Speed DIFFOUT L5p 1A VRFFB1N0 ADC1IN6 DIFFIO RX L5p Low Speed /REFB1N0 ADC1IN7 DIFFIO RX L7n Low Speed ADC1IN8 IFFIO_RX_L7p DIFFOUT_L7p JTAGEN 15 DIFFIO RX L11n DIFFOUT L11n /REFB1N0 Low Speed VREFB1N0 10 VREFB1N0 17 VREFB1N0 DIFFIO RX L11p DIFFOUT L11p Low Speed 18 DIFFIO RX I 12r DIFFOLIT I 12r 19 VREFB1N0 VREFB1N0 DIFFIO RX L12p DIFFOUT_L12p DIFFOUT_L14n Low_Speed Low Speed 10 TDO 20 IFFIO RX L14n IFFIO RX I 14r DIFFOLIT I 14r Low Speed VREFB1N0 VREFB1N0 IO DIFFIO RX L16n DIFFOUT_L16n DIFFOUT_L16p Low_Speed 24 25 DIFFIO RX L16p Low Speed VREFB2N0 CI K0n DIFFIO RX L18r DIFFOUT L18r High_Speed CLK0p DIFFIO RX L18p DIFFOUT_L18p High Speed 27 VREFB2N0 DIFFOUT L20n DIFFIO RX L20n CLK1n High Speed CLK1p High Speed VRFFB2N0 VRFFB2N0 PLL L CLKOUTn DIFFIO RX L27n DIFFOUT L27n High Speed VREFB2N0 VRFFB3N0 DIFFIO_RX_L27p DIFFOUT_L27p High_Speed High_Speed IO PLL L CLKOUTP IFFIO TX RX B1r DIFFIO TX RX B1p DIFFOUT B1p REFB3N0 High Speed 39 VREFB3N0 DIFFIO_TX_RX_B3n DIFFOUT_B3n High_Speed 41 10 High Speed REFR3N0 IFFIO TX RX B5n DIFFOLIT B5r High Speed 44 DIFFIO TX RX B5p DIFFOUT_B5p DIFFOUT_B7n VREFB3N0 High_Speed High_Speed 10 45 /RFFR3N0 DIFFIO TX RX B7n DIFFOLIT B7n High Speed 47 VREFB3N0 IO DIFFIO TX RX B9n DIFFOUT_B9n High_Speed 50 48 /REFB3N0 VREFB3N0 /REFB3N0 DIFFIO TX RX B9r DIFFOUT B9r High Speed VRFFB3N0 54 55 DIFFOUT_B12n VREFB3N0 DIFFIO_TX_RX_B12n High_Speed DIFFIO TX RX B12p DIFFIO TX RX B14n DIFFOUT B12p DIFFOUT B14n 56 57 58 High Speed DIFFIO_TX_RX_B14p DIFFOUT_B14p /REFB3N0 High Speed VREFB3N0 DIFFIO TX RX B16n DIFFOUT B16n 59 10 High Speed DIFFIO TX RX B16r DIFFOLIT B16n 60 VREFB4N0 VREFB4N0 61 62 VREFB4N0 10 DIFFIO_TX_RX_B23n DIFFOUT_B23n High_Speed VRFFB4N0 DIFFIO TX RX B23p DIFFOUT B23p High Speed 65 66 69 VREFB4N0 10 DIFFIO_TX_RX_B27n /REFB4N0 DIFFOUT_B27n High_Speed DIFFOUT_B27p DIFFOUT_R1p DIFFOUT_R2p DIFFIO_TX_RX_B27p IFFIO RX R1p High Speed High_Speed IFFIO_RX_R2p VREFB5N0 DIFFIO RX R1n DIFFOUT_R1n High_Speed VREFB5N0 VREFB5N0 DIFFIO_RX_R2n DIFFIO_RX_R7p DIFFOUT R2n DIFFOUT_R7p High Speed High_Speed DIFFIO RX R7n DIFFOUT R7n High Speed 81 VREFB5N0 VREFB5N0 80 DIFFIO_RX_R10p DIFFOUT_R10p Ю High_Speed 85 DIFFIO RX R11 DIFFOLIT R11n High Speed 84 VRFFB5N0 DIFFIO RX R10n DIFFOUT R10n High Speed 87 VREFB5N0 10 DIFFIO_RX_R11n DIFFOUT_R11n 86 High_Speed DIFFIO RX R14c DIFFOUT R14p DIFFOUT_R14n DIFFOUT_R16p DIFFOUT_R16n High_Speed High_Speed High_Speed VREFB6N0 VREFB6N0 CLK2n CLK3p DIFFIO RX R14r IFFIO_RX_R16p REFB6N0 IFFIO RX R16r High_Speed DIFFIO_RX_R18p DIFFOUT_R18p VREFB6N0 DIFFOUT R18r DIFFIO RX R18n High Speed 93 96 High Spee VREFB6N0 VREFB6N0 DIFFIO RX R26n DIFFOUT R26n VREFR6N0 DPCLK2 High Speed 98 0 /REFB6N0 DIFFIO RX R27p DIFFOUT R27p High Speed 99 DIFFIO_RX_R28p DIFFOUT_R28p 100 High_Speed DIFFIO RX R27r DIFFOLIT R27r High Speed High Speed High_Speed VRFFB6N0 DIFFIO RX R28n DIFFOUT R28n 102 105 VREFB6N0 DIFFIO RX R33n DIFFOUT R33n High_Speed 106 VRFFB7N0 DIFFIO RX T1p DIFFOUT T1p High Speed 110 VREFB7N0 DIFFIO_RX_T1n DIFFOUT_T1n High Speed 111 VREER7N0 VRFFB7N0 113 VREFB7N0 114 VREFB7N0 IFFIO_RX_T10p DIFFOUT_T10p High_Speed 118 VRFFB7N0 DIFFIO RX T10n DIFFOUT T10n High Speed 119 VREFB8N0 DIFFIO RX T16p DIFFOUT T16p Low Speed 120 IFFIO RX T16n 121 VREFB8N0 10 DEV_CLRr DIFFOUT_T16 Low Speed VREFB8N0 122

Pin List E144

VRFFR8N0

8 VREFB8N0

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IO

VREFB8N0

CONFIG_SEL

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Pin Information for the MAX®10 10M08SA Device Version 2016.12.23

now part of I	ntel							Note (1)
Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	IO Performance	E144 (2)
	8 VREFB8N0	IO			DIFFIO_RX_T19p	DIFFOUT_T19p	Low_Speed	124
	8 VREFB8N0	Input only		nCONFIG				129
	8 VREFB8N0	10			DIFFIO RX T19n	DIFFOUT T19n	Low Speed	12
	8 VREFB8N0	10			DIFFIO_RX_T20p	DIFFOUT_T20p	Low Speed	130
	8 VREFB8N0	10			DIFFIO_RX_T20n	DIFFOUT_T20n	Low_Speed	13
	8 VREFB8N0	10			DIFFIO RX T22p	DIFFOUT T22p	Low Speed	13:
	8 VREFB8N0	10		CRC_ERROR	DIFFIO_RX_T22n	DIFFOUT_T22n	Low_Speed	13
	8 VREFB8N0	10						13
	8 VREFB8N0	10		nSTATUS	DIFFIO RX T24p	DIFFOUT T24p	Low Speed	13
	8 VREFB8N0	10		CONF_DONE	DIFFIO_RX_T24n	DIFFOUT_T24n	Low_Speed	13
	8 VREFB8N0	10			DIFFIO_RX_T26p	DIFFOUT_T26p	Low_Speed	14
	8 VREFB8N0	10			DIFFIO RX T26n	DIFFOUT T26n	Low Speed	14
		GND						9
		GND						8
		GND						6
		GND						6
		GND						5
		GND						4
		GND						14
		GND						13
		GND						13
		GND						12
		GND						11
		GND						10
		REFGND						
		VCCIO1A						
		VCCIO1B						2
	1	VCCIO2						3
		VCCIO3						4
		VCCIO3						4
	1	VCCIO4						6
		VCCIO5						8
		VCCIO6						9
		VCCIO6						10
		VCCIO7						11
		VCCIO8						13
	1	VCCIO8					1	12
	1	VCCA1					1	3
	1	VCCA2	†					3
		VCCA3	+					10
		VCCA4				+		14
		VCCA5	+					7
	1	VCCA6	1				 	- '
	1	VCC ONE	1				 	7
		VCC ONE	+					7
	1	VCC ONE	1				 	5
	1	VCC_ONE	1			+	1	3
	1	VCC ONE	1				<u> </u>	3
	+	VCC ONE	+				1	14
	+	VCC_ONE				+		14
	+	VCC_ONE	+					11
	-	VCC ONE	-					100
	+	VCC_ONE	+					
	1	IVCC ONE	1	1	ı			

(1) For more information about pin definition and pin connection guidelines, refer to the MAX 10 FPGA Device Family Pin Connection Guidelines.

VCC_ONE ADC_VREF ANAIN1

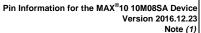
(2) The E144-pin package has an exposed ground pad at the bottom of the package. The exposed ground pad is used for electrical connectivity and not for thermal purposes. You must connect the exposed ground pad to the ground plane of the PCB.

Pin List E144 Page 2 of 7



Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	IO Borforn	Note (1)
Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated TX/RX Channel	Emulated LVDS Output Channel	IO Performance	M153
1A	VREFB1N0	10	ADC1IN1		DIFFIO_RX_L1n	DIFFOUT_L1n	Low_Speed	D2
A	VREFB1N0	IO	ADC1IN2		DIFFIO RX L1p	DIFFOUT_L1p	Low_Speed	C2
A	VREFB1N0	10	ADC1IN3		DIFFIO RX L3n	DIFFOUT L3n	Low Speed	F5
A	VREFB1N0	10	ADC1IN4		DIFFIO_RX_L3p	DIFFOUT_L3p	Low Speed	G5
A	VREFB1N0	IO	ADC1IN5		DIFFIO_RX_L5n	DIFFOUT_L5n	Low_Speed	C1
A	VREFB1N0	10	ADC1IN6		DIFFIO RX L5p	DIFFOUT L5p	Low Speed	B1
A	VREFB1N0	10	ADC1IN7		DIFFIO_RX_L7n	DIFFOUT_L7n	Low_Speed	E1
IA.	VREFB1N0	10	ADC1IN8	TT OF U	DIFFIO_RX_L7p	DIFFOUT_L7p	Low_Speed	E2
B B	VREFB1N0	10		JTAGEN	DIFFIO RX L11n	DIEGOLIE I I I		G7
	VREFB1N0	10	VDEEDANG	TMS	DIFFIO_RX_L11n	DIFFOUT_L11n	Low_Speed	G1
<u>В</u> В	VREFB1N0 VREFB1N0	10	VREFB1N0	TCK	DIFFIO RX L11p	DIFFOUT L11p	Low Speed	G2
В	VREFB1N0	10		TDI	DIFFIO RX L12n	DIFFOUT_L12n	Low_Speed	H5
В	VREFB1N0	10		TDO	DIFFIO RX L12p	DIFFOUT_L12p	Low_Speed	H4
В	VREFB1N0	10		1100	DIFFIO RX L14n	DIFFOUT L14n	Low Speed	H3
В	VREFB1N0	IO			DIFFIO RX L14p	DIFFOUT_L14p	Low Speed	J2
В	VREFB1N0	IO			DIFFIO_RX_L16n	DIFFOUT_L16n	Low_Speed	L1
В	VREFB1N0	10			DIFFIO RX L16p	DIFFOUT L16p	Low Speed	K2
- 2	2 VREFB2N0	10	CLK0n		DIFFIO_RX_L18n	DIFFOUT_L18n	High_Speed	J4
- 2	2 VREFB2N0	10	CLK0p		DIFFIO_RX_L18p	DIFFOUT_L18p	High_Speed	J5
- 2	2 VREFB2N0	10	CLK1n		DIFFIO RX L20n	DIFFOUT L20n	High Speed	K5
	2 VREFB2N0	IO	CLK1p		DIFFIO RX L20p	DIFFOUT L20p	High_Speed	K4
	2 VREFB2N0	10	DPCLK0		DIFFIO_RX_L22n	DIFFOUT_L22n	High_Speed	L5
	VREFB2N0	IU	VREFB2N0		DISTING BY LOS	DIFFOUT LOS		P1
	2 VREFB2N0 2 VREFB2N0	10	DPCLK1		DIFFIO_RX_L22p	DIFFOUT_L22p	High_Speed	L4
	VREFB2N0 VREFB2N0	10	PLL L CLKOUTn		DIFFIO RX L27n	DIFFOUT 1.27n	High Speed	R2 N1
	2 VREFB2N0 2 VREFB2N0	10	PLL_L_CLKOUTp		DIFFIO RX L2/n DIFFIO_RX_L27p	DIFFOUT_L27p	High Speed High_Speed	N1 P2
-	3 VREFB2N0	10	1 LL_L_CLNOUTP		DIFFIO_RX_L2/p	DIFFOUT_L27p DIFFOUT_B1n	High_Speed	M4
-	3 VREFB3N0	10	†		DIFFIO TX RX BIII	DIFFOUT B2n	High Speed	P3
-	3 VREFB3N0	IO	†		DIFFIO TX RX B1p	DIFFOUT B1p	High Speed	M5
	3 VREFB3N0	10	1		DIFFIO RX B20	DIFFOUT_B2p	High_Speed	R3
	3 VREFB3N0	10	1		DIFFIO TX RX B3n	DIFFOUT B3n	High Speed	L6
-	3 VREFB3N0	IO			DIFFIO RX B4n	DIFFOUT_B4n	High_Speed	P4
-	3 VREFB3N0	IO			DIFFIO_TX_RX_B3p	DIFFOUT_B3p	High_Speed	L7
	3 VREFB3N0	10			DIFFIO RX B4p	DIFFOUT B4p	High Speed	R5
	3 VREFB3N0	10			DIFFIO_TX_RX_B5n	DIFFOUT_B5n	High_Speed	P6
	3 VREFB3N0	10			DIFFIO_RX_B6n	DIFFOUT_B6n	High_Speed	R7
	3 VREFB3N0	IO			DIFFIO TX RX B5p	DIFFOUT B5p	High Speed	P7
	3 VREFB3N0	10			DIFFIO_RX_B6p	DIFFOUT_B6p	High_Speed	P8
	3 VREFB3N0	10			DIFFIO_TX_RX_B7n	DIFFOUT_B7n	High_Speed	L8
	3 VREFB3N0	10			DIFFIO RX B8n	DIFFOUT B8n	High Speed	P9
-	3 VREFB3N0	10			DIFFIO_TX_RX_B7p	DIFFOUT_B7p	High_Speed	M7 R9
	3 VREFB3N0 3 VREFB3N0	10	-		DIFFIO_RX_B8p DIFFIO_TX_RX_B9n	DIFFOUT B9n	High_Speed	M8
	3 VREFB3N0	10	VREFB3N0		DIFFIO TA RA B9II	DIFFOUT BBIT	High Speed	R11
-	3 VREFB3N0	10	VICEI BONO		DIFFIO_TX_RX_B9p	DIFFOUT_B9p	High Speed	N8
	3 VREFB3N0	10			DIFFIO TA KA Bap	DIFFOOT BSp	Tilgit_Speed	P12
	3 VREFB3N0	IO			DIFFIO TX RX B10n	DIFFOUT B10n	High_Speed	R14
	3 VREFB3N0	IO			DIFFIO_TX_RX_B10p	DIFFOUT_B10p	High_Speed	P15
	3 VREFB3N0	IO			DIFFIO TX RX B12n	DIFFOUT B12n	High Speed	L9
	3 VREFB3N0	10			DIFFIO_TX_RX_B12p	DIFFOUT_B12p	High_Speed	M9
	3 VREFB3N0	10			DIFFIO_TX_RX_B14n	DIFFOUT_B14n	High_Speed	L10
	VREFB3N0	10			DIFFIO TX RX B14p	DIFFOUT B14p	High Speed	M11
	3 VREFB3N0	10	1		DIFFIO_TX_RX_B16n	DIFFOUT_B16n	High_Speed	P14
	VREFB3N0	10	1		DIFFIO_TX_RX_B16p	DIFFOUT_B16p	High_Speed	R13
	VREFB5N0	10	1		DIFFIO RX R1p	DIFFOUT R1p	High Speed	M12
	VREFB5N0 VREFB5N0	10	1		DIFFIO_RX_R2p DIFFIO_RX_R1n	DIFFOUT_R2p	High_Speed	N15
	VREFB5N0	10	+		DIFFIO_RX_R1n	DIFFOUT R2n	High_Speed	L11 N14
	VREFB5N0 VREFB5N0	10	+		DIFFIO RX R2n DIFFIO RX R7p	DIFFOUT R2n DIFFOUT_R7p	High Speed High Speed	N14 K11
	VREFB5N0	10	†		DITTO NA NIP	Dil 1 COT_K/p	i iiqii_Specu	M14
	VREFB5N0	IO	İ		DIFFIO RX R7n	DIFFOUT R7n	High Speed	K12
į	VREFB5N0	IO	VREFB5N0				J	L15
į	VREFB5N0	IO			DIFFIO_RX_R10p	DIFFOUT_R10p	High_Speed	J9
	VREFB5N0	IO			DIFFIO RX R11p	DIFFOUT R11p	High Speed	K14
	VREFB5N0	10	1		DIFFIO_RX_R10n	DIFFOUT_R10n	High_Speed	J11
	VREFB5N0	10			DIFFIO_RX_R11n	DIFFOUT_R11n	High_Speed	J14
	VREFB6N0	10	CLK2p		DIFFIO RX R14p	DIFFOUT R14p	High Speed	J12
	VREFB6N0	10	CLK2n		DIFFIO_RX_R14n	DIFFOUT_R14n	High_Speed	H11
	6 VREFB6N0	IU	CLK3p		DIFFIO_RX_R16p	DIFFOUT_R16p	High_Speed	H12
	VREFB6N0	10	CLK3n		DIFFIO RX R16n	DIFFOUT R16n	High Speed	H13
	6 VREFB6N0	10	+		DIFFIO_RX_R18p	DIFFOUT_R18p	High_Speed	J15
	6 VREFB6N0 6 VREFB6N0	10	DPCLK3		DIFFIO_RX_R18n DIFFIO_RX_R26p	DIFFOUT_R18n	High_Speed	G15 G11
	SIVREFB6N0	10	VREFB6N0		DIFFIO KA KZOP	DIFFOUT R26p	High Speed	G11 F15
	VREFB6N0	10	DPCLK2		DIFFIO_RX_R26n	DIFFOUT_R26n	High_Speed	G12
	6 VREFB6N0	10	D. CLIVE		SILLIO_IXX_IXZUII	51 001_R20II	. ligit_opecu	E14
-	6 VREFB6N0	10	†		DIFFIO RX R27p	DIFFOUT_R27p	High Speed	F11
i	VREFB6N0	IO	1		DIFFIO RX R28p	DIFFOUT_R28p	High Speed	C15
	VREFB6N0	IO	1		DIFFIO RX R27n	DIFFOUT R27n	High Speed	F12
	6 VREFB6N0	IO	1		DIFFIO RX R28n	DIFFOUT_R28n	High_Speed	C14
	VREFB6N0	10	1		DIFFIO_RX_R33p	DIFFOUT_R33p	High_Speed	E11
	VREFB6N0	IO			DIFFIO RX R33n	DIFFOUT R33n	High Speed	D12
	VREFB8N0	IO			DIFFIO_RX_T14p	DIFFOUT_T14p	Low_Speed	D11
	VREFB8N0	10			DIFFIO RX T15p	DIFFOUT T15p	Low_Speed	B15
	VREFB8N0	10	1		DIFFIO RX T14n	DIFFOUT T14n	Low Speed	D10
- 5	8 VREFB8N0	10	1		DIFFIO_RX_T15n	DIFFOUT_T15n	Low_Speed	B14
	VREFB8N0	IO			DIFFIO_RX_T16p	DIFFOUT_T16p	Low_Speed	C8

Pin List M153



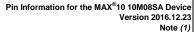


nk Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	IO Performance	M153
	VREFB8N0	IO			DIFFIO_RX_T17p	DIFFOUT_T17p	Low_Speed	B13
	VREFB8N0	10		DEV_CLRn	DIFFIO_RX_T16n	DIFFOUT_T16n	Low_Speed	B8
8	VREFB8N0	10			DIFFIO RX T17n	DIFFOUT T17n	Low Speed	A14
	VREFB8N0	IO		DEV_OE	DIFFIO_RX_T18p	DIFFOUT_T18p	Low_Speed	E10
8	VREFB8N0	10			DIFFIO_RX_T18n	DIFFOUT_T18n	Low_Speed	E9
3	VREFB8N0	10	VREFB8N0					A13
	VREFB8N0	10		CONFIG_SEL				D8
8	VREFB8N0	10			DIFFIO_RX_T19p	DIFFOUT_T19p	Low_Speed	B12
3	VREFB8N0	Input only		nCONFIG				E8
8	VREFB8N0	10			DIFFIO_RX_T19n	DIFFOUT_T19n	Low_Speed	B11
8	VREFB8N0	IO			DIFFIO_RX_T20p	DIFFOUT_T20p	Low Speed	B7
8	VREFB8N0	10			DIFFIO RX T21p	DIFFOUT T21p	Low Speed	A9
8	VREFB8N0	10			DIFFIO_RX_T20n	DIFFOUT_T20n	Low_Speed	B6
8	VREFB8N0	10			DIFFIO_RX_T21n	DIFFOUT_T21n	Low Speed	A11
8	VREFB8N0	10			DIFFIO RX T22p	DIFFOUT T22p	Low Speed	D7
8	VREFB8N0	10			DIFFIO_RX_T23p	DIFFOUT_T23p	Low_Speed	A7
8	VREFB8N0	IO		CRC_ERROR	DIFFIO_RX_T22n	DIFFOUT_T22n	Low Speed	E7
8	VREFB8N0	IO		_	DIFFIO RX T23n	DIFFOUT T23n	Low Speed	A5
	VREFB8N0	IO		nSTATUS	DIFFIO_RX_T24p	DIFFOUT_T24p	Low_Speed	D6
	VREFB8N0	IO						B4
8	VREFB8N0	IO		CONF DONE	DIFFIO RX T24n	DIFFOUT T24n	Low Speed	E6
8	VREFB8N0	IO			DIFFIO_RX_T26p	DIFFOUT_T26p	Low_Speed	A2
8	VREFB8N0	IO			DIFFIO_RX_T26n	DIFFOUT_T26n	Low_Speed	A3
		GND						R15
	1	GND			İ	İ		R1
		GND						M6
		GND						M2
		GND						M10
		GND						L12
		GND						J7
		GND						H8
		GND						H14
		GND						G9
		GND						G4
		GND						E5
		GND						E12
		GND						D9
		GND						D5
		GND						B2
		GND						A15
		GND						A1
		REFGND						E4
		VCCIO1A						F2
		VCCIO1B						H2
	1	VCCIO2				<u> </u>		L2
	1	VCCIO3				<u> </u>		P5
	1	VCCIO3				<u> </u>		P11
	1	VCCIO3				†	1	P10
	1	VCCIO5				<u> </u>		L14
	1	VCCIO6				<u> </u>		G14
	†	VCCIO6			<u> </u>	+	- 	F14
	1	VCCIO8				<u> </u>		B9
	1	VCCIO8				<u> </u>		B5
	†	VCCIO8			<u> </u>	+	- 	B10
	1	VCCA1				<u> </u>		N2
	1	VCCA2				<u> </u>		D14
	†	VCCA3			<u> </u>	+	- 	B3
	1	VCCA3	<u> </u>		+	+	<u> </u>	P13
	1	VCC ONE	<u> </u>		+	+	<u> </u>	J8
	1	VCC_ONE	1			+	+	H9
	1	VCC ONE				+	-	H9 H7
	1	VCC_ONE				+	-	H/ G8
	1	ADC VREF						F4
	1		-					D4
	1	ANAIN1	1	1	ı			D4

(1) For more information about pin definition and pin connection guidelines, refer to the MAX 10 FPGA Device Family Pin Connection Guidelines.



Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	IO Performance	U169
1A	VREFB1N0	10	ADC1IN1		DIFFIO RX L1n	DIFFOUT L1n	Low Speed	D1
1A	VREFB1N0	10	ADC1IN2		DIFFIO RX L1p	DIFFOUT I In	Low Speed	C2
	VREFB1N0	10	ADC1IN3		DIFFIO RX L3n	DIFFOUT L3n	Low Speed	E3
1A	VREFB1N0	Ю	ADC1IN4		DIFFIO RX L3p	DIFFOUT L3p	Low Speed	E4
1A	VREFB1N0	IO	ADC1IN5		DIFFIO RX L5n	DIFFOUT L5n	Low Speed	C1
1A	VREFB1N0	IO	ADC1IN6		DIFFIO RX L5p	DIFFOUT L5p	Low Speed	B1
1A	VREFB1N0	IO	ADC1IN7		DIFFIO RX L7n	DIFFOUT L7n	Low Speed	F1
	VREFB1N0	IO	ADC1IN8		DIFFIO RX L7p	DIFFOUT L7p		E1
	VREFB1N0	IO		JTAGEN				E5
	VREFB1N0	IO		TMS	DIFFIO RX L11n	DIFFOUT L11n	Low Speed	G1
	VREFB1N0	Ю	VREFB1N0					H1
	VREFB1N0	Ю		TCK	DIFFIO RX L11p	DIFFOUT L11p	Low Speed	G2
1B	VREFB1N0	Ю		TDI	DIFFIO RX L12n	DIFFOUT L12n	Low Speed	F5
	VREFB1N0	Ю		TDO	DIFFIO RX L12p	DIFFOUT L12p		F6
	VREFB1N0	10			DIFFIO RX L14n	DIFFOUT L14n		F4
	VREFB1N0	10			DIFFIO RX L14p	DIFFOUT L14p		G4
	VREFB1N0	10			DIFFIO RX L16n	DIFFOUT L16n		H2
1B	VREFB1N0	10	0.170		DIFFIO RX L16p	DIFFOUT L16p		H3
2	VREFB2N0	10	CLK0n		DIFFIO RX L18n	DIFFOUT L18n	High Speed	G5
2	VREFB2N0	IO .	0.140		DIFFIO RX L19n	DIFFOUT L19n	High Speed	J1
	VREFB2N0	10	CLK0p		DIFFIO RX L18p	DIFFOUT L18p		H6
	VREFB2N0	10	0.14		DIFFIO RX L19p		High Speed	J2
	VREFB2N0 VREFB2N0	10	CLK1n		DIFFIO RX L20n	DIFFOUT L20n DIFFOUT L21n		H5 M1
		10	0.14				riigir Opood	
2	VREFB2N0	10	CLK1p		DIFFIO RX L20p	DIFFOUT L20p	High Speed	H4
	VREFB2N0	10	20011/2		DIFFIO RX L21p	DIFFOUT L21p		M2
2	VREFB2N0	10	DPCLK0		DIFFIO RX L22n	DIFFOUT L22n	High Speed	N2
	VREFB2N0 VREFB2N0	10	VREFB2N0		DIFFIO RX L22p	DIFFOLIT 1 22°		L1
		10	DPCLK1		DIFFIU KX L22p	DIFFOUT L22p		N3
	VREFB2N0	10	DIL I CIKOLITA		DIEEIO DV 1 27-	DIFFOLIT LOZ-		L2 M3
	VREFB2N0	IO	PLL L CLKOUTn		DIFFIO RX L27n	DIFFOUT L27n		
	VREFB2N0	IU	DIL I OLIVOUT-		DIFFIO RX L28n	DIFFOUT L28n		K1
2	VREFB2N0	10	PLL L CLKOUTp		DIFFIO RX L27p	DIFFOUT L27p	High Speed	L3
	VREFB2N0	IO			DIFFIO RX L28p	DIFFOUT L28p	High Speed	K2
	VREFB3N0	10			DIFFIO TX RX B1n			L5
	VREFB3N0	10			DIFFIO RX B2n	DIFFOUT B2n		M4
	VREFB3N0	10			DIFFIO TX RX B1p			L4
	VREFB3N0	10			DIFFIO RX B2p	DIFFOUT B2p		M5 K5
	VREFB3N0	10			DIFFIO TX RX B3n	DIFFOUT B3n		N4
3	VREFB3N0	10			DIFFIO RX B4n	DIFFOUT B4n	High Speed	
	VREFB3N0	IO			DIFFIO TX RX B3p	DIFFOUT B3p	High Speed	J5
	VREFB3N0	10			DIFFIO RX B4p			N5
	VREFB3N0 VREFB3N0	10			DIFFIO TX RX B5n	DIFFOUT B5n DIFFOUT B6n		N6 N7
							High Speed	
3	VREFB3N0	10			DIFFIO TX RX B5p DIFFIO RX B6p	DIFFOUT B5p		M7 N8
3	VREFB3N0 VREFB3N0	10			DIFFIO RX B6p DIFFIO TX RX B7n	DIFFOUT B6p DIFFOUT B7n	High Speed High Speed	J6
	VREFB3N0	0			DIFFIO TX RX B/II	DIFFOUT B8n		M8
3	VREFB3N0	IO			DIFFIO TX RX B7p			K6
	VREFB3N0	IO .			DIFFIO IX RX B/p	DIFFOUT B8p		Mg
	VREFB3N0	IO .			DIFFIO TX RX B9n	DIFFOUT B9n		.17
	VREFB3N0	10	VREFB3N0		DIFFIC TA RA B9II	DIFFOOT Ball	rligir Speed	N11
2	VREFB3N0	10	VKEFBSNO		DIFFIO TX RX B9p	DIFFOUT B9p	High Speed	V7
	VREFB3N0	IO			DIFFIO TA KA Bap	ынгоот вэр	rligir Speed	N12
	VREFB3N0	10			DIFFIO TX RX B10n	DIFFOUT B10n		M13
		10			DIFFIO TX RX B1011			N10
	VREFB3N0	IO .			DIFFIO TX RX B10p			M12
	VREFB3N0	IO .		<u> </u>	DIFFIO IX RX B10p	DIFFOUT B10p DIFFOUT B11p		N9
	VREFB3N0	10		<u> </u>	DIFFIO TX RX B12n	DIFFOUT B12n	High Speed	M11
	VREFB3N0	IO.		<u> </u>	DIFFIO TX RX B121	DIFFOUT B12p	High Speed	L11
3	VREFB3N0	10			DIFFIO TX RX B12p	DIFFOUT B12p	High Speed	JB
	VREFB3N0	10		<u> </u>	DIFFIO TX RX B14II			K8
	VREFB3N0	10		 	DIFFIO TX RX B14p			M10
	VREFB3N0	10		 	DIFFIO TX RX B16n	DIFFOUT B16p		110
	VREFB5N0	10			DIFFIO RX R1p	DIFFOUT R1p	High Speed	K10
5	VREFB5N0	10			DIFFIO RX R1p	DIFFOUT R2p	High Speed	K11
5	VREFB5N0	10		<u> </u>	DIFFIO RX R1n	DIFFOUT R1n	High Speed	J10
5	VREFB5N0	10			DIFFIO RX R2n	DIFFOUT R2n		L12
5	VREFB5N0	10		<u> </u>	DIFFIO RX R7p	DIFFOUT R7p	High Speed	K12
	VREFB5N0	10		<u> </u>				113
	VREFB5N0	10		<u> </u>	DIFFIO RX R7n	DIFFOUT R7n		J12
	VREFB5N0	10	VREFB5N0	 				K13
5	VREFB5N0	10	50.10	<u> </u>	DIFFIO RX R8p	DIFFOUT R8p	High Speed	J9
	VREFB5N0	IO			DIFFIO RX R9p	DIFFOUT R9p	High Speed	J13
	VREFB5N0	10		<u> </u>	DIFFIO RX R8n	DIFFOUT R8n		H10
	VREFB5N0	10			DIFFIO RX R9n	DIFFOUT R9n		H13
	VREFB5N0	10		<u> </u>	DIFFIO RX R10p			H9
	VREFB5N0	10			DIFFIO RX R11p	DIFFOUT R11p		G13
	VREFB5N0	10		<u> </u>	DIFFIO RX R10n	DIFFOUT R10n	High Speed	H8
5		10		<u> </u>	DIFFIO RX R11n	DIFFOUT R11n	High Speed	G12
5 5			CLK2p	<u> </u>	DIFFIO RX R11II	DIFFOUT R14p	High Speed	G9
5 5 5	VREFB5N0	IC		1				G10
5 5 5 6	VREFB5N0 VREFB6N0	0						
5 5 5 6 6	VREFB5N0 VREFB6N0 VREFB6N0	10 10	CLK2n		DIFFIO RX R14n			
5 5 5 6 6	VREFB5N0 VREFB6N0 VREFB6N0 VREFB6N0	10	CLK2n CLK3p		DIFFIO RX R16p	DIFFOUT R16p	High Speed	F13
5 5 5 6 6	VREFB5N0 VREFB6N0 VREFB6N0 VREFB6N0 VREFB6N0	IO IO	CLK2n		DIFFIO RX R16p DIFFIO RX R16n	DIFFOUT R16p DIFFOUT R16n	High Speed High Speed	F13 E13
5 5 5 6 6 6 6	VREFB5N0 VREFB6N0 VREFB6N0 VREFB6N0 VREFB6N0 VREFB6N0 VREFB6N0	10 10 10	CLK2n CLK3p		DIFFIO RX R16p DIFFIO RX R16n DIFFIO RX R18p	DIFFOUT R16p DIFFOUT R16n DIFFOUT R18p	High Speed High Speed High Speed	F13 E13 F12
5 5 6 6 6 6 6	VREFB5N0 VREFB6N0 VREFB6N0 VREFB6N0 VREFB6N0 VREFB6N0 VREFB6N0 VREFB6N0	10 10 10	CLK2n CLK3p CLK3n		DIFFIO RX R16p DIFFIO RX R16n DIFFIO RX R18p DIFFIO RX R18n	DIFFOUT R16p DIFFOUT R16n DIFFOUT R18p DIFFOUT R18n	High Speed High Speed High Speed High Speed High Speed	F13 E13 F12 E12
5 5 5 6 6 6 6 6	VREFB5N0 VREFB6N0 VREFB6N0 VREFB6N0 VREFB6N0 VREFB6N0 VREFB6N0 VREFB6N0 VREFB6N0	10 10 10	CLK2n CLK3p CLK3n		DIFFIO RX R16p DIFFIO RX R16n DIFFIO RX R18p	DIFFOUT R16p DIFFOUT R16n DIFFOUT R18p	High Speed High Speed High Speed	F13 E13 F12 E12 F9
5 5 6 6 6 6 6 6	VREFBSNO VREFB6NO VREFB6NO VREFB6NO VREFB6NO VREFB6NO VREFB6NO VREFB6NO VREFB6NO VREFB6NO VREFB6NO VREFB6NO	10 10 10 10 10 10	CLK2n CLK3p CLK3n DPCLK3 VREFB6N0		DIFFIO RX R16p DIFFIO RX R16n DIFFIO RX R18p DIFFIO RX R18p DIFFIO RX R18n DIFFIO RX R26p	DIFFOUT R16p DIFFOUT R16n DIFFOUT R18p DIFFOUT R18p DIFFOUT R18n DIFFOUT R26p	High Speed High Speed High Speed High Speed High Speed High Speed	F13 E13 F12 E12 F9 D13
5 5 6 6 6 6 6 6 6	VREFB5N0 VREFB6N0 VREFB6N0 VREFB6N0 VREFB6N0 VREFB6N0 VREFB6N0 VREFB6N0 VREFB6N0	10 10 10	CLK2n CLK3p CLK3n		DIFFIO RX R16p DIFFIO RX R16n DIFFIO RX R18p DIFFIO RX R18n	DIFFOUT R16p DIFFOUT R16n DIFFOUT R18p DIFFOUT R18n	High Speed High Speed High Speed High Speed High Speed High Speed	F13 E13 F12 E12 F9





Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	IO Performance	U169
	VREFB6N0	IO			DIFFIO RX R28p	DIFFOUT R28p	High Speed	B12
6	VREFB6N0	Ю			DIFFIO RX R27n	DIFFOUT R27n	High Speed	E9
ε	VREFB6N0	Ю			DIFFIO RX R28n	DIFFOUT R28n	High Speed	B11
ε	VREFB6N0	Ю			DIFFIO RX R29p	DIFFOUT R29p	High Speed	C12
6	VREFB6N0	Ю			DIFFIO RX R30p	DIFFOUT R30p	High Speed	B13
6	VREFB6N0	Ю			DIFFIO RX R29n	DIFFOUT R29n	High Speed	C11
6	VREFB6N0	Ю			DIFFIO RX R30n	DIFFOUT R30n	High Speed	A12
6	VREFB6N0	Ю			DIFFIO RX R31p	DIFFOUT R31p	High Speed	E10
	VREFB6N0	Ю			DIFFIO RX R31n	DIFFOUT R31n	High Speed	D9
6	VREFB6N0	Ю			DIFFIO RX R33p	DIFFOUT R33p	High Speed	D12
6	VREFB6N0	10			DIFFIO RX R33n	DIFFOUT R33n	High Speed	D11
	VREFB8N0	10			DIFFIO RX T14p	DIFFOUT T14p	Low Speed	C10
8	VREFB8N0	10			DIFFIO RX T15p	DIFFOUT T15p	Low Speed	A8
	VREFB8N0	IO			DIFFIO RX T14n	DIFFOUT T14n	Low Speed	C9
	VREFB8N0	IO			DIFFIO RX T15n	DIFFOUT T15n	Low Speed	A9
8	VREFB8N0	10			DIFFIO RX T16p	DIFFOUT T16p	Low Speed	B10
	VREFB8N0	10			DIFFIO RX T17p	DIFFOUT T17p	Low Speed	A10
	VREFB8N0	IO		DEV CLRn	DIFFIO RX T16n	DIFFOUT T16n	Low Speed	B9
	VREFB8N0	IO		l com	DIFFIO RX T17n	DIFFOUT T17n	Low Speed	A11
	VREFB8N0	IO .	<u> </u>	DEV OE	DIFFIO RX T18p	DIFFOUT T18p	Low Speed	D8
	VREFB8N0	IO .	<u> </u>	DEV OL	DIFFIO RX T18p	DIFFOUT T18n	Low Speed	E8
	VREFB8N0	10	VREFB8N0		DILLIO KY LIGH	DIT 701 11011	Low Speed	B7
	VREFB8N0 VREFB8N0	IO IO	VICE DOINU	CONFIG SEL		+	+	B7
	VREFB8N0	10	+	CONFIG SEL	DIFFIO RX T19p	DIFFOUT T19p	Low Speed	D7
		least eats	+	-CONFIC	DILLIO KY 119b	DIFFOUT 119p	Low Speed	
	VREFB8N0	Input only	+	nCONFIG	DIFFIO DV T40=	DIFFOUT TAGE	Law Casad	E7
	VREFB8N0				DIFFIO RX T19n	DIFFOUT T19n	Low Speed	A6
	VREFB8N0	10	+		DIFFIO RX T20p	DIFFOUT T20p	Low Speed	B6
	VREFB8N0	10	ļ		DIFFIO RX T21p	DIFFOUT T21p	Low Speed	A4
	VREFB8N0	IO .	ļ		DIFFIO RX T20n	DIFFOUT T20n	Low Speed	B5
	VREFB8N0	IO .	ļ		DIFFIO RX T21n	DIFFOUT T21n	Low Speed	A3
	VREFB8N0	Ю			DIFFIO RX T22p	DIFFOUT T22p	Low Speed	E6
	VREFB8N0	IO	1		DIFFIO RX T23p	DIFFOUT T23p	Low Speed	B3
	VREFB8N0	Ю		CRC ERROR	DIFFIO RX T22n	DIFFOUT T22n	Low Speed	D6
8	VREFB8N0	Ю			DIFFIO RX T23n	DIFFOUT T23n	Low Speed	B4
	VREFB8N0	Ю		nSTATUS	DIFFIO RX T24p	DIFFOUT T24p	Low Speed	C4
8	VREFB8N0	Ю						A5
	VREFB8N0	Ю		CONF DONE	DIFFIO RX T24n	DIFFOUT T24n	Low Speed	C5
8	VREFB8N0	Ю			DIFFIO RX T26p	DIFFOUT T26p	Low Speed	A2
8	VREFB8N0	Ю			DIFFIO RX T26n	DIFFOUT T26n	Low Speed	B2
		GND						N13
		GND						N1
		GND						M6
		GND						19
		GND						.14
		GND						H12
		GND						G7
		GND	<u> </u>				-	F3
		GND	<u> </u>				-	E11
		GND			<u> </u>		+	D5
		GND					_	C3
							_	
	1	GND						B8
	 	GND	 		+		+	A13
	ļ	GND	ļ		1		_	A1
	1	REFGND	1					E2
	1	VCCIO1A	1					F2
		VCCIO1B						G3
		VCCIO2						K3
	<u> </u>	VCCIO2						J3
		VCCIO3						L8
		VCCIO3						L7
		VCCIO3						L6
		VCCIO5						J11
		VCCIO5						H11
		VCCIO6						G11
		VCCIO6						F11
	1	VCCIO8						C8
	1	VCCIO8	<u> </u>		+		+	C7
		VCCIO8	1		1			C6
	†	VCCA1	1			+	+	K4
	1	VCCA1	<u> </u>		1	+	+	D10
	1		+		+		+	
	 	VCCA3	ļ			-	_	D4
	 	VCCA4	ļ			-	_	K9
		VCC ONE						H7
		VCC ONE						G8
		VCC ONE						G6
		VCC ONE						F7
	1	ADC VREF				1		D3
		ANAIN1						D2

(1) For more information about pin definition and pin connection guidelines, refer to the MAX 10 FPGA Device Family Pin Connection Guidelines.

Pin List U169



Pin Information for the MAX[®]10 10M08SA Device Version 2016.12.23

Date Version		Changes Made	
September 2014	2014.09.22	Initial release.	
December 2014		-Updated the BOOT_SEL pin name to CONFIG_SEL pin nameRemoved differential pair pins for non-differential function support.	
May 2015	2015.05.08	Added note (2) to Pin List E144.	
December 2016	2016.12.23	Removed I/O performance for single-ended pins.	