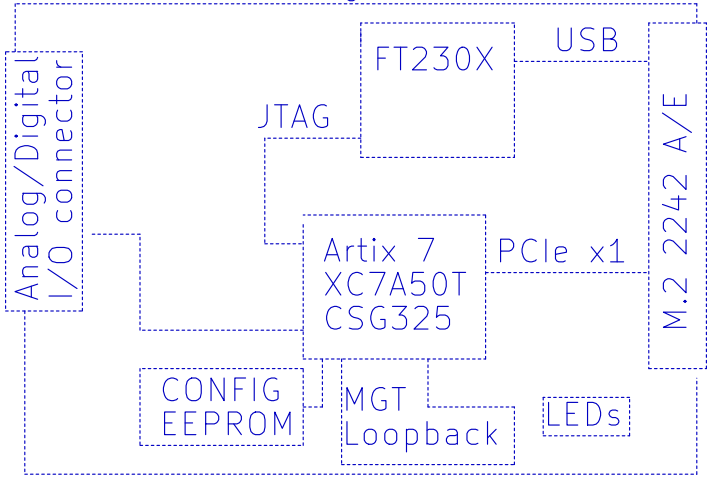


TOP LEVEL

RHS Research, LLC		
Sheet: /		
File: DualEVB.sch		
Title: NanoEVB-X1/PicoEVB-X1		
Size: A	Date: 2017-05-17	Rev: D
KiCad E.D.A. kicad 4.0.6-e0-634952ubuntu16.10.1		Id: 1/15

PicoEVB Block Diagram



Power



power_b.sch

FPGA PCIe



tpga_pcie_b.sch

USB IO



USB_IO_b.sch

FPGA Power & Config



tpga_pwr_cfg_b.sch

FPGA IO



tpga_io_b.sch

M2 edge



M2_edge_b.sch

TOP LEVEL

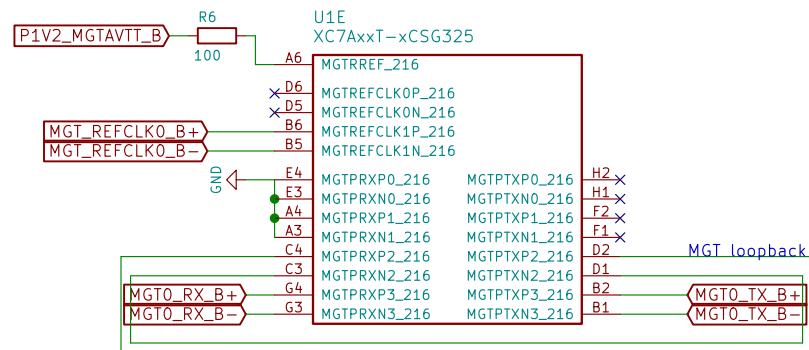
RHS Research, LLC

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Title: PicoEVB-X1

Size: A Date: 2017-05-17
KiCad E.D.A. kicad 4.0.6-e0-634952ubuntu16.10.1

Rev: B
Id: 2/15



PCI Express / MGT loopback

RHS Research, LLC

Sheet: /PicoEVB/FPGA PCIe/

File: fpga_pcie_b.sch

Title: PicoEVB-X1

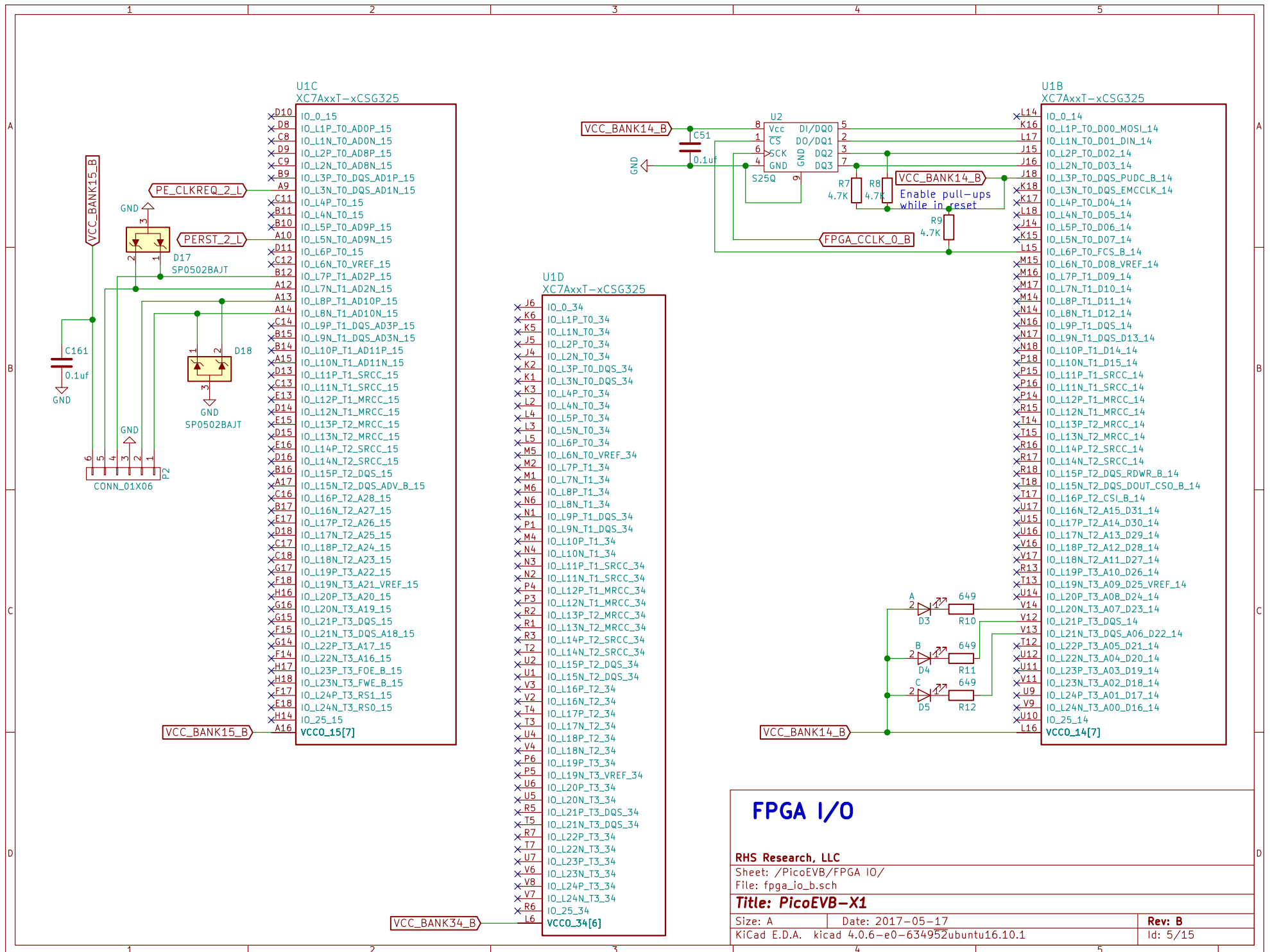
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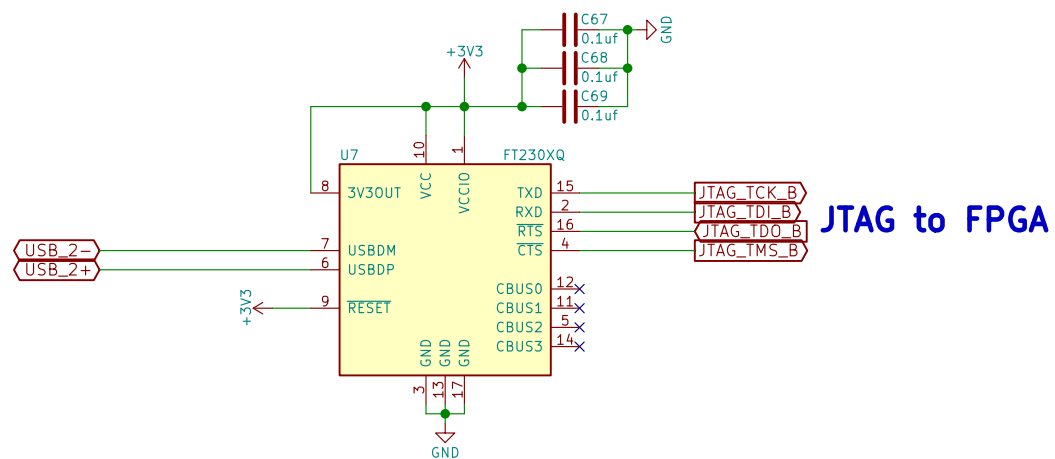
Date: 2017-05-17

Rev: B

KiCad E.D.A. kicad 4.0.6-e0-634952ubuntu16.10.1

Id: 4/15





USB-based JTAG cable

RHS Research, LLC

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File: USB_IO_b.sch

Title: PicoEVB-X1

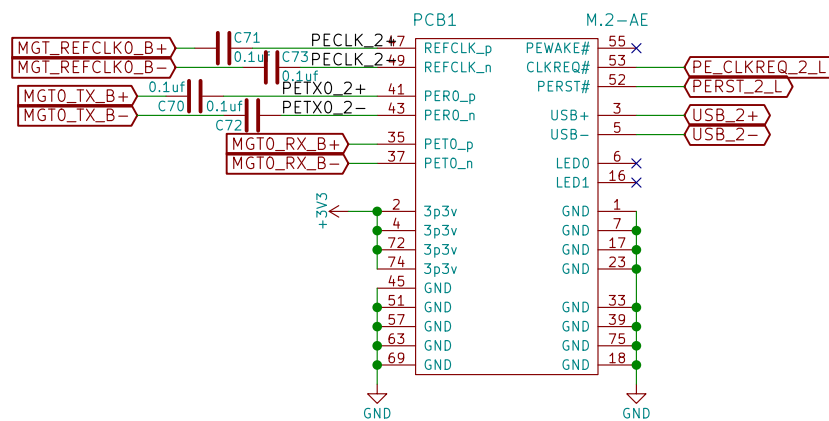
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Date: 2017-05-17

Rev: B

KiCad E.D.A. kicad 4.0.6-e0-634952ubuntu16.10.1

Id: 7/15



M.2 edge connections

RHS Research, LLC

Sheet: /PicoEVB/M2 edge/

File: M2_edge_b.sch

Title: PicoEVB-X1

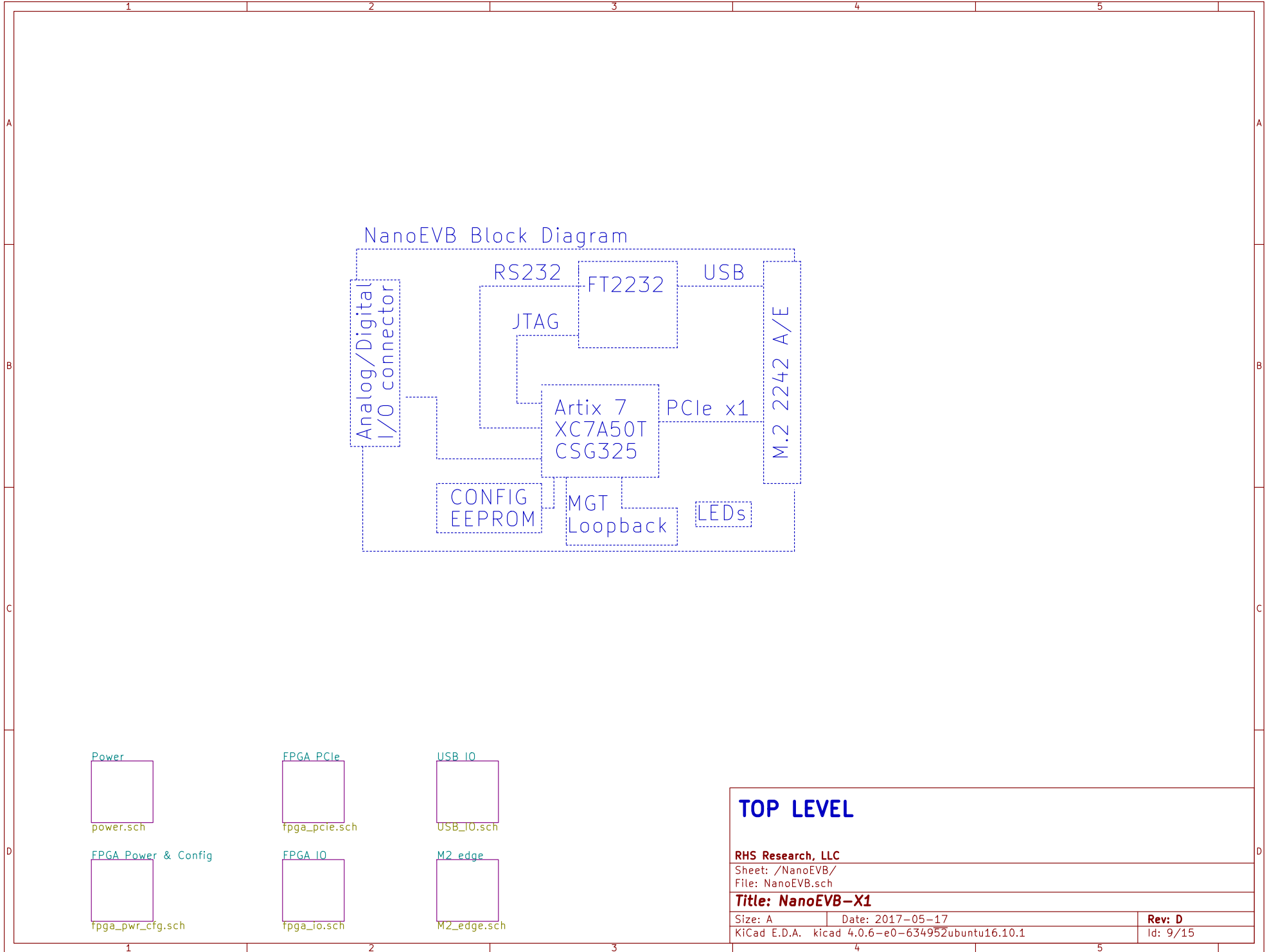
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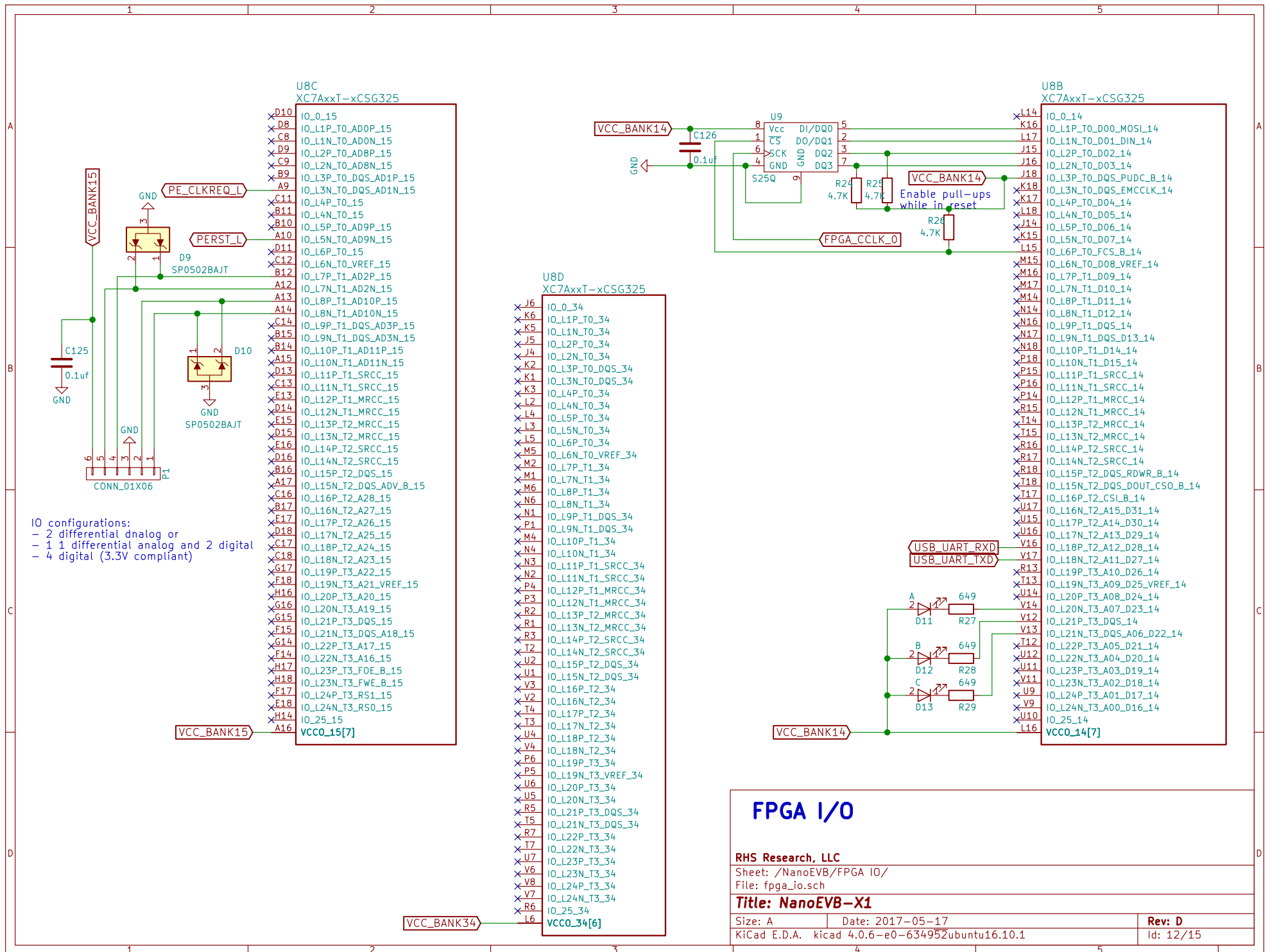
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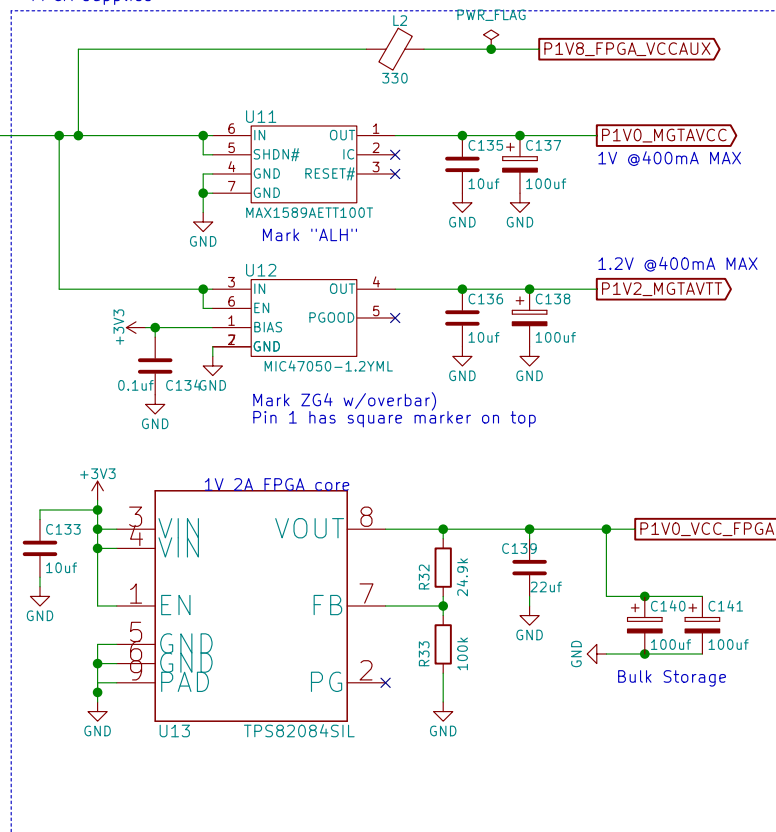
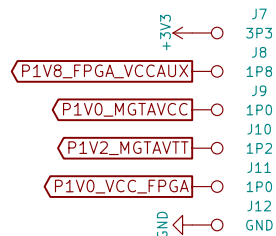
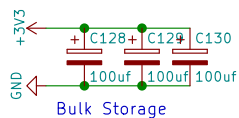
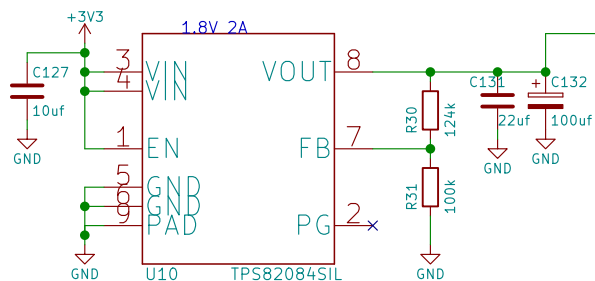
Rev: B

KiCad E.D.A. kicad 4.0.6-e0-634952ubuntu16.10.1

Id: 8/15







RHS Research, LLC

Sheet: /NanoEVb/Power/
File: power.sch

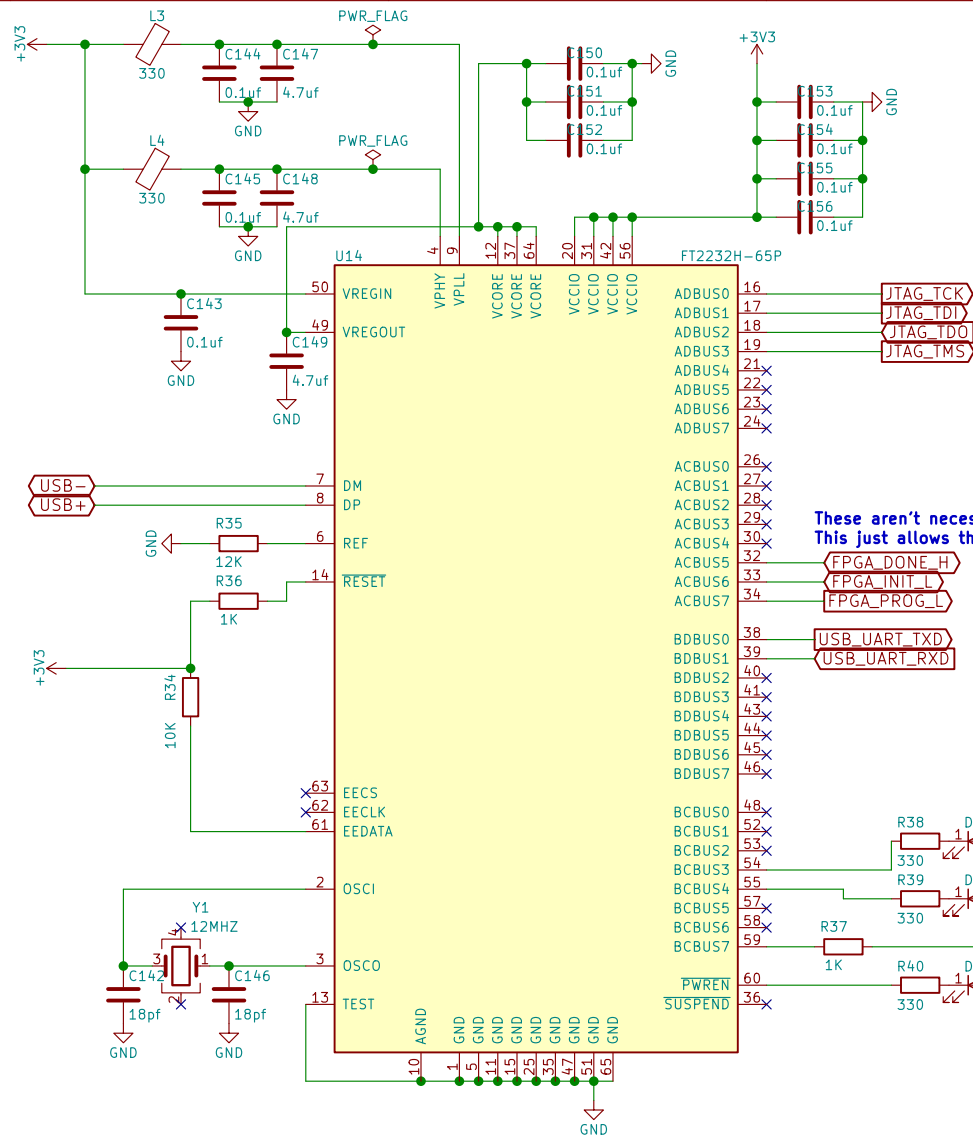
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Size: A	Date: 2017-05-17
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Rev: D

Id: 13/15



JTAG to FPGA

These aren't necessary for the cable to work
This just allows the host to poll the done/init lines and force a reprogram

FPGA_DONE_H
FPGA_INIT_L
FPGA_PROG_L

USB_UART_TXD
USB_UART_RXD

TX: Transmitting data to host computer
RX: Receiving data from host computer

USB-based JTAG cable & debug UART

RHS Research, LLC

Sheet: /NanoEVb/USB IO/
File: USB_IO.sch

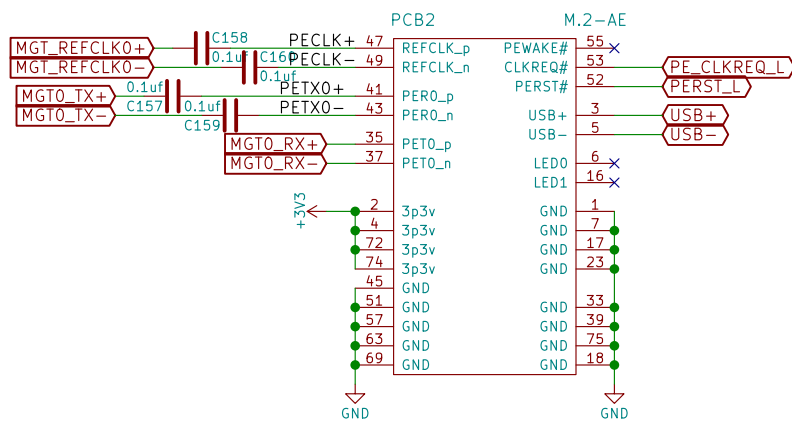
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Rev: D

Id: 14/15



M.2 edge connections

RHS Research, LLC

Sheet: /NanoEVb/M2 edge/
File: M2_edge.sch

Title: NanoEVb-X1

Size: A Date: 2017-05-17

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Rev: D

Id: 15/15