COVER PAGE

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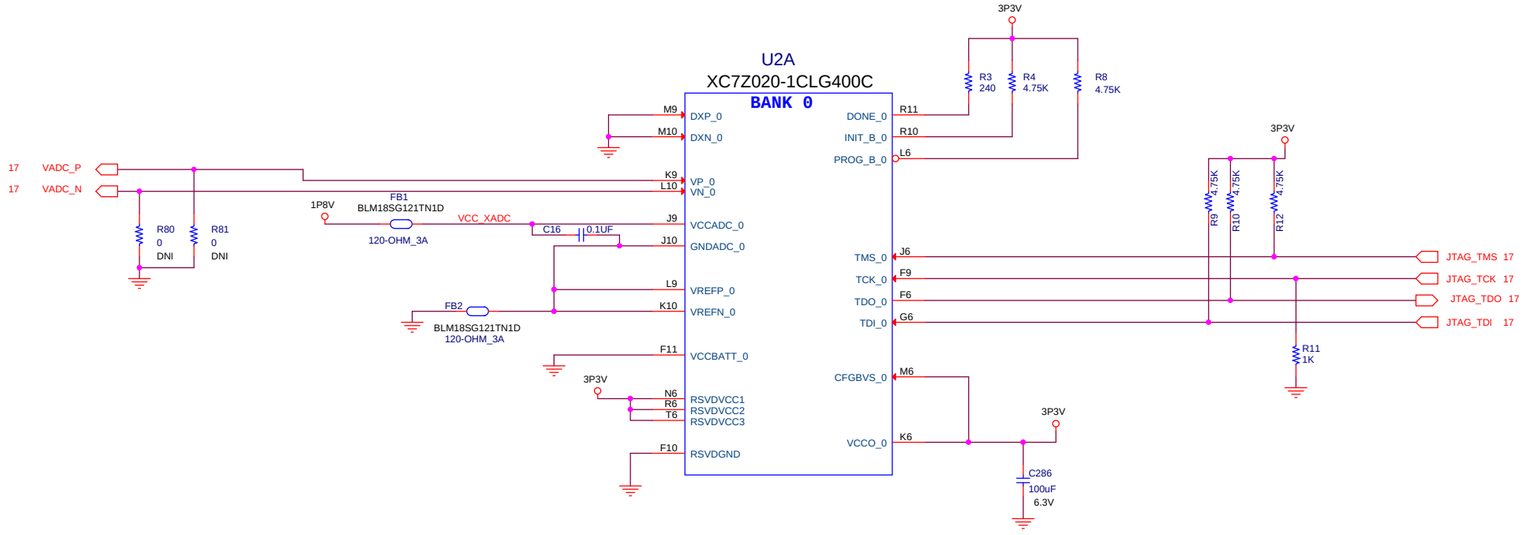
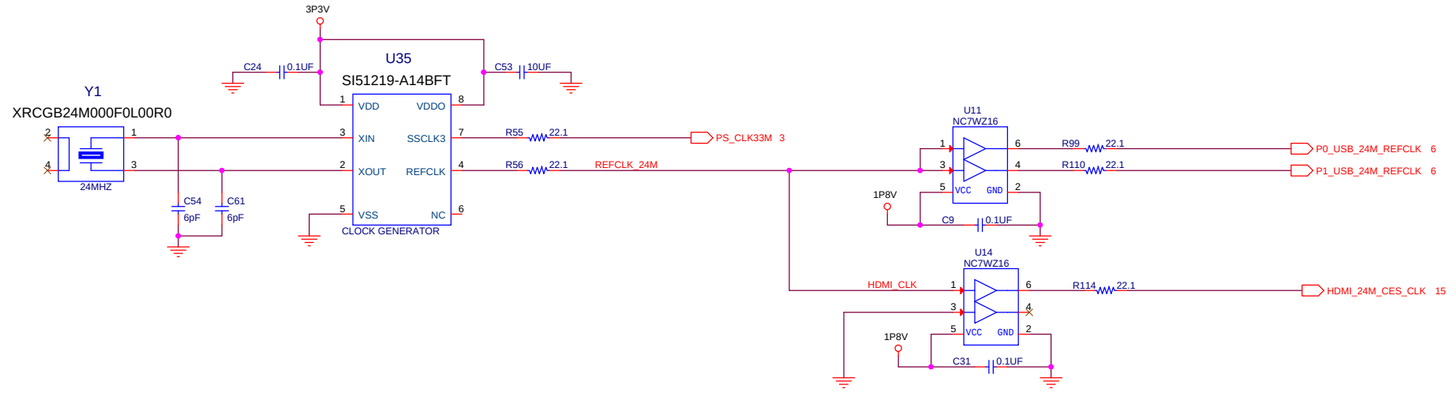
ZYNQ BANK0



BANK 0 OPERATING VOLTAGE = 3.3V

PROGRAMMABLE CLOCK GENERATOR

Place Close to U2



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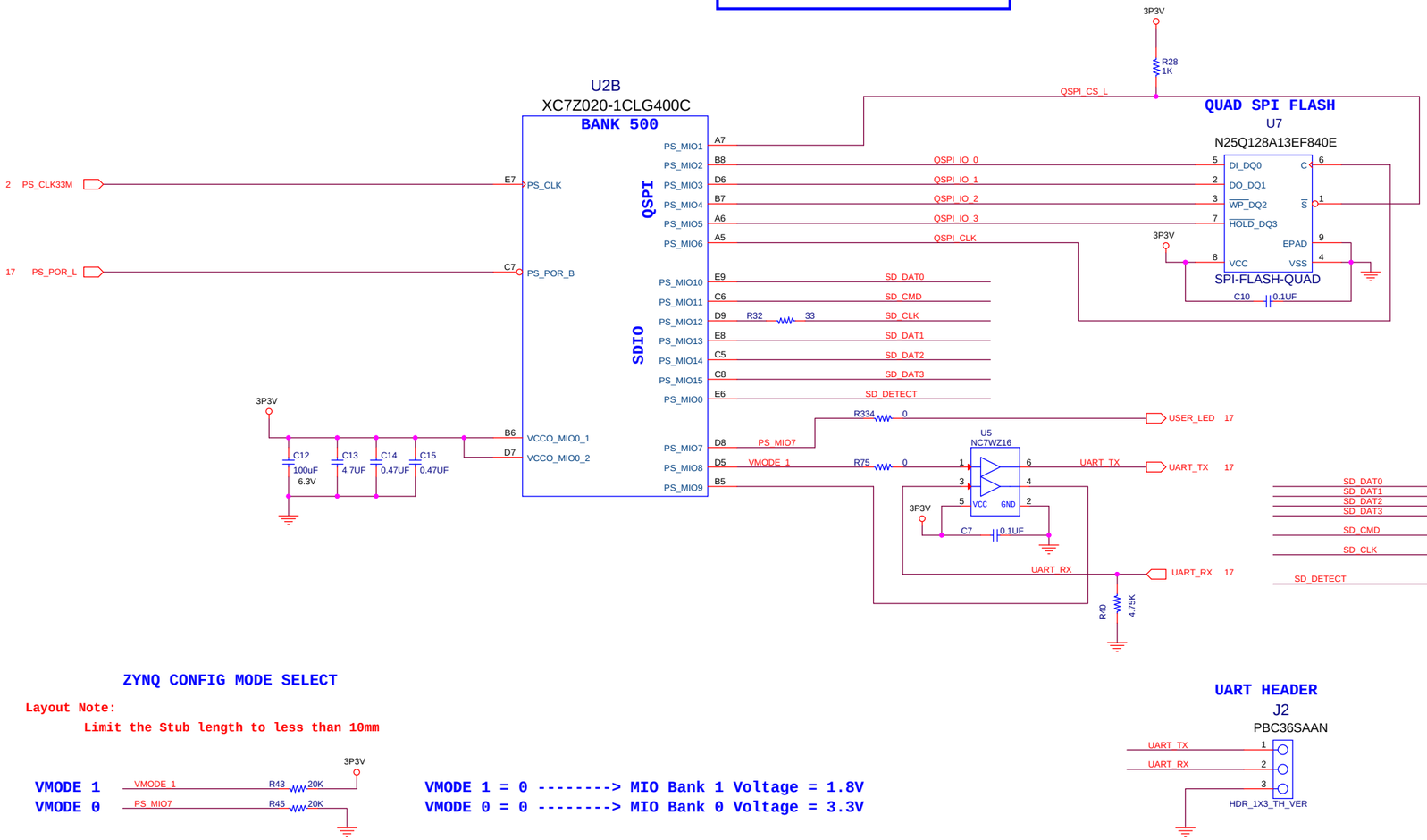
ZYNQ BANK 500

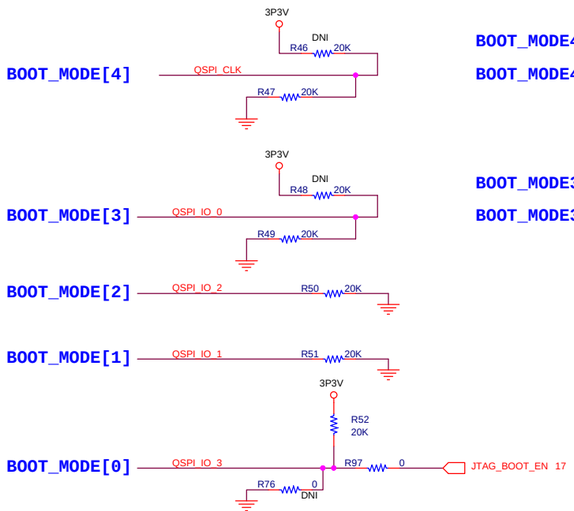


ZYNQ CONFIG MODE SELECT

Layout Note:
Limit the Stub length to less than 10mm

VMODE 1
VMODE 0

VMODE 1 = 0 --------> MIO Bank 1 Voltage = 1.8V
VMODE 0 = 0 --------> MIO Bank 0 Voltage = 3.3V



BOOT_MODE4 = 1 ---------> PLL Bypassed
BOOT_MODE4 = 0 ---------> PLL Used

BOOT_MODE3 = 1 ---------> Independant JTAG
BOOT_MODE3 = 0 ---------> Cascaded JTAG

BOOT_MODE[0]	BOOT_MODE[1]	BOOT_MODE[2]	BOOT_MODE[3]	
0	0	0	0	Boot from JTAG
1	0	0	x	Boot from QSPI

UART HEADER

J2
PBC36SAAN

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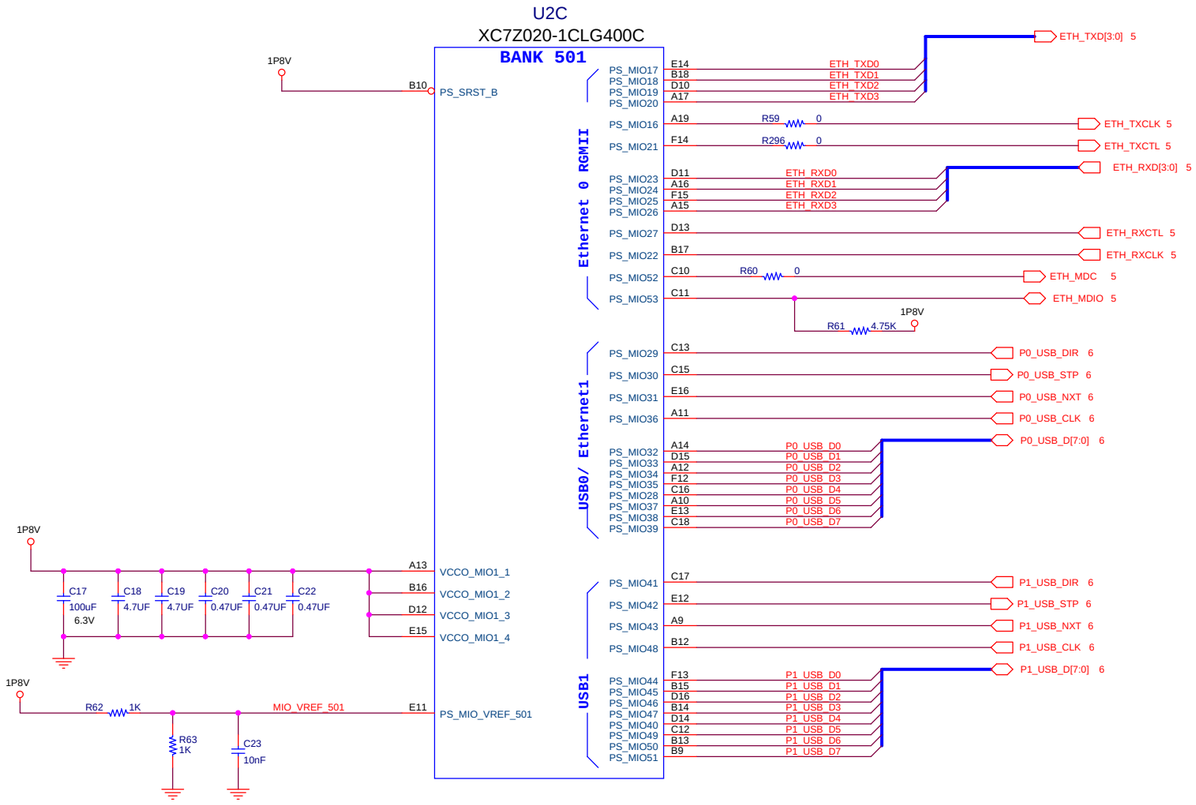
ZYNQ BANK 501



1.8V Interface IO

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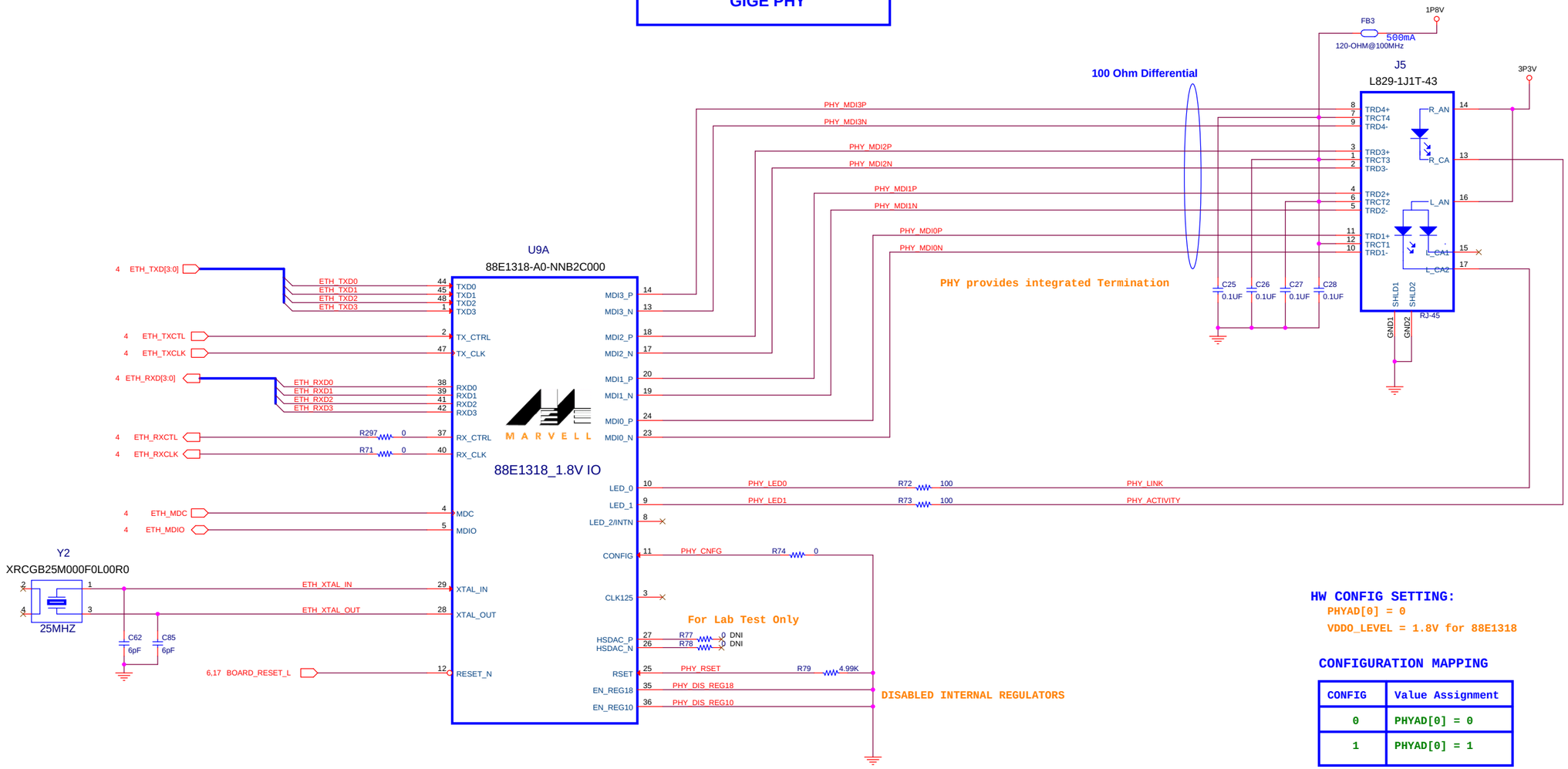
GIGE PHY



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USB PORTS

U12 — USB3320C-EZK-TR

USB_ULPI_XCVR

Pin	Name	Net
3	DATA[0]	P0_USB_D0
4	DATA[1]	P0_USB_D1
5	DATA[2]	P0_USB_D2
6	DATA[3]	P0_USB_D3
7	DATA[4]	P0_USB_D4
9	DATA[5]	P0_USB_D5
10	DATA[6]	P0_USB_D6
13	DATA[7]	P0_USB_D7
31	DIR	4 P0_USB_DIR
29	STP	4 P0_USB_STP
2	NXT	4 P0_USB_NXT
1	CLKOUT	4 P0_USB_CLK
26	REFCLK	2 P0_USB_24M_REFCLK
25	XO	
27	RESETB	5,17 BOARD_RESET_L
8	REFSEL[0]	1P8V
11	REFSEL[1]	1P8V
14	REFSEL[2]	1P8V
33	GND	
18	DP	P0_USB_DP
19	DM	P0_USB_DN
23	ID	R85 0 DNI; P0_USB_ID
22	VBUS	R86 1K; R116 0; P0_VBUS_DET
16	SPK_R	
15	SPK_L	
17	CPEN	P0_USB_CPEN
12	NC	
24	RBIAS	R90 8.06K
28	VDD18_1	1P8V; C55 0.1UF
30	VDD18_2	1P8V; C56 0.1UF
20	VDD33	C57 2.2UF
21	VBAT	SYS_5P0V
32	VDDIO	1P8V; C59 0.1UF; C60 0.1UF

100-ohm Differential

USB_PWR_GD

CR4 GREEN LTST-C193KGKT-5A DNI; R84 620 DNI

J6 — 10104111-0001LF

USB_MICRO_AB_RA

Pin	Name	Net
1	VBUS	P0_VBUS; C51 0.1UF
2	D_N	P0_USB_DN
3	D_P	P0_USB_DP
4	ID	P0_USB_ID
5	GND	
6	SHLD1	
7	SHLD2	
8	SHLD3	
9	SHLD4	

C260 0.1UF

USB HOST POWER

U13 MIC2025-1YM (USB PWR DIST)

Pin	Name	Net
1	EN	P0_USB_CPEN
7	IN	SYS_5P0V; C52 0.1UF
2	FLAG	P0_USB_FLAG
3	GND	
6	OUT1	P0_VBUS; C84 100uF 6.3V
8	OUT2	
5	NC2	
4	NC1	

3P3V; R89 240 DNI; CR5 RED LTST-C193KRKT-5A

USB_PWR_FAULT

U17 — USB3320C-EZK-TR

USB_ULPI_XCVR

Pin	Name	Net
3	DATA[0]	P1_USB_D0
4	DATA[1]	P1_USB_D1
5	DATA[2]	P1_USB_D2
6	DATA[3]	P1_USB_D3
7	DATA[4]	P1_USB_D4
9	DATA[5]	P1_USB_D5
10	DATA[6]	P1_USB_D6
13	DATA[7]	P1_USB_D7
31	DIR	4 P1_USB_DIR
29	STP	4 P1_USB_STP
2	NXT	4 P1_USB_NXT
1	CLKOUT	4 P1_USB_CLK
26	REFCLK	2 P1_USB_24M_REFCLK
25	XO	
27	RESETB	5,17 BOARD_RESET_L
8	REFSEL[0]	1P8V
11	REFSEL[1]	1P8V
14	REFSEL[2]	1P8V
33	GND	
18	DP	P1_USB_DP
19	DM	P1_USB_DN
23	ID	R101 0
22	VBUS	R103 10K; P1_VBUS_DET
16	SPK_R	
15	SPK_L	
17	CPEN	
12	NC	
24	RBIAS	R106 8.06K
28	VDD18_1	1P8V; C64 0.1UF
30	VDD18_2	1P8V; C65 0.1UF
20	VDD33	C66 2.2UF
21	VBAT	USB_VBUS; 1P8V
32	VDDIO	1P8V; C68 0.1UF; C69 0.1UF

100-ohm Differential

USB_PWR_GD

CR6 GREEN LTST-C193KGKT-5A DNI; R100 620 DNI

USB_VBUS

USB PC CONNECTOR

J7 — 10118193-0001LF

USB_MICRO_B_RA

Pin	Name	Net
1	VBUS	P1_VBUS; C63 4.7UF 16V
2	D_N	P1_USB_DN
3	D_P	P1_USB_DP
4	ID	
5	GND	
6	SHLD1	
7	SHLD2	
8	SHLD3	
9	SHLD4	

C261 0.1UF

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ZYNQ BANK 502

U2D

XC7Z020-1CLG400C

BANK 502

8 DDR_DQ[31:0]

DDR_DQ31	V3	PS_DDR_DQ31
DDR_DQ30	V2	PS_DDR_DQ30
DDR_DQ29	W3	PS_DDR_DQ29
DDR_DQ28	Y2	PS_DDR_DQ28
DDR_DQ27	Y4	PS_DDR_DQ27
DDR_DQ26	W1	PS_DDR_DQ26
DDR_DQ25	Y3	PS_DDR_DQ25
DDR_DQ24	V1	PS_DDR_DQ24
DDR_DQ23	U3	PS_DDR_DQ23
DDR_DQ22	U2	PS_DDR_DQ22
DDR_DQ21	U4	PS_DDR_DQ21
DDR_DQ20	T4	PS_DDR_DQ20
DDR_DQ19	R1	PS_DDR_DQ19
DDR_DQ18	R3	PS_DDR_DQ18
DDR_DQ17	P3	PS_DDR_DQ17
DDR_DQ16	P1	PS_DDR_DQ16
DDR_DQ15	J1	PS_DDR_DQ15
DDR_DQ14	H1	PS_DDR_DQ14
DDR_DQ13	H2	PS_DDR_DQ13
DDR_DQ12	J3	PS_DDR_DQ12
DDR_DQ11	H3	PS_DDR_DQ11
DDR_DQ10	G3	PS_DDR_DQ10
DDR_DQ9	E3	PS_DDR_DQ9
DDR_DQ8	E2	PS_DDR_DQ8
DDR_DQ7	E1	PS_DDR_DQ7
DDR_DQ6	C1	PS_DDR_DQ6
DDR_DQ5	D1	PS_DDR_DQ5
DDR_DQ4	D3	PS_DDR_DQ4
DDR_DQ3	A4	PS_DDR_DQ3
DDR_DQ2	A2	PS_DDR_DQ2
DDR_DQ1	B3	PS_DDR_DQ1
DDR_DQ0	C3	PS_DDR_DQ0

PS_DDR_A14	F4	DDR3_A14	R302	33	DDR_A14
PS_DDR_A13	D4	DDR3_A13	R303	33	DDR_A13
PS_DDR_A12	E4	DDR3_A12	R304	33	DDR_A12
PS_DDR_A11	G4	DDR3_A11	R305	33	DDR_A11
PS_DDR_A10	F5	DDR3_A10	R306	33	DDR_A10
PS_DDR_A9	J4	DDR3_A9	R307	33	DDR_A9
PS_DDR_A8	K1	DDR3_A8	R308	33	DDR_A8
PS_DDR_A7	K4	DDR3_A7	R309	33	DDR_A7
PS_DDR_A6	L4	DDR3_A6	R310	33	DDR_A6
PS_DDR_A5	L1	DDR3_A5	R311	33	DDR_A5
PS_DDR_A4	M4	DDR3_A4	R312	33	DDR_A4
PS_DDR_A3	K3	DDR3_A3	R313	33	DDR_A3
PS_DDR_A2	M3	DDR3_A2	R314	33	DDR_A2
PS_DDR_A1	K2	DDR3_A1	R315	33	DDR_A1
PS_DDR_A0	N2	DDR3_A0	R316	33	DDR_A0

DDR_A[14:0] 8

PS_DDR_BA2	J5	DDR3_BA2	R317	33	DDR_BA2 8
PS_DDR_BA1	R4	DDR3_BA1	R318	33	DDR_BA1 8
PS_DDR_BA0	L5	DDR3_BA0	R319	33	DDR_BA0 8

PS_DDR_ODT	N5	DDR3_ODT	R320	33	DDR_ODT 8
PS_DDR_CS_B	N1	DDR3_CS_L	R321	33	DDR_CS_L 8
PS_DDR_WE_B	M5	DDR3_WE_L	R322	33	DDR_WE_L 8
PS_DDR_CAS_B	P5	DDR3_CAS_L	R323	33	DDR_CAS_L 8
PS_DDR_RAS_B	P4	DDR3_RAS_L	R324	33	DDR_RAS_L 8

PS_DDR_CKE	N3	DDR3_CKE	R325	10	DDR_CKE 8

PS_DDR_CKP	L2	DDR_CLK_P 8
PS_DDR_CKN	M2	DDR_CLK_N 8

8 DDR_DQS_P3 → W5 PS_DDR_DQS_P3
8 DDR_DQS_N3 → W4 PS_DDR_DQS_N3
8 DDR_DQS_P2 → R2 PS_DDR_DQS_P2
8 DDR_DQS_N2 → T2 PS_DDR_DQS_N2
8 DDR_DQS_P1 → G2 PS_DDR_DQS_P1
8 DDR_DQS_N1 → F2 PS_DDR_DQS_N1
8 DDR_DQS_P0 → C2 PS_DDR_DQS_P0
8 DDR_DQS_N0 → B2 PS_DDR_DQS_N0

PS_DDR_DM3	Y1	DDR_DM3 8
PS_DDR_DM2	T1	DDR_DM2 8
PS_DDR_DM1	F1	DDR_DM1 8
PS_DDR_DM0	A1	DDR_DM0 8

PS_DDR_DRST_B — B4 — R111 4.75K — DDR_RST_L 8

PS_DDR_VRN — G5 — R112 80.6 — 1P35V
PS_DDR_VRP — H5 — R113 80.6

PS_DDR_VREF0 — H6
PS_DDR_VREF1 — P6 — DDR_VREF — C82 10nF — C83 0.1UF — R66 1K — R67 1K — 1P35V

1P35V

A3	VCCO_DDR_1	C70 100uF 6.3V
D2	VCCO_DDR_2	C71 100uF 6.3V
E5	VCCO_DDR_3	C72 4.7UF
G1	VCCO_DDR_4	C73 4.7UF
H4	VCCO_DDR_5	C74 4.7UF
L3	VCCO_DDR_6	C75 0.47UF
P2	VCCO_DDR_7	C76 0.47UF
R5	VCCO_DDR_8	C77 0.47UF
U1	VCCO_DDR_9	C78 0.47UF
V4	VCCO_DDR_10	C79 0.47UF
		C80 0.47UF
		C81 0.47UF

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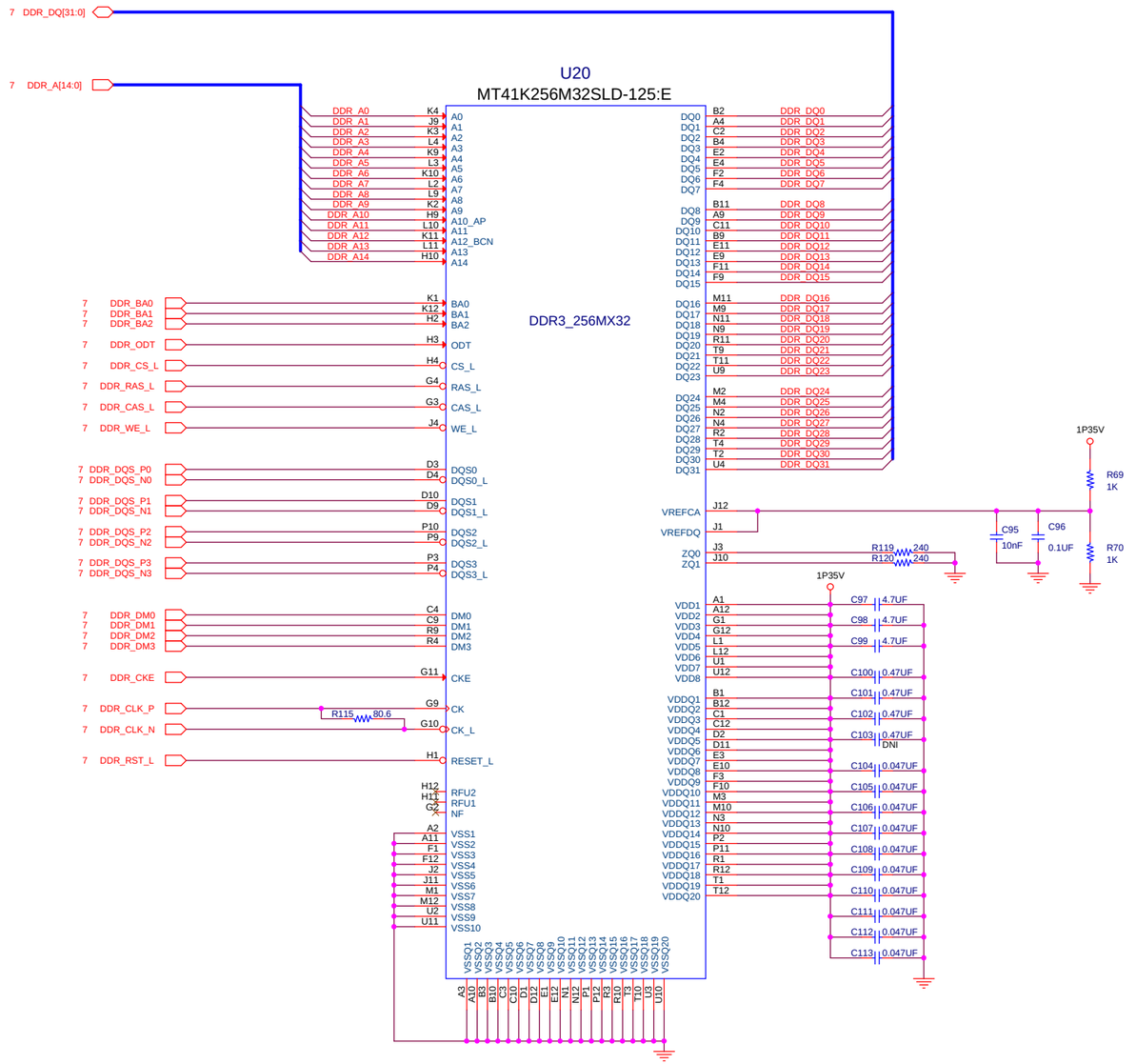
DDR3 - 256M X 32



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BANKS 34 & 35

Enable 100-ohm internal termination on all LVDS inputs

15 HDMI_D[23:8]

U2F
XC7Z020-1CLG400C
BANK 34

		HDMI_D18	R19	IO_0_34	
				IO_25_34	T19 HDMI_D17
15	GPIO11_P		T11	IO_L1P_T0_34	
15	GPIO11_N		T10	IO_L1N_T0_34	
15	GPIO10_P		T12	IO_L2P_T0_34	
15	GPIO10_N		U12	IO_L2N_T0_34	
15	GPIO8_P		U13	IO_L3P_T0_DQS_PUDC_B_34	
15	GPIO8_N		V13	IO_L3N_T0_DQS_34	
15	GPIO9_P		V12	IO_L4P_T0_34	
15	GPIO9_N		W13	IO_L4N_T0_34	
15	GPIO5_P		T14	IO_L5P_T0_34	
15	GPIO5_N		T15	IO_L5N_T0_34	
15	GPIO4_P		P14	IO_L6P_T0_34	
15	GPIO4_N		R14	IO_L6N_T0_VREF_34	
15,17	SPDIF	22.1 R82	Y16	IO_L7P_T1_34	
15	HDMI_DE	22.1 R94	Y17	IO_L7N_T1_34	
15	GPIO7_P		W14	IO_L8P_T1_34	
15	GPIO7_N		Y14	IO_L8N_T1_34	
15	GPIO0_P		T16	IO_L9P_T1_DQS_34	
15	GPIO0_N		U17	IO_L9N_T1_DQS_34	
		HDMI_D11	V15	IO_L10P_T1_34	
		HDMI_D16	W15	IO_L10N_T1_34	
15	GPIO6_P		U14	IO_L11P_T1_SRCC_34	
15	GPIO6_N		U15	IO_L11N_T1_SRCC_34	
15	GPIO3_P		U18	IO_L12P_T1_MRCC_34	
15	GPIO3_N		U19	IO_L12N_T1_MRCC_34	
			N18	IO_L13P_T2_MRCC_34	
		HDMI_D19	P19	IO_L13N_T2_MRCC_34	
			N20	IO_L14P_T2_SRCC_34	
			P20	IO_L14N_T2_SRCC_34	
		HDMI_D23	T20	IO_L15P_T2_DQS_34	
		HDMI_D22	U20	IO_L15N_T2_DQS_34	
		HDMI_D21	V20	IO_L16P_T2_34	
		HDMI_D20	W20	IO_L16N_T2_34	
		HDMI_D8	Y18	IO_L17P_T2_34	
		HDMI_D14	Y19	IO_L17N_T2_34	
			V16	IO_L18P_T2_34	
			W16	IO_L18N_T2_34	
			R16	IO_L19P_T3_34	
		R41 22.1	R17	IO_L19N_T3_VREF_34	
		R44 22.1	T17	IO_L20P_T3_34	
		HDMI_D12	R18	IO_L20N_T3_34	
		R42 22.1	V17	IO_L21P_T3_DQS_34	
		HDMI_D10	V18	IO_L21N_T3_DQS_34	
		HDMI_D9	W18	IO_L22P_T3_34	
		HDMI_D15	W19	IO_L22N_T3_34	
			N17	IO_L23P_T3_34	
		HDMI_D13	P18	IO_L23N_T3_34	
			P15	IO_L24P_T3_34	
			P16	IO_L24N_T3_34	

VDD_GPIO
R20 4.75K
PS_I2C_SCL 15
PROG_IO 17
HDMI_INT 15
GPIO1_P 15
GPIO1_N 15
TURBO_MODE 16,17
HDMI_CLK 15
HDMI_HSYNC 15
HDMI_VSYNC 15
VDD_GPIO
R18 4.75K
PS_I2C_SDA 15
GPIO2_P 15
GPIO2_N 15

R223 1K

VDD_GPIO
N19 VCCO_34_1
R15 VCCO_34_2
T18 VCCO_34_3
V14 VCCO_34_4
W17 VCCO_34_5
Y20 VCCO_34_6

C126 0.47UF, C127 0.47UF, C128 0.47UF, C129 0.47UF, C130 0.47UF, C131 4.7UF, C132 4.7UF, C133 4.7UF, C134 100uF 6.3V

U2G
XC7Z020-1CLG400C
BANK 35

11	DSP_RESET_L	DSP_RESET_L R178 1K	G14	IO_0_35	
				IO_25_34	J15 RXO_EA_RD_WAIT 11
11	RXI_EA_DATA1_P		C20	IO_L1P_T0_AD0P_35	
11	RXI_EA_DATA1_N		B20	IO_L1N_T0_AD0N_35	
11	RXI_EA_DATA0_P		B19	IO_L2P_T0_AD8P_35	
11	RXI_EA_DATA0_N		A20	IO_L2N_T0_AD8N_35	
11	RXI_EA_DATA4_P		E17	IO_L3P_T0_DQS_AD1P_35	
11	RXI_EA_DATA4_N		D18	IO_L3N_T0_DQS_AD1N_35	
11	RXI_EA_DATA2_P		D19	IO_L4P_T0_35	
11	RXI_EA_DATA2_N		D20	IO_L4N_T0_35	
11	RXI_EA_DATA3_P		E18	IO_L5P_T0_AD9P_35	
11	RXI_EA_DATA3_N		E19	IO_L5N_T0_AD9N_35	
11	RXI_EA_LCLK_P		F16	IO_L6P_T0_35	
11	RXI_EA_LCLK_N		F17	IO_L6N_T0_VREF_35	
11	TXO_EA_DATA5_P		M19	IO_L7P_T1_AD2P_35	
11	TXO_EA_DATA5_N		M20	IO_L7N_T1_AD2N_35	
11	TXO_EA_DATA6_P		M17	IO_L8P_T1_AD10P_35	
11	TXO_EA_DATA6_N		M18	IO_L8N_T1_AD10N_35	
11	TXO_EA_DATA4_P		L19	IO_L9P_T1_DQS_AD3P_35	
11	TXO_EA_DATA4_N		L20	IO_L9N_T1_DQS_AD3N_35	
11	TXO_EA_DATA0_P		K19	IO_L10P_T1_AD11P_35	
11	TXO_EA_DATA0_N		J19	IO_L10N_T1_AD11N_35	
11	TXO_EA_DATA2_P		L16	IO_L11P_T1_SRCC_35	
11	TXO_EA_DATA2_N		L17	IO_L11N_T1_SRCC_35	
11	TXO_EA_LCLK_P		K17	IO_L12P_T1_MRCC_35	
11	TXO_EA_LCLK_N		K18	IO_L12N_T1_MRCC_35	
			H16	IO_L13P_T2_MRCC_35	
			H17	IO_L13N_T2_MRCC_35	
			J18	IO_L14P_T2_AD4P_SRCC_35	
			H18	IO_L14N_T2_AD4N_SRCC_35	
			F19	IO_L15P_T2_DQS_AD12P_35	
			F20	IO_L15N_T2_DQS_AD12N_35	
			G17	IO_L16P_T2_35	
			G18	IO_L16N_T2_35	
			J20	IO_L17P_T2_AD5P_35	
			H20	IO_L17N_T2_AD5N_35	
			G19	IO_L18P_T2_AD13P_35	
			G20	IO_L18N_T2_AD13N_35	
			H15	IO_L19P_T3_35	
			G15	IO_L19N_T3_VREF_35	
			K14	IO_L20P_T3_AD6P_35	
			J14	IO_L20N_T3_AD6N_35	
			N15	IO_L21P_T3_DQS_AD14P_35	
			N16	IO_L21N_T3_DQS_AD14N_35	
			L14	IO_L22P_T3_AD7P_35	
			L15	IO_L22N_T3_AD7N_35	
			M14	IO_L23P_T3_35	
			M15	IO_L23N_T3_35	
			K16	IO_L24P_T3_AD15P_35	
			J16	IO_L24N_T3_AD15N_35	

RXI_CCLK_P 13
RXI_CCLK_N 13
RXO_EA_WR_WAIT_P 11
RXO_EA_WR_WAIT_N 11
RXI_EA_DATA5_P 11
RXI_EA_DATA5_N 11
RXI_EA_DATA6_P 11
RXI_EA_DATA6_N 11
TXO_EA_FRAME_P 11
TXO_EA_FRAME_N 11
RXI_EA_DATA7_P 11
RXI_EA_DATA7_N 11
RXI_EA_FRAME_P 11
RXI_EA_FRAME_N 11
TXI_EA_RD_WAIT_P 11
TXI_EA_RD_WAIT_N 11
TXO_EA_DATA7_P 11
TXO_EA_DATA7_N 11
TXO_EA_DATA1_P 11
TXO_EA_DATA1_N 11
TXO_EA_DATA3_P 11
TXO_EA_DATA3_N 11
TXI_EA_WR_WAIT_P 11
TXI_EA_WR_WAIT_N 11

2P5V
C19 VCCO_35_1
F18 VCCO_35_2
H14 VCCO_35_3
J17 VCCO_35_4
K20 VCCO_35_5
M16 VCCO_35_6

C135 0.47UF, C136 0.47UF, C137 0.47UF, C138 0.47UF, C139 0.47UF, C140 4.7UF, C141 4.7UF, C142 4.7UF, C143 100uF 6.3V

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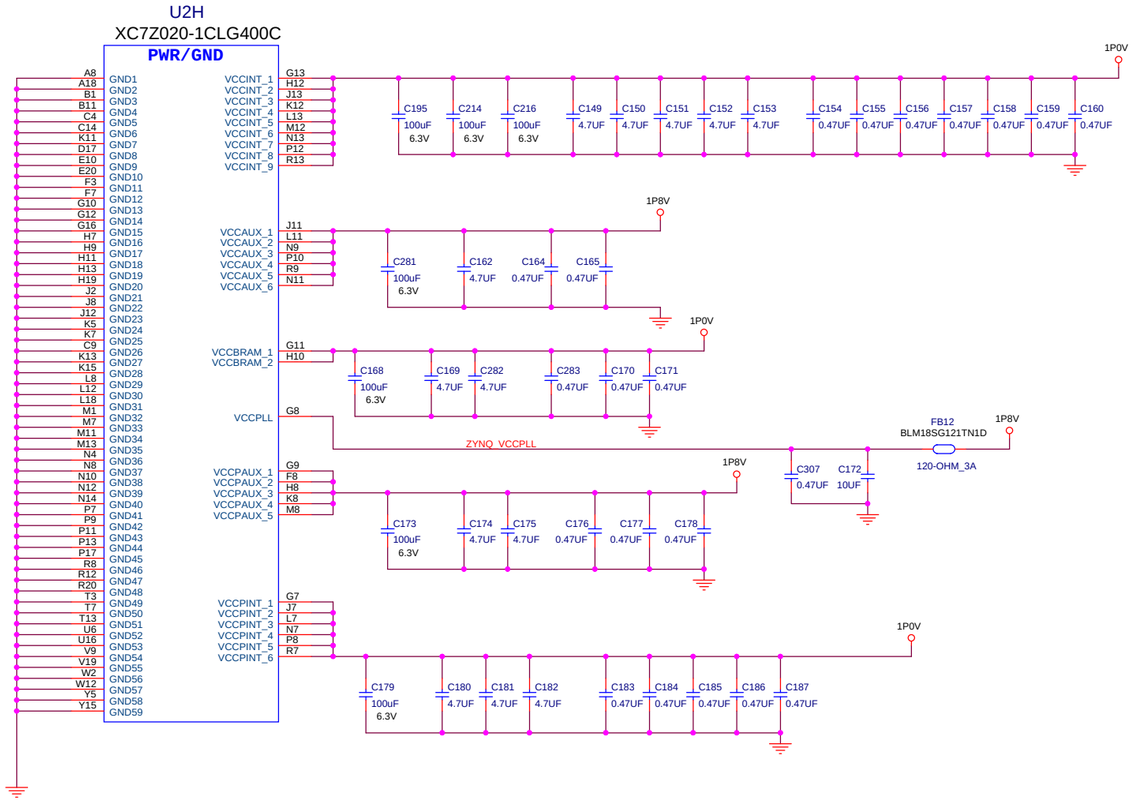
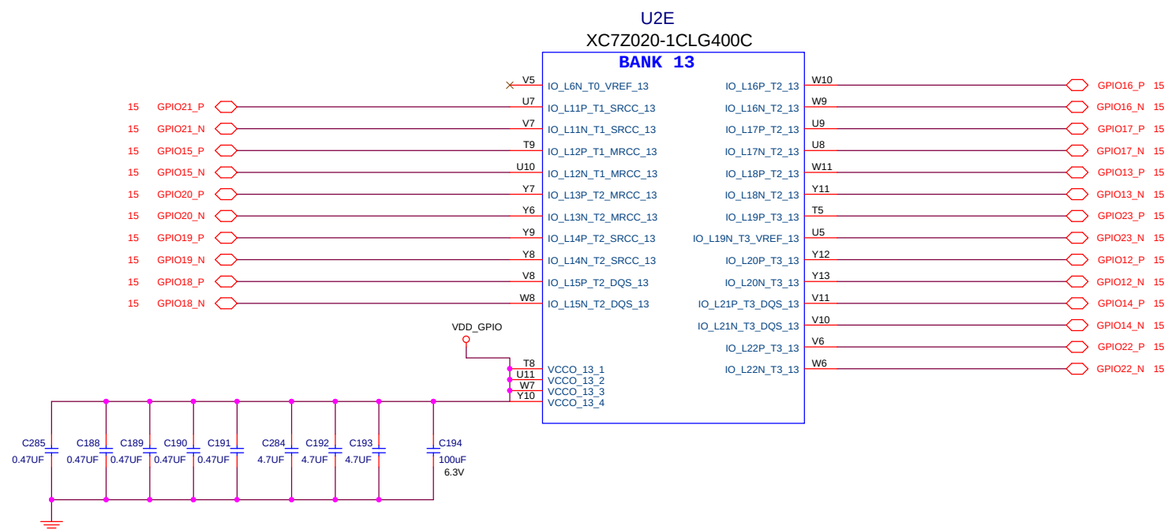
ZYNQ POWER & GROUND





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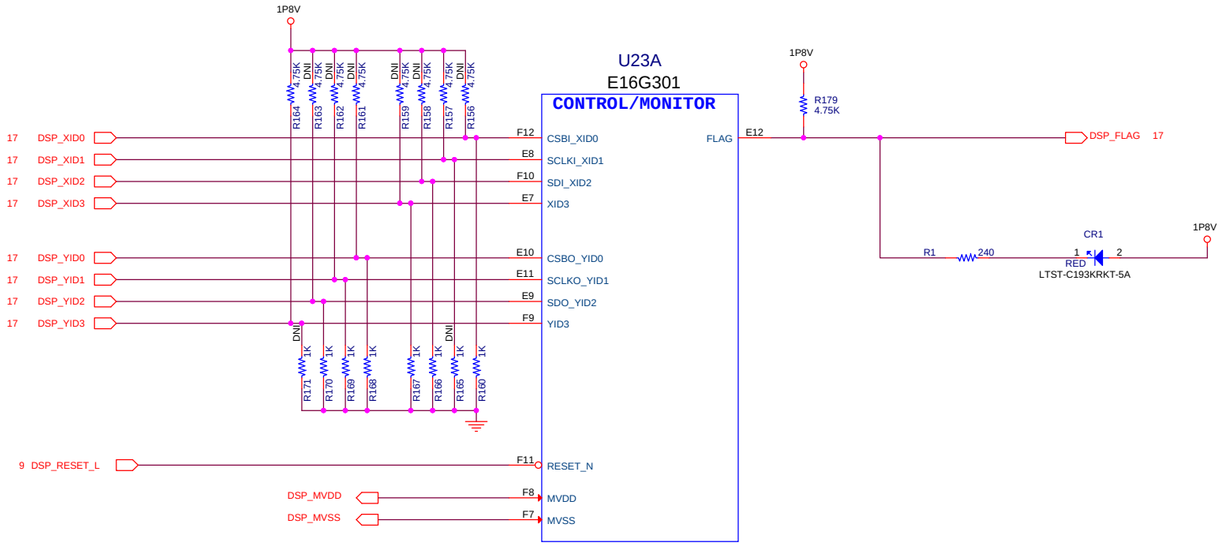
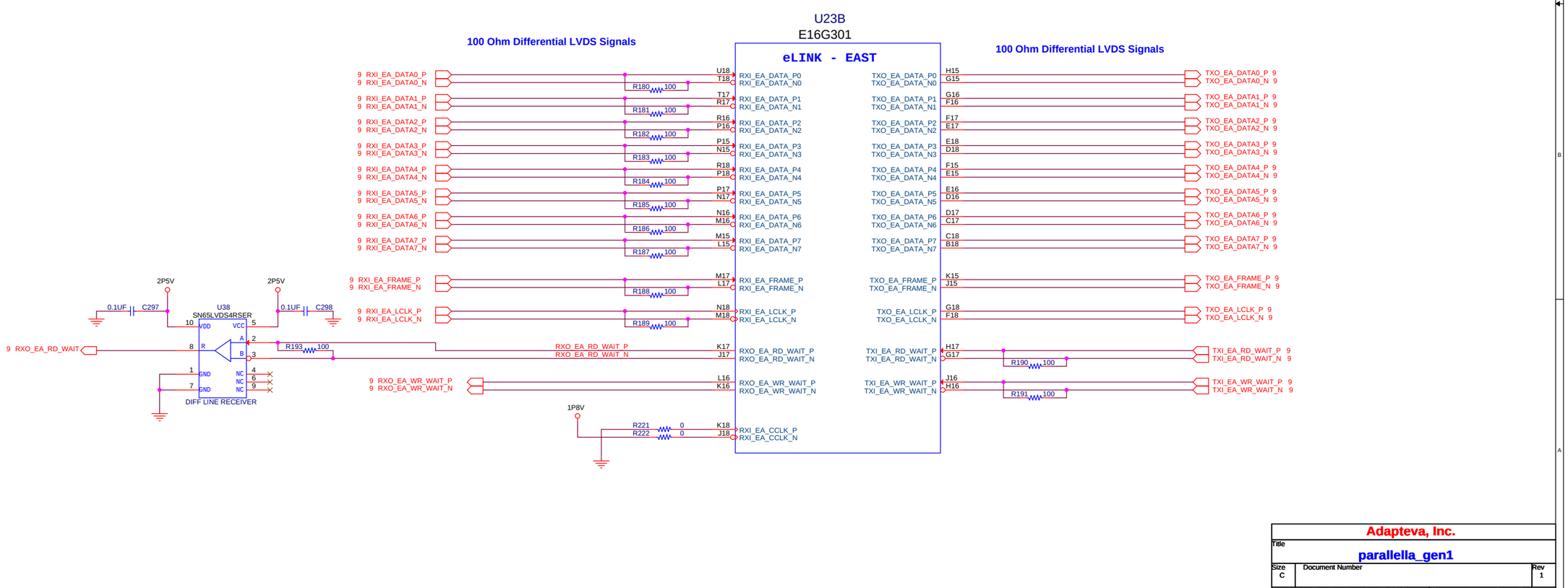
DSP PROCESSOR 1-OF-3





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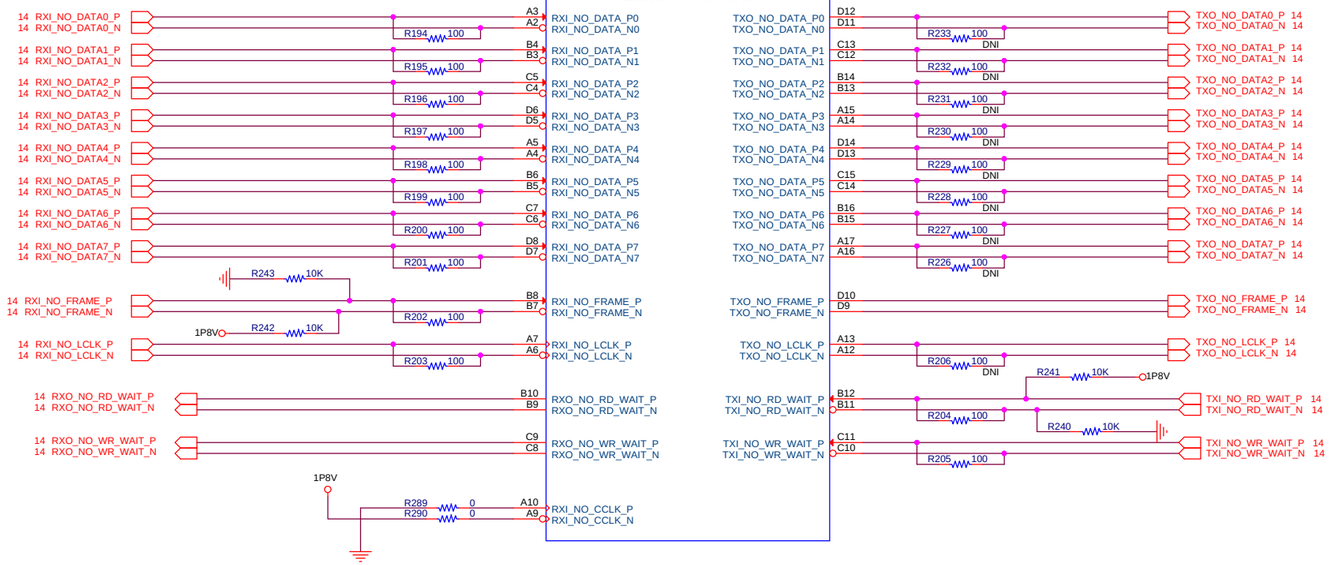
DSP PROCESSOR 2-OF-3

U23C
E16G301

100 Ohm Differential LVDS Signals

eLINK - NORTH

100 Ohm Differential LVDS Signals

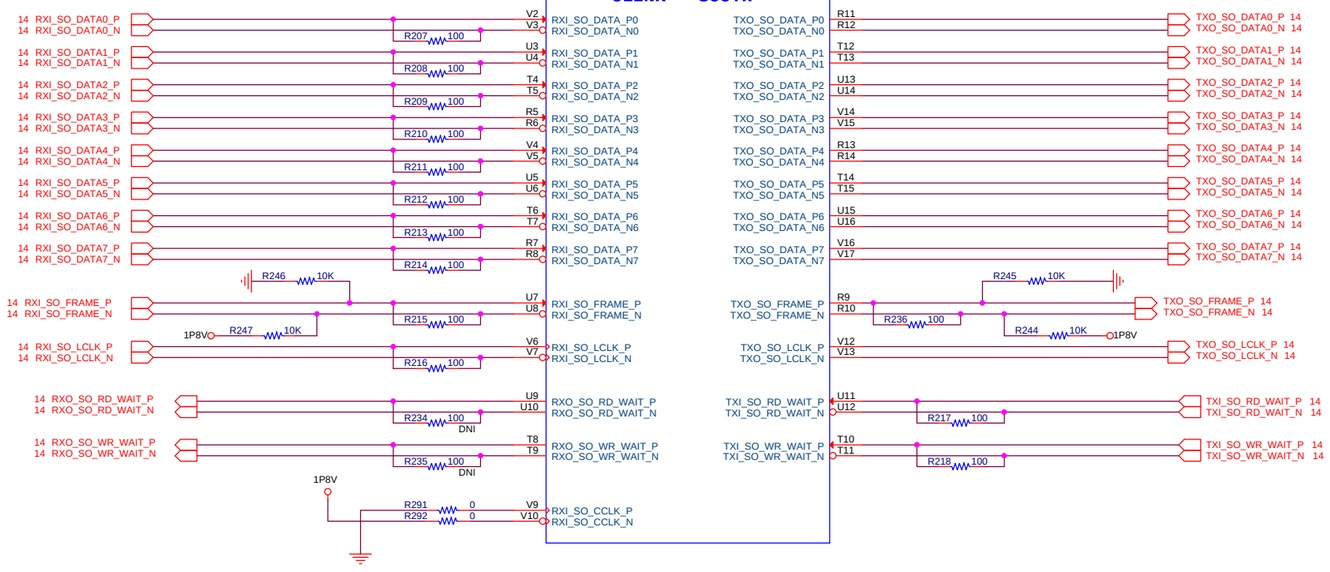


U23D
E16G301

100 Ohm Differential LVDS Signals

eLINK - SOUTH

100 Ohm Differential LVDS Signals



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DSP PROCESSOR 3-OF-3

U23F
E16G301

POWER/GROUND

VDD_DSP

C213 0.1UF, C215 0.1UF, C217 0.1UF, C219 0.1UF, C221 0.1UF, C223 0.1UF, C225 0.1UF, C227 0.1UF

VDD1 H6, VDD2 H8, VDD3 H10, VDD4 H12, VDD5 J7, VDD6 J9, VDD7 J11, VDD8 J13, VDD9 K6, VDD10 K8, VDD11 K10, VDD12 K12, VDD13 L7, VDD14 L9, VDD15 L11, VDD16 L13, VDD17 M6, VDD18 M8, VDD19 M10, VDD20 M12, VDD21 N7, VDD22 N9, VDD23 N11, VDD24 N13

VSS1 A1, VSS2 A8, VSS3 A11, VSS4 A18, VSS5 B2, VSS6 B17, VSS7 C3, VSS8 C16, VSS9 D4, VSS10 D15, VSS11 E5, VSS12 E6, VSS13 E13, VSS14 E14, VSS15 F5, VSS16 F6, VSS17 F13, VSS18 F14, VSS19 G6, VSS20 G8, VSS21 G10, VSS22 G12, VSS23 G14, VSS24 H1, VSS25 H5, VSS26 H7

VSS27 H9, VSS28 H11, VSS29 H13, VSS30 H18, VSS31 J6, VSS32 J8, VSS33 J10, VSS34 J12, VSS35 J14, VSS36 K5, VSS37 K7, VSS38 K9, VSS39 K11, VSS40 K13, VSS41 L1, VSS42 L6, VSS43 L8, VSS44 L10, VSS45 L12, VSS46 L14, VSS47 L18

VSS48 M5, VSS49 M7, VSS50 M9, VSS51 M11, VSS52 M13, VSS53 N6, VSS54 N8, VSS55 N10, VSS56 N12, VSS57 N14, VSS58 P5, VSS59 P7, VSS60 P9, VSS61 P11, VSS62 P13, VSS63 R4, VSS64 R15, VSS65 T3, VSS66 T16, VSS67 U2, VSS68 U17, VSS69 V1, VSS70 V8, VSS71 V11, VSS72 V18

1P8V

DVDD1 G5, DVDD2 G7, DVDD3 G9, DVDD4 G11, DVDD5 G13, DVDD6 H14, DVDD7 J5, DVDD8 K14, DVDD9 L5, DVDD10 M14, DVDD11 N5, DVDD12 P6, DVDD13 P8, DVDD14 P10, DVDD15 P12, DVDD16 P14

C197 0.1UF, C198 10nF DNI, C199 0.1UF, C200 10nF DNI, C201 0.1UF, C202 10nF DNI, C203 0.1UF, C204 10nF DNI, C205 0.1UF, C206 10nF DNI, C207 0.1UF, C208 10nF DNI, C209 0.1UF, C210 10nF DNI, C211 0.1UF, C212 10nF DNI

U23E
E16G301

eLINK - WEST

RXI_WE_DATA_P0 T1, RXI_WE_DATA_N0 U1
RXI_WE_DATA_P1 R2, RXI_WE_DATA_N1 T2
RXI_WE_DATA_P2 P3, RXI_WE_DATA_N2 R3
RXI_WE_DATA_P3 N4, RXI_WE_DATA_N3 P4
RXI_WE_DATA_P4 P1, RXI_WE_DATA_N4 R1
RXI_WE_DATA_P5 N2, RXI_WE_DATA_N5 P2
RXI_WE_DATA_P6 M3, RXI_WE_DATA_N6 N3
RXI_WE_DATA_P7 L4, RXI_WE_DATA_N7 M4

TXO_WE_DATA_P0 G4, TXO_WE_DATA_N0 H4
TXO_WE_DATA_P1 F3, TXO_WE_DATA_N1 G3
TXO_WE_DATA_P2 E2, TXO_WE_DATA_N2 F2
TXO_WE_DATA_P3 D1, TXO_WE_DATA_N3 E1
TXO_WE_DATA_P4 E4, TXO_WE_DATA_N4 F4
TXO_WE_DATA_P5 D3, TXO_WE_DATA_N5 E3
TXO_WE_DATA_P6 C2, TXO_WE_DATA_N6 D2
TXO_WE_DATA_P7 B1, TXO_WE_DATA_N7 C1

1P8V

R219 0, R220 0

RXI_WE_FRAME_P L2, RXI_WE_FRAME_N M2

TXO_WE_FRAME_P J4, TXO_WE_FRAME_N K4

R238 0, R239 0 DNI

1P8V

RXI_WE_LCLK_P M1, RXI_WE_LCLK_N N1

TXO_WE_LCLK_P F1, TXO_WE_LCLK_N G1

RXO_WE_RD_WAIT_P J2, RXO_WE_RD_WAIT_N K2

TXI_WE_RD_WAIT_P G2, TXI_WE_RD_WAIT_N H2

RXO_WE_WR_WAIT_P K3, RXO_WE_WR_WAIT_N L3

TXI_WE_WR_WAIT_P H3, TXI_WE_WR_WAIT_N J3

9 RXI_CCLK_P, 9 RXI_CCLK_N

R192 100

RXI_WE_CCLK_P J1, RXI_WE_CCLK_N K1

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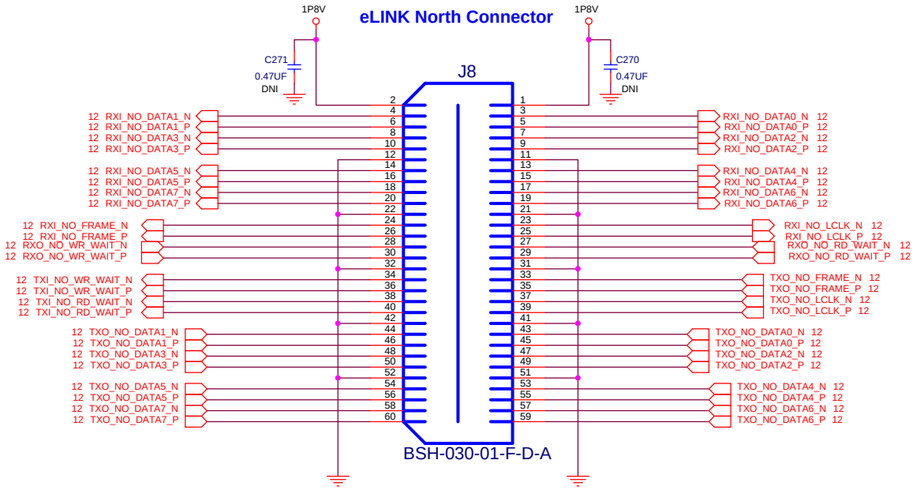
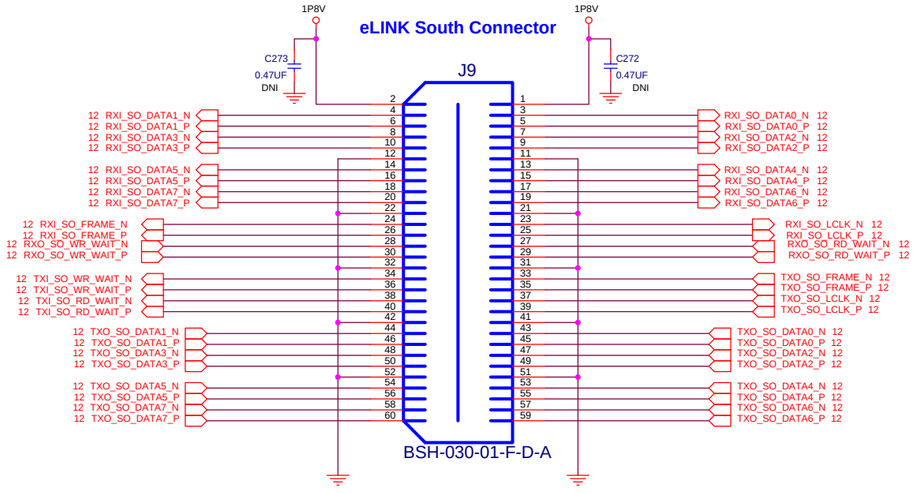
DSP eLINK CONNECTORS





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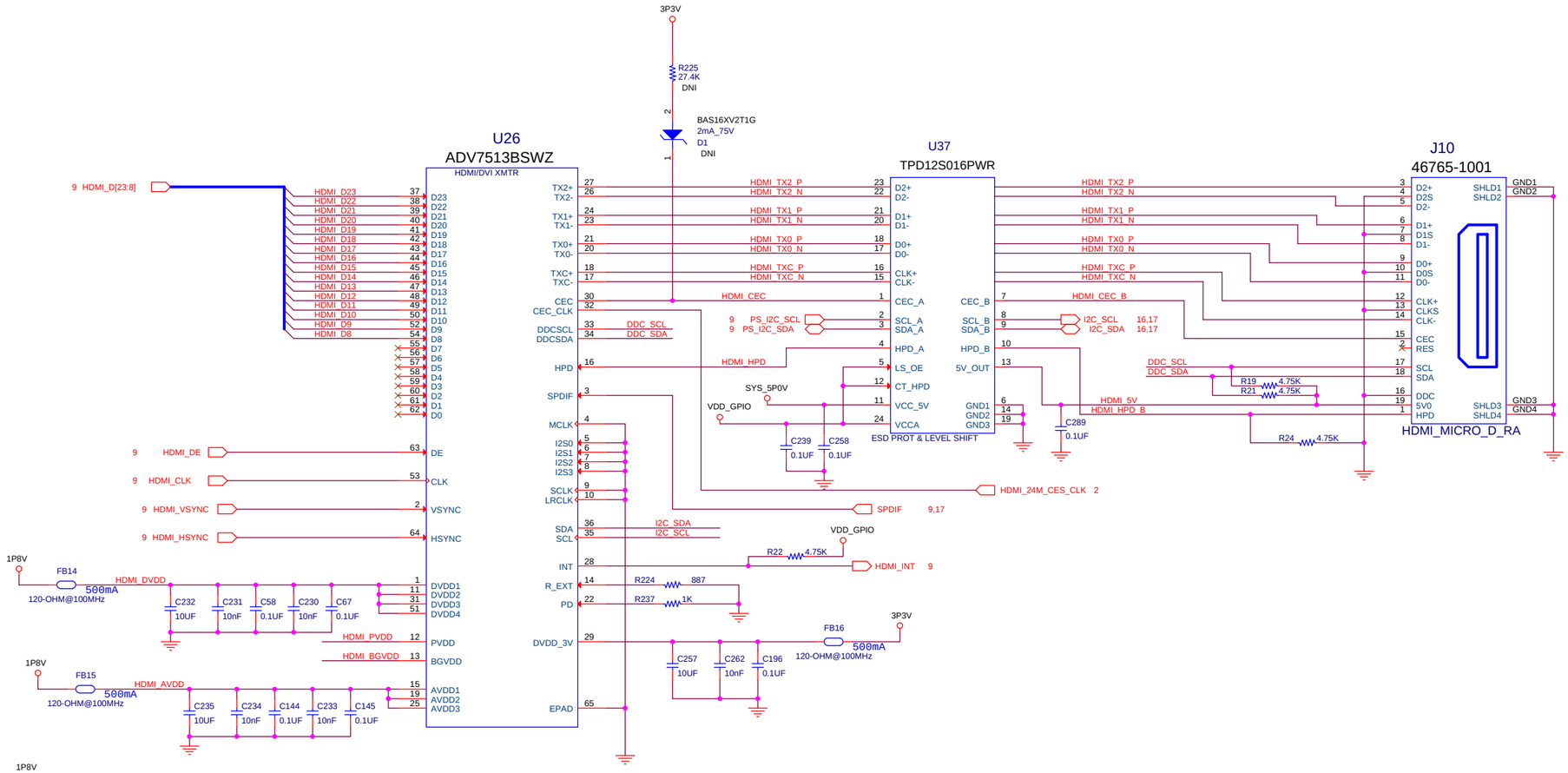
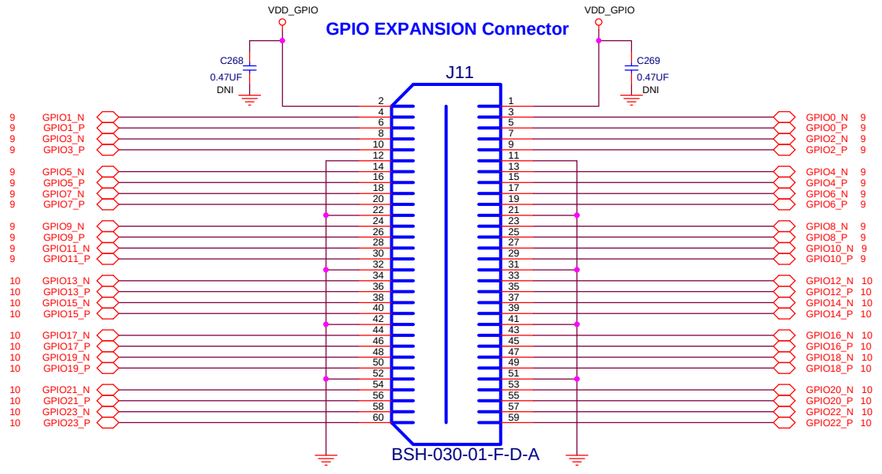
HDMI TRANSMITTER





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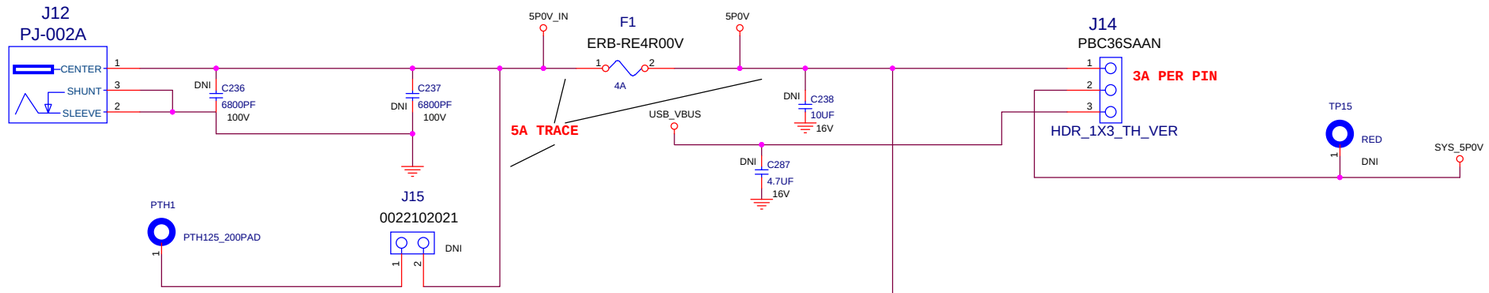
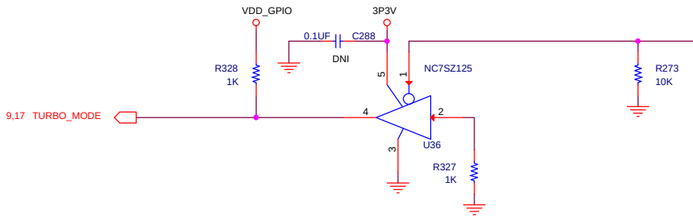
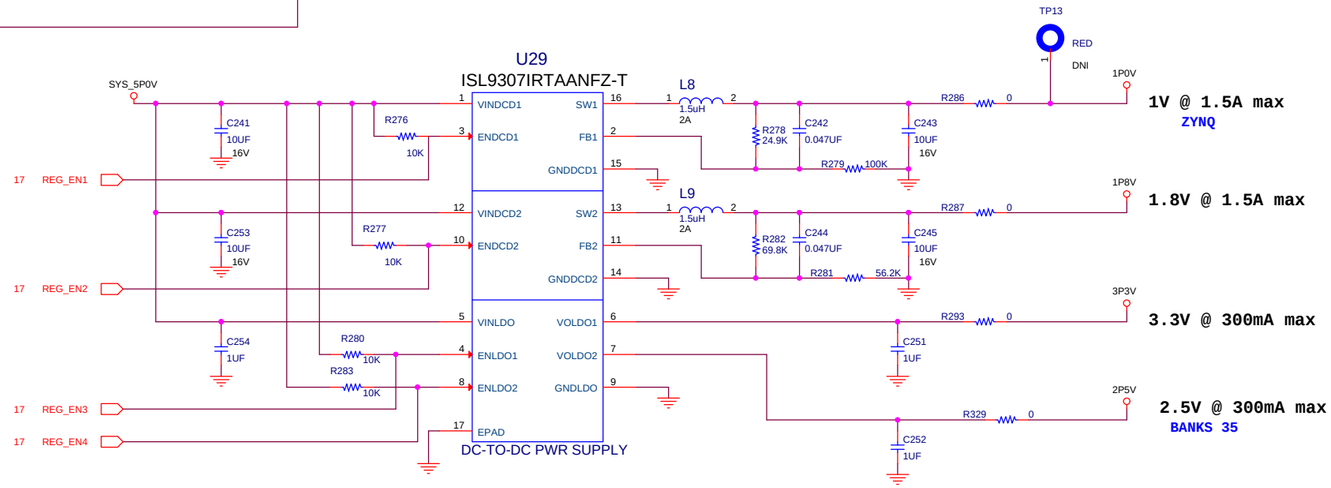
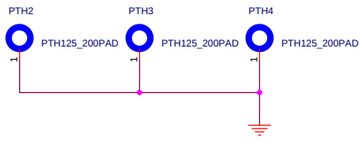
POWER MANAGEMENT

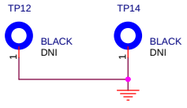


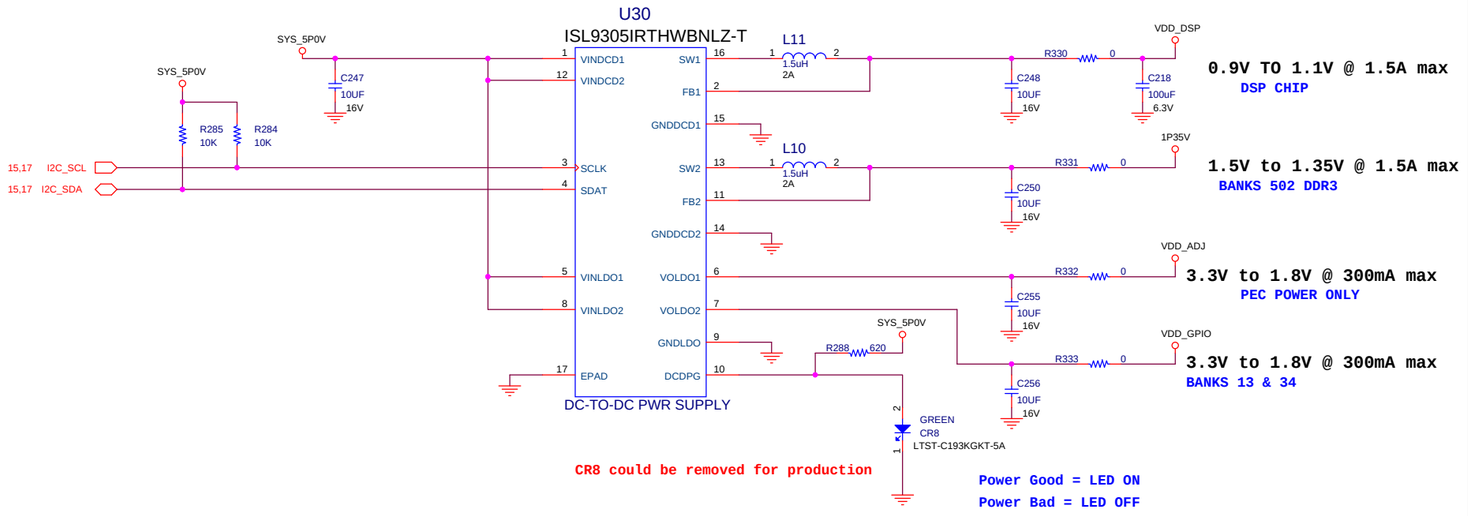




BOARD MOUNTING HOLES







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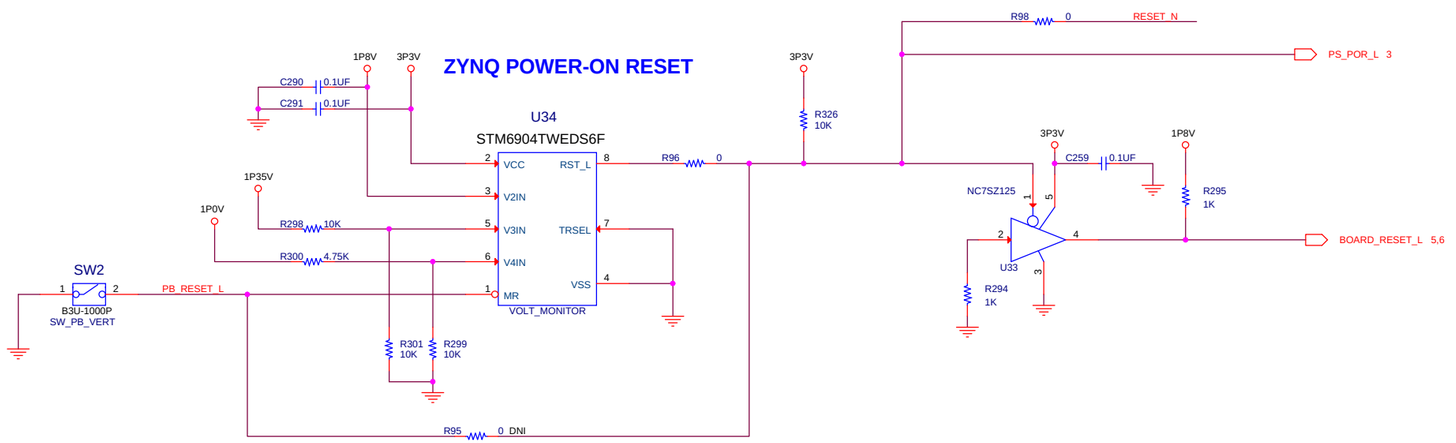
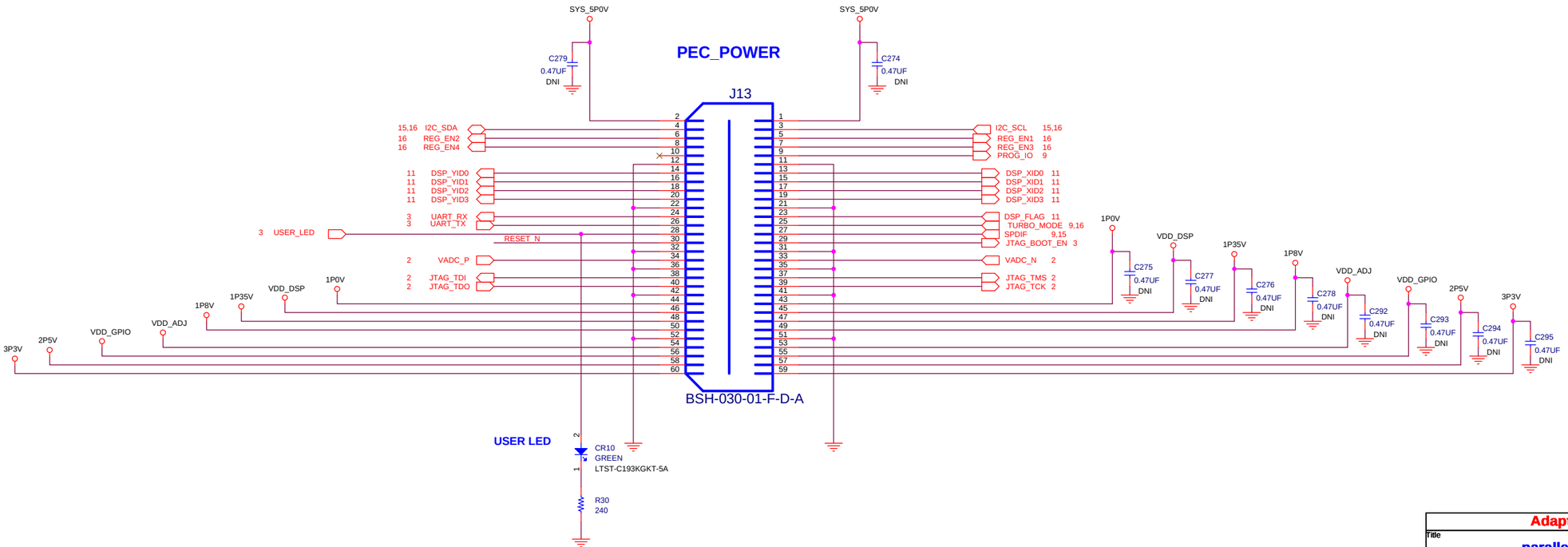
RESET GENERATION

ZYNQ POWER-ON RESET



PEC_POWER



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