TwinDie™ 1.35V DDR3L-RS SDRAM

MT41K256M32 – 32 Meg x 32 x 8 Banks

Description

The 8Gb TwinDie DDR3L-RS SDRAM (1.35V) is a low-current self refresh version, via a TCSR feature, of the DDR3L SDRAM (1.35V) device. It uses two Micron 4Gb DDR3L-RS SDRAM x16 die for a quad byte device in one package. Unless stated otherwise, the DDR3L-RS meets the functional and timing specifications listed in the equivalent density DDR3L SDRAM data sheets. Refer to Micron's 4Gb DDR3L SDRAM data sheet for the specifications not included in this document. Specifications for base part number MT41K256M16 correlate to manufacturing part number MT41K256M32.

Features

- Uses two 4Gb Micron die
- Single rank with dual ZQ balls - combines two 4Gb x16 devices in one package
- $V_{DD} = V_{DDQ}$ = 1.35V (1.283–1.425V); backward compatible to 1.5V operation
- 1.35V center-terminated push/pull I/O
- JEDEC-standard ball-out
- Low-profile package
- T_C of 0°C to 95°C
  - 0°C to 85°C: 8192 refresh cycles in 64ms
  - 85°C to 95°C: 8192 refresh cycles in 32ms
- Temperature-compensated self refresh (TCSR)
- Very low current self refresh mode when T_C < 45°C

Options	Marking
• Configuration	
– 32 Meg x 32 x 8 banks	256M32
• FBGA package (Pb-free)	
– 136-ball FBGA (10mm x 14mm x 1.2mm) Rev. E	SLD
• Timing – cycle time[1]	
– 1.25ns @ CL = 11 (DDR3L-1600)	-125
– 1.5ns @ CL = 9 (DDR3L-1333)	-15E
– 1.87ns @ CL = 7 (DDR3L-1066)	-187E
• Power Saving	
– TCSR	M
• Operating temperature	
– Commercial (0°C ≤ T_C ≤ 95°C)	None
• Revision	:E

Note: 1. CL = CAS (READ) latency.

Table 1: Key Timing Parameters

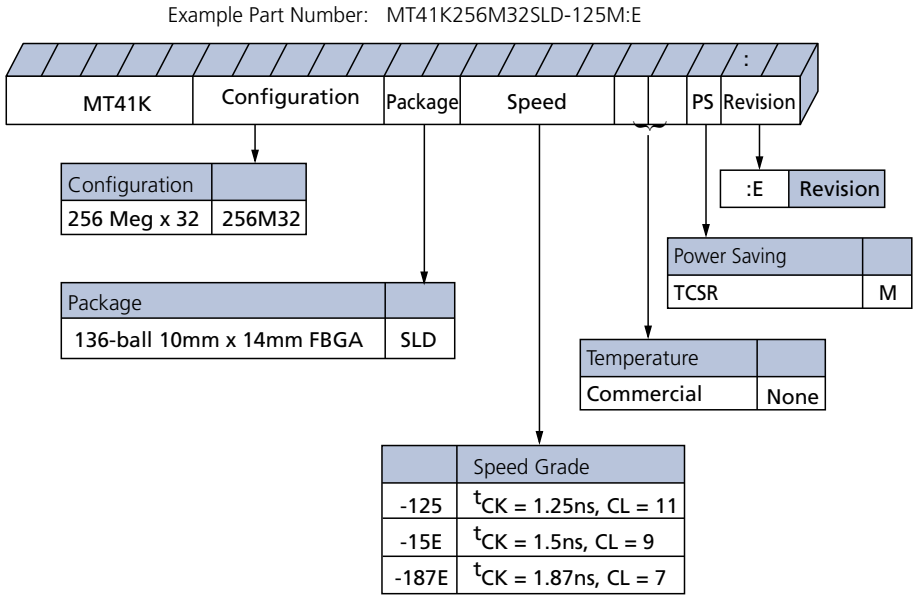
Speed Grade	Data Rate (MT/s)	Target ^{t}RCD-^{t}RP-CL	^{t}RCD (ns)	^{t}RP (ns)	CL (ns)
-125[1, 2]	1600	11-11-11	13.75	13.75	13.75
-15E[1]	1333	9-9-9	13.5	13.5	13.5
-187E	1066	7-7-7	13.1	13.1	13.1

Notes: 1. Backward compatible to 1066, CL = 7 (-187E).
2. Backward compatible to 1333, CL = 9 (-15E).

Table 2: Addressing

Parameter	256 Meg x 32
Configuration	32 Meg x 32 x 8 banks
Refresh count	8K
Row address	32K A[14:0]
Bank address	8 BA[2:0]
Column address	1K A[9:0]
Page size	2KB

Figure 1: 8Gb: x32 DDR3L-RS Part Numbers



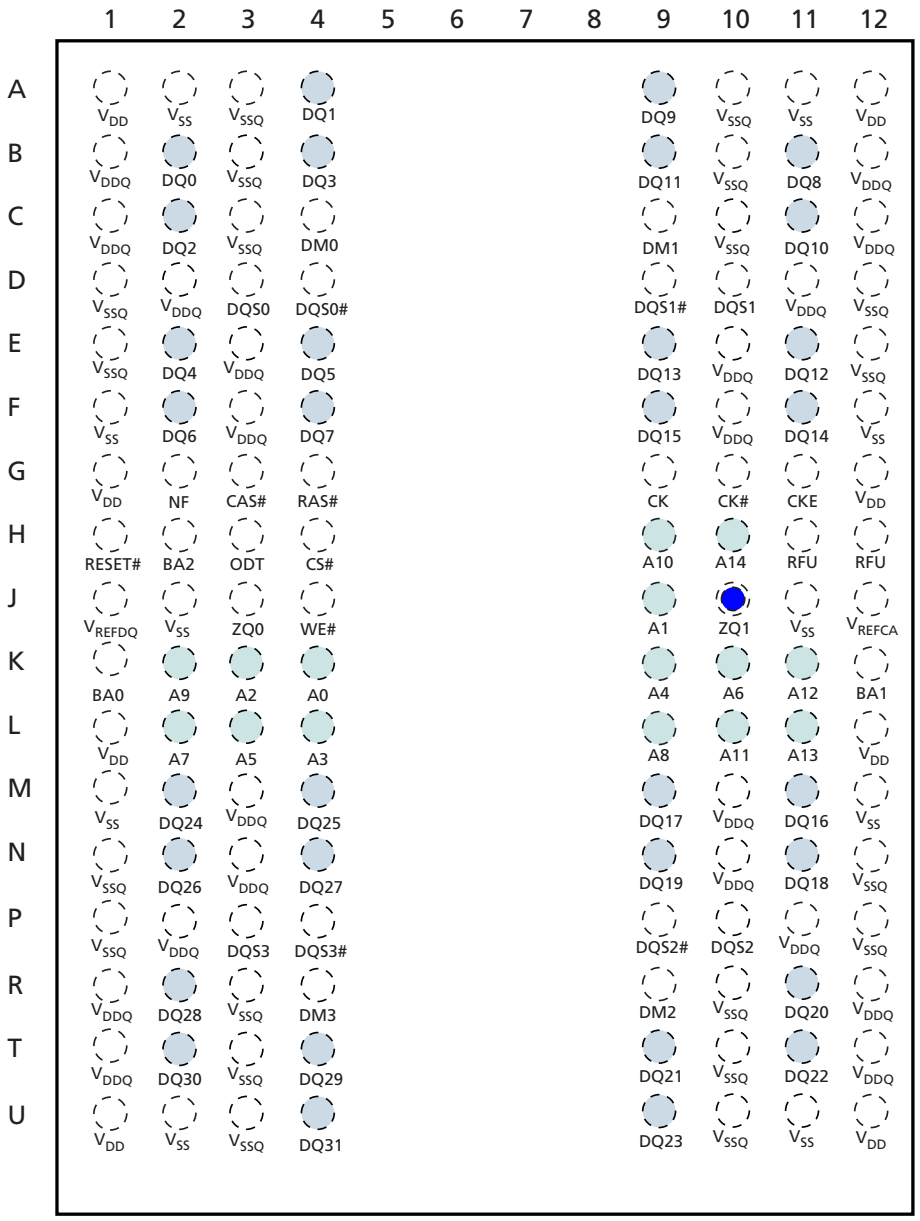
Note: 1. Not all options listed can be combined to define an offered product. Use the part catalog search on http://www.micron.com for available offerings.

FBGA Part Marking Decoder

Due to space limitations, FBGA-packaged components have an abbreviated part marking that is different from the part number. Micron's FBGA part marking decoder is available at www.micron.com/decoder.

Ball Assignments and Descriptions

Figure 2: 136-Ball FBGA Ball Assignments (Top View)



Note: 1. ZQ1 (dark ball) designates the ball that differs from the monolithic version.

Table 3: FBGA 136-Ball Descriptions

Symbol	Type	Description
A14, A13, A12/BC#, A11, A10/AP, A[9:0]	Input	**Address inputs:** Provide the row address for ACTIVATE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BA[2:0]) or all banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE command. Address inputs are referenced to V_{REFCA}. A12/BC#: When enabled in the mode register (MR), A12 is sampled during READ and WRITE commands to determine whether burst chop (on-the-fly) will be performed (HIGH = burst length (BL) of 8 or no burst chop, LOW = burst chop (BC) of 4, burst chop).
BA[2:0]	Input	**Bank address inputs:** BA[2:0] define the bank to which an ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. BA[2:0] define which mode register (MR0, MR1, MR2, or MR3) is loaded during the LOAD MODE command. BA[2:0] are referenced to V_{REFCA}.
CK, CK#	Input	**Clock:** CK and CK# are differential clock inputs. All command, address, and control input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#. Output data strobe (DQS, DQS#) is referenced to the crossings of CK and CK#.
CKE	Input	**Clock enable:** CKE enables (registered HIGH) and disables (registered LOW) internal circuitry and clocks on the DRAM. The specific circuitry that is enabled/disabled is dependent upon the DDR3L SDRAM configuration and operating mode. Taking CKE LOW provides PRECHARGE power-down and SELF REFRESH operations (all banks idle) or active power-down (row active in any bank). CKE is synchronous for power-down entry and exit and for self refresh entry. CKE is asynchronous for self refresh exit. Input buffers (excluding CK, CK#, CKE, RESET#, and ODT) are disabled during power-down. Input buffers (excluding CKE and RESET#) are disabled during SELF REFRESH. CKE is referenced to V_{REFCA}.
CS#	Input	**Chip select:** CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# provides for external rank selection on systems with multiple ranks. CS0# is considered part of the command code.
DM[3:0]	Input	**Input data mask:** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH, along with the input data, during a write access. Although the DM ball is input-only, the DM loading is designed to match that of the DQ and DQS balls. DM is referenced to V_{REFDQ}. There is one DM per byte.
ODT	Input	**On-die termination:** ODT enables (registered HIGH) and disables (registered LOW) termination resistance internal to the DDR3 SDRAM. When enabled in normal operation, ODT is only applied to DQ[31:0], DQS[3:0], DQS#[3:0], and DM[3:0]. The ODT input is ignored if disabled via the LOAD MODE command. ODT is referenced to V_{REFCA}.
RAS#, CAS#, WE#	Input	**Command inputs:** RAS#, CAS#, and WE# (along with CS#) define the command being entered and are referenced to V_{REFCA}.
RESET#	Input	**Reset:** RESET# is an active LOW CMOS input referenced to V_{SS}. The RESET# input receiver is a CMOS input defined as a rail-to-rail signal with DC HIGH ≥ 0.8 × V_{DDQ} and DC LOW ≤ 0.2 × V_{DDQ}. RESET# assertion and desertion are asynchronous.
DQ[31:0]	I/O	**Data input/output:** Bidirectional data bus. DQ[31:0] are referenced to V_{REFDQ}.
DQS[3:0], DQS#[3:0]	I/O	**Data strobe:** DQS and DQS# pairs are differential data strobes; there is one DQS and DQS# pair per byte. The DQS strobes output with read data; edge aligned with read data; input with write data; center-aligned with write data.

Table 3: FBGA 136-Ball Descriptions (Continued)

Symbol	Type	Description
V_{DD}	Supply	**Power supply:** 1.35V (1.283–1.45V operational)
V_{DDQ}	Supply	**DQ power supply:** 1.35V (1.283–1.45V operational)
V_{REFCA}	Supply	**Reference voltage for control, command, and address:** V_{REFCA} must be maintained at all times (including self refresh) for proper device operation.
V_{REFDQ}	Supply	**Reference voltage for data:** V_{REFDQ} must be maintained at all times (including self refresh) for proper device operation.
V_{SS}	Supply	Ground.
V_{SSQ}	Supply	**DQ ground:** Isolated on the device for improved noise immunity.
ZQ[1:0]	Reference	**External reference ball for output drive calibration:** Each ball is tied to its own external 240Ω resistor (RZQ), which is tied to V_{SSQ}. Each resistor is connected to a seperate x16 die.
NC	–	**No connect:** These balls should be left unconnected (the ball has no connection to the DRAM or to other balls).
NF	–	**No function:** These balls should be left unconnected (the ball may have connection to the DRAM or to other balls).

Functional Description

The TwinDie DDR3L SDRAM is a high-speed, CMOS dynamic random access memory device internally configured as two 8-bank DDR3L SDRAM devices.

Although each die is tested individually within the dual-die package, some TwinDie test results may vary from a like-die tested within a monolithic die package.

The DDR3L SDRAM uses a double data rate architecture to achieve high-speed operation. The double data rate architecture is an 8*n*-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O balls. A single read or write access consists of a single 8*n*-bit-wide, one-clock-cycle data transfer at the internal DRAM core and eight corresponding *n*-bit-wide, one-half-clock-cycle data transfers at the I/O balls.

The differential data strobe (DQS, DQS#) is transmitted externally, along with data, for use in data capture at the DDR3L SDRAM input receiver. DQS is center-aligned with data for WRITEs. The read data is transmitted by the DDR3L SDRAM and edge-aligned to the data strobes.

Read and write accesses to the DDR3L SDRAM are burst oriented. Accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVATE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVATE command are used to select the bank and row to be accessed. The address bits (including CS*n*#, BA*n*, and A*n*) registered coincident with the READ or WRITE command are used to select the rank, bank, and starting column location for the burst access.

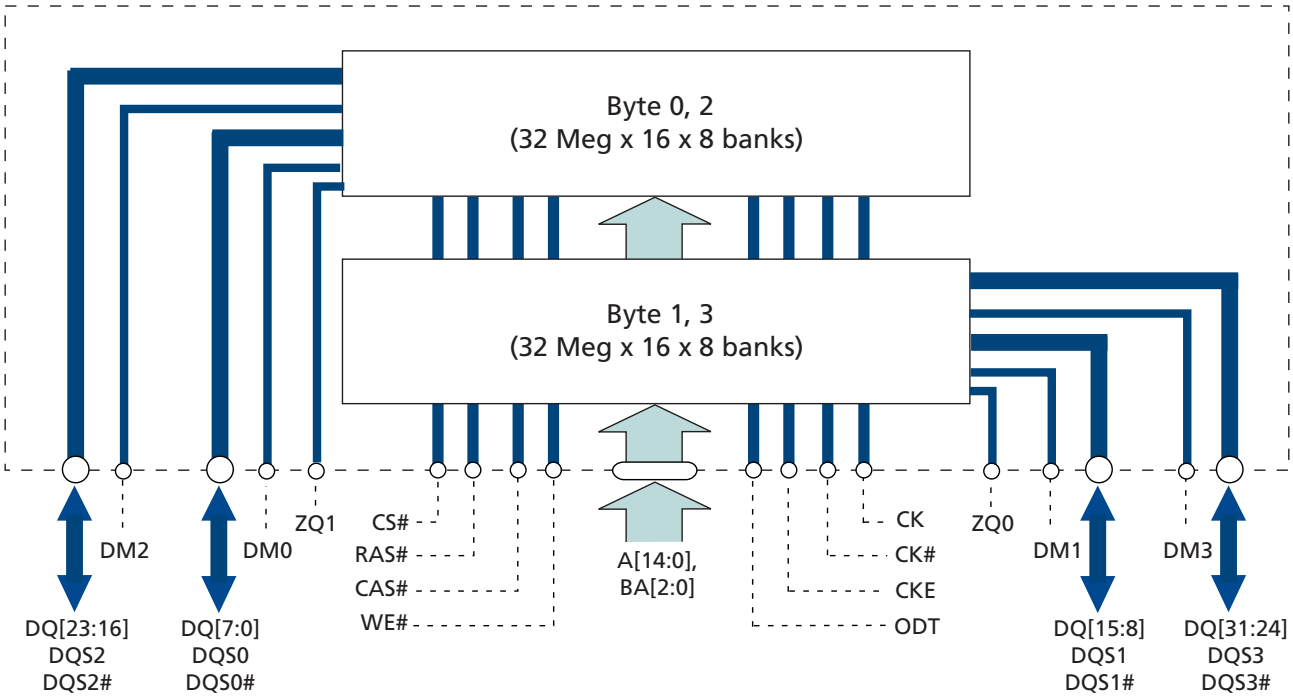
This data sheet provides a general description, package dimensions, and the package ballout. Refer to the Micron monolithic DDR3L data sheet for complete information regarding individual die initialization, register definition, command descriptions, and die operation.

Industrial Temperature

The industrial temperature (IT) option, if offered, requires that the case temperature not exceed –40°C or 95°C. JEDEC specifications require the refresh rate to double when T_C exceeds 85°C; this also requires use of the high-temperature self refresh option. Additionally, ODT resistance, I_{DD} values, some IDD specifications and the input/output impedance must be derated when T_C is < 0°C or > 95°C. See the DDR3 monolithic data sheet for details.

Functional Block Diagram

Figure 3: Functional Block Diagram (32 Meg x 32 x 8 Banks)



Electrical Specifications

Absolute Rating

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions outside those indicated in the device data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may adversely affect reliability.

Table 4: Absolute Maximum DC Ratings

Parameter	Symbol	Min	Max	Units	Notes
V_{DD} supply voltage relative to V_{SS}	V_{DD}	–0.4	1.975	V	1
V_{DD} supply voltage relative to V_{SSQ}	V_{DDQ}	–0.4	1.975	V	
Voltage on any ball relative to V_{SS}	V_{IN}, V_{OUT}	–0.4	1.975	V	
Input leakage current Any input 0V ≤ V_{IN} ≤ V_{DD}, V_{REF} pin 0V ≤ V_{IN} ≤ 1.1V (All other pins not under test = 0V)	I_I	–4	4	µA	
V_{REF} supply leakage current V_{REFDQ} = V_{DD}/2 or V_{REFCA} = V_{DD}/2 (All other pins not under test = 0V)	I_{VREF}	–2	2	µA	2
Operating case temperature	T_C	0	95	°C	3, 4
Storage temperature	T_{STG}	–55	150	°C	

Notes:
1. V_{DD} and V_{DDQ} must be within 300mV of each other at all times, and V_{REF} must not be greater than 0.6 × V_{DDQ}. When V_{DD} and V_{DDQ} are less than 500mV, V_{REF} may be ≤300mV.
2. The minimum limit requirement is for testing purposes. The leakage current on the V_{REF} pin should be minimal.
3. MAX operating case temperature. T_C is measured in the center of the package (see figure: Temperature Test Point Location).
4. Device functionality is not guaranteed if the DRAM device exceeds the maximum T_C during operation.

Input/Output Capacitance

The lump capacitance values are not listed. Simulations should use actual models and not lumped capacitance.

Temperature and Thermal Impedance

It is imperative that the DDR3L-RS SDRAM device's temperature specifications, shown in the following table, be maintained in order to ensure the junction temperature is in the proper operating range to meet data sheet specifications. An important step in maintaining the proper junction temperature is using the device's thermal impedances correctly. Thermal impedances listed in the Thermal Characteristics table apply to the current die revision and packages.

Incorrectly using thermal impedances can produce significant errors. Read Micron technical note TN-00-08, "Thermal Applications," prior to using the values listed in the thermal impedance table. For designs that are expected to last several years and require the flexibility to use several DRAM die shrinks, consider using final target theta values (rather than existing values) to account for increased thermal impedances from the die size reduction.

The DDR3 SDRAM device's safe junction temperature range can be maintained when the T_C specification is not exceeded. In applications where the device's ambient temperature is too high, use of forced air and/or heat sinks may be required to satisfy the case temperature specifications.

Table 5: Thermal Characteristics

Notes 1–3 apply to entire table

Parameter	Symbol	Value	Units	Notes
Operating temperature	T_C	0 to 85	°C	
		0 to 95	°C	4

Notes:
1. MAX operating case temperature T_C is measured in the center of the package, as shown below.
2. A thermal solution must be designed to ensure that the device does not exceed the maximum T_C during operation.
3. Device functionality is not guaranteed if the device exceeds maximum T_C during operation.
4. If T_C exceeds 85°C, the DRAM must be refreshed externally at 2x refresh, which is a 3.9µs interval refresh rate. The use of self refresh temperature (SRT) or automatic self refresh (ASR), if available, must be enabled.

Figure 4: Temperature Test Point Location

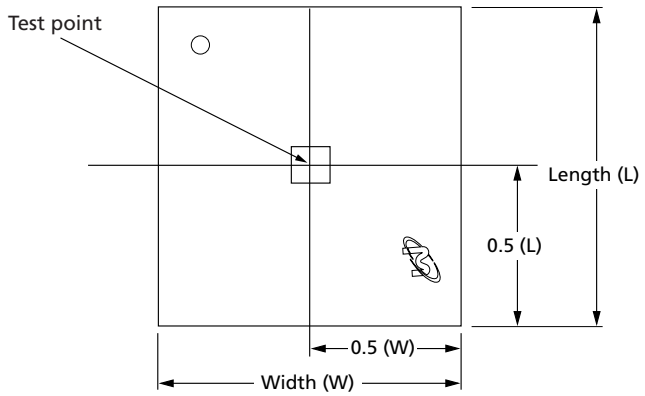


Table 6: Thermal Impedance

Die Rev	Package	Substrate	ΘJA (°C/W) Airflow = 0m/s	ΘJA (°C/W) Airflow = 1m/s	ΘJA (°C/W) Airflow = 2m/s	ΘJB (°C/W)	ΘJC (°C/W)	Notes
E	136-ball	2-layer	TBD	TBD	TBD	TBD	TBD	1
		4-layer	TBD	TBD	TBD	TBD		

Note: 1. Thermal resistance data is based on a number of samples from multiple lots and should be viewed as a typical number.

Timing Adjustments

The base data sheet timing specifications are generally applicable but some parameters will require some adjustments. The clock to strobe skews will require adjustments (see table below). V_{OX} will be offset.

Table 7: Timing Adjustments

Note 1 applies to the entire table

Parameter Skewed	Symbols	DDR3L -800 Typ	DDR3L -1066 Typ	DDR3L -1333 Typ	DDR3L -1600 Typ	Unit
Byte 1: CK, CK# to DQS1	^{t}DQSCK, ^{t}DQSS	–24	–24	–24	–24	ps
Byte 1: CK, CK# to DQS1#	^{t}DQSCK, ^{t}DQSS	–14.5	–14.5	–14.5	–14.5	ps
Byte 0: CK, CK# to DQS0	^{t}DQSCK, ^{t}DQSS	–23.5	–23.5	–23.5	–23.5	ps
Byte 0: CK, CK# to DQS0#	^{t}DQSCK, ^{t}DQSS	–12	–12	–12	–12	ps
Byte 2: CK, CK# to DQS2#	^{t}DQSCK, ^{t}DQSS	38.5	38.5	38.5	38.5	ps
Byte 2: CK, CK# to DQS3	^{t}DQSCK, ^{t}DQSS	44	44	44	44	ps
Byte 3: CK, CK# to DQS3#	^{t}DQSCK, ^{t}DQSS	41.5	41.5	41.5	41.5	ps
Byte 3: CK, CK# to DQS3	^{t}DQSCK, ^{t}DQSS	44	44	44	44	ps

Electrical Specifications – I_{CDD} Parameters

Table 8: DDR3L-RS$_{CDD}$ Specifications and Conditions (Rev. E)

Note 8 applies to the entire table

Combined Symbol	Individual Die Status	Bus Width	-187E	-15E	-125	Units	Notes
I_{CDD0}	$I_{CDD0} = 2 \times I_{DD0}$	x32	110	117	131	mA	1
I_{CDD1}	$I_{CDD1} = 2 \times I_{DD1}$	x32	160	167	175	mA	1
I_{CDD2P0} (slow exit)	$I_{CDD2P0} = 2 \times I_{DD2P0}$	x32	24	24	24	mA	1
I_{CDD2P1} (fast exit)	$I_{CDD2P1} = 2 \times I_{DD2P1}$	x32	49	52	61	mA	1
I_{CDD2Q}	$I_{CDD2Q} = 2 \times I_{DD2Q}$	x32	44	48	54	mA	1
I_{CDD2N}	$I_{CDD2N} = 2 \times I_{DD2N}$	x32	44	47	53	mA	1
I_{CDD2NT}	$I_{CDD2NT} = 2 \times I_{DD2NT}$	x32	60	67	74	mA	1
I_{CDD3P}	$I_{CDD3P} = 2 \times I_{DD3P}$	x32	54	60	66	mA	1
I_{CDD3N}	$I_{CDD3N} = 2 \times I_{DD3N}$	x32	73	79	85	mA	1
I_{CDD4R}	$I_{CDD4R} = 2 \times I_{DD4R}$	x32	353	386	454	mA	1
I_{CDD4W}	$I_{CDD4W} = 2 \times I_{DD4W}$	x32	258	289	327	mA	1
I_{CDD5B}	$I_{CDD5B} = 2 \times I_{DD5B}$	x32	282	288	302	mA	1
Room temperature self refresh $_{CDD6}$	$I_{CDD6} = 2 \times I_{DD6}$	x32	7.0	7.0	7.0	mA	2
self refresh 45ºC	$I_{CDD6\ 45} = 2 \times I_{DD6\ 45}$	x32	7.4	7.4	7.4	mA	3
Elevated temperature self refresh I_{CDD6}	$I_{CDD6} = 2 \times I_{DD6}$	x32	14	14	14	mA	4
			17	17	17	mA	5
Extended temperature self refresh I_{CDD6ET}	$I_{CDD6ET} = 2 \times I_{DD6ET}$	x32	28	28	28	mA	6
			36	36	36	mA	7
I_{CDD7}	$I_{CDD7} = 2 \times I_{DD7}$	x32	388	426	479	mA	1
I_{CDD8}	$I_{CDD8} = 2 \times I_{DD8}$	x32	$I_{CDD2P0} + 4$	$I_{CDD2P0} + 4$	$I_{CDD2P0} + 4$	mA	1

Notes:
1. $T_C = 85°C$; SRT is disabled, ASR is disable. Value is maximum.
2. Room temperature; SRT is disabled, ASR is enabled. Value is typical.
3. $T_C \leq 45°C$; SRT is disabled, ASR is enabled). Value is typical.
4. $T_C = 80°C$; SRT is disabled, ASR is enabled). Value is typical.
5. $45°C < T_C \leq 80°C$; SRT is disabled, ASR is enabled. Value is maximum.
6. $T_C = 95°C$; SRT is disabled, ASR is enabled. Value is typical.
7. $85°C < T_C \leq 95°C$; SRT is disabled, ASR is enabled. Value is maximum.
8. I_{CDD} values reflect the combined current of both individual die. I_{DDx} represents individual die values.

Temperature-Compensated Self Refresh (TCSR)

The temperature-compensated self refresh (TCSR) feature substantially reduces the self refresh current (I_{DD6}). TCSR takes affect when T_C is less than 45°C and the auto self refresh (ASR) function is enabled. ASR is required to use the TCSR feature and is enabled manually via mode register 2 (MR2[6]). See Mode Register 2 (MR2) Definition below.

Enabling ASR also automatically changes the DRAM self refresh rate from 1x to 2x when the case temperature exceeds 85°C. This allows the user to operate the DRAM beyond the standard 85°C limit up to the optional extended temperature range of 95°C while in self refresh mode.

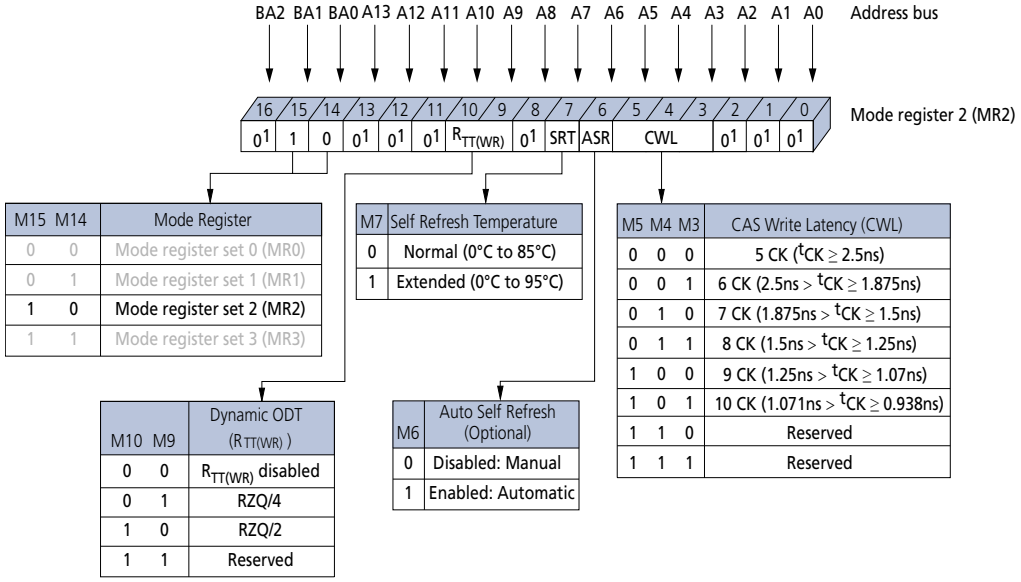
When ASR is disabled and T_C is 0°C to 85°C, the self refresh mode's refresh rate is assumed to be at the normal rate (sometimes referred to as 1x refresh rate). Also, if ASR is disabled and T_C is 85°C to 95°C, the user must select the SRT extended-temperature self refresh rate (sometimes referred to as 2x refresh rate). SRT is selected via mode register 2 (MR2[7]) register. See Mode Register 2 (MR2) Definition below.

SPD settings should always support 05h (101 binary) in Byte 31.

Mode Register 2 (MR2)

Mode register 2 (MR2) controls additional functions and features not available in the other mode registers. The auto self refresh (ASR) function is of particular interest for the DDR3L-RS SDRAM because the Micron DDR3L-RS SDRAM goes into TCSR mode when ASR has been enabled. This function is controlled via the bits shown in the figure below.

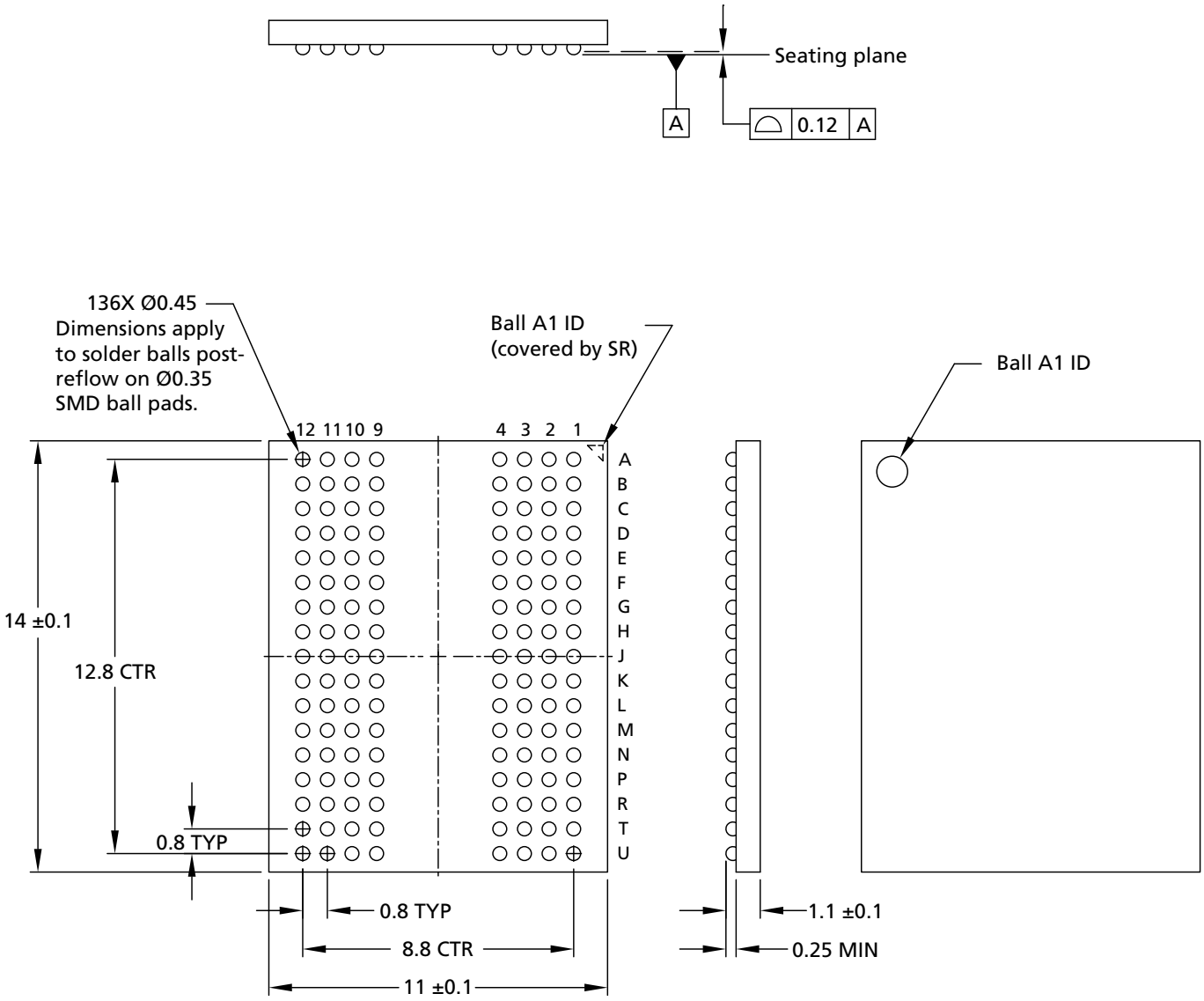
Figure 5: Mode Register 2 (MR2) Definition



Note: 1. MR2[17, 14:11, 8, and 2:0] are reserved for future use and must all be programmed to 0.

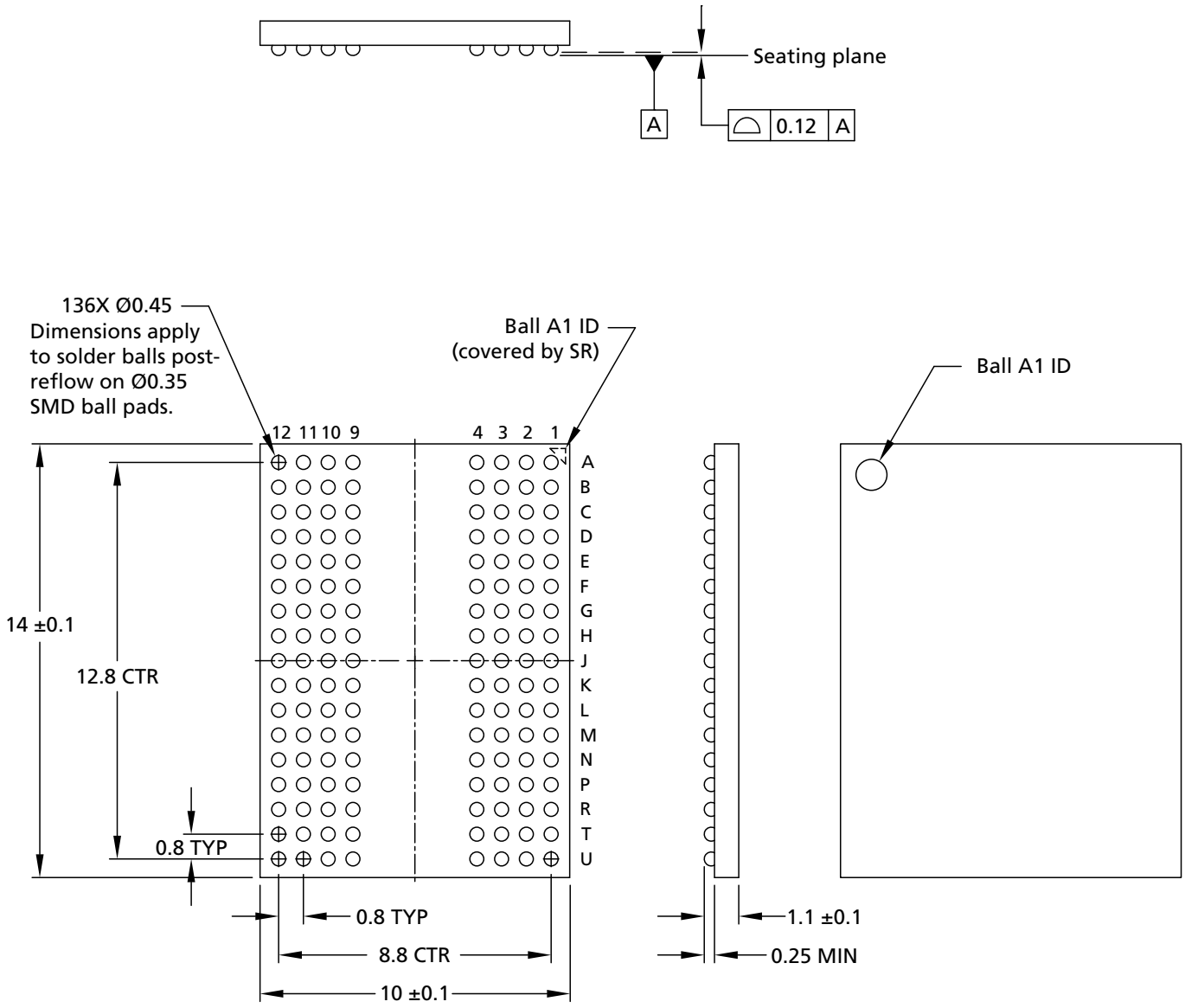
Package Dimensions

Figure 6: 136-Ball FBGA Die Rev. D (Package Code SGB)



Notes:
1. All dimensions are in millimeters.
2. Solder ball material: SAC305 (96.5% Sn, 3% Ag, 0.5% Cu).

Figure 7: 136-Ball FBGA Die Rev. E (Package Code SLD)



Notes:
1. All dimensions are in millimeters.
2. Solder ball material: SAC305 (96.5% Sn, 3% Ag, 0.5% Cu).