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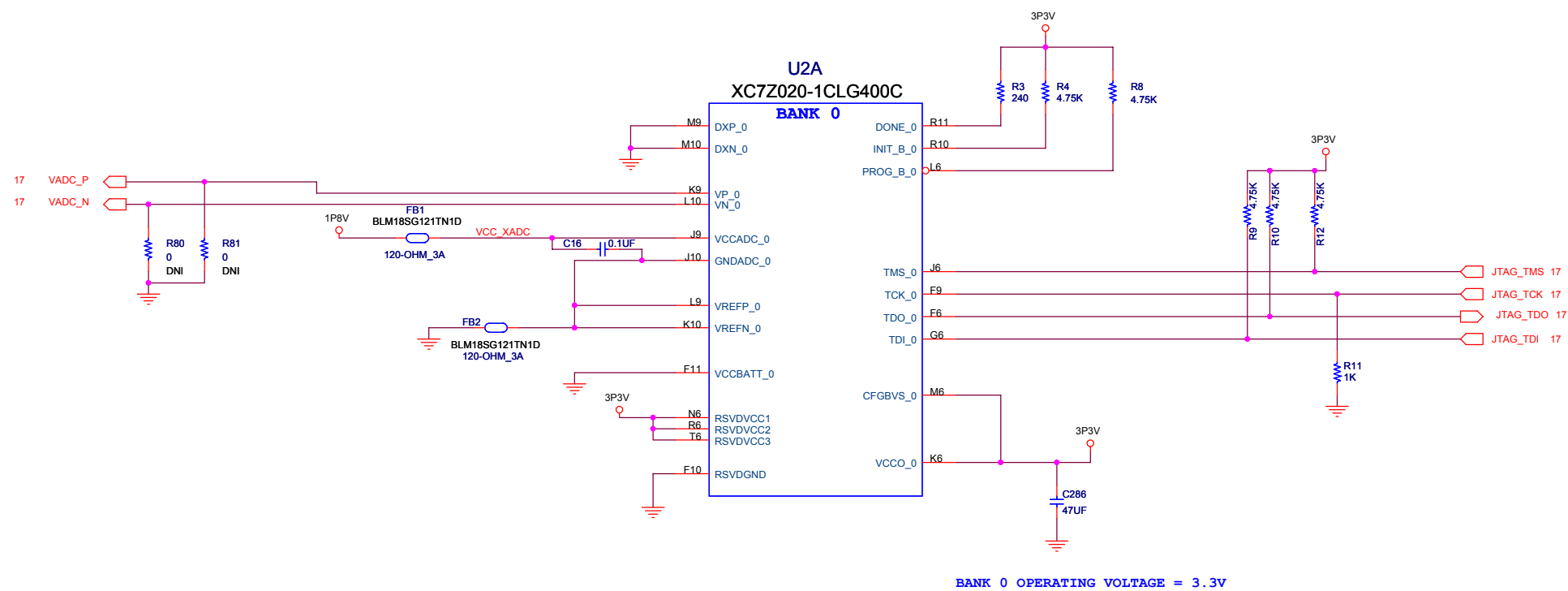
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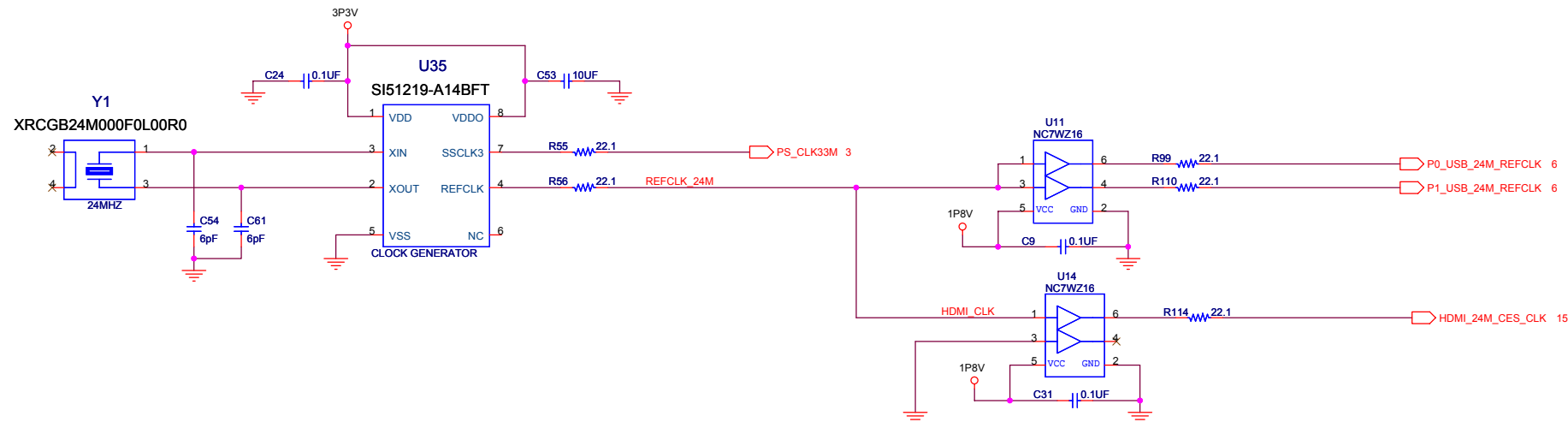
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ZYNQ BANK0



PROGRAMMABLE CLOCK GENERATOR

Place Close to U2

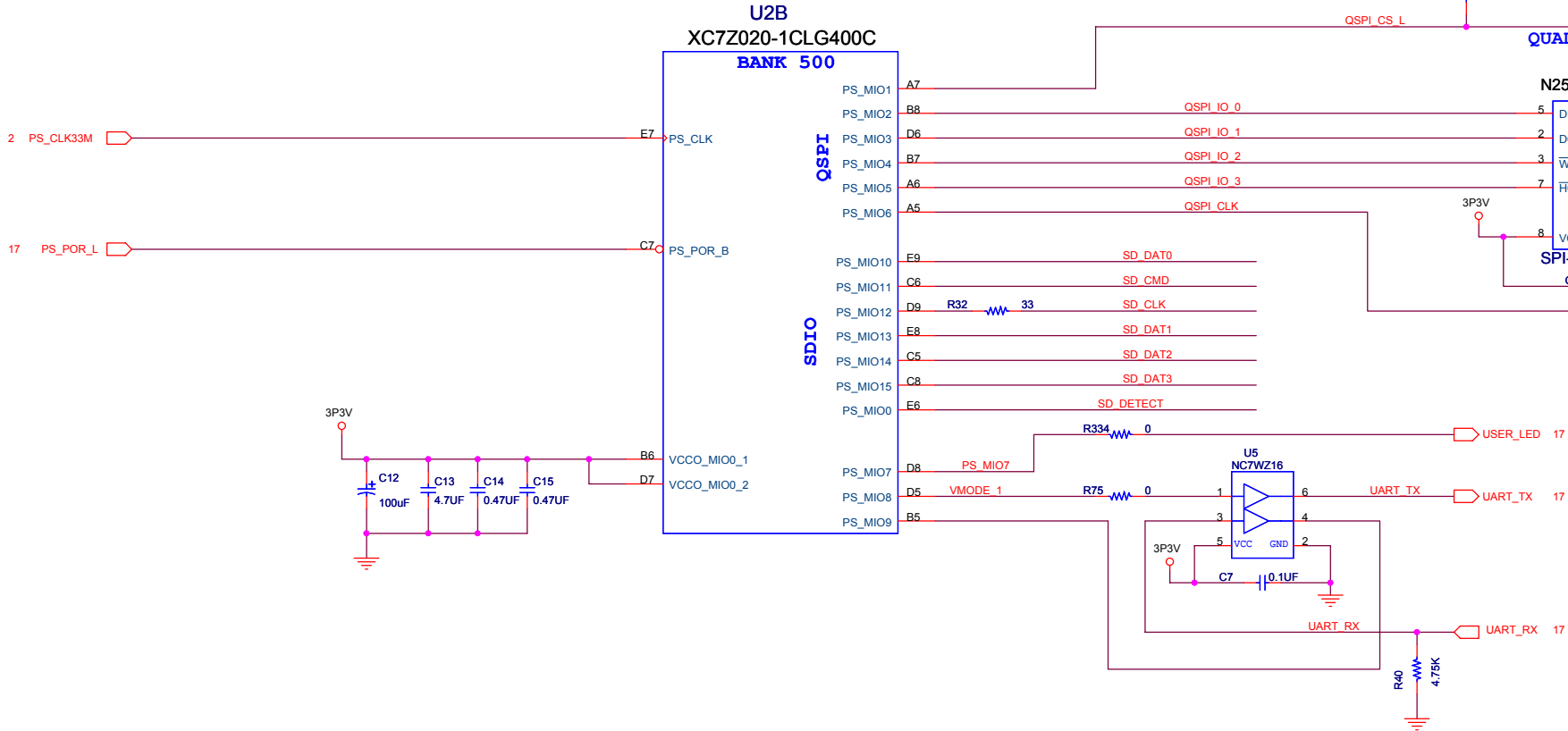


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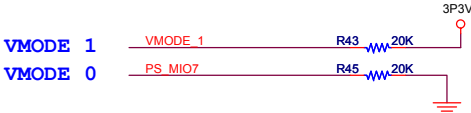
ZYNQ BANK 500



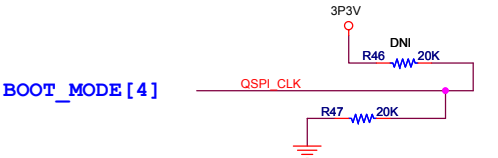
ZYNQ CONFIG MODE SELECT

Layout Note:

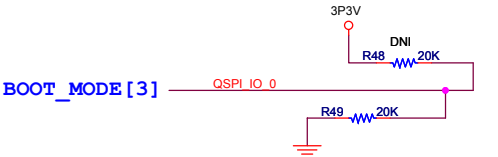
Limit the Stub length to less than 10mm



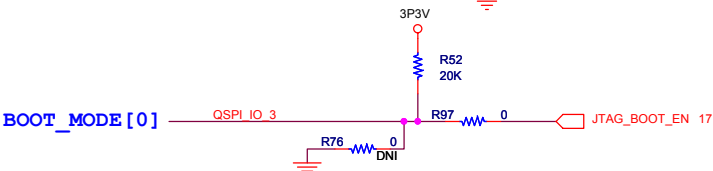
```
VMODE 1 = 0 -----> MIO Bank 1 Voltage = 1.8V
VMODE 0 = 0 -----> MIO Bank 0 Voltage = 3.3V
```



```
BOOT_MODE4 = 1 -----> PLL Bypassed
BOOT_MODE4 = 0 -----> PLL Used
```

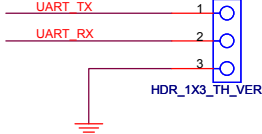


```
BOOT_MODE3 = 1 -----> Independant JTAG
BOOT_MODE3 = 0 -----> Cascaded JTAG
```



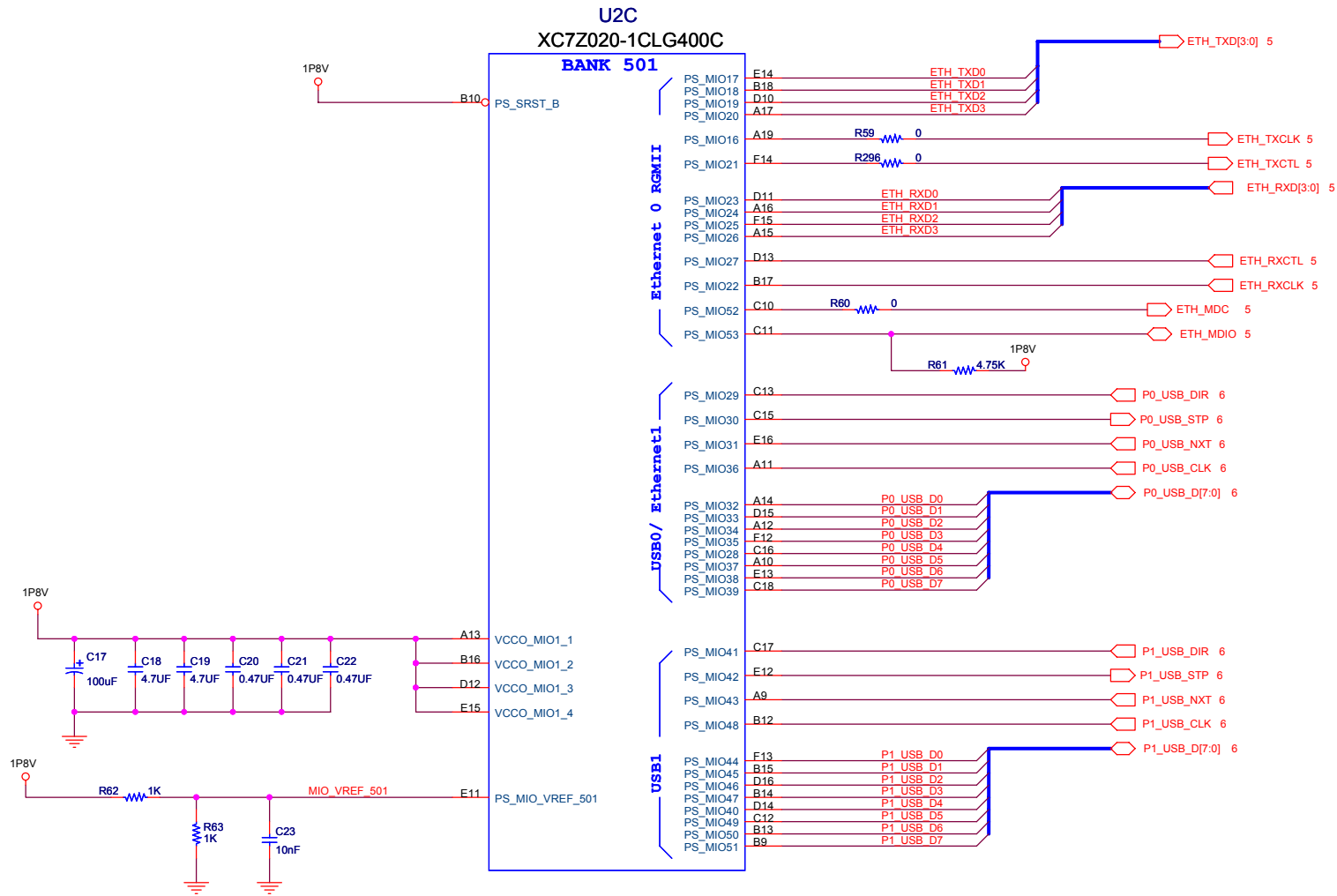
J2

PBC36SAAN



BOOT_MODE[0]	BOOT_MODE[1]	BOOT_MODE[2]	BOOT_MODE[3]	
0	0	0	0	Boot from JTAG
1	0	0	x	Boot from QSPI

ZYNQ BANK 501



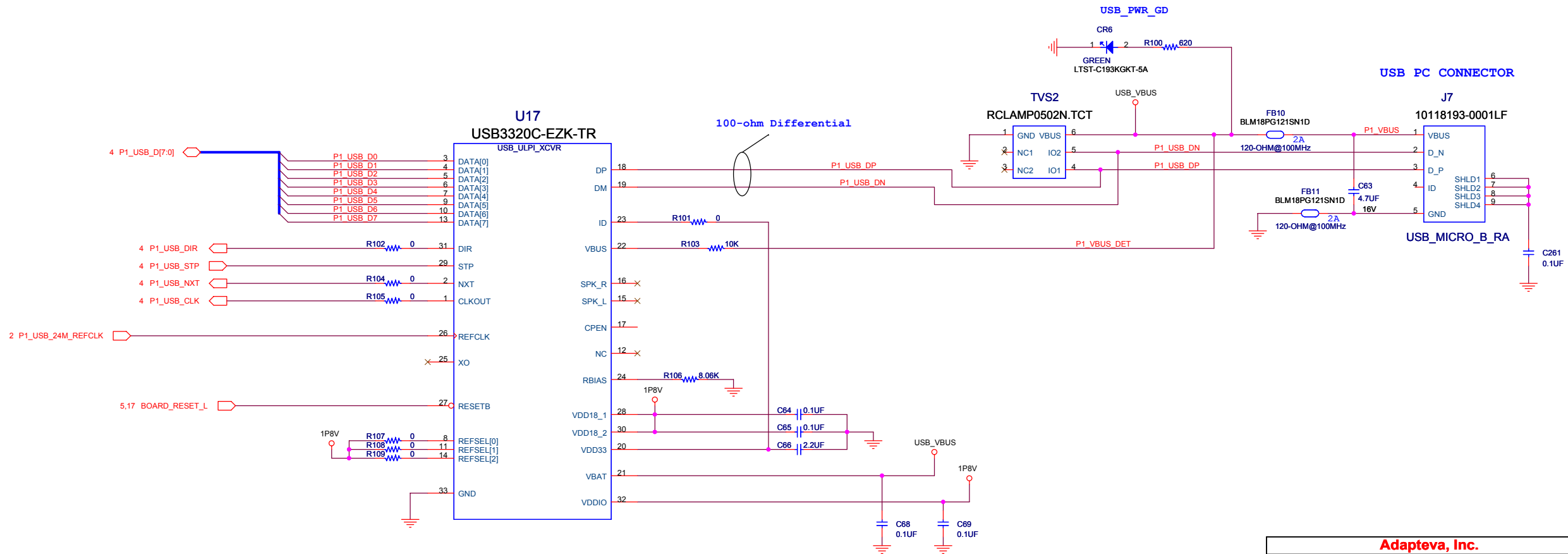
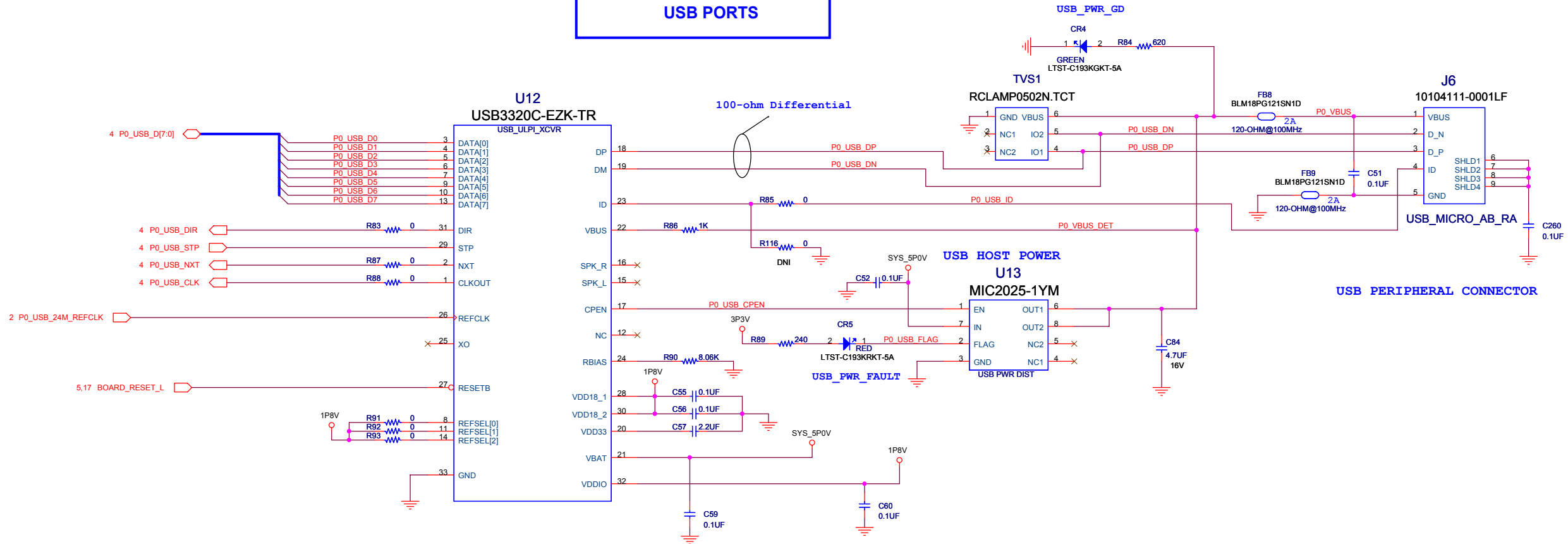
1.8V Interface IO

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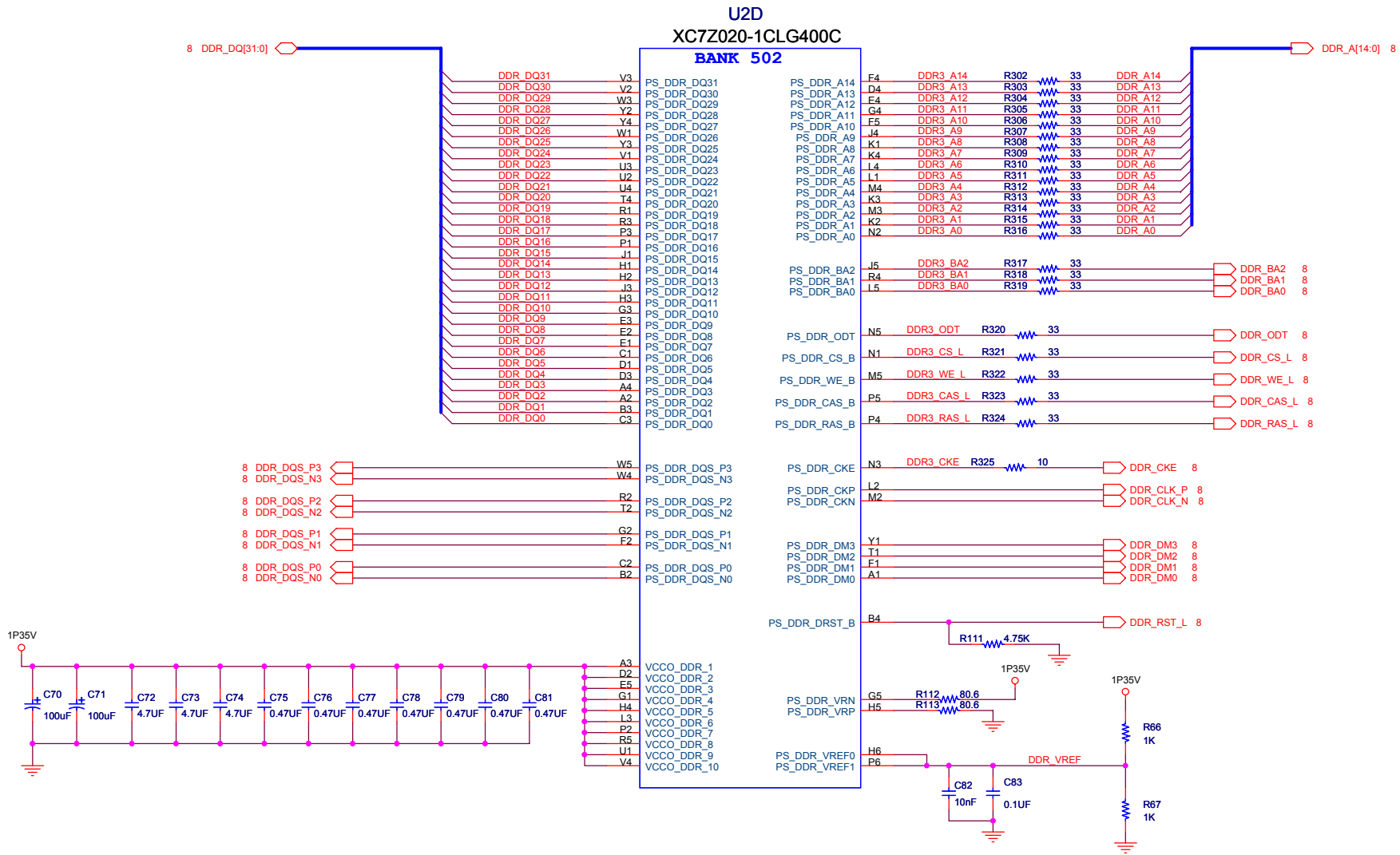
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USB PORTS



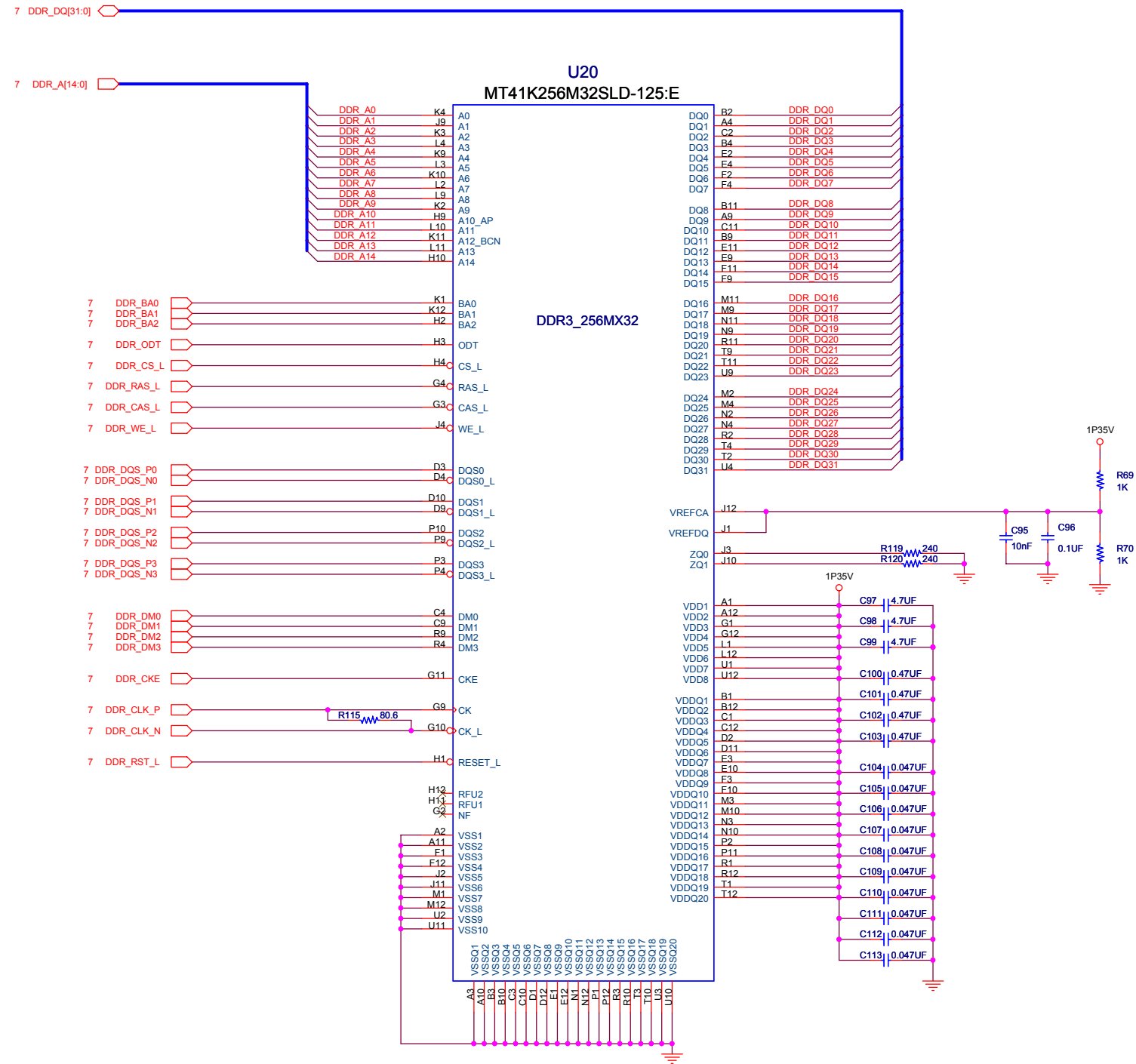
ZYNQ BANK 502



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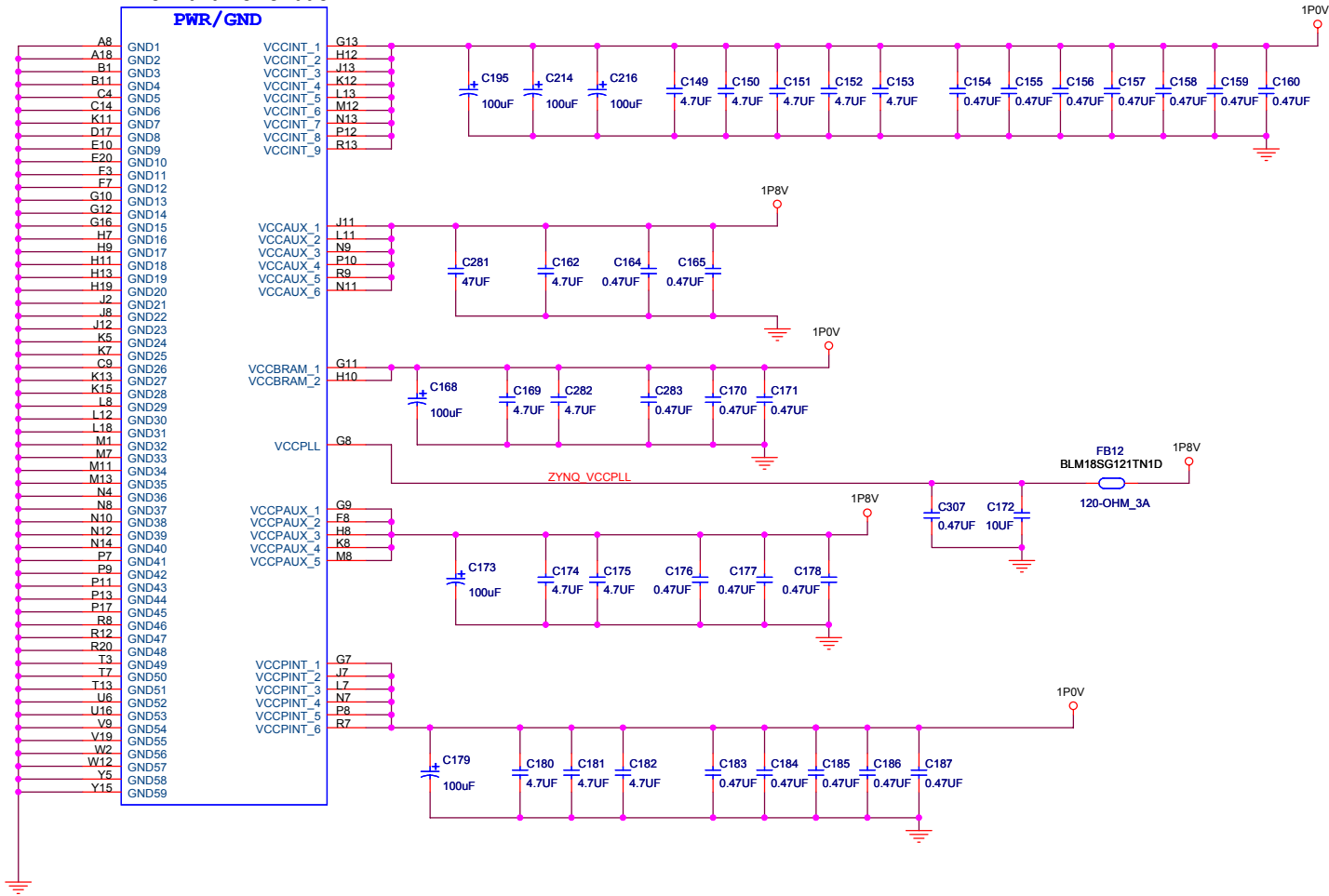
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DDR3 - 256M X 32

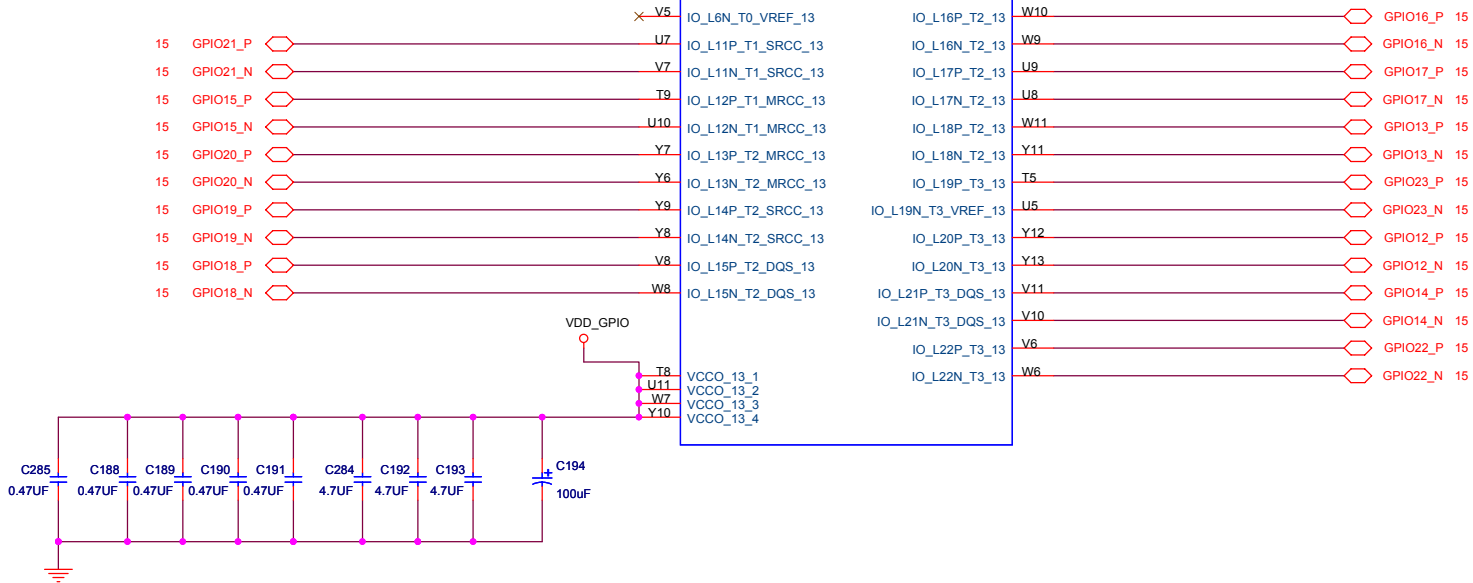


ZYNQ POWER & GROUND

U2H
XC7Z020-1CLG400C
PWR/GND



U2E
XC7Z020-1CLG400C
BANK 13

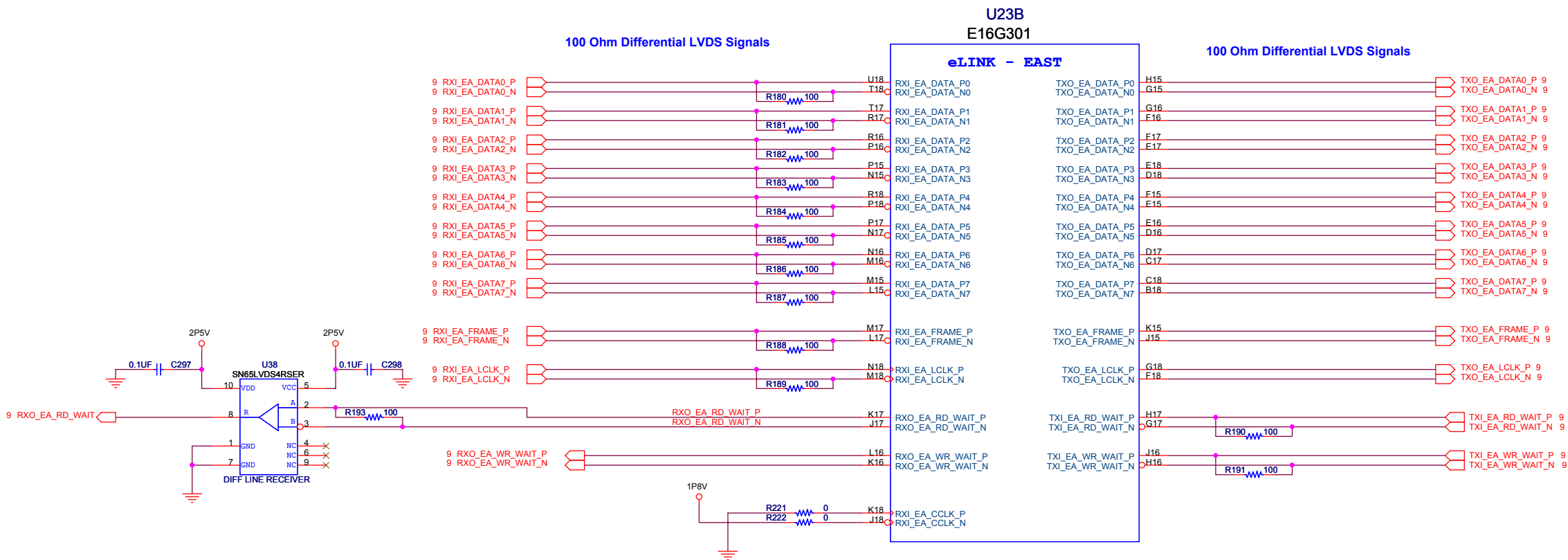
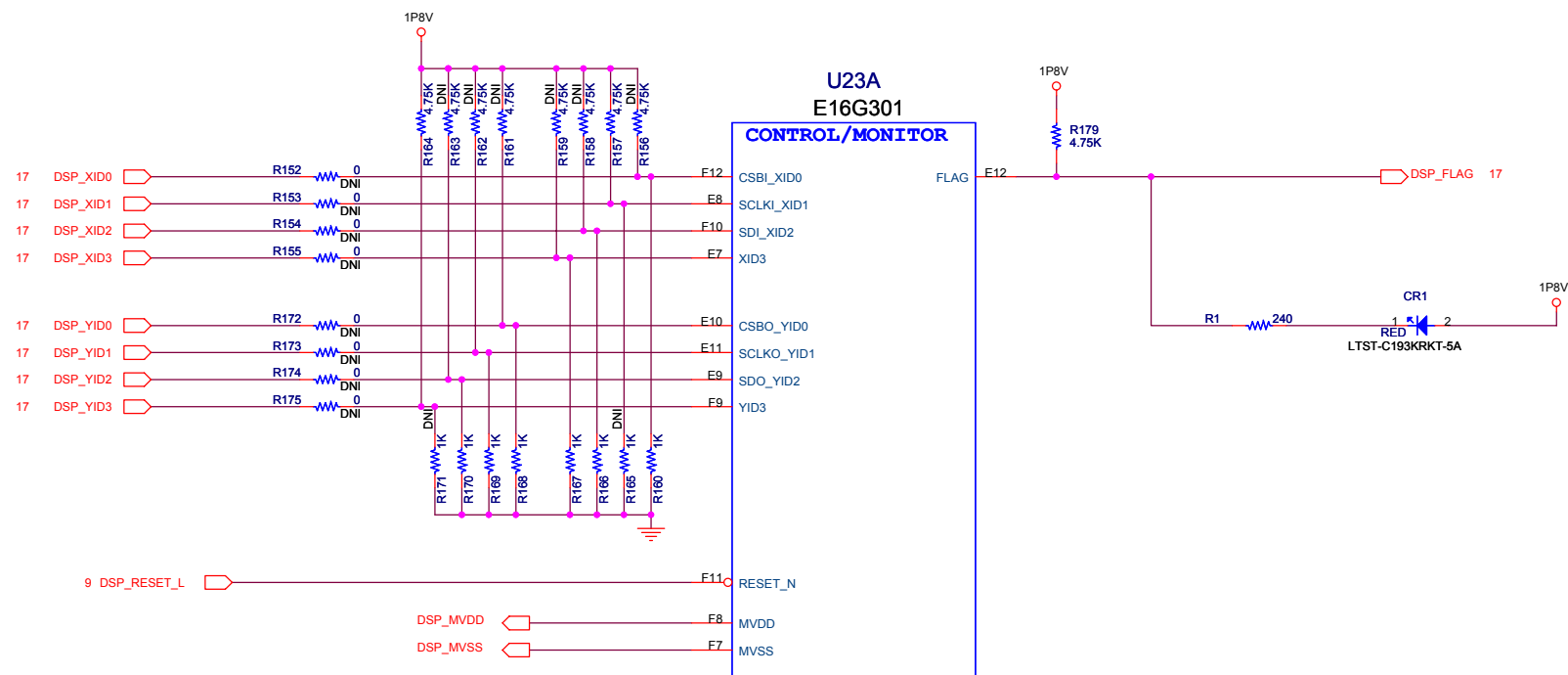


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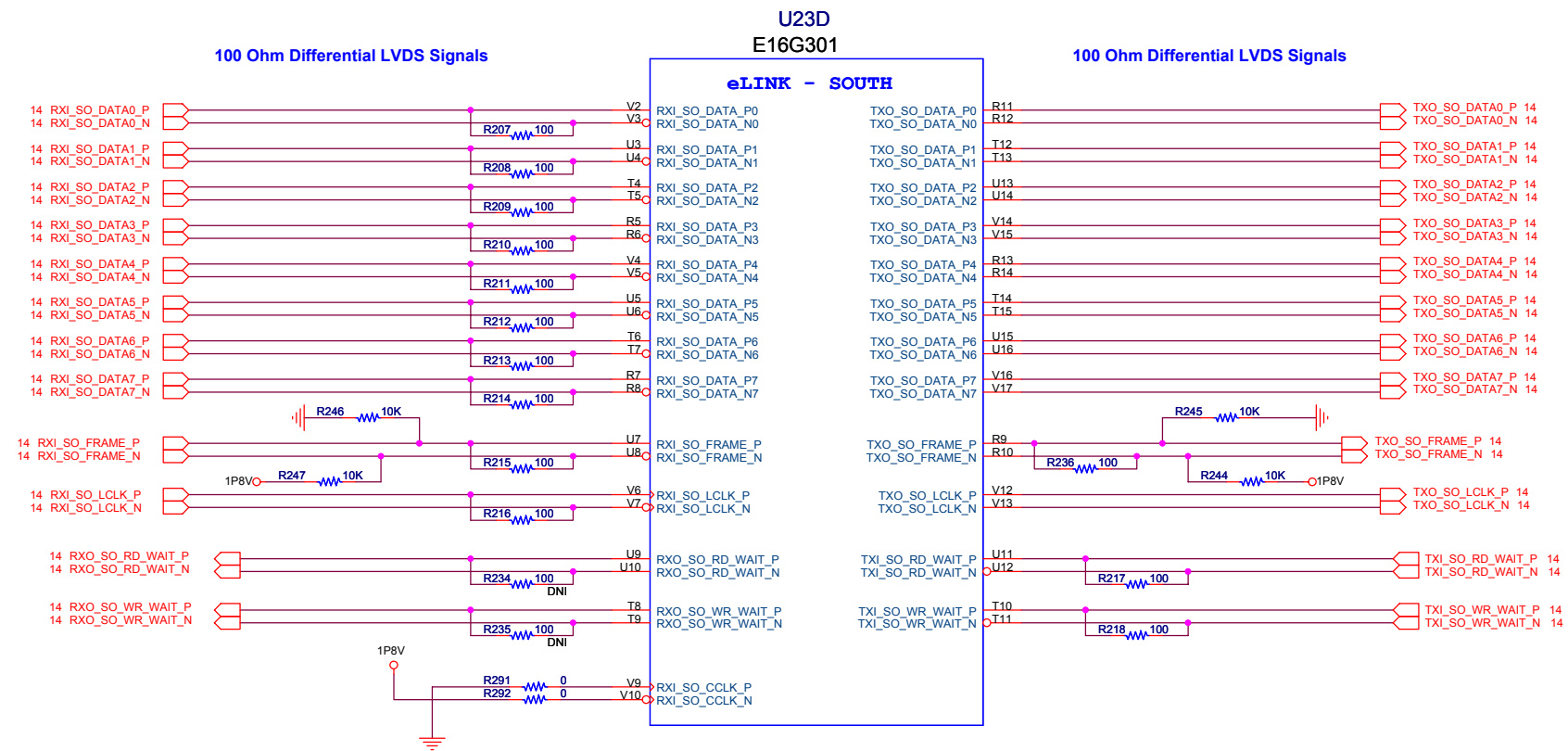
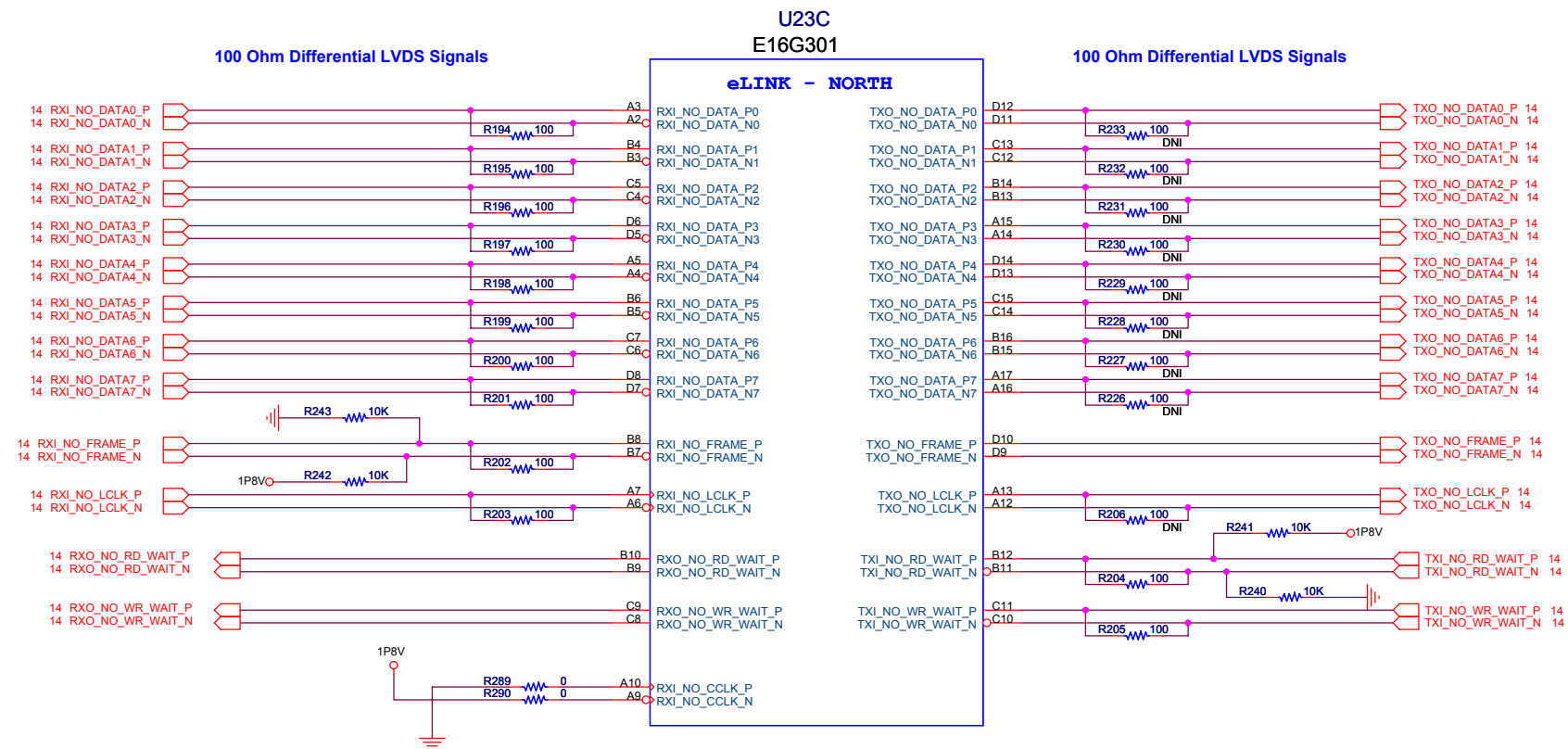
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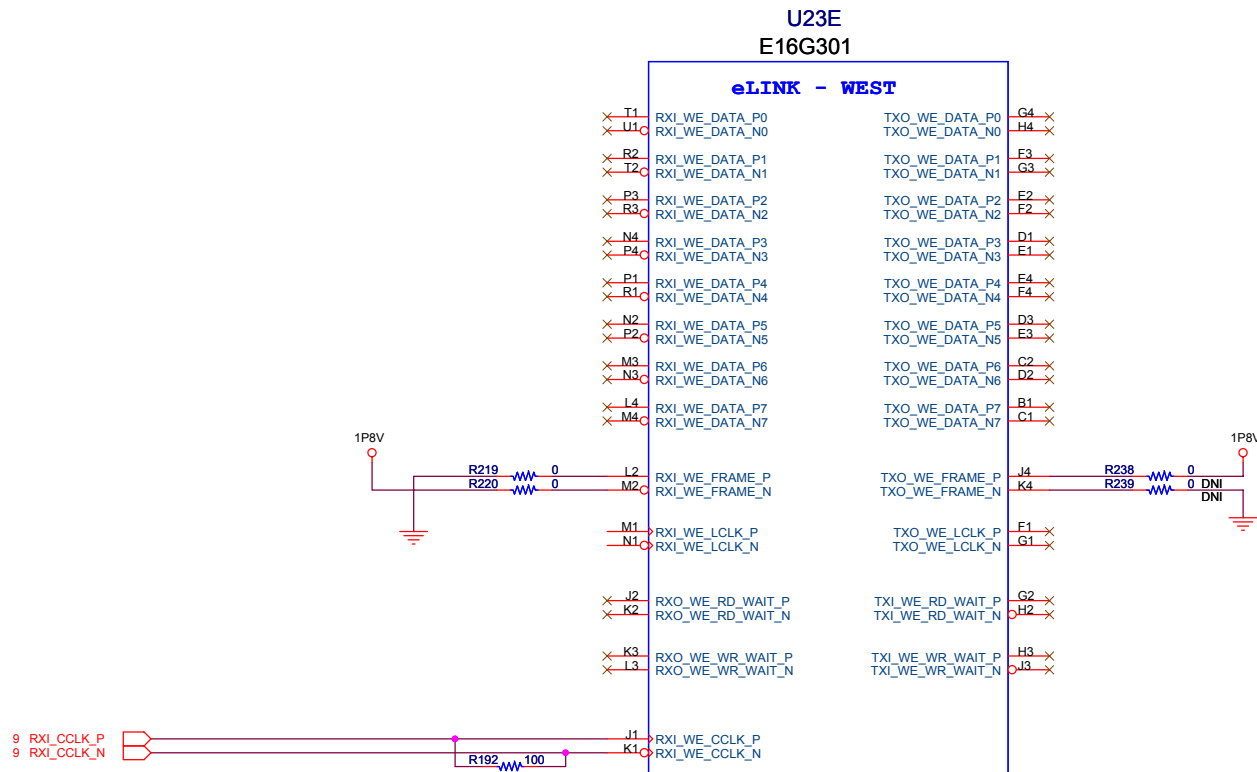
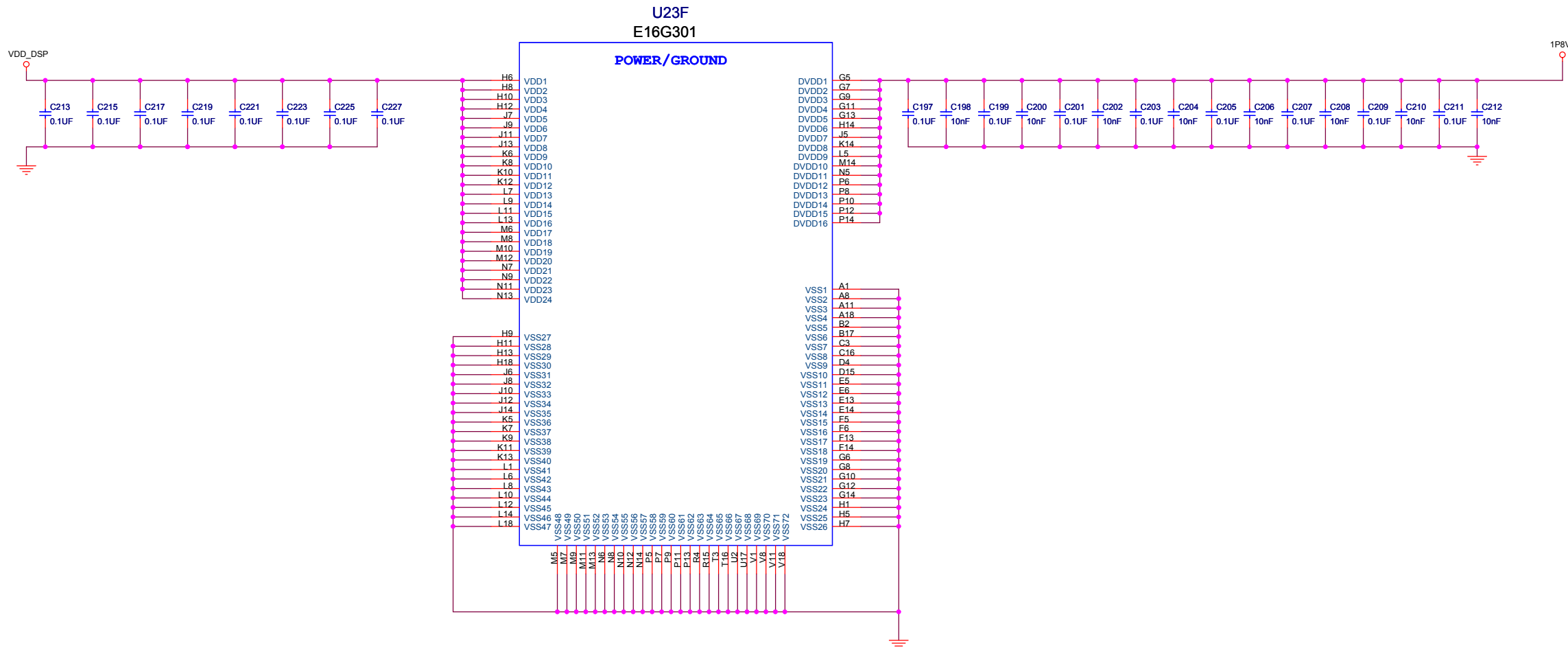
DSP PROCESSOR 1-OF-3



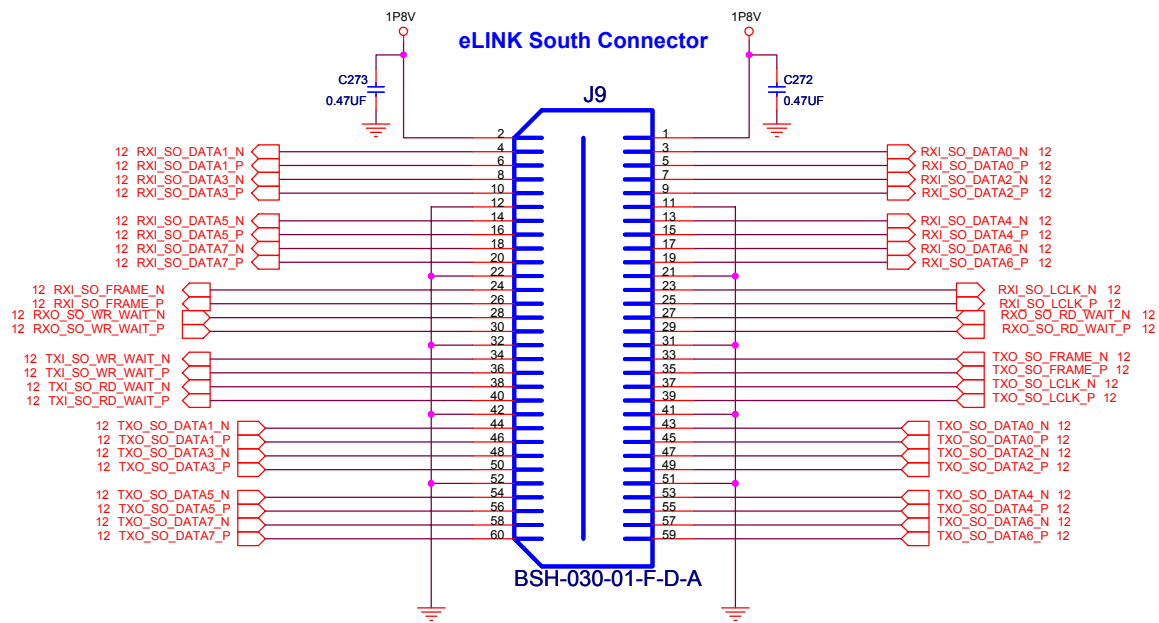
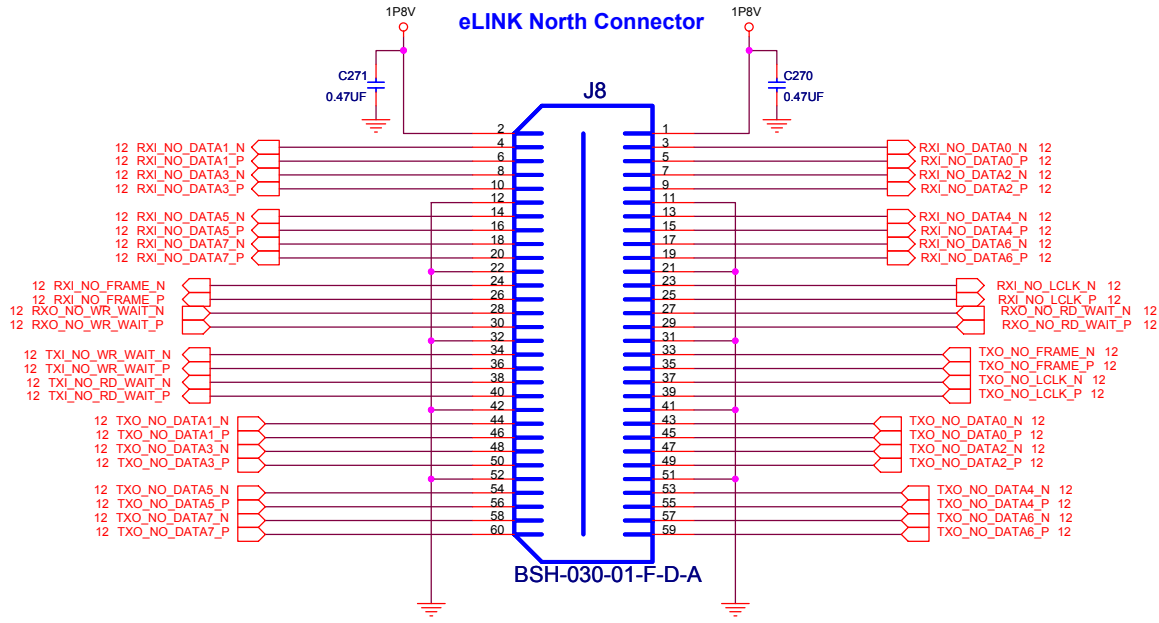
DSP PROCESSOR 2-OF-3



DSP PROCESSOR 3-OF-3



DSP eLINK CONNECTORS

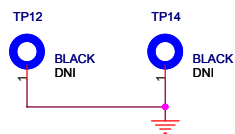


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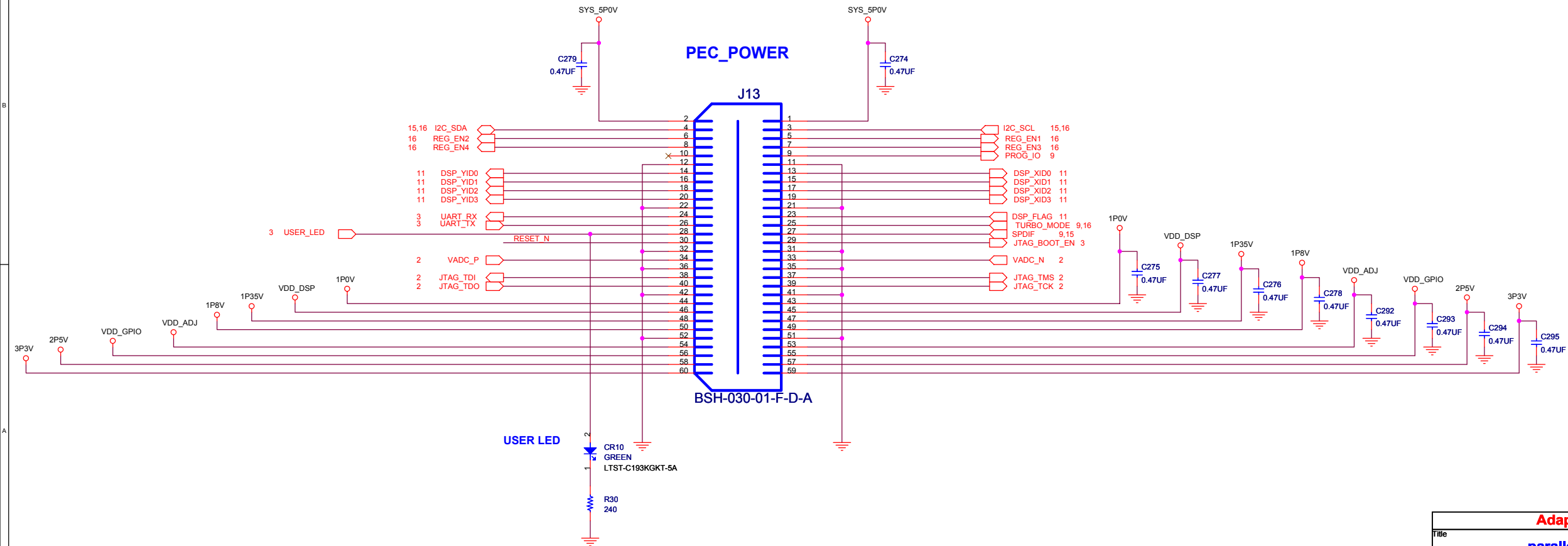
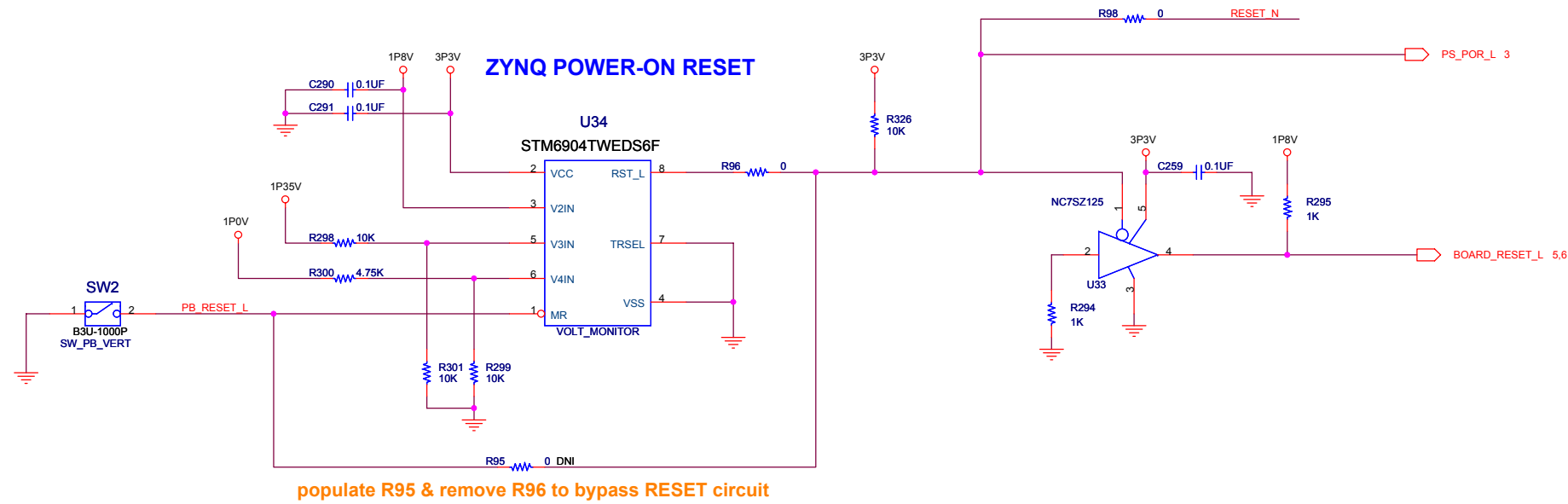
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POWER MANAGEMENT



Power Good = LED ON
Power Bad = LED OFF

RESET GENERATION



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