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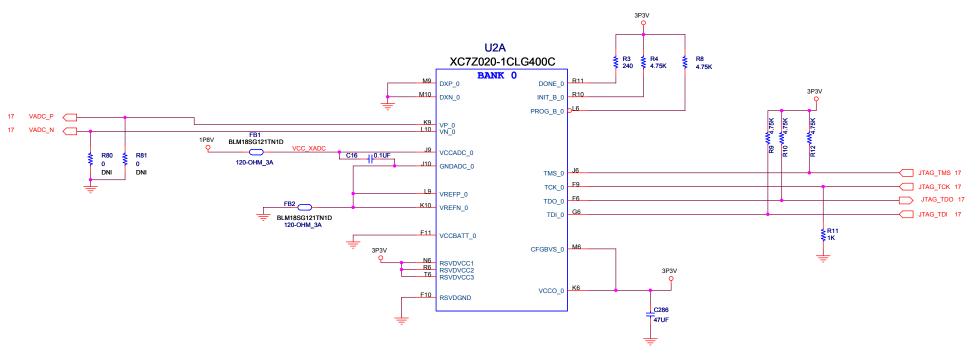
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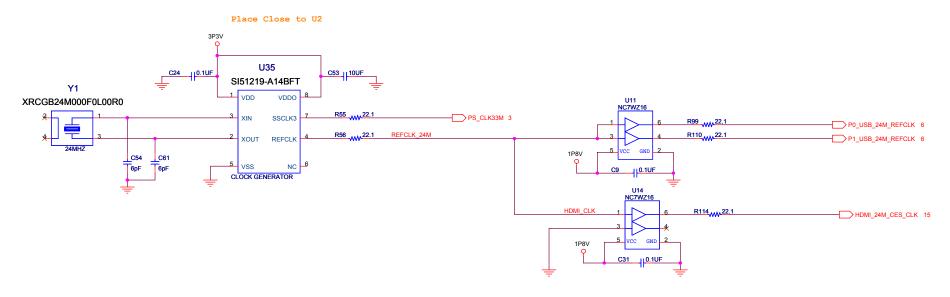
ZYNQ BANK0

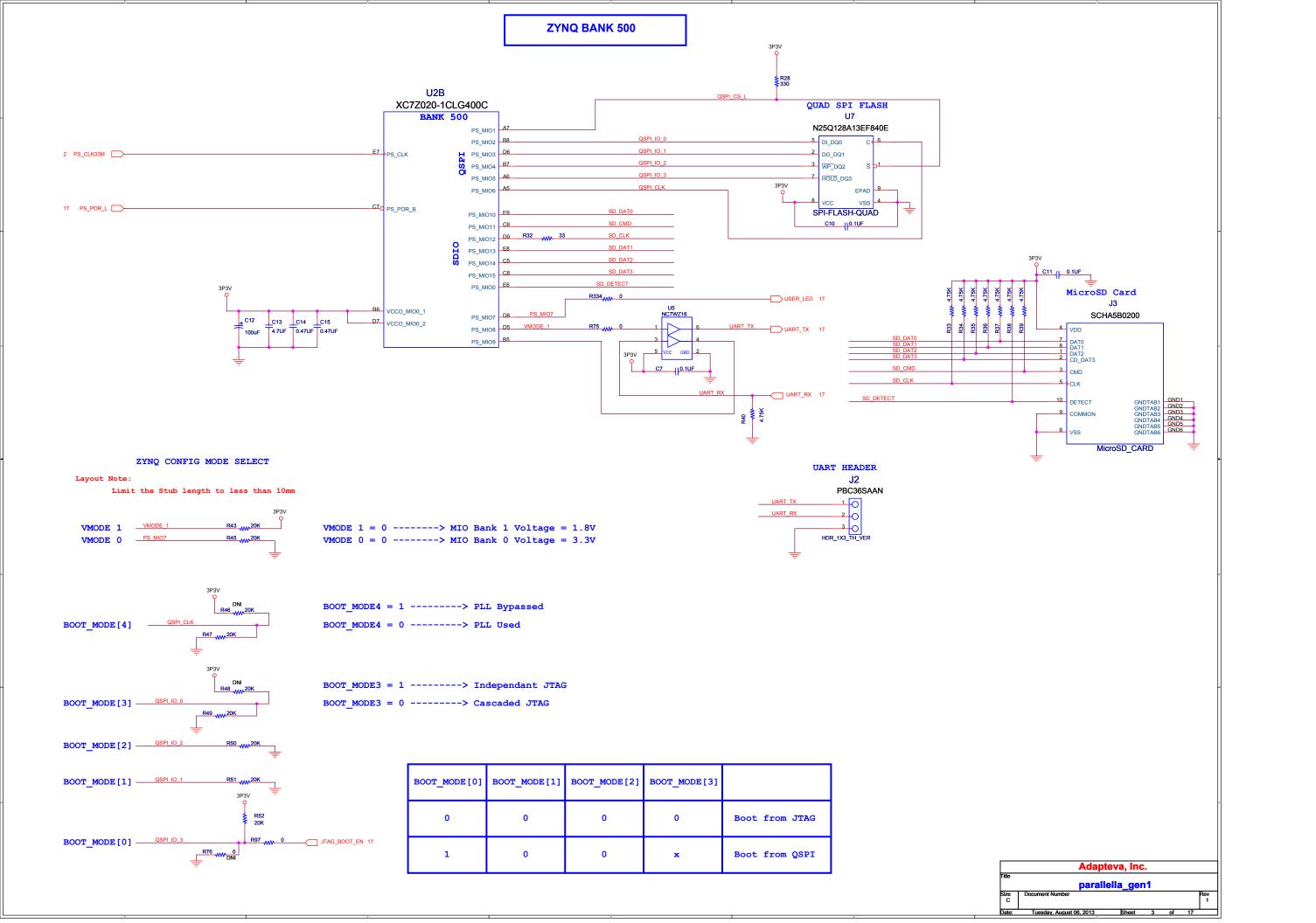


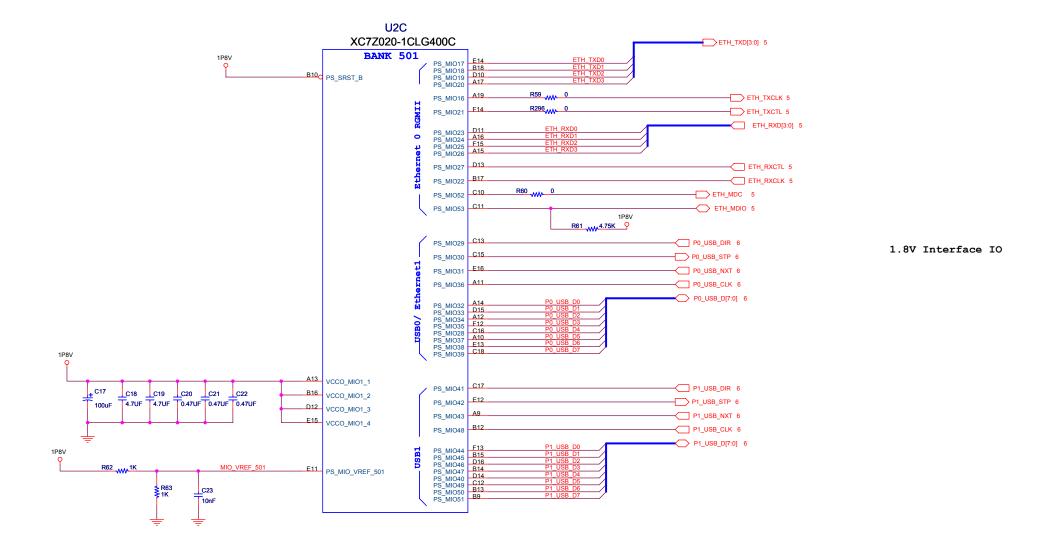
BANK 0 OPERATING VOLTAGE = 3.3V

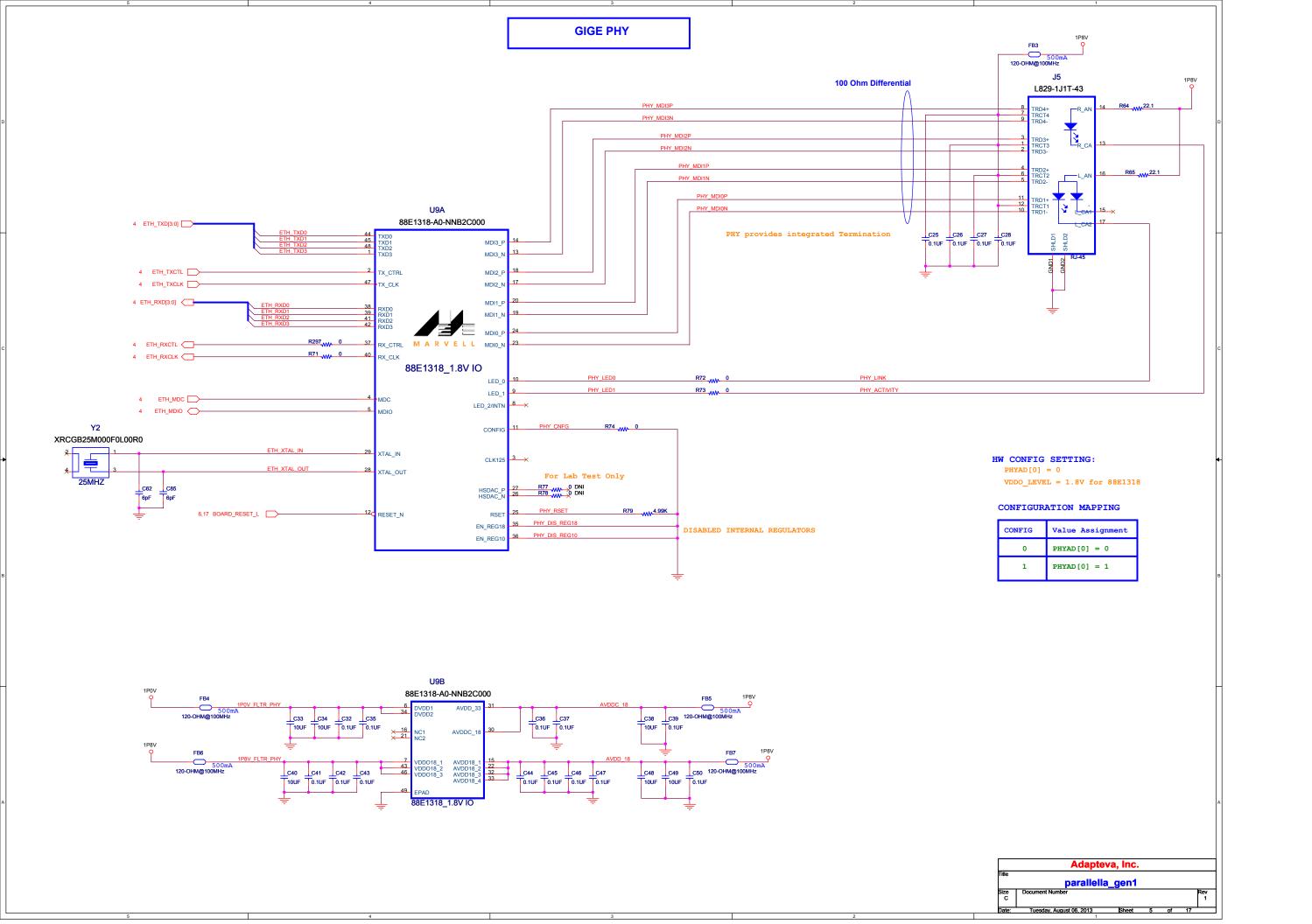
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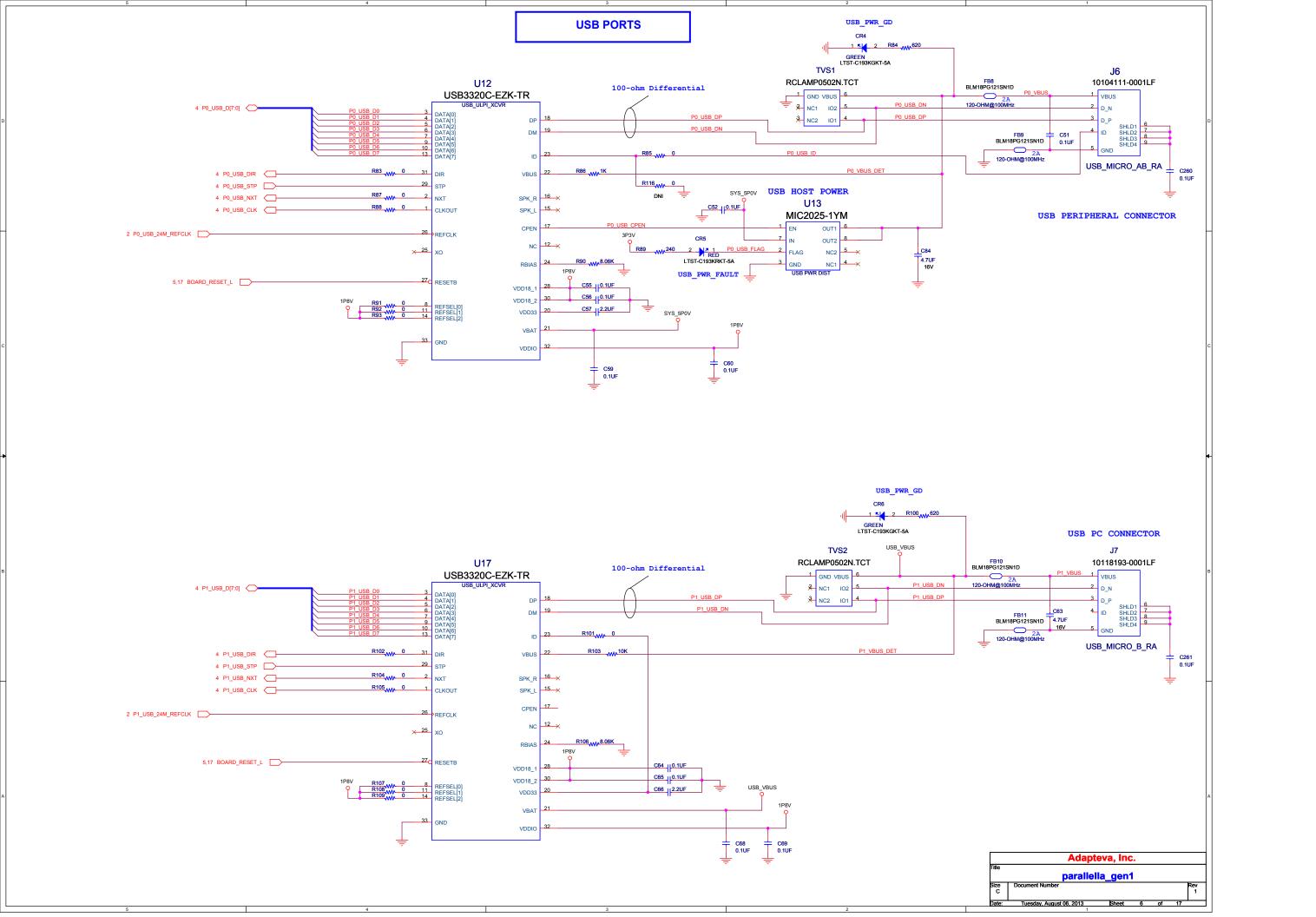
PROGRAMMABLE CLOCK GENERATOR







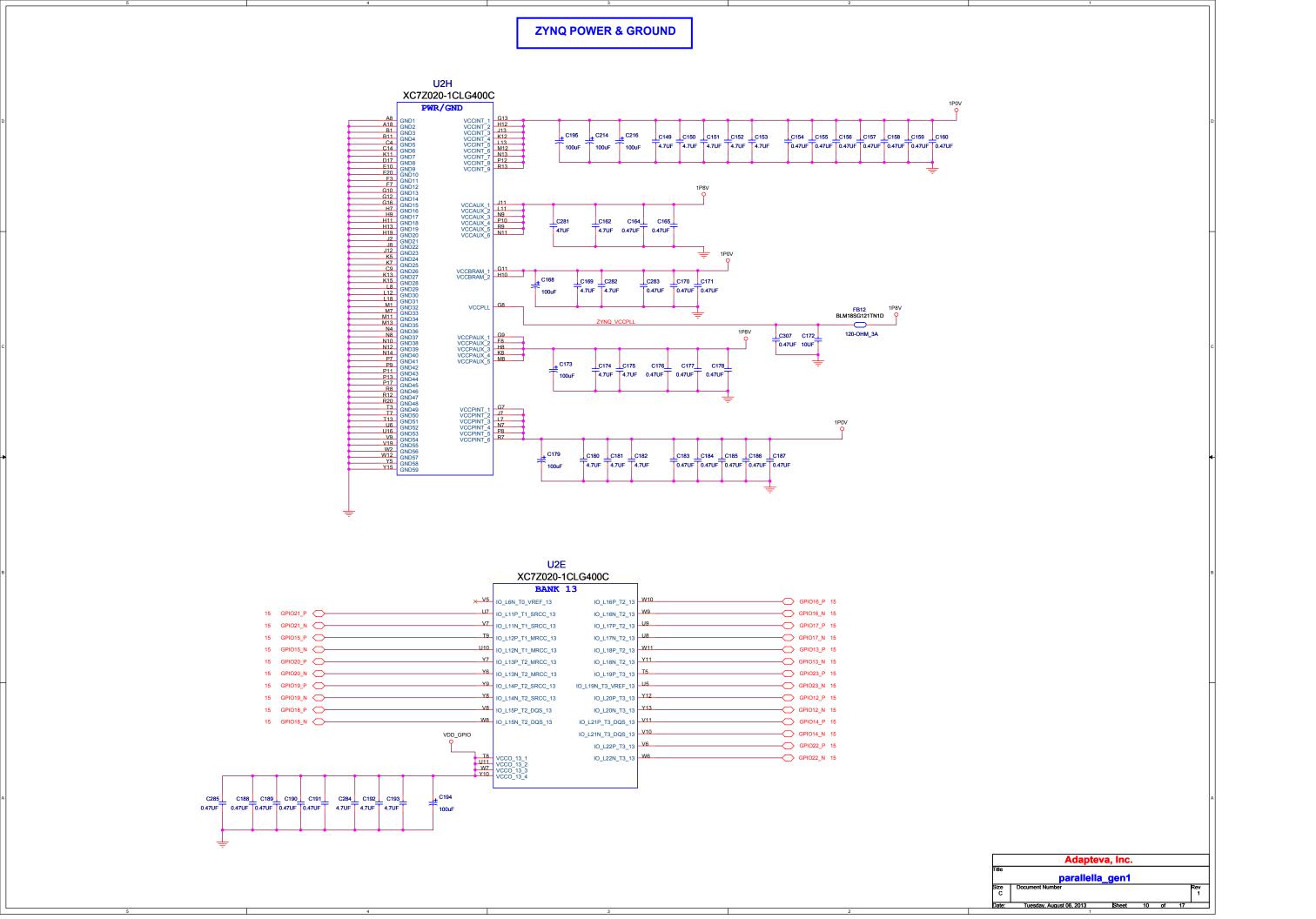


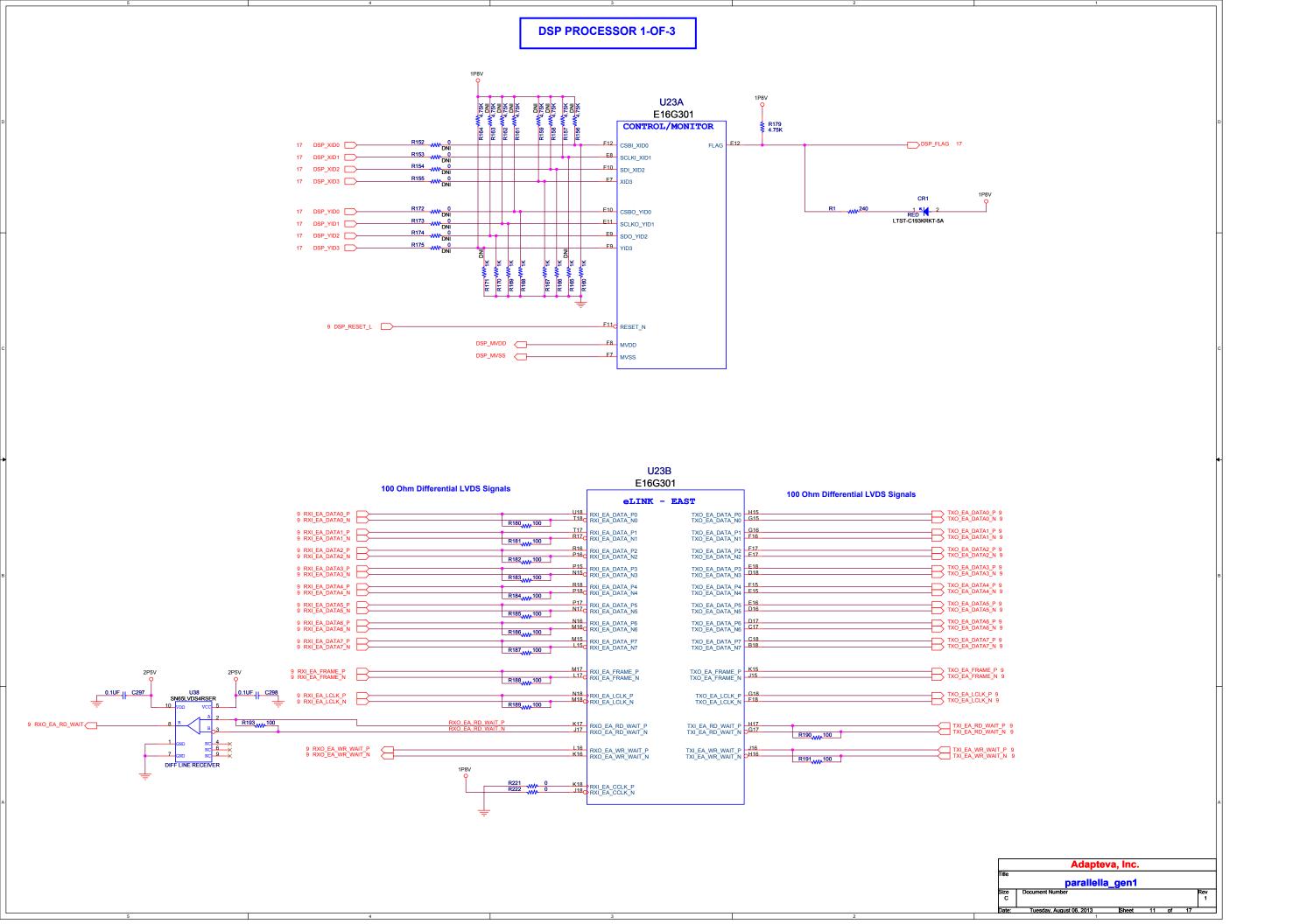


ZYNQ BANK 502 U2D XC7Z020-1CLG400C 8 DDR_DQ[31:0] DDR_A[14:0] 8 **BANK** 502 PS_DDR_A14
PS_DDR_A13
PS_DDR_A15
PS_DDR_A10
PS_DDR_A10
PS_DDR_A9
PS_DDR_A9
PS_DDR_A7
PS_DDR_A7
PS_DDR_A7
PS_DDR_A6
PS_DDR_A7
PS_DDR_A6
PS_DDR_A3
PS_DDR_A3
PS_DDR_A3
PS_DDR_A3
PS_DDR_A3
PS_DDR_A3
PS_DDR_A2
PS_DDR_A1
PS_DDR_A1 PS_DDR_BA2
PS_DDR_BA1
PS_DDR_BA0
PS_DDR_BA0
PS_DDR_BA0
PS_DDR_BA0
PS_DDR_BA0
PS_DDR_BA0
PS_DDR_BA0
PS_DDR_BA2
PS_DDR_BA3
PS_DDR_BA3 PS_DDR_ODT N5 DDR3_ODT R320 33 DDR_ODT 8 PS_DDR_CS_B N1 DDR3_CS_L R321 WW 33 DDR_CS_L 8 PS_DDR_WE_B M5 DDR3 WE L R322 33 DDR_WE_L 8 PS_DDR_CAS_B P5 DDR3_CAS_L R323 WW 33 DDR_CAS_L 8 PS_DDR_CKE N3 DDR3_CKE R325 WW 10 DDR_CKE 8 W5 PS_DDR_DQS_P3 PS_DDR_DQS_N3 R2 PS_DDR_DQS_P2 PS_DDR_DQS_N2 _G2 _F2 PS_DDR_DQS_P1 _PS_DDR_DQS_N1 PS_DDR_DM3 PS_DDR_DM2 PS_DDR_DM1 PS_DDR_DM0 Y1 T1 F1 F1 A1 C2 PS_DDR_DQS_P0 PS_DDR_DQS_N0 8 DDR_DQS_P0 8 DDR_DQS_N0 PS_DDR_DRST_B B4 DDR_RST_L 8 1P35V R111_{WW}4.75K A3 VCCO_DDR_1
D2 VCCO_DDR_2
E5 VCCO_DDR_3
G1 VCCO_DDR_5
H4 VCCO_DDR_5
1.3 VCCO_DDR_7
R5 VCCO_DDR_9
VCCO_DDR_10 1P35V + C70 + C71 PS_DDR_VRN PS_DDR_VRP H5 PS_DDR_VREF0 PS_DDR_VREF1 P6 C82 C83 R67 1K Adapteva, Inc. parallella_gen1 Tuesday, August 06, 2013

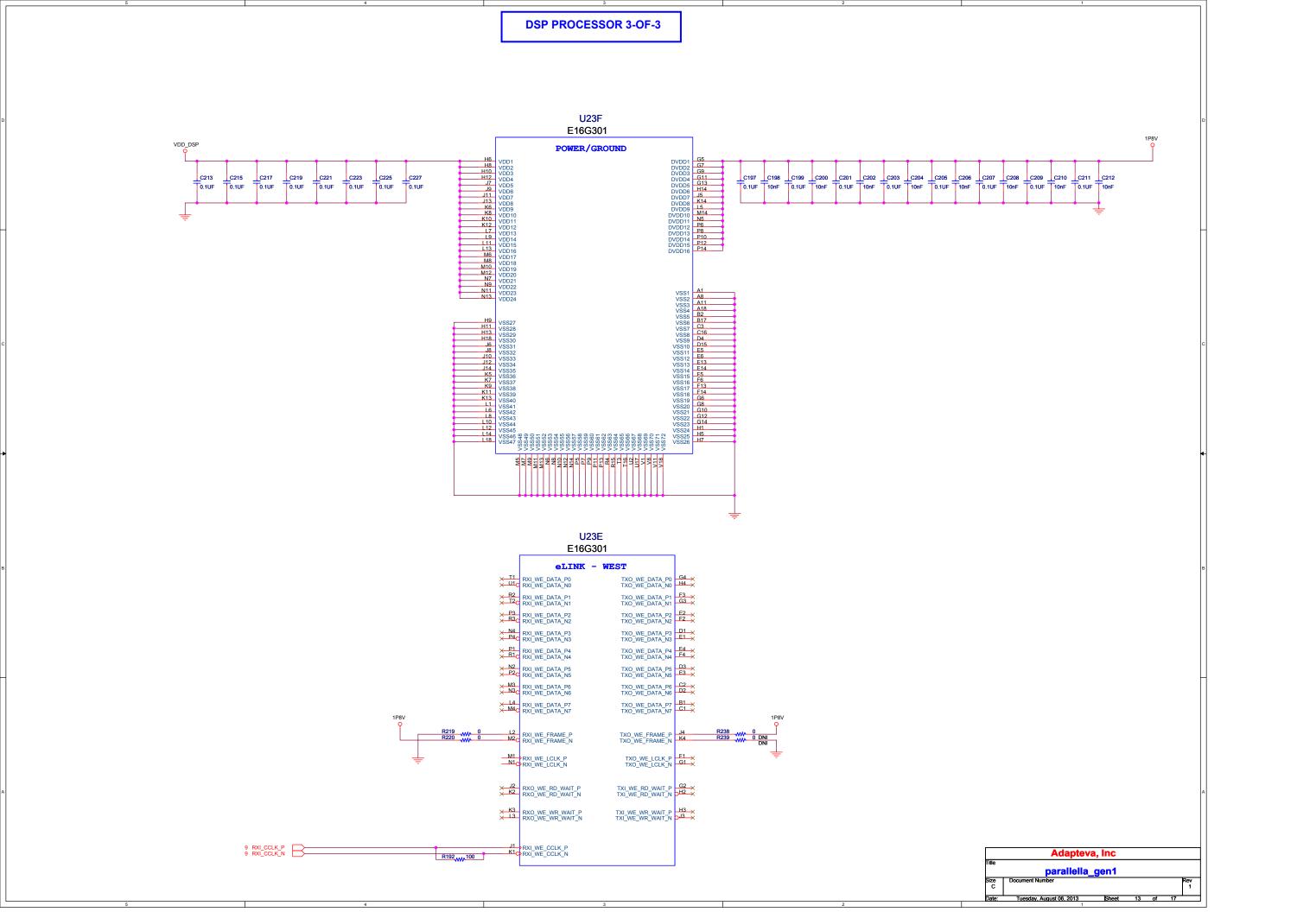
DDR3 - 256M X 32 7 DDR_DQ[31:0] ___ U20 MT41K256M32SLD-125:E 7 DDR_A[14:0] DQ0 A4 DQ1 A2 DQ2 B4 DQ3 E2 DQ4 E4 DQ5 DQ6 DQ7 DQ16 DQ17 DQ18 DQ19 DQ20 DQ21 DQ21 DQ22 DQ23 DDR3_256MX32 7 DDR_ODT 7 DDR_CS_L 7 DDR_RAS_L G40 RAS_L DQ24 DQ25 DQ26 DQ26 DQ27 DQ28 DQ28 DQ30 DQ31 7 DDR_CAS_L _G3_C CAS_L 7 DDR_WE_L 1P35V C95 C96 R70 1K P10 DQS2 DQS2_L VREFDQ J1 P3 DQS3 DQS3_L 1P35V C97 4.7UF VDD1 A1 A12 VDD3 VDD4 VDD5 VDD6 VDD7 VDD8 C98 4.7UF C99 4.7UF C100 0.47UF 7 DDR_CKE VDD01 81
VDD01 81
VDD02 812
VDD03 C1
VDD04 C12
VDD05 D1
VDD06 D1
VDD07 E3
VDD08 E10
VDD01 M3
VDD01 M3
VDD01 M3
VDD01 M3
VDD01 M3
VDD01 P1
VDD01 R1
VDD01 R1
VDD01 R1
VDD01 R1
VDD01 R1
VDD01 R1 C101 0.47UF R115_{WW}80.6 C102 0.47UF 7 DDR_CLK_N C103 0.47UF 7 DDR_RST_L ____ H10 RESET_L C104 0.047UF C105 0.047UF C106 0.047UF C107 0.047UF C108 0.047UF C109 0.047UF C110 0.047UF C111 0.047UF C112 0.047UF V8801 V8802 V8803 V8804 V8804 V8804 V8801 V8901 C113 0.047UF Adapteva, Inc. parallella_gen1

BANKS 34 & 35 Enable 100-ohm internal termination on all LVDS inputs 15 HDMI_D[23:8] U2F U2G XC7Z020-1CLG400C XC7Z020-1CLG400C BANK 34 VDD GPIO BANK 35 R20 _{WW} 4.75K R19 IO_0_34 IO 25 34 IO_25_34 J15__ RXO_EA_RD_WAIT 11 15 GPIO11_P -IO_L1P_T0_34 IO_L13P_T2_MRCC_34 N18 PS_I2C_SCL 15 11 RXI_EA_DATA1_P ____ RXI_CCLK_P 13 IO_L13P_T2_MRCC_35 H16 IO_L13N_T2_MRCC_34 P19 HDMI_D19 15 GPIO11_N ____ IO_L1N_T0_34 11 RXI_EA_DATA1_N ____ RXI_CCLK_N 13 IO_L1N_T0_AD0N_35 IO_L13N_T2_MRCC_35 _T12 | IO_L2P_T0_34 PROG_IO 17 15 GPIO10_P — 11 RXI_EA_DATA0_P RXO_EA_WR_WAIT_P 11 _U12_ IO_L2N_T0_34 IO_L14N_T2_SRCC_34 P20 15 GPIO10_N — HDMI_INT 15 11 RXI_EA_DATAO_N ____ RXO_EA_WR_WAIT_N 11 IO_L3P_T0_DQS_PUDC_B_34 IO_L15P_T2_DQS_34 T20__ 15 GPIO8_P 🔷 11 RXI_EA_DATA4_P RXI_EA_DATA5_P 11 V13 IO_L3N_T0_DQS_34 IO_L15N_T2_DQS_34 U20___ GPIO8 N 🔷 11 RXI_EA_DATA4_N ____ RXI_EA_DATA5_N 11 IO_L3N_T0_DQS_AD1N<u>I**0**5</u>L15N_T2_DQS_AD12N_35 <mark>-</mark>-V12 IO_L4P_T0_34 IO_L16P_T2_34 V20_ GPIO9 P 11 RXI_EA_DATA2_P RXI_EA_DATA6_P 11 IO_L4P_T0_35 IO_L16P_T2_35 _W13__IO_L4N_T0_34 IO_L16N_T2_34 W20__ GPIO9_N < IO_L16N_T2_35 G18_ RXI_EA_DATA6_N 11 11 RXI_EA_DATA2_N ____ IO_L4N_T0_35 IO_L5P_T0_34 IO_L17P_T2_34 Y18__ GPIO5_P 🔷 11 RXI_EA_DATA3_P IO_L5P_T0_AD9P_35 IO_L17P_T2_AD5P_35 J20 TXO_EA_FRAME_P 11 T15 IO_L5N_T0_34 IO_L17N_T2_34 GPIO5_N 11 RXI_EA_DATA3_N ____ IO_L5N_T0_AD9N_35 IO_L17N_T2_AD5N_35 TXO_EA_FRAME_N 11 P14 IO_L6P_T0_34 GPIO4_P 🔷 IO_L18P_T2_34 —— GPIO1_P 15 11 RXI_EA_LCLK_P ____ RXI_EA_DATA7_P 11 IO_L6P_T0_35 IO_L18P_T2_AD13P_35 __R14__ IO_L6N_T0_VREF_34 IO_L18N_T2_34 W16_ —— GPIO1_N 15 11 RXI_EA_LCLK_N ____ RXI_EA_DATA7_N 11 IO_L6N_T0_VREF_35 IO_L18N_T2_AD13N_35 ___Y16__IO_L7P_T1_34 SPDIF ___ IO_L19P_T3_34 R16 TURBO_MODE 16,17 11 TXO_EA_DATA5_P M19 RXI_EA_FRAME_P 11 IO_L7P_T1_AD2P_35 IO_L19P_T3_35 IO_L19N_T3_VREF_34 R17 R41 WW 22.1 __Y17__IO_L7N_T1_34 15 HDMI_DE ____ HDMI_CLK 15 RXI_EA_FRAME_N 11 O_L7N_T1_AD2N_35 IO_L19N_T3_VREF_35 G15__ HDMI_HSYNC 15 GPIO7_P 🔷 W14 IO_L8P_T1_34 IO_L20P_T3_AD6P_35 K14 TXI_EA_RD_WAIT_P 11 IO_L8P_T1_AD10P_35 Y14 IO_L8N_T1_34 GPIO7_N 🔷 IO_L8N_T1_AD10N_35 GPIO0_P 🔷 HDMI_VSYNC 15 L19 IO_L9P_T1_DQS_AD3P_066_L21P_T3_DQS_AD14P_35 N15 TXO_EA_DATA7_P 11 11 TXO_EA_DATA4_P ____ IO_L21N_T3_DQS_34 V18 HDMI_D10 _U17_ IO_L9N_T1_DQS_34 GPIO0_N 🔷 L20 IO_L9N_T1_DQS_AD3N<u>IO5</u>L21N_T3_DQS_AD14N_35 N16 11 TXO_EA_DATA4_N ____ IO_L22P_T3_34 W18 HDMI_D9 V15 IO_L10P_T1_34 VDD_GPIO ___K19 | IO_L10P_T1_AD11P_35 IO_L22P_T3_AD7P_35 11 TXO_EA_DATAO_P TXO_EA_DATA1_P 11 _W15__IO_L10N_T1_34 IO_L22N_T3_34 W19 R18 4.75K IO_L22N_T3_AD7N_35 L15___ 11 TXO_EA_DATAO_N TXO_EA_DATA1_N 11 U14 IO_L11P_T1_SRCC_34 IO_L23P_T3_34 _L16_ IO_L11P_T1_SRCC_35 IO_L23P_T3_35 M14 TXO_EA_DATA3_P 11 11 TXO_EA_DATA2_P _U15 | IO_L11N_T1_SRCC_34 IO_L23N_T3_34 P18 GPIO6 N > __L17__ IO_L11N_T1_SRCC_35 IO_L23N_T3_35 M15__ 11 TXO_EA_DATA2_N ____ TXO_EA_DATA3_N 11 __U18__ IO_L12P_T1_MRCC_34 GPIO3 P IO_L24P_T3_34 → GPIO2 P 15 11 TXO_EA_LCLK_P ____ ___U19__IO_L12N_T1_MRCC_34 IO_L24N_T3_34 P16 GPI02_N 15 __K18 | IO_L12N_T1_MRCC_35 | IO_L24N_T3_AD15N_35 | J16___ TXI_EA_WR_WAIT_N 11 11 TXO_EA_LCLK_N ____ VDD GPIO N19 R15 T18 V14 C126 C127 C128 C129 C130 C131 C132 C133 0.47UF 0.47UF 0.47UF 0.47UF 4.7UF 4.7UF 4.7UF 4.7UF . C134 . C143 100uF Adapteva, Inc. parallella_gen1

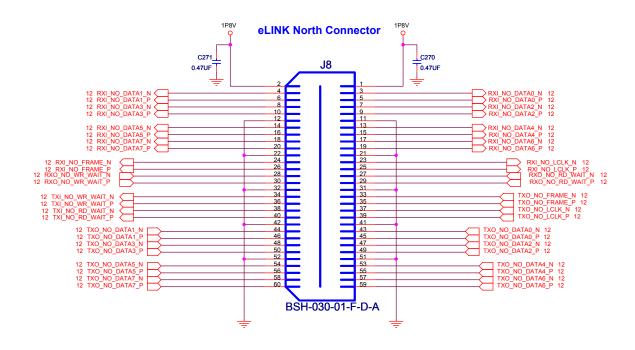


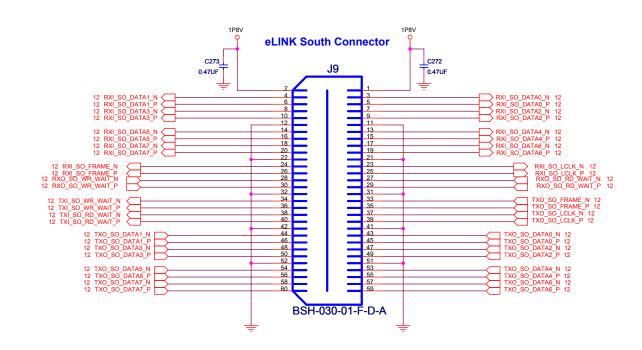


DSP PROCESSOR 2-OF-3 U23C E16G301 100 Ohm Differential LVDS Signals 100 Ohm Differential LVDS Signals eLINK - NORTH TXO_NO_DATA_P0 D12
TXO_NO_DATA_N0 D11 TXO_NO_DATA0_P 14
TXO_NO_DATA0_N 14 A3 RXI_NO_DATA_P0 RXI_NO_DATA_N0 R233_{WW} 100 R194_{MM}100 TXO_NO_DATA_P1 C13
TXO_NO_DATA_N1 TXO_NO_DATA1_P 14
TXO_NO_DATA1_N 14 R232_{WW} 100 R195_{MM}100 TXO_NO_DATA_P2 B14 TXO_NO_DATA_N2 B13 TXO_NO_DATA2_P 14
TXO_NO_DATA2_N 14 R196_{MM}100 R231_{WW} 100 TXO_NO_DATA3_P 14
TXO_NO_DATA3_N 14 R197_{MM}100 R230_{MM}100 TXO_NO_DATA_P4
TXO_NO_DATA_N4
D13 A5 RXI_NO_DATA_P4 RXI_NO_DATA_N4 TXO_NO_DATA4_P 14
TXO_NO_DATA4_N 14 14 RXI_NO_DATA4_P
14 RXI_NO_DATA4_N R198_{MM}100 R229_{WM} 100 TXO_NO_DATA5_P 14
TXO_NO_DATA5_N 14 14 RXI_NO_DATA5_P 14 RXI_NO_DATA5_N R199_{MM}100 R228_{WW}100 DNI C7 RXI_NO_DATA_P6 RXI_NO_DATA_N6 TXO_NO_DATA6_P 14
TXO_NO_DATA6_N 14 TXO_NO_DATA_P6 B16 TXO_NO_DATA_N6 B15 14 RXI_NO_DATA6_P 14 RXI NO DATA6 N R227_{WW} 100 R200_{MM}100 TXO_NO_DATA_P7 A16 TXO_NO_DATA7_P 14
TXO_NO_DATA7_N 14 D8 RXI_NO_DATA_P7 RXI_NO_DATA_N7 14 RXI_NO_DATA7_P 14 RXI_NO_DATA7_N R226_{WW} 100 R243 WW 10K TXO_NO_FRAME_P 14
TXO_NO_FRAME_N 14 14 RXI_NO_FRAME_P 14 RXI_NO_FRAME_N TXO_NO_FRAME_P D10
TXO_NO_FRAME_N D9 R202 1P8VO R242 WW 10K TXO_NO_LCLK_P 14
TXO_NO_LCLK_N 14 R203_{AAA}100 R206_{WW}100 R241 ______10K B10 RXO_NO_RD_WAIT_P RXO_NO_RD_WAIT_N TXI_NO_RD_WAIT_P B12
TXI_NO_RD_WAIT_N OB11 R204_{WW}100 R240 _{WW} 10K R205_{MM}100 U23D E16G301 100 Ohm Differential LVDS Signals 100 Ohm Differential LVDS Signals eLINK - SOUTH TXO_SO_DATA0_P 14
TXO_SO_DATA0_N 14 TXO_SO_DATA_P0 R11
TXO_SO_DATA_N0 R12 R207_{AAA}100 U3 RXI_SO_DATA_P1
U4C RXI_SO_DATA_N1 TXO_SO_DATA1_P 14
TXO_SO_DATA1_N 14 14 RXI_SO_DATA1_P 14 RXI_SO_DATA1_N R208_{MM}100 TXO_SO_DATA2_P 14 TXO_SO_DATA2_N 14 T4 RXI_SO_DATA_P2
T50 RXI_SO_DATA_N2 14 RXI_SO_DATA2_P 14 RXI_SO_DATA2_N R209_{MM}100 TXO_SO_DATA3_P 14 TXO_SO_DATA3_N 14 RS RXI_SO_DATA_P3 RXI_SO_DATA_N3 14 RXI_SO_DATA3_P 14 RXI_SO_DATA3_N R210_{MM}100 V4 RXI_SO_DATA_P4
V5_ RXI_SO_DATA_N4 14 RXI_SO_DATA4_P 14 RXI_SO_DATA4_N TXO_SO_DATA_P4 R13
TXO_SO_DATA_N4 R14 R211_{MM}100 TXO_SO_DATA5_P 14 TXO_SO_DATA5_N 14 U5 RXI_SO_DATA_P5 RXI_SO_DATA_N5 14 RXI_SO_DATA5_P 14 RXI_SO_DATA5_N TXO_SO_DATA_P5 T15 R212_{MM}100 TXO_SO_DATA6_P 14 TXO_SO_DATA6_N 14 14 RXI_SO_DATA6_P 14 RXI_SO_DATA6_N T6 RXI_SO_DATA_P6 RXI_SO_DATA_N6 TXO_SO_DATA_P6 U15
TXO_SO_DATA_N6 U16 R213_{AAA}100 R7 RXI_SO_DATA_P7 RXI_SO_DATA_N7 14 RXI_SO_DATA7_P 14 RXI_SO_DATA7_N TXO_SO_DATA7_P 14
TXO_SO_DATA7_N 14 R214_{MM}100 R246 _______10K R245 _{WW} 10K TXO_SO_FRAME_P R10 R236 MM 100 14 RXI_SO_FRAME_P 14 RXI_SO_FRAME_N R215_{MM}100 1P8VO R247 WW 10K R244 ______10K ______01P8V R216_{MM}100 TXI_SO_RD_WAIT_P
TXI_SO_RD_WAIT_N U9 RXO_SO_RD_WAIT_P RXO_SO_RD_WAIT_N TXI_SO_RD_WAIT_P 14
TXI_SO_RD_WAIT_N 14 R234_{WW} 100 R217_{AAA}100 14 RXO_SO_WR_WAIT_P
14 RXO_SO_WR_WAIT_N T8 RXO_SO_WR_WAIT_P RXO_SO_WR_WAIT_N TXI_SO_WR_WAIT_P
TXI_SO_WR_WAIT_N R235_{WM} 100 R218_{MM}100 Adapteva, Inc. parallella_gen1



DSP eLINK CONNECTORS





Adapteva, Inc.

Title

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