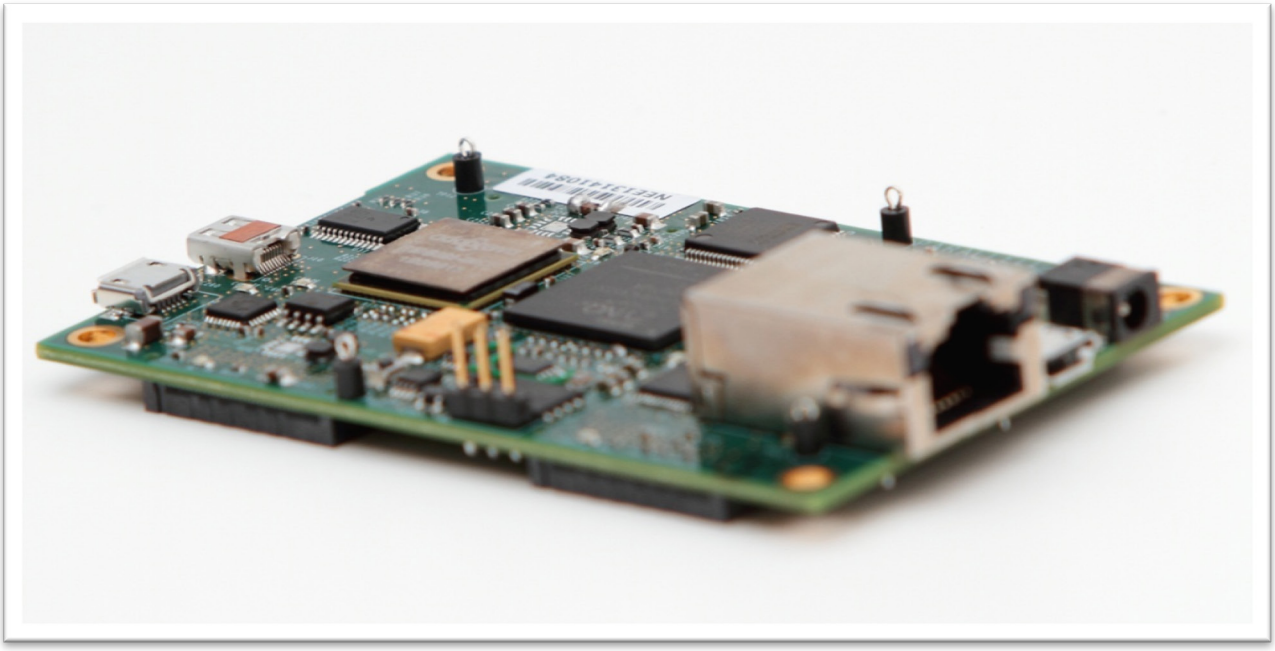
Parallella Reference Manual

GEN0

REV-0.13.06.29

(THIS BOARD HAS BEEN REPLACED BY GEN1!)

(FOR REVIEW PURPOSES ONLY!)



Revision History

Version	Comments
0.13.2.13	Initial release
0.13.6.29	Changed licensing information

Related Documents:

Zynq Technical Reference Manuals:

http://www.xilinx.com/support/documentation/zynq-7000.htm

Epiphany Architecture Reference Manual:

http://www.adapteva.com/support/docs/e3-reference-manual

Epiphany SDK Reference Manual:

http://www.adapteva.com/support/docs/esdk3-manual

Epiphany-III Datasheet:

http://www.adapteva.com/products/silicon-devices/e16g301/

Epiphany-IV Datasheet:

http://www.adapteva.com/products/silicon-devices/e16g401/

Parallella Expansion Connector Datasheet:

https://www.samtec.com/technical-specifications/Default.aspx?SeriesMaster=BSH

Software Repositories:

Parallella Software Development Kit:

https://github.com/parallella/

SD Card Images: (early access account needed)

ftp://ftp.parallella.org

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1 Overview

The Parallella board is a high performance computing platform based on a dual-core ARM-A9 Zynq System-On-Chip and Adapteva's Epiphany multicore coprocessor. The Parallella board will be made available with two different coprocessor options: The *Parallella-16* with a16-core Epiphany-III chip and the *Parallella-64* with a 64-core Epiphany-IV chip.

Table 1: Parallella Feature Summary

Feature	Specification
CPU	Xilinx Zynq7000 Series Dual-Core ARM-A9 with 512KB L2 Shared Cache
Coprocessor	Epiphany Multicore Coprocessor The Parallella-16 board includes the 16-core Epiphany-III processor The Parallella-64 board includes the 64-cire Epiphany-IV processor
Memory	1024MB DDR3L
Boot Flash	32Mb NOR Flash
Indicators	2 User controlled LEDs
USB 2.0 Port	Connects to a host machine (PC/tablet/smartphone)
USB 2.0 Port	Connect peripheral devices
Ethernet	10/100/1000 Ethernet, RJ45 with magnetics, LEDs
SD Connector	MicroSD, 3.3V
Video	Micro HDMI connector
Expansion Connectors	Four 60-pin high speed Samtec connectors for: • Epiphany link expansion connector(s) • Zynq programmable logic extension connector • Power, JTAG, debug connector
Power Source	USB or 5.0V DC
PCB	86.36mm x 53.34mm (3.4'' x 2.15'')

Table 2: Parallella Performance Goals

Performance Goal	Value
Peak Instruction Issue Rate	25 GIPS (Parallella-16) 90 GIPS (Parallella-64)
Peak Epiphany Frequency	800MHz(Parallella-16 700MHz(Parallella-64)
Peak Floating Point Performance	25 GFLOPS (Parallella-16) 90 GFLOPS (Parallella-64)
Peak Bandwidth between Zynq and Epiphany	1.6GB/s
PEC_FPGA Peak Bandwidth	2.85GB/s (22.8 Gbps)
PEC_NORTH/PEC_SOUTH Peak Bandwidth	3.2GB/s (25.6 Gbps)
Typical Power Consumption	5 Watts

Figure 1: Zynq Connectivity Diagram

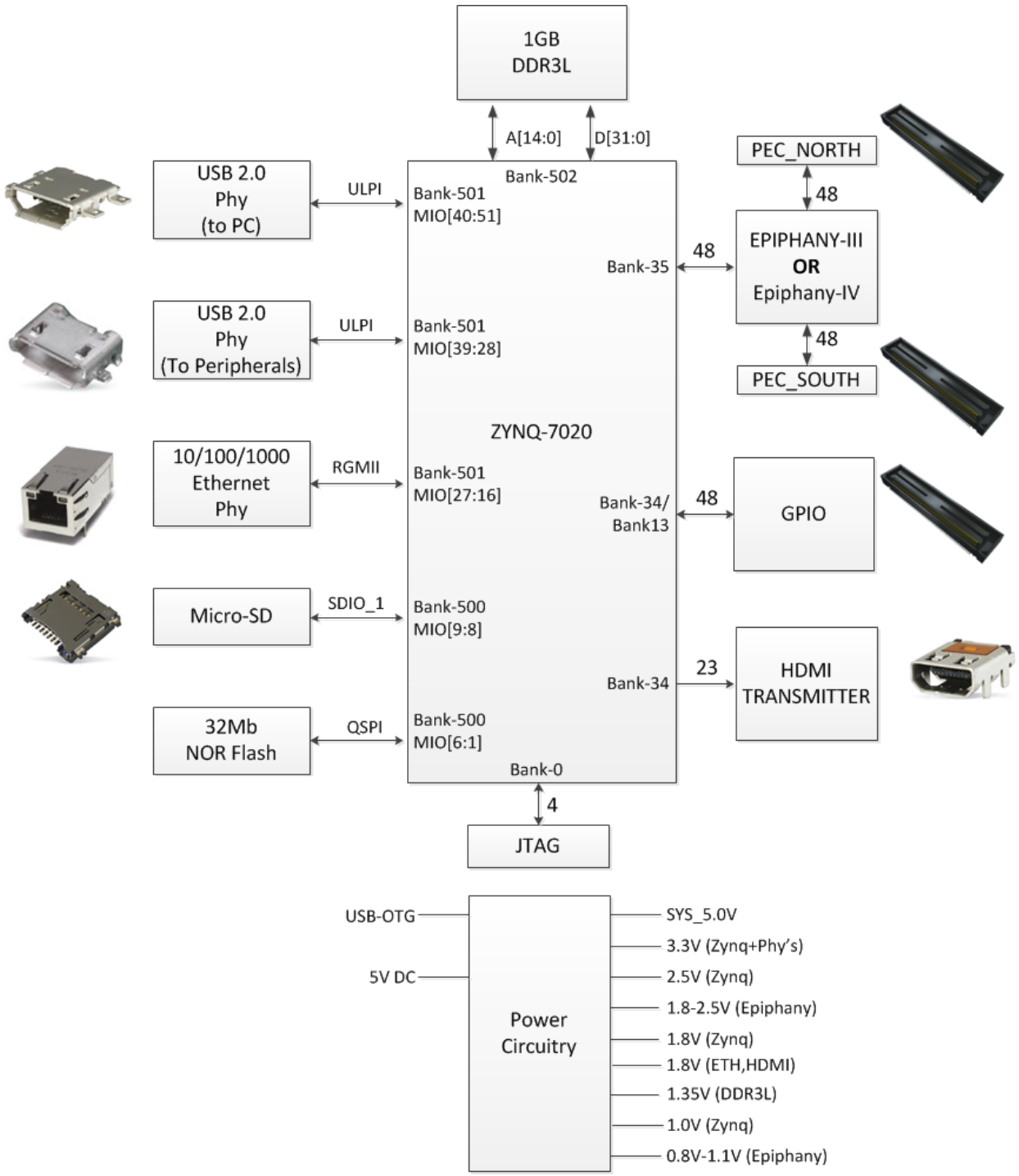
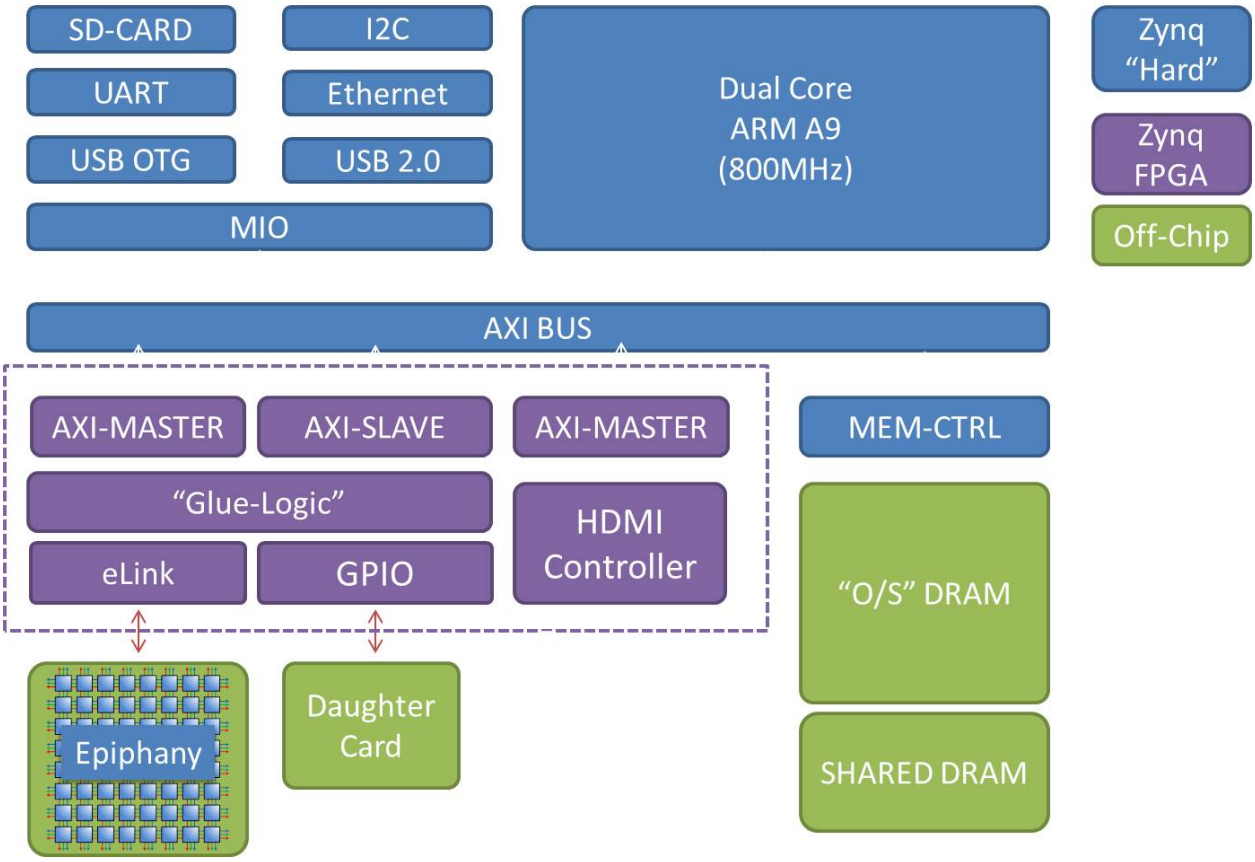
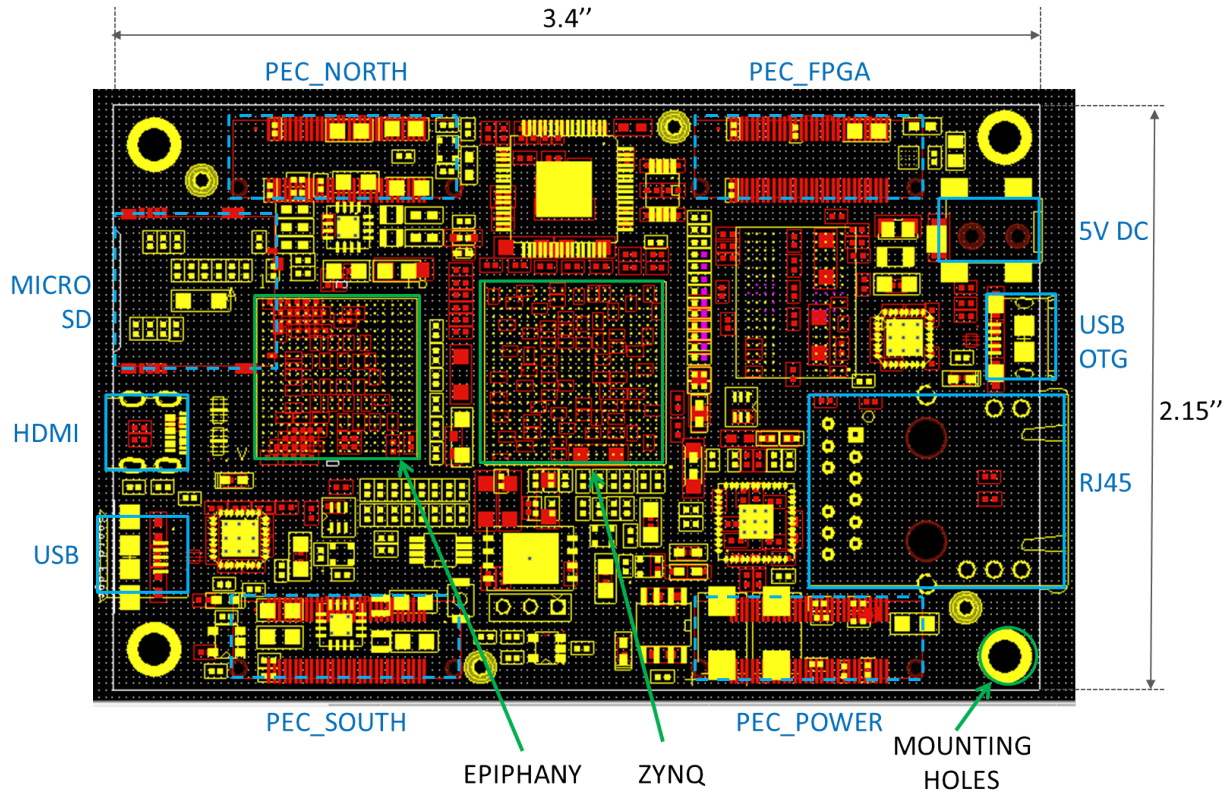


Figure 2: Zynq Connectivity



The Epiphany coprocessor is connected to the Zynq SOC via the 48 eLink. An Epiphany eLink protocol is implemented in the programmable logic portion of the Zynq SOC. In addition to the eLink interface, the programmable logic block shipped with the Parallella board includes an AXI master interface, an AXI slave interface, and an HDMI controller. The Hardware Description Language (HDL) source code for the eLink and remaining logic will be available as free open source code once the final Parallella boards ship.

Figure 3: Parallella Board Placement



The Parallella is a dense credit card sized board. The active components and the majority of the standard connectors are placed on the top side of the board. The expansion connectors and MicroSD card connector are placed at the bottom side of the board. The standard connectors on opposite sides of the cards to allow easy access when sitting in a rack or closed box. To fit all the connectors on two edges, we had to minimize the size of the standard connectors.

There are 0.125'' diameter mounting holes in the each corner of the Parallella board.

2 Parallella Specifications

2.1 CPU

Zynq-7020 SOC

2.2 Coprocessor

16-core Epiphany-III or 64-core Epiphany-IV Manycore Coprocessor

2.3 SDRAM

1GB 32-bit wide DDR3L SDRAM

2.4 Flash

32Mb QSPI Flash Memory

2.5 Power Source

Parallella board can be powered from the USB OTG port (limited performance) or from a 5V DC supply (full performance).

2.6 Gigabit Ethernet

10/100/1000 Ethernet, RJ45 connector with magnetics and LED indicators

2.7 USB 2.0 (0) Connector

Connects to a host PC. Connector can be used to power the Parallella board.

2.8 USB 2.0 (1) Connector

Connects to peripheral devices such as mice, keyboard, camera, etc.

2.9 MicroSD

Primary boot source and main Parallella board storage medium.

2.10 Micro HDMI Port

High quality connection to most modern DVI/HDMI monitors and TVs.

2.11 LED Indicators

Two LEDs controllable by GPIO pins through software.

2.12 Reset Button

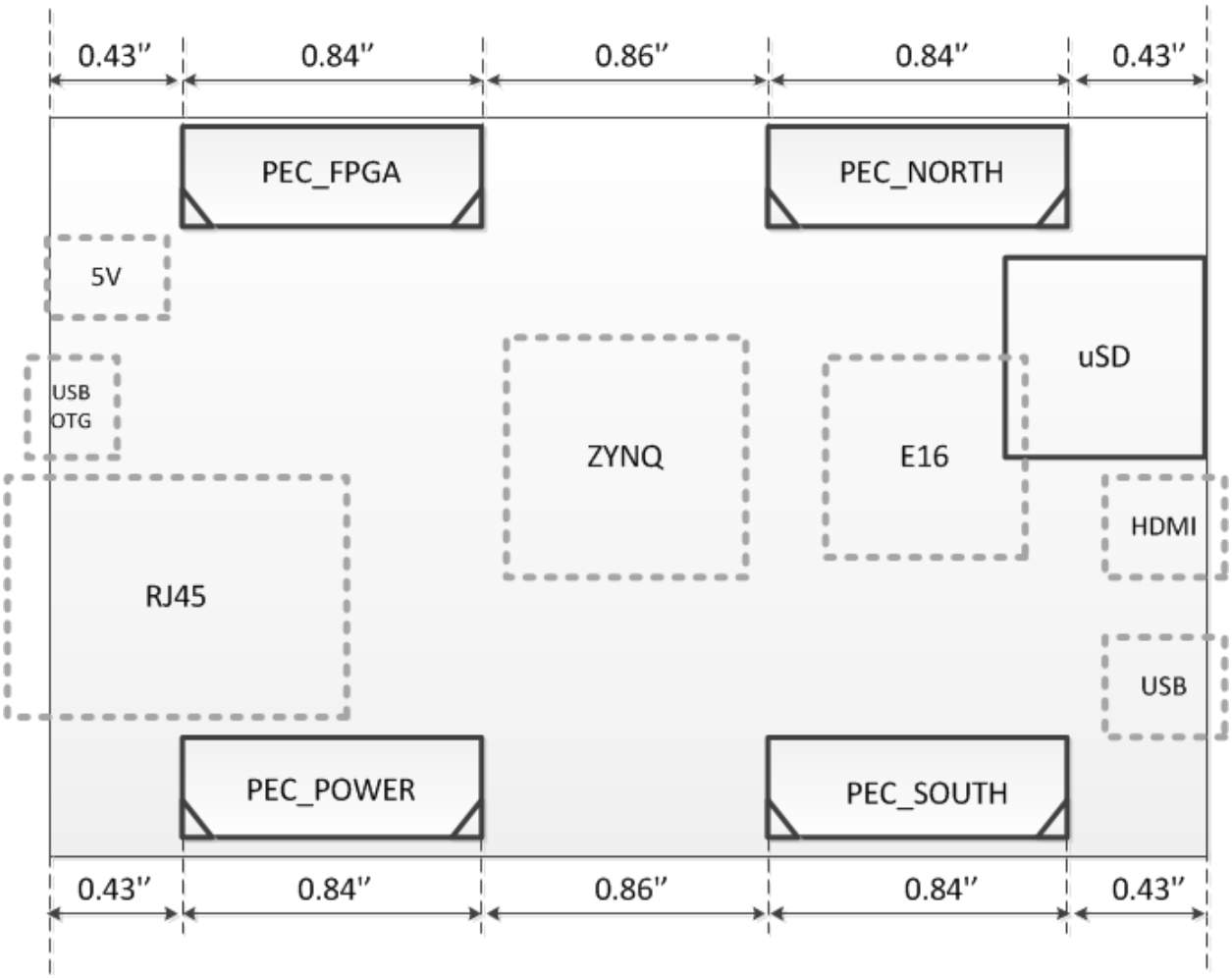
Pushing the reset button resets all components on board including the Zynq CPU and initiates a system reboot.

3 Parallella Expansion Connector (PEC)

3.1 Overview

The Parallella board has four expansions connectors placed on the opposite edges of the bottom side of the board shown in Figure 4. For exact connector and placement information, please refer to the Parallella mechanical drawings. The following figure shows the expansion connector placements as seen from the bottom side of the board.

Figure 4: PEC Placement



The Parallella Expansion Connectors uses the 60 pin BSH-030-01-FDA high speed connector from Samtec. The corresponding mating connector to be placed on the expansion card is BTH-030-01-FDA. The complete data sheets can be found at:

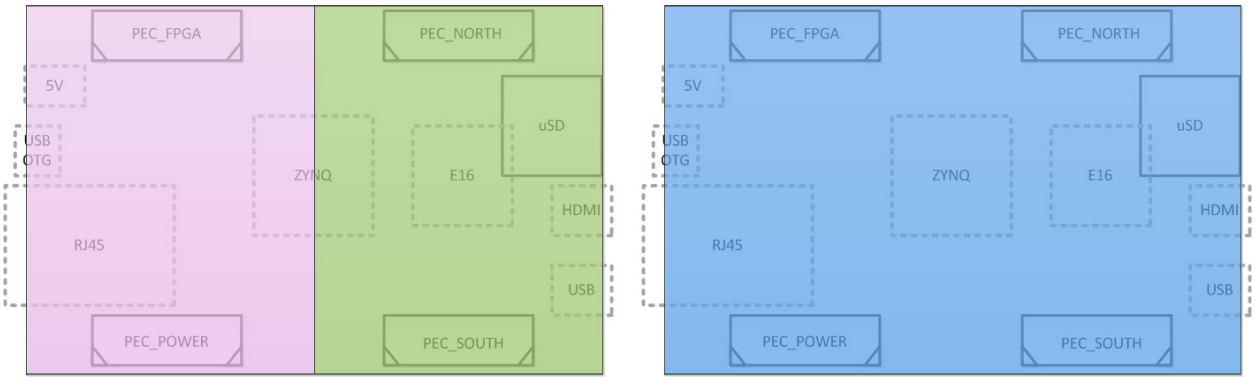
https://www.samtec.com/technical-specifications/Default.aspx?SeriesMaster=BSH

Table 3: Parallella Expansion Connectors (PEC)

Connector	Functions
PEC_POWER	Power and control signal expansion connector
PEC_FPGA	Zynq programmable logic expansion connector
PEC_NORTH	Epiphany north link expansion connector
PEC_SOUTH	Epiphany south link expansion connector

The four symmetrically placed connectors allow for robust mating of expansion cards and the Parallella board using matching BTH-030-01-FDA connectors. As shown in Figure 5, it is possible to connect a single full length credit card sized expansion cards or two half-length expansion cards. The left side shows two half-length expansion boards (pink/green transparent) connected to the backside of the Parallella board and the right side shows a full length (blue transparent) expansion board connected to the backside of the Parallella board.

Figure 5: Expansion Card Configuration



3.2 PEC_POWER

The PEC_POWER provides convenient access to various key Parallella board signals and can provide power to expansion boards with modest current requirements. Expansion boards with substantial current requirements should draw power from the SYS_5P0V connection or generate supply rails from a completely independent DC supply.

Table 4: PEC_POWER Signal Summary

Signal	Direction	Signaling	Notes
SYS_5P0V	Output	5.0V	5.0 V Parallella expansion board supply. Driven by output of power selector IC that selects between DC power and USB power. Maximum current that can be delivered to an expansion card is TBD.
1P0V	Output	1.0V	1.0V Parallella expansion board supply shared with the Zyng chip. Maximum current that can delivered to an expansion card is TBD.
1P35V	Output	1.35V	1.35V Parallella expansion board supply shared with the DDR3L memory system. Maximum current that can delivered to an expansion card is TBD.
1P8V	Output	1.8V	1.8V Parallella expansion board supply shared with the Zynq. Maximum current that can delivered to an expansion card is TBD.
3.3V	Output	3.3V	3.3V Parallella expansion board supply shared with the Zynq. Maximum current that can delivered to an expansion card is TBD.
GND	Inout	0.0V	System Ground
I2C_SDA	Inout	2.5V	I2C bidirectional open-drain Serial Data Line
I2C_SCL	Inout	2.5V	I2C bidirectional open-drain Serial Clock Line
UART_TX	Output	3.3V	UART transmit signal
UART_RX	Input	3.3V	UART receive signal
SPDIF	Output	2.5V	Single bit SPDIF audio interface output
PG	Output	5.0V	Indicator that the Parallella board power is good
LED0	Output	3.3V	On board LED0 signal driven by Zynq
LED1	Output	3.3V	On board LED1 signal driven by Zynq
DSP_XID[3:0]	Input	2.5V/1.8V	Sets the relative chip column ID of the Epiphany chip on the Parallella board, overriding the default board settings. These signals must be driven correctly in systems that utilize the

			PEC_NORTH/PEC_SOUTH to connect multiple Parallella boards.
DSP_YID[3:0]	Input	2.5V/1.8V	Sets the relative chip row ID of the Epiphany chip on the Parallella board, overriding the default board settings. These signals must be driven correctly in systems that utilize the PEC_NORTH/PEC_SOUTH to connect multiple Parallella boards.
DSP_FLAG	Output	2.5V/1.8V	Flag signal driven by the Epiphany.
TURBO_MODE	Output	3.3V	Driven high when the Parallella board is powered from a 5V DC supply.
JTAG_TCK	Input	3.3V	JTAG Clock
JTAG_TMS	Input	3.3V	JTAG Test Mode
JTAG_TDI	Input	3.3V	JTAG Data Input
JTAG_TDO	Output	3.3V	JTAG Data Output

Table 5: PEC_POWER Pin Mapping

Signal	Pin	Pin	Signal
SYS_5P0V	1	2	SYS_5P0V
GND	3	4	GND
I2C_SCL	5	6	UART_RX
I2C_SDA	7	8	UART_TX
PG	9	10	USER_LED
GND	11	12	GND
DSP_XID[0]	13	14	DSP_YID[0]
DSP_XID[1]	15	16	DSP_YID[1]
DSP_XID[2]	17	18	DSP_YID[2]
DSP_XID[3]	19	20	DSP_YID[3]
GND	21	22	GND
1P0V	23	24	1P0V
DSP_FLAG	25	26	TURBO_MODE
GND	27	28	GND
SPDIF	29	30	N/A
GND	31	32	GND
1PV8	33	34	1P8V
JTAG_TMS	35	36	JTAG_TDI
GND	37	38	GND
JTAG_TCK	39	40	JTAG_TDO
GND	41	42	GND
2P5V	43	44	2P5V
N/A	45	46	N/A
N/A	47	48	N/A
N/A	49	50	N/A
N/A	51	52	N/A
3P3V	53	54	3P3V
GND	55	56	GND
VADC_N	57	58	VADC_P
GND	59	60	GND

3.3 PEC_FPGA

The PEC_FPGA can be used to connect the Zynq programmable logic to expansion cards or other PEC_FPGA interfaces on another Parallella boards. The PEC_FPGA includes 48 bidirectional signals that can be configured within the Zynq device to support a number of different signal standards. When configured as LVDS signals, each differential signal pair provides a maximum bandwidth of 950Mbps. In aggregate, the PEC_FPGA connections can provide 22Gbps of total IO bandwidth. [Note: With faster speed grades available versions of Zynq devices available, these maximum throughput numbers could increase to 1.25Gbps/30Gbps respectively]

Table 6: PEC_FPGA Signal Summary

Signal	Direction	Notes
VDD_2P5V	Output	2.5V supply driven by power management IC on the Parallella board. Maximum current that can be delivered to an expansion card is TBD.
GND	Inout	System Ground
GPIOx_{N,P}	Inout	A differential pair or two single ended signals that connect between an expansion card and the Zynq device on the Parallella board.

Table 7: PEC_FPGA Pin Mapping

Signal	Pin	Pin	Signal
VDD_2P5V	1	2	VDD_2P5V
GPIO0_N	3	4	GPIO1_N
GPIO0_P	5	6	GPIO1_P
GPIO2_N	7	8	GPIO3_N
GPIO2_P	9	10	GPIO3_P
GND	11	12	GND
GPIO4_N	13	14	GPIO5_N
GPIO4_P	15	16	GPIO5_P
GPIO6_N	17	18	GPIO7_N
GPIO6_P	19	20	GPIO7_P
GND	21	22	GND
GPIO8_N	23	24	GPIO9_N
GPIO8_P	25	26	GPIO9_P
GPIO10_N	27	28	GPIO11_N
GPIO10_P	29	30	GPIO11_P
GND	31	32	GND
GPIO12_N	33	34	GPIO13_N
GPIO12_P	35	36	GPIO13_P
GPIO14_N	37	38	GPIO15_N
GPIO14_P	39	40	GPIO15_P
GND	41	42	GND
GPIO16_N	43	44	GPIO17_N
GPIO16_P	45	46	GPIO17_P
GPIO18_N	47	48	GPIO19_N
GPIO18_P	49	50	GPIO19_P
GND	51	52	GND
GPIO20_N	53	54	GPIO21_N
GPIO20_P	55	56	GPIO21_P
GPIO22_N	57	58	GPIO23_N
GPIO22_P	59	60	GPIO23_P

3.4 PEC_NORTH/PEC_SOUTH

The PEC_NORTH and PEC_SOUTH are connected to the north and south link of the Epiphany chip on the Parallella board. These expansion connectors can be used to connect multiple Parallella boards in a bidirectional line or ring configuration or they can be connected to an FPGA device with an Epiphany eLink interface implemented in RTL. The Parallella-16 board support 2.5V standard differential LVDS signaling while the Parallella-64 board supports 1.8V sub-LVDS signaling.

Table 8: PEC_NORTH/PEC_SOUTH Signal Summary

Signal Name	Direction	Signal Description
VDD_ADJ	Output	2.5V supply driven by power management IC on the Parallella board. Maximum current that can be delivered to an expansion card is TBD.
GND	Inout	System ground
RXI_{NO,SO}_DATA_{P,N}[7:0]	Input	Receiver data
RXI_{NO,SO}_FRAME_{P,N}	Input	Receiver packet framing signal
RXI_{NO,SO}_LCLK_{P,N}	Input	Receiver clock
RXO_{NO,SO}_WR_WAIT_{P,N}	Output	Push-back for transmitter indicating that device must hold off on sending another write packet.
RXO_{NO,SO}_RD_WAIT_{P,N}	Output	Push-back for transmitter indicating that device must hold off on sending another read packet.
TXO_{NO,SO}_DATA_{P,N}[7:0]	Output	Transmitter data
TXO_{NO,SO}_FRAME_{P,N}	Output	Transmitter packet framing signal
TXO_{NO,SO}_LCLK_{P,N}	Output	Transmitter clock
TXI_{NO,SO}_WR_WAIT_{P,N}	Input	Push-back from receiver indicating that transmitter must hold off on sending another write packet.
TXI_{NO,SO}_RD_WAIT_{P,N}	Input	Push-back from transmitter indicating that transmitter must hold off on sending another read packet.

Table 9: PEC_NORTH Pin Mapping for Parallella-16

Signal	Pin	Pin	Signal
VDD_ADJ	1	2	VDD_ADJ
RXI_NO_DATA_N[0]	3	4	RXI_NO_DATA_N[1]
RXI_NO_DATA_P[0]	5	6	RXI_NO_DATA_P[1]
RXI_NO_DATA_N[2]	7	8	RXI_NO_DATA_N[3]
RXI_NO_DATA_P[2]	9	10	RXI_NO_DATA_P[3]
GND	11	12	GND
RXI_NO_DATA_N[4]	13	14	RXI_NO_DATA_N[5]
RXI_NO_DATA_P[4]	15	16	RXI_NO_DATA_P[5]
RXI_NO_DATA_N[6]	17	18	RXI_NO_DATA_N[7]
RXI_NO_DATA_P[6]	19	20	RXI_NO_DATA_P[7]
GND	21	22	GND
RXI_NO_LCLK_N	23	24	RXI_NO_FRAME_N
RXI_NO_LCLK_P	25	26	RXI_NO_FRAME_P
RXO_NO_RD_WAIT_N	27	28	RXO_SO_WR_WAIT_N
RXO_NO_RD_WAIT_P	29	30	RXO_NO_WR_WAIT_P
GND	31	32	GND
TXO_NO_FRAME_N	33	34	TXI_NO_WR_WAIT_N
TXO_NO_FRAME_P	35	36	TXI_NO_WR_WAIT_P
TXO_NO_LCLK_N	37	38	TXI_NO_RD_WAIT_N
TXO_NO_LCLK_P	39	40	TXI_NO_RD_WAIT_P
GND	41	42	GND
TXO_NO_DATA_N[0]	43	44	TXO_NO_DATA_N[1]
TXO_NO_DATA_P[0]	45	46	TXO_NO_DATA_P[1]
TXO_NO_DATA_N[2]	47	48	TXO_NO_DATA_N[3]
TXO_NO_DATA_P[2]	49	50	TXO_NO_DATA_P[3]
GND	51	52	GND
TXO_NO_DATA_N[4]	53	54	TXO_NO_DATA_N[5]
TXO_NO_DATA_P[4]	55	56	TXO_NO_DATA_P[5]
TXO_NO_DATA_N[6]	57	58	TXO_NO_DATA_N[7]
TXO_NO_DATA_P[6]	59	60	TXO_NO_DATA_P[7]

Table 10: PEC_NORTH Pin Mapping for Parallella-64

Signal	Pin	Pin	Signal
VDD_ADJ	1	2	VDD_ADJ
TXO_NO_DATA_P[7]	3	4	TXO_NO_DATA_P[6]
TXO_NO_DATA_N[7]	5	6	TXO_NO_DATA_N[6]
TXO_NO_DATA_P[5]	7	8	TXO_NO_DATA_P[4]
TXO_NO_DATA_N[5]	9	10	TXO_NO_DATA_N[4]
GND	11	12	GND
TXO_NO_DATA_P[3]	13	14	TXO_NO_DATA_P[2]
TXO_NO_DATA_N[3]	15	16	TXO_NO_DATA_N[2]
TXO_NO_DATA_P[1]	17	18	TXO_NO_DATA_P[0]
TXO_NO_DATA_N[1]	19	20	TXO_NO_DATA_N[0]
GND	21	22	GND
TXO_NO_LCLK_P	23	24	TXI_NO_RD_WAIT_P
TXO_NO_LCLK_N	25	26	TXI_NO_RD_WAIT_N
RXO_NO_WR_WAIT_P	27	28	RXO_NO_RD_WAIT_P
RXO_NO_WR_WAIT_N	29	30	RXO_NO_RD_WAIT_N
GND	31	32	GND
TXO_NO_FRAME_P	33	34	TXI_NO_WR_WAIT_N
TXO_NO_FRAME_N	35	36	TXI_NO_WR_WAIT_P
RXI_NO_LCLK_P	37	38	RXI_NO_FRAME_P
RXI_NO_LCLK_N	39	40	RXI_NO_FRAME_N
GND	41	42	GND
RXI_NO_DATA_P[7]	43	44	RXI_NO_DATA_P[6]
RXI_NO_DATA_N[7]	45	46	RXI_NO_DATA_N[6]
RXI_NO_DATA_P[5]	47	48	RXI_NO_DATA_P[4]
RXI_NO_DATA_N[5]	49	50	RXI_NO_DATA_N[4]
GND	51	52	GND
RXI_NO_DATA_P[3]	53	54	RXI_NO_DATA_P[2]
RXI_NO_DATA_N[3]	55	56	RXI_NO_DATA_N[2]
RXI_NO_DATA_P[1]	57	58	RXI_NO_DATA_P[0]
RXI_NO_DATA_N[1]	59	60	RXI_NO_DATA_N[0]

Table 11: PEC_SOUTH Pin Mapping for Parallella-16

Signal	Pin	Pin	Signal
VDD_ADJ	1	2	VDD_ADJ
RXI_SO_DATA_N[0]	3	4	RXI_SO_DATA_N[1]
RXI_SO_DATA_P[0]	5	6	RXI_SO_DATA_P[1]
RXI_SO_DATA_N[2]	7	8	RXI_SO_DATA_N[3]
RXI_SO_DATA_P[2]	9	10	RXI_SO_DATA_P[3]
GND	11	12	GND
RXI_SO_DATA_N[4]	13	14	RXI_SO_DATA_N[5]
RXI_SO_DATA_P[4]	15	16	RXI_SO_DATA_P[5]
RXI_SO_DATA_N[6]	17	18	RXI_SO_DATA_N[7]
RXI_SO_DATA_P[6]	19	20	RXI_SO_DATA_P[7]
GND	21	22	GND
RXI_SO_LCLK_N	23	24	RXI_SO_FRAME_N
RXI_SO_LCLK_P	25	26	RXI_SO_FRAME_P
RXO_SO_RD_WAIT_N	27	28	RXO_SO_WR_WAIT_N
RXO_SO_RD_WAIT_P	29	30	RXO_SO_WR_WAIT_P
GND	31	32	GND
TXO_SO_FRAME_N	33	34	TXI_SO_WR_WAIT_N
TXO_SO_FRAME_P	35	36	TXI_SO_WR_WAIT_P
TXO_SO_LCLK_N	37	38	TXI_SO_RD_WAIT_N
TXO_SO_LCLK_P	39	40	TXI_SO_RD_WAIT_P
GND	41	42	GND
TXO_SO_DATA_N[0]	43	44	TXO_SO_DATA_N[1]
TXO_SO_DATA_P[0]	45	46	TXO_SO_DATA_P[1]
TXO_SO_DATA_N[2]	47	48	TXO_SO_DATA_N[3]
TXO_SO_DATA_P[2]	49	50	TXO_SO_DATA_P[3]
GND	51	52	GND
TXO_SO_DATA_N[4]	53	54	TXO_SO_DATA_N[5]
TXO_SO_DATA_P[4]	55	56	TXO_SO_DATA_P[5]
TXO_SO_DATA_N[6]	57	58	TXO_SO_DATA_N[7]
TXO_SO_DATA_P[6]	59	60	TXO_SO_DATA_P[7]

Table 12: PEC_SOUTH Pin Mapping for Parallella-64

Signal	Pin	Pin	Signal
VDD_ADJ	1	2	VDD_ADJ
RXI_SO_DATA_N[7]	3	4	RXI_SO_DATA_N[6]
RXI_SO_DATA_P[7]	5	6	RXI_SO_DATA_P[6]
RXI_SO_DATA_N[5]	7	8	RXI_SO_DATA_N[4]
RXI_SO_DATA_P[5]	9	10	RXI_SO_DATA_P[4]
GND	11	12	GND
RXI_SO_DATA_N[3]	13	14	RXI_SO_DATA_N[2]
RXI_SO_DATA_P[3]	15	16	RXI_SO_DATA_P[2]
RXI_SO_DATA_N[1]	17	18	RXI_SO_DATA_N[0]
RXI_SO_DATA_P[1]	19	20	RXI_SO_DATA_P[0]
GND	21	22	GND
RXI_SO_LCLK_N	23	24	RXO_SO_RD_WAIT_N
RXI_SO_LCLK_P	25	26	RXO_SO_RD_WAIT_P
TXI_SO_WR_WAIT_N	27	28	TXI_SO_RD_WAIT_N
TXI_SO_WR_WAIT_P	29	30	TXI_SO_RD_WAIT_P
GND	31	32	GND
RXI_SO_FRAME_N	33	34	RXO_SO_WR_WAIT_N
RXI_SO_FRAME_P	35	36	RXO_SO_WR_WAIT_P
TXO_SO_LCLK_N	37	38	TXO_SO_FRAME_N
TXO_SO_LCLK_P	39	40	TXO_SO_FRAME_P
GND	41	42	GND
TXO_SO_DATA_N[7]	43	44	TXO_SO_DATA_N[6]
TXO_SO_DATA_P[7]	45	46	TXO_SO_DATA_P[6]
TXO_SO_DATA_N[5]	47	48	TXO_SO_DATA_N[4]
TXO_SO_DATA_P[5]	49	50	TXO_SO_DATA_P[3]
GND	51	52	GND
TXO_SO_DATA_N[3]	53	54	TXO_SO_DATA_N[2]
TXO_SO_DATA_P[3]	55	56	TXO_SO_DATA_P[2]
TXO_SO_DATA_N[1]	57	58	TXO_SO_DATA_N[0]
TXO_SO_DATA_P[1]	59	60	TXO_SO_DATA_P[0]

4 About the Parallella Board

4.1 Design Information

The board is open source hardware and the Parallella project provides all the files required to study, modify and manufacture the design.

The design resources provided include:

- Complete reference manual
- Schematic sources in OrCAD format
- PCB layout sources in Allegro format
- PCB manufacturing files in Gerber format
- Assembled board 3D CAD model(s)
- Bill of material

All design files can be found at:

http://github.com/parallella/parallella-hw/gen0

4.2 Build Options

The following Parallella assembly options will be supported in manufacturing:

- **Zynq Device**: Z-7010 or Z-7020
- **Epiphany Device:** E16G301 or E64G401
- **IO:** With our without Samtec expansion connectors
- **Ethernet:** With or without Ethernet (RJ45 and Ethernet Phy)

4.3 Contributors

- **Adapteva:** (http://www.adapteva.com)
  - Parallella architecture and board design (Andreas Olofsson)
  - FPGA design (Roman Trogan)
  - Linux distribution (Roman Trogan)
  - Board bringup (Roman Trogan, Andreas Olofsson)
  - Reference manuals (Andreas Olofsson)

- **Boston Design Solutions:** (http://www.bostondesignsolutions.com/)
  - Schematic and board layout (Mike Bakhtiari, Mike Damiano)
  - Board bringup (Joe Galibois)

- **Review and Feedback:**
  - Gunnar Hillerström

4.4 Attributions

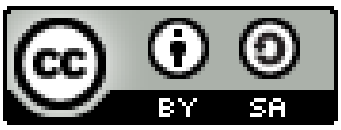
- Warranty notice and Disclaimers based on those found in the Beaglebone Black System Reference Manual Rev A5.2, authored by Gerald Coley of Texas Instruments and published under the Creative Commons Attribution Share-Alike 3.0 Unported License.

- The Parallella project benefited greatly from being able to study the design of the following open board projects:
    - Arduino
    - Beaglebone

- The Parallella project also drew inspiration from the following projects:
    - Zedboard
    - Raspberry Pi

4.5 Licensing

Send all comments and errors concerning this document to andreas@adapteva.com



4.6 Disclaimers

These design materials referred to in this document are ***NOT SUPPORTED*** and **DO NOT** constitute a reference design. Only "community" support is allowed via resources at http://forums.parallella.org

THERE IS NO WARRANTY FOR THE DESIGN MATERIALS DESCRIBED IN THIS REFERENCE MANUAL, TO THE EXTENT PERMITTED BY APPLICABLE LAW. EXCEPT WHEN OTHERWISE STATED IN WRITING THE COPYRIGHT HOLDERS AND/OR OTHER PARTIES PROVIDE THE DESIGN MATERIALS "AS IS" WITHOUT WARRANTY OF ANY KIND, EITHER EXPRESSED OR IMPLIED, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. THE ENTIRE RISK AS TO THE QUALITY AND PERFORMANCE OF THE DESIGN MATERIALS IS WITH YOU. SHOULD THE DESIGN MATERIALS PROVE DEFECTIVE, YOU ASSUME THE COST OF ALL NECESSARY SERVICING, REPAIR OR
CORRECTION

This Parallella board was designed as an evaluation and development tool. It was not designed with any other application in mind. As such, these design materials may or may not be suitable for any other purposes. If used, the design material becomes your responsibility as to whether or not it meets your specific needs or your specific applications and may require changes to meet your requirements.

For Feasibility Evaluation Only, in Laboratory/Development Environments: The Parallella Board is not a complete product. It is intended solely for use for preliminary feasibility evaluation in laboratory/development environments by technically qualified electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems and subsystems. It should not be used as all or part of a finished end product.

Your Sole Responsibility and Risk you acknowledge, represent, and agree that:

1. You have unique knowledge concerning Federal, State and local regulatory requirements (including but not limited to Food and Drug Administration regulations, if applicable) which relate to your products and which relate to your use (and/or that of your employees, affiliates, contractors or designees) of the Parallella for evaluation, testing and other purposes.
2. You have full and exclusive responsibility to assure the safety and compliance of your products with all such laws and other applicable regulatory requirements, and also to

assure the safety of any activities to be conducted by you and/or your employees, affiliates, contractors or designees, using the Parallella. Further, you are responsible to assure that any interfaces (electronic and/or mechanical) between the\Parallella and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard.

3. Since the Parallella is not a completed product, it may not meet all applicable regulatory and safety compliance standards which may normally be associated with similar items. You assume full responsibility to determine and/or assure compliance with any such standards and related certifications as may be applicable. You will employ reasonable safeguards to ensure that your use of the Parallella will not result in any property damage, injury or death, even if the Parallella should fail to perform as described or expected.

Certain Instructions: It is important to operate the Parallella Black within Supplier's recommended specifications and environmental considerations per the user guidelines. Exceeding the specified Parallella ratings (including but not limited to input and output voltage, current, power, and environmental ranges) may cause property damage, personal injury or death. If there are questions concerning these ratings please contact the Supplie representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may result in unintended and/or inaccurate operation and/or possible permanent damage to the Parallella and/or interface electronics. Please consult the System Reference Manual prior to connecting any load to the Parallella output. If there is uncertainty as to the load specification, please contact the Supplier representative. During normal operation, some circuit components may have case temperatures greater than 60 C as long as the input and output are maintained at a normal ambient operating temperature. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors which can be identified using the Parallella schematic located at the link in the Parallella System Reference Manual. When placing measurement probes near these devices during normal operation, please be aware that these devices may be very warm to the touch. As with all electronic evaluation tools, only qualified personnel knowledgeable in electronic measurement and diagnostics normally found in development environments should use the Parallella.

Agreement to Defend, Indemnify and Hold Harmless: You agree to defend, indemnify and hold the Suppliers, its licensors and their representatives harmless from and against any and all claims, damages, losses, expenses, costs and liabilities (collectively, "Claims") arising out of or in connection with any use of the Parallella that is not in accordance with the terms of the agreement. This obligation shall apply whether Claims arise under law of tort or contract or any other legal theory, and even if the Parallella fails to perform as described or expected.

Safety-Critical or Life-Critical Applications: If you intend to evaluate the components for possible use in safety critical applications (such as life support) where a failure of the Supplier's product would reasonably be expected to cause severe personal injury or death, such as devices which are classified as FDA Class III or similar classification, then you must specifically notify Suppliers of such intent and enter into a separate Assurance and Indemnity Agreement.

4.7 Warranty

Parallella.org and Adapteva, Inc (Supplier) provide the Parallella board under the following conditions:

- The user assumes all responsibility and liability for proper and safe handling of the goods. Further, the user indemnifies Supplier from all claims arising from the handling or use of the goods.
- Should the Parallella not meet the specifications indicated in the Parallella Reference Manual, the Parallella may be returned within 90 days from the date of delivery to the distributor of purchase for a full refund.

THE FOREGOING LIMITED WARRANTY IS THE EXCLUSIVE WARRANTY MADE BY SELLER TO BUYER AND IS IN LIEU OF ALL OTHER WARRANTIES, EXPRESSED, IMPLIED, OR STATUTORY, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PARTICULAR PURPOSE. EXCEPT TO THE EXTENT OF THE INDEMNITY SET FORTH ABOVE, NEITHER PARTY SHALL BE LIABLE TO THE OTHER FOR ANY INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES.

For up to date board information, please refer to:
http://github.com/parallella/parallella-hw

All support for this board is provided via community support at
http://forums.parallella.org

Before returning the board, please request an RMA at:
www.parallella.org/support/rma

Please DO NOT return the board without approval from the Parallella RMA team first. All boards received without RMA approval will not be worked on.