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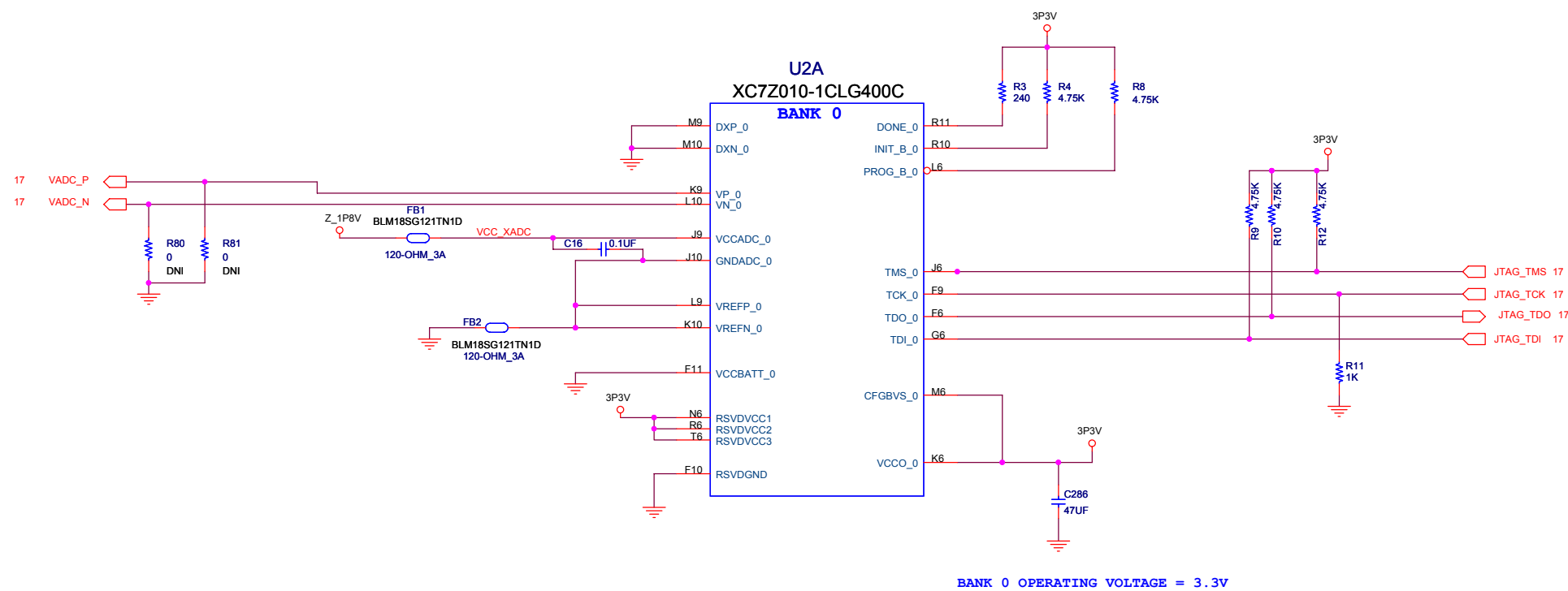
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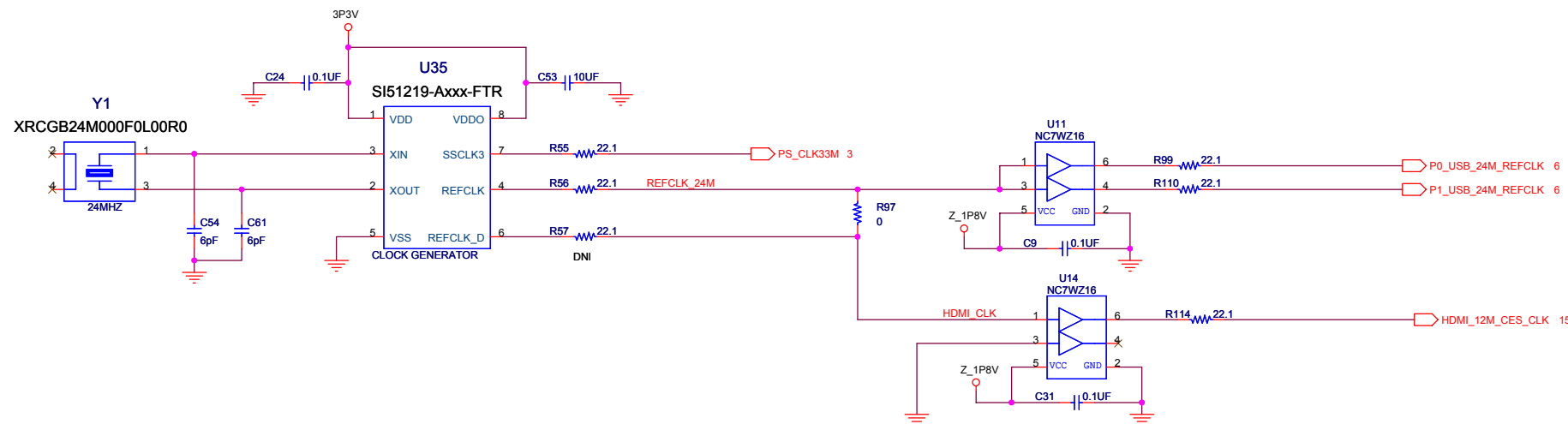
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# ZYNQ BANK0



## PROGRAMMABLE CLOCK GENERATOR

Place Close to U2

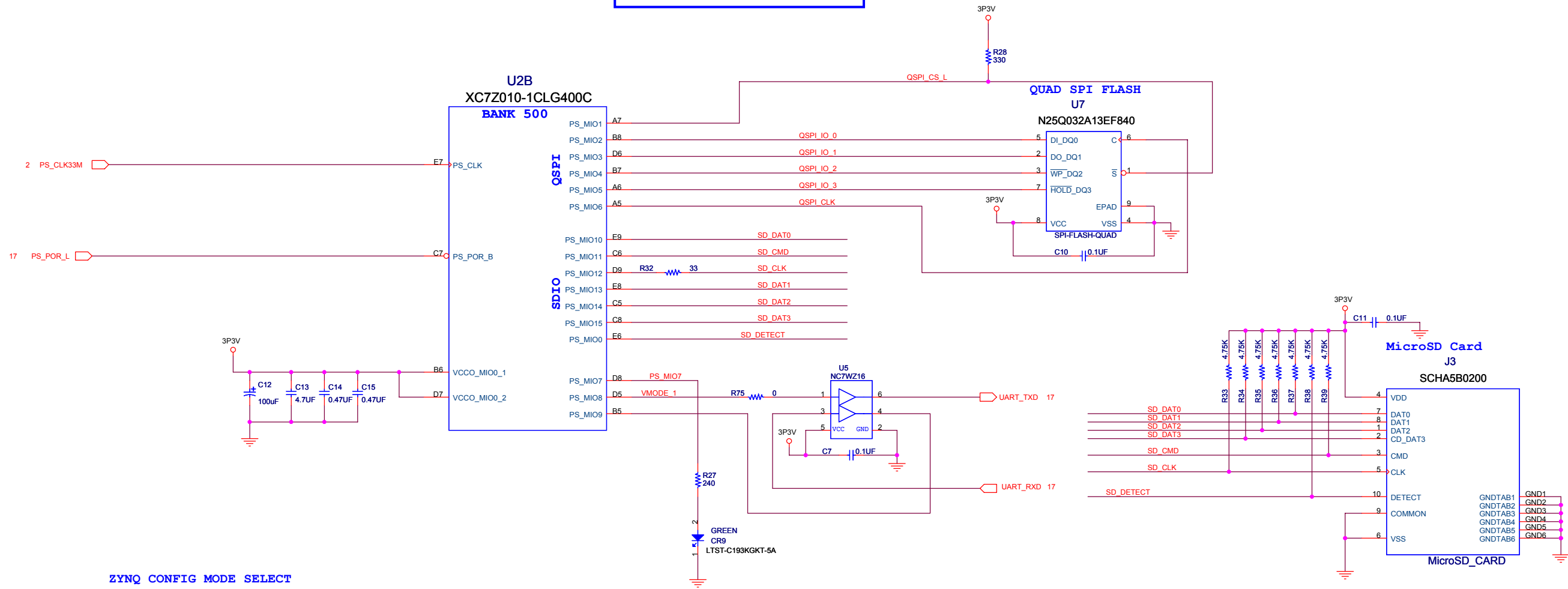


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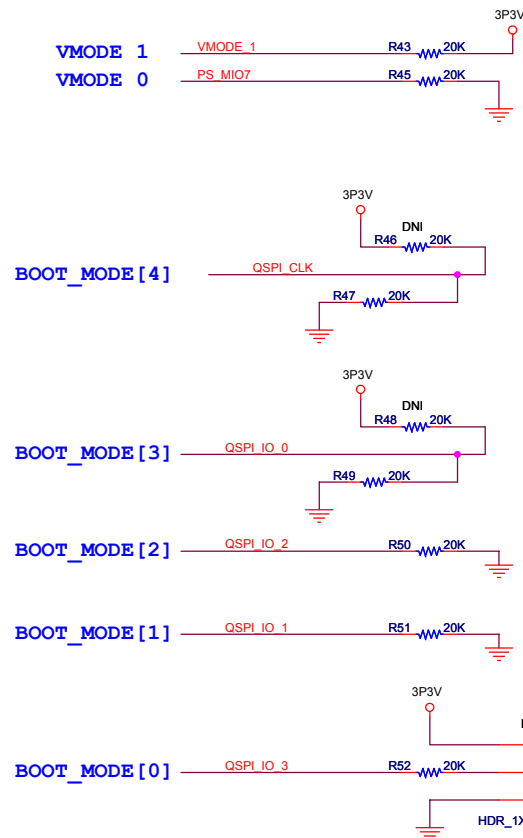
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ZYNQ BANK 500



ZYNQ CONFIG MODE SELECT

Layout Note:  
Limit the Stub length to less than 10mm



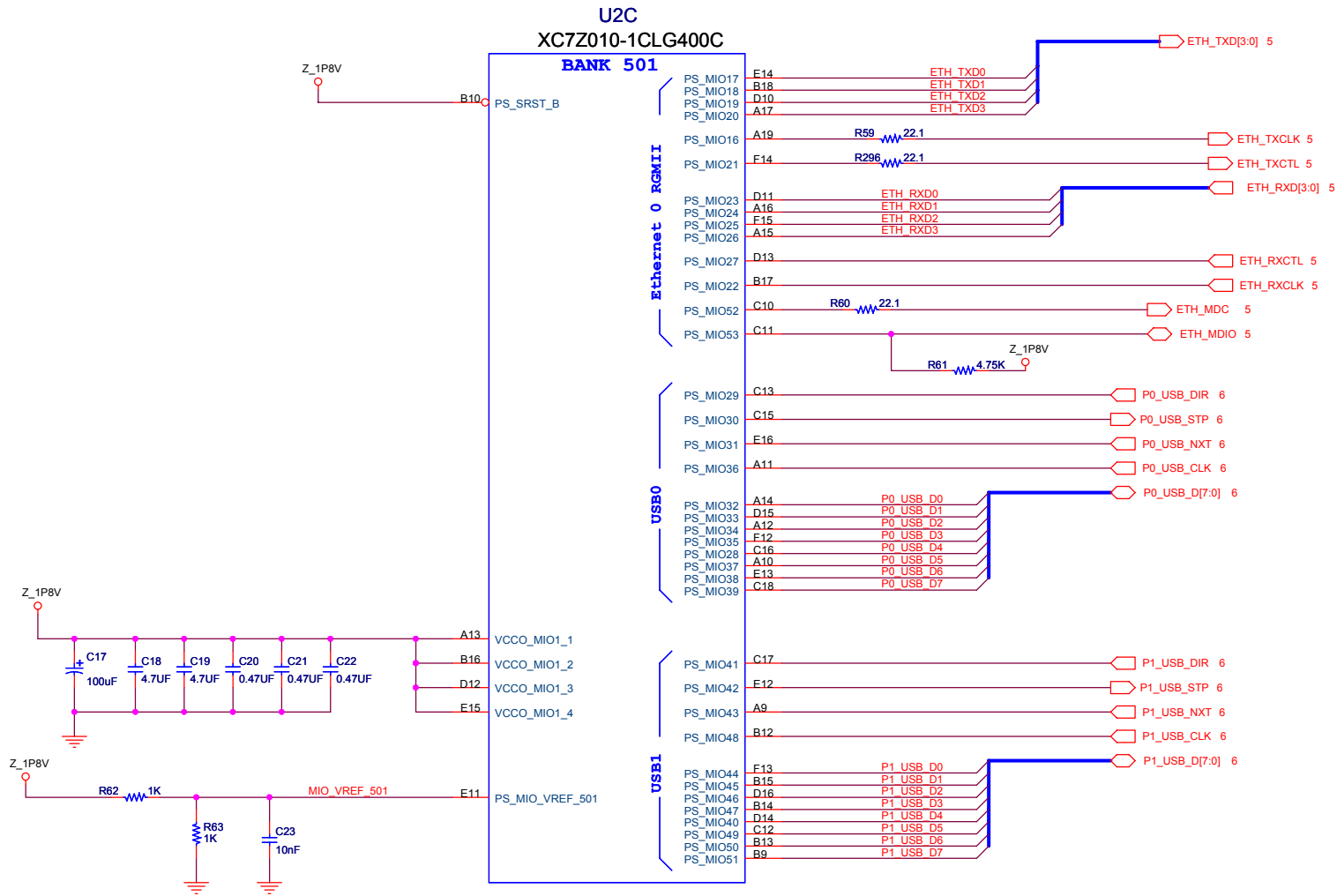
VMODE 1 = 0 -----> MIO Bank 1 Voltage = 1.8V  
VMODE 0 = 0 -----> MIO Bank 0 Voltage = 3.3V

BOOT\_MODE4 = 1 -----> PLL Bypassed  
BOOT\_MODE4 = 0 -----> PLL Used

BOOT\_MODE3 = 1 -----> Independant JTAG  
BOOT\_MODE3 = 0 -----> Cascaded JTAG

BOOT_MODE[0]	BOOT_MODE[1]	BOOT_MODE[2]	BOOT_MODE[3]	
0	0	0	0	Boot from JTAG
1	0	0	x	Boot from QSPI

ZYNQ BANK 501



1.8V Interface IO

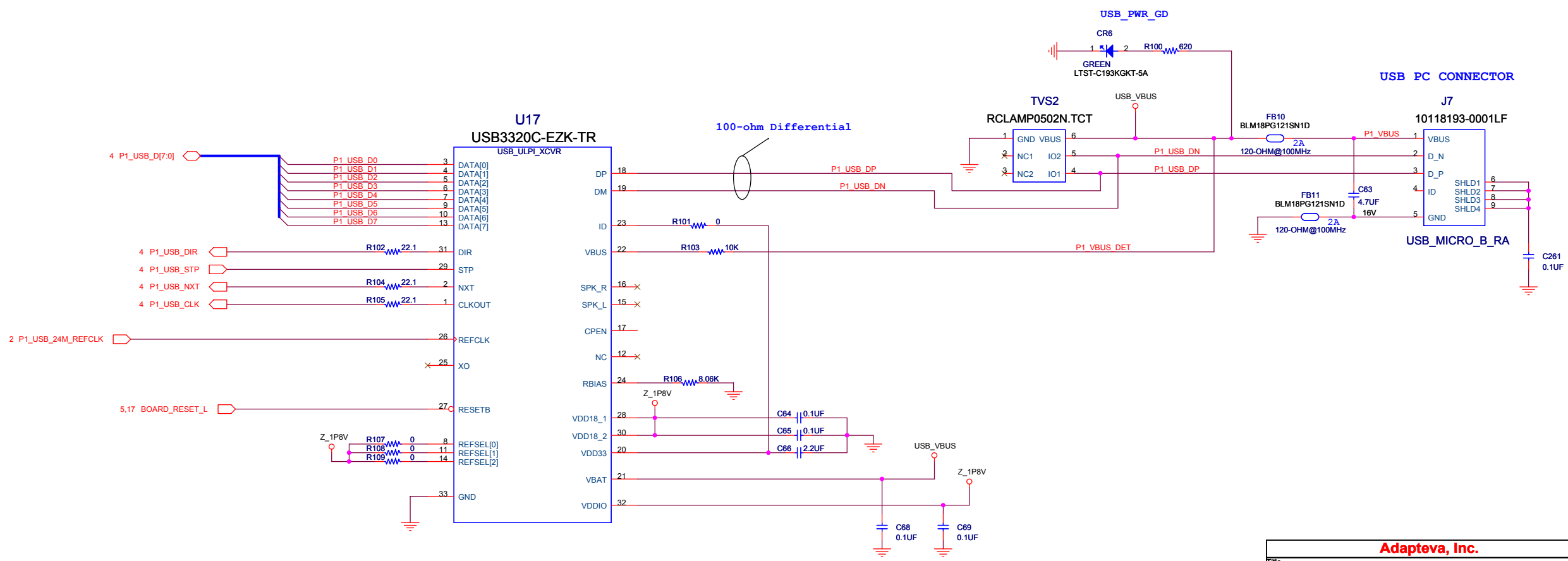
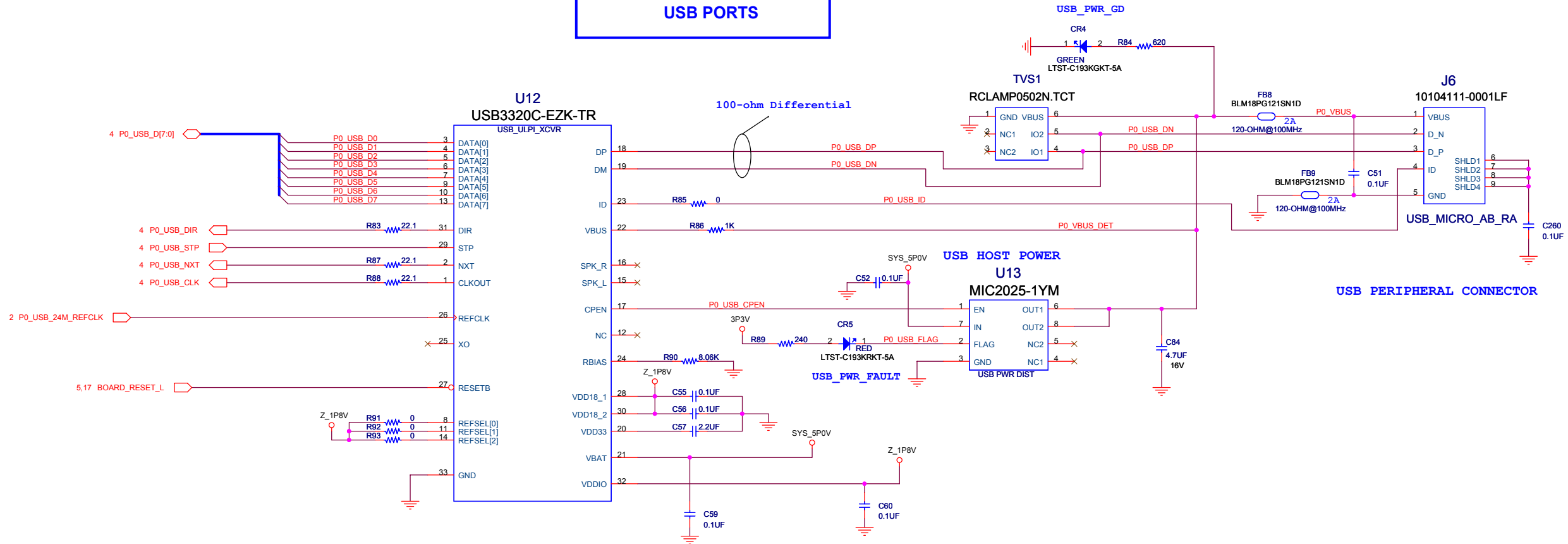
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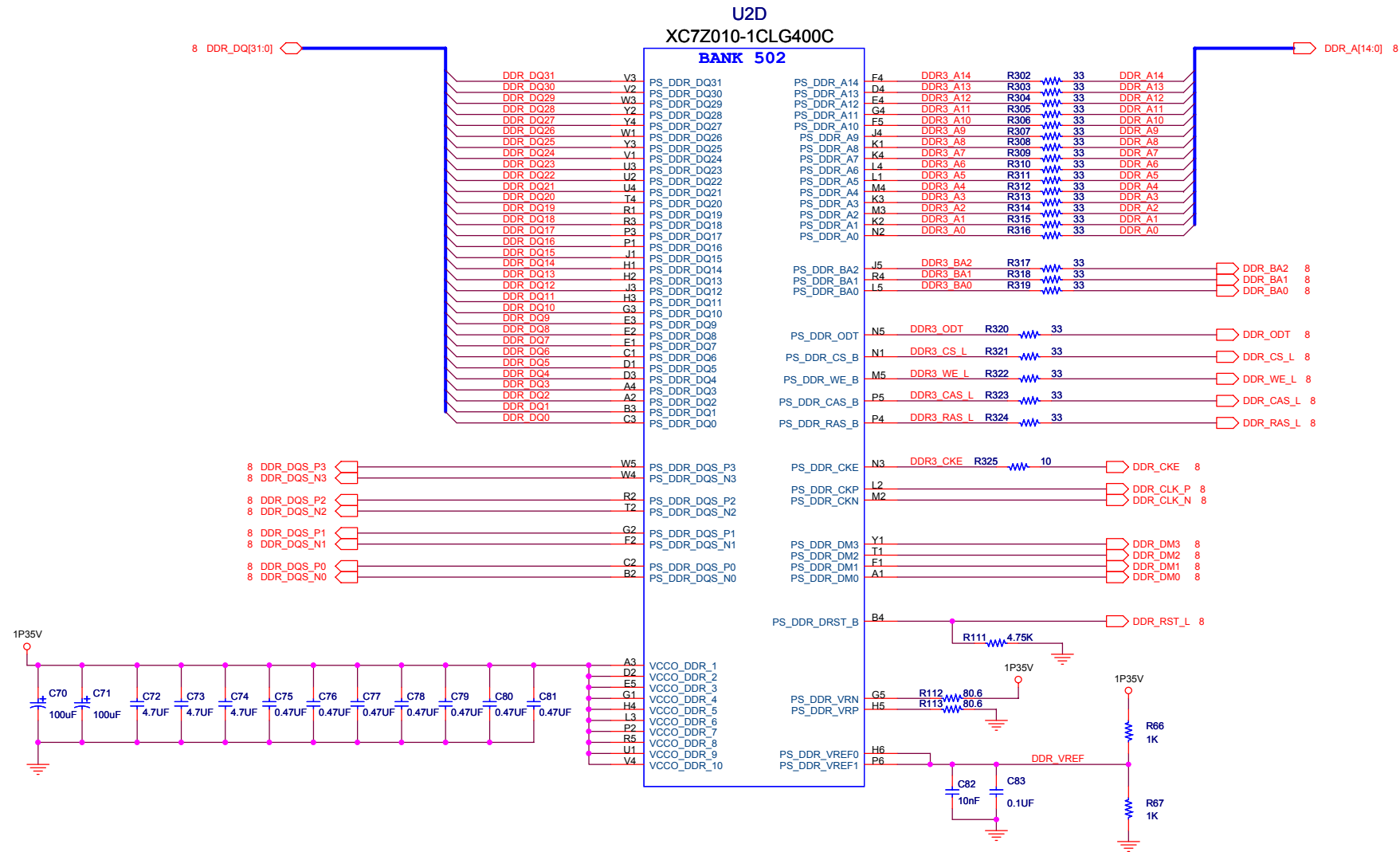
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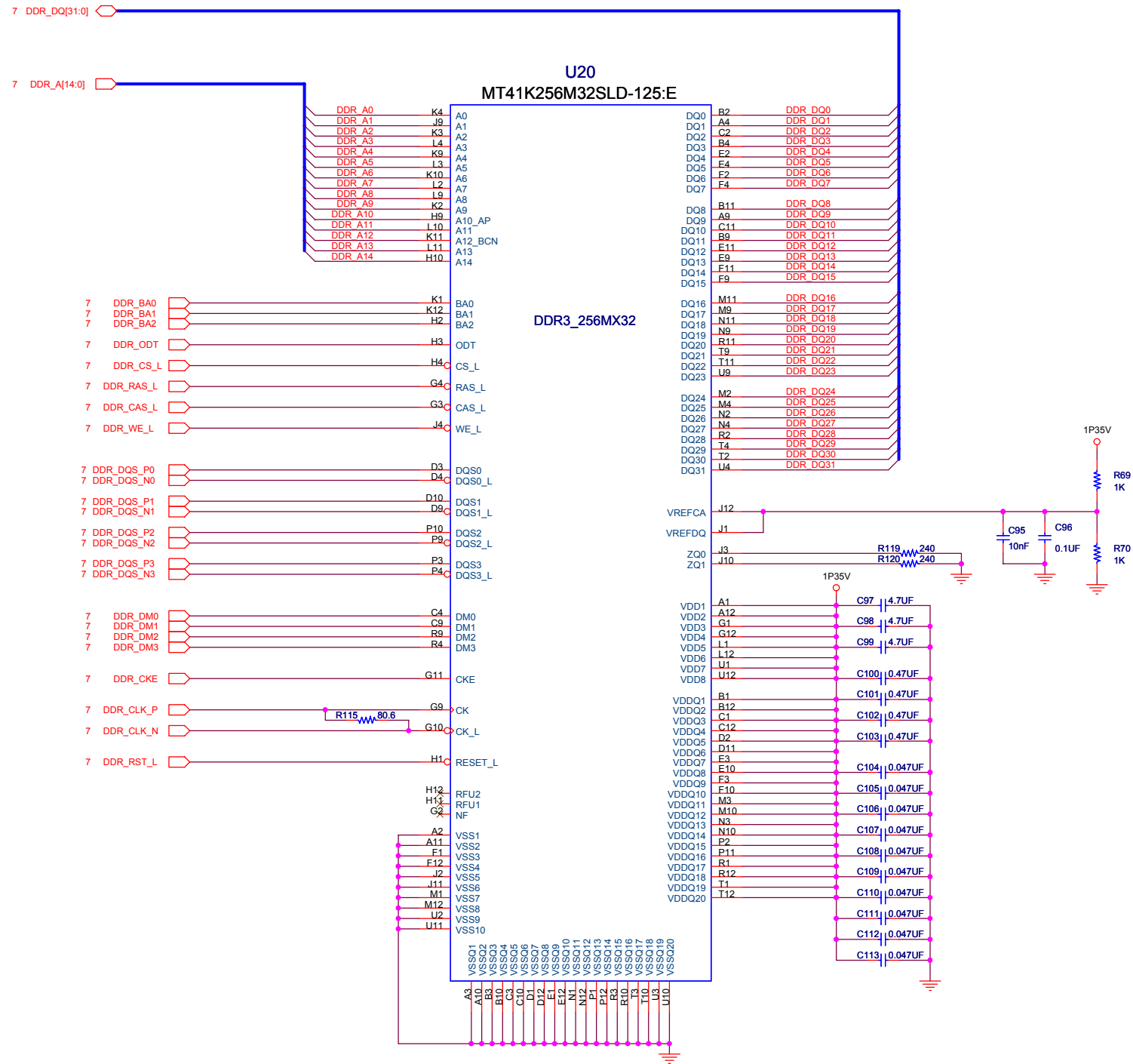
# USB PORTS



## ZYNQ BANK 502



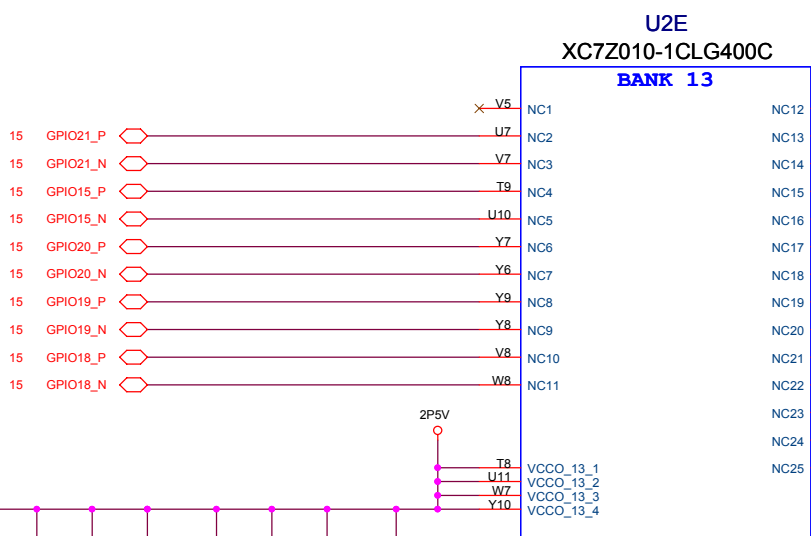
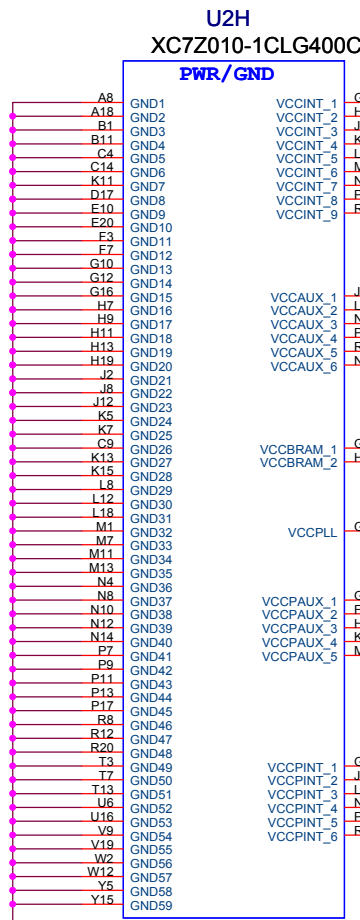
DDR3 - 256M X 32



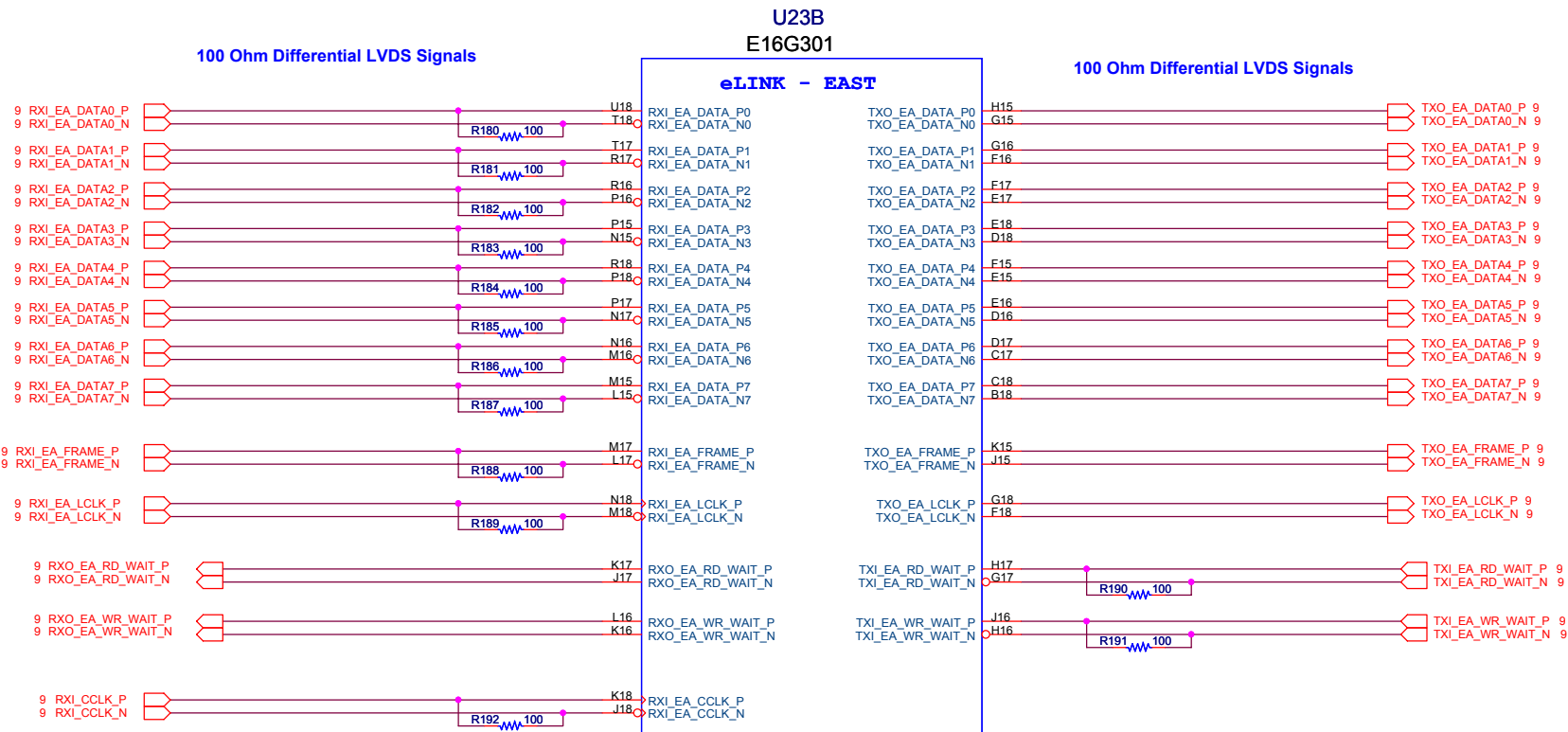
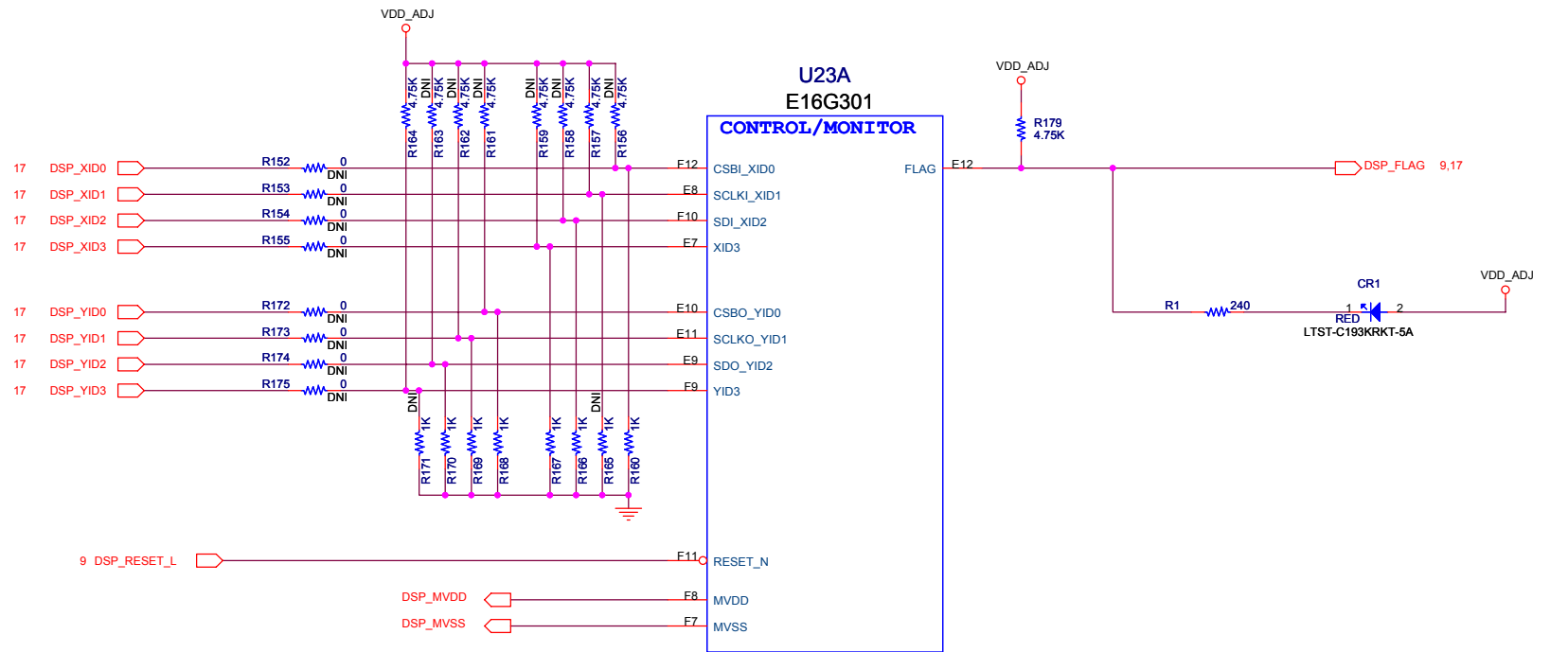




## ZYNQ POWER & GROUND



DSP PROCESSOR 1-OF-3

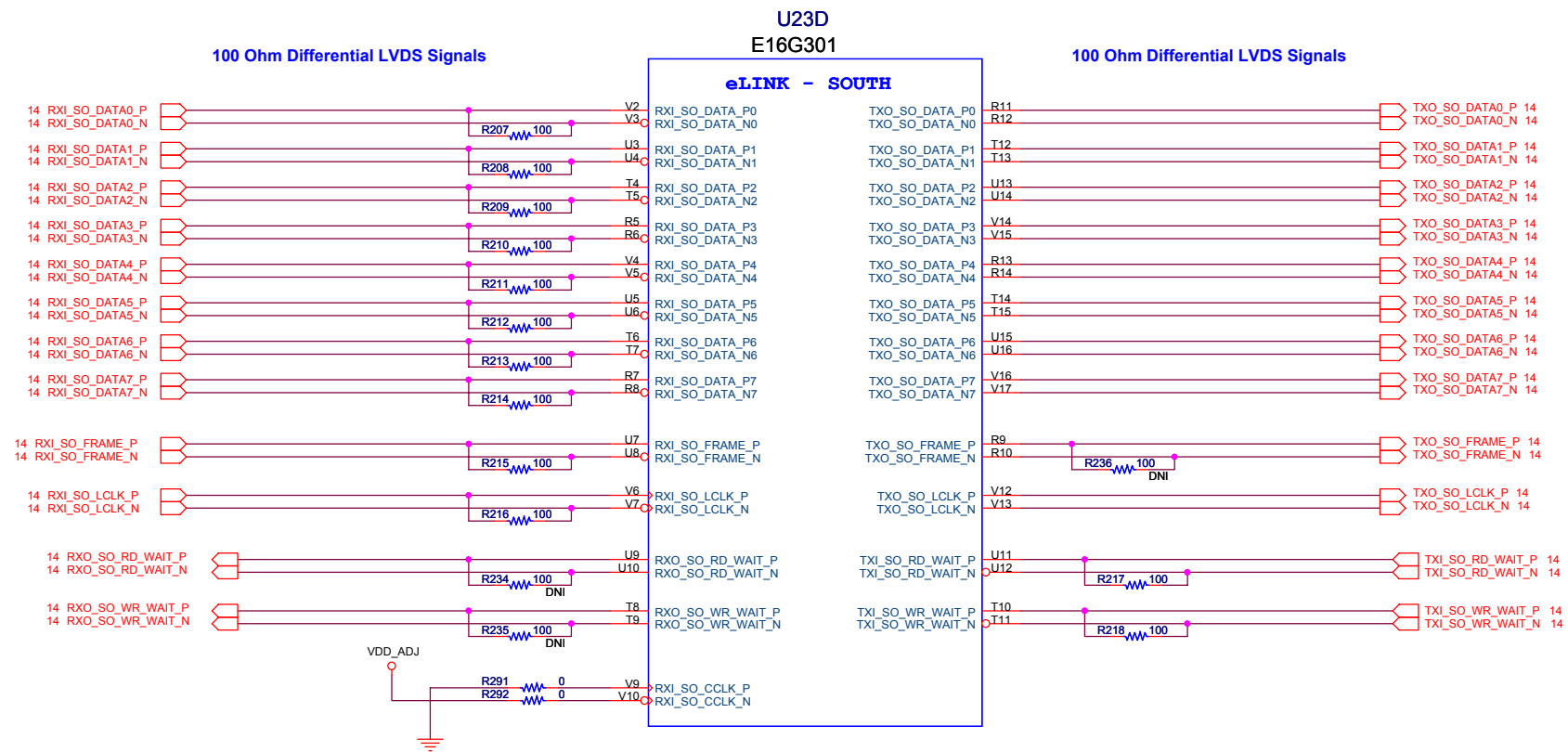
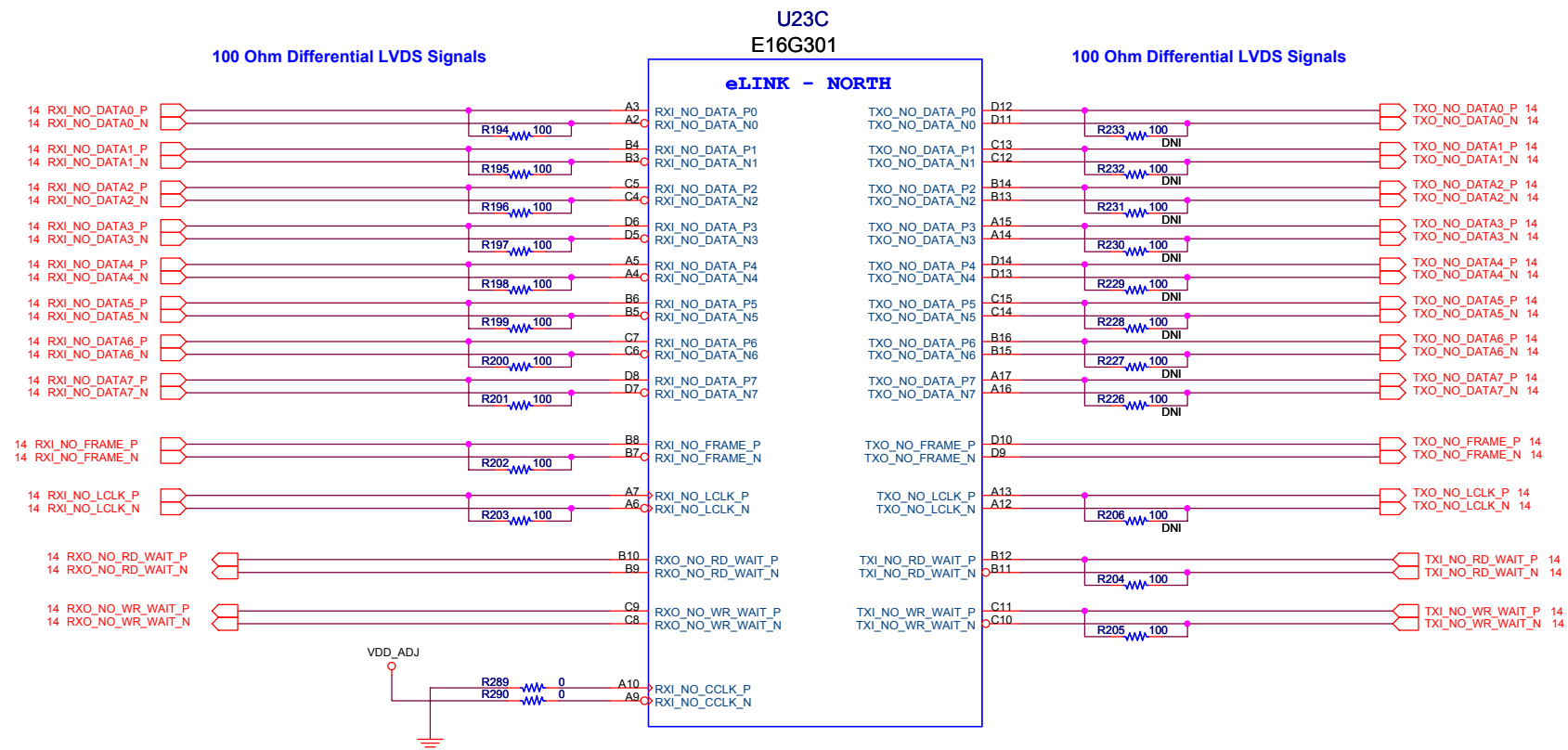


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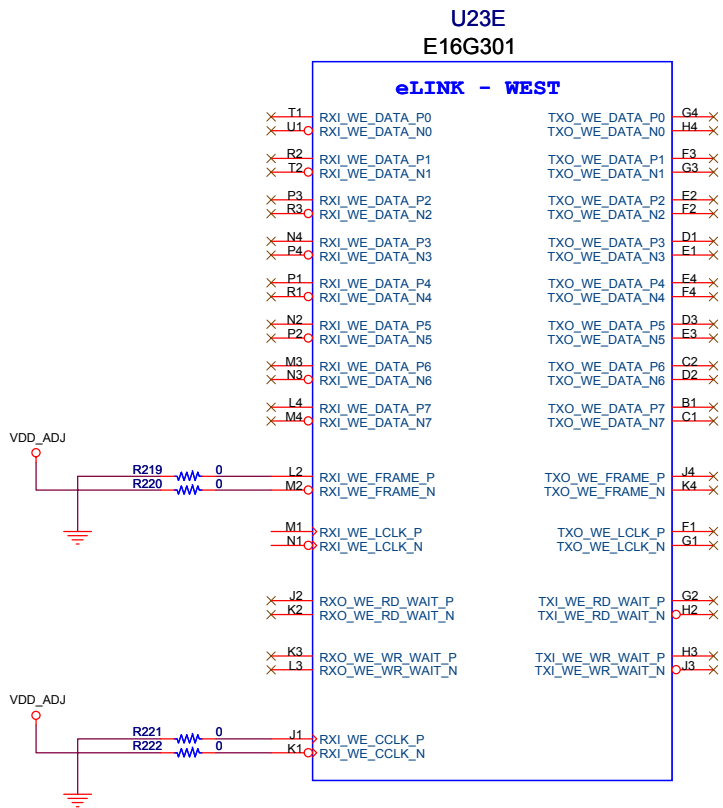
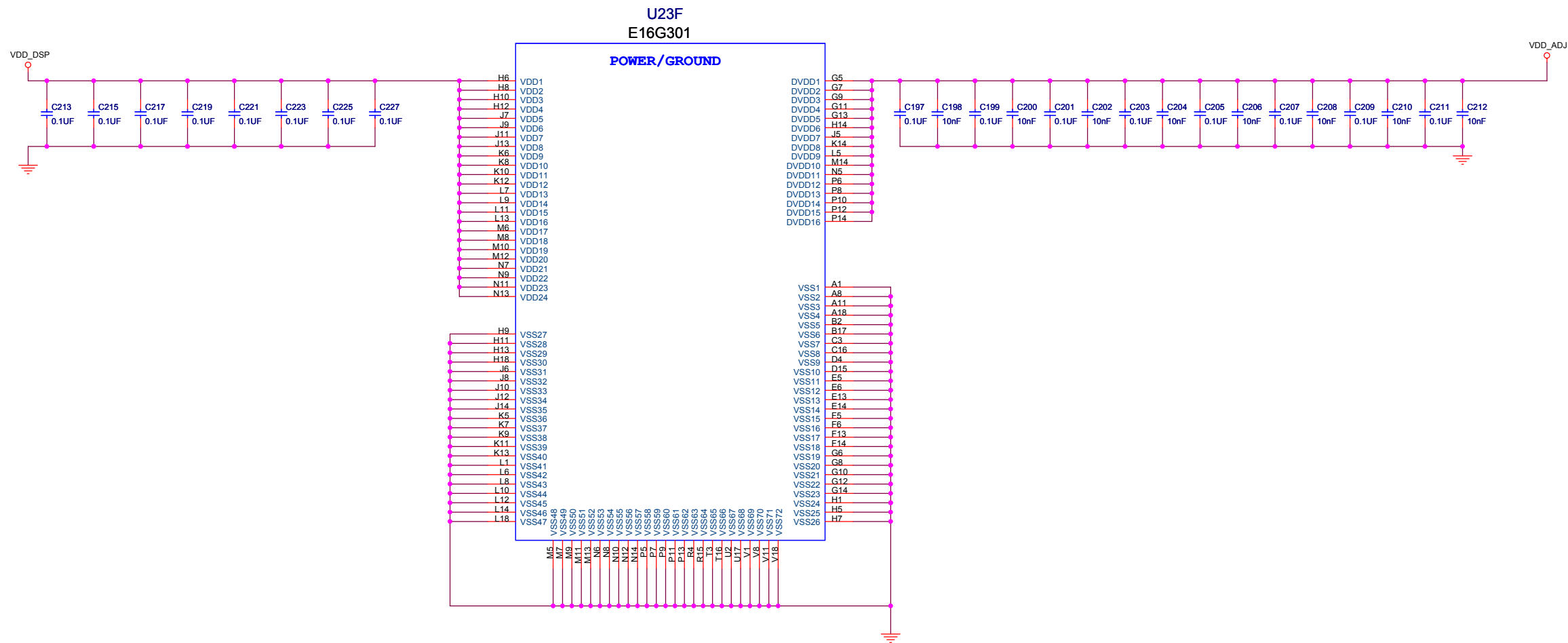
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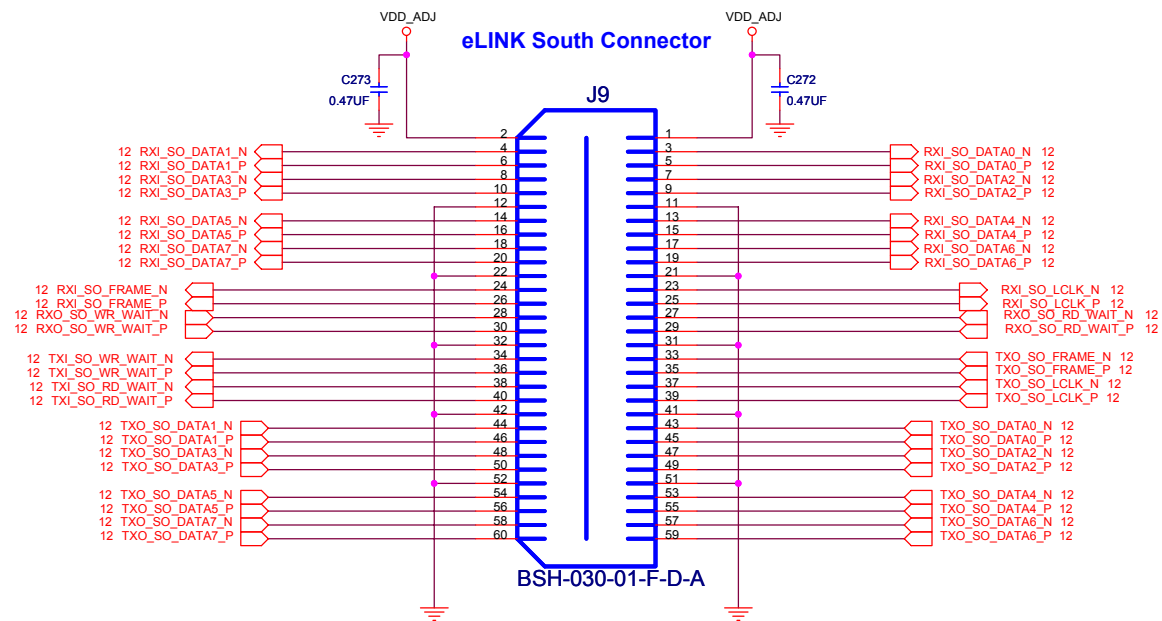
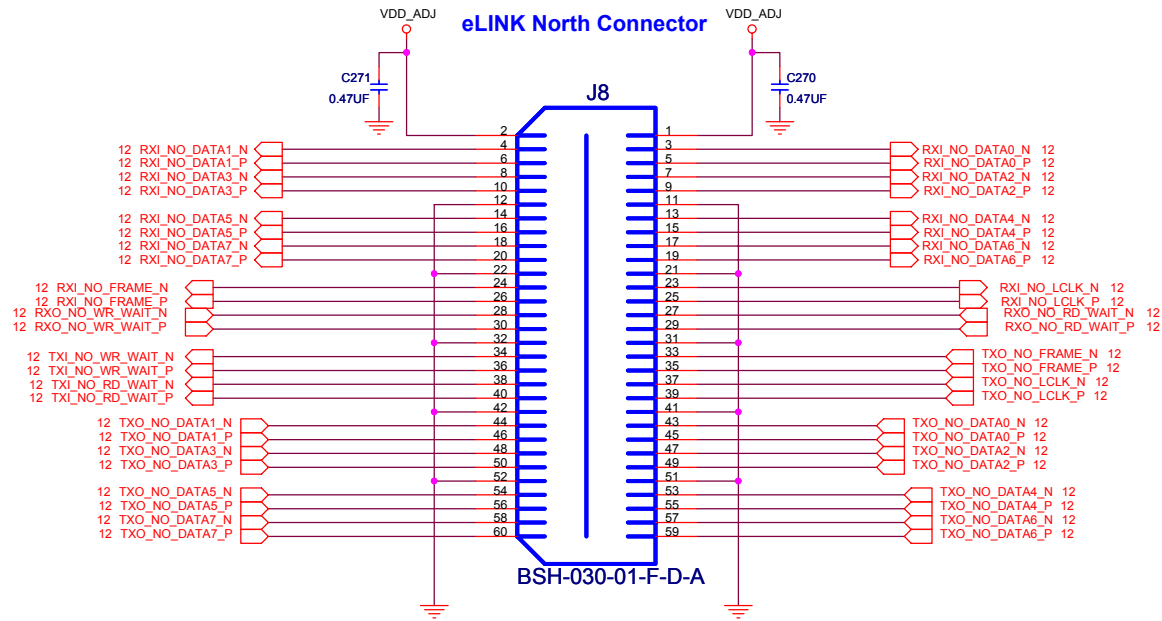
## DSP PROCESSOR 2-OF-3



DSP PROCESSOR 3-OF-3



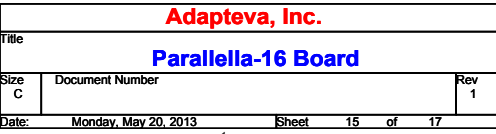
DSP eLINK CONNECTORS



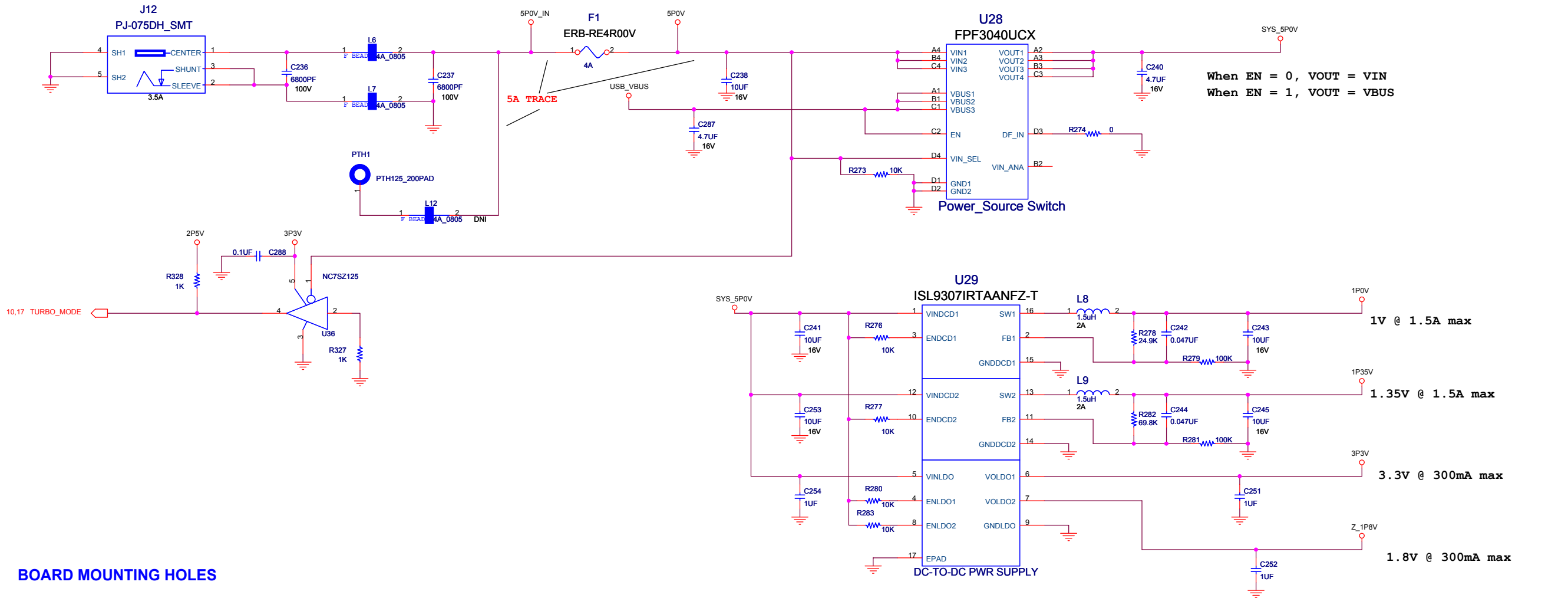
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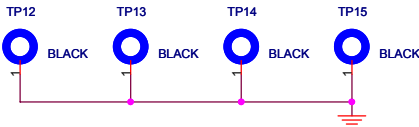
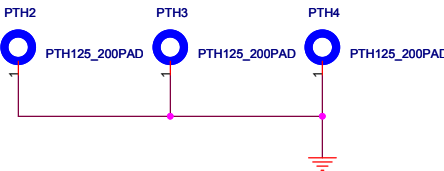
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# POWER MANAGEMENT



## BOARD MOUNTING HOLES



Place in 4 quadrants of the board

Could be removed for production

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RESET GENERATION

