COVER PAGE

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This schematic is *NOT SUPPORTED* and DOES NOT constitute a reference design.
Only *community* support is allowed via resources at forums.parallella.org.

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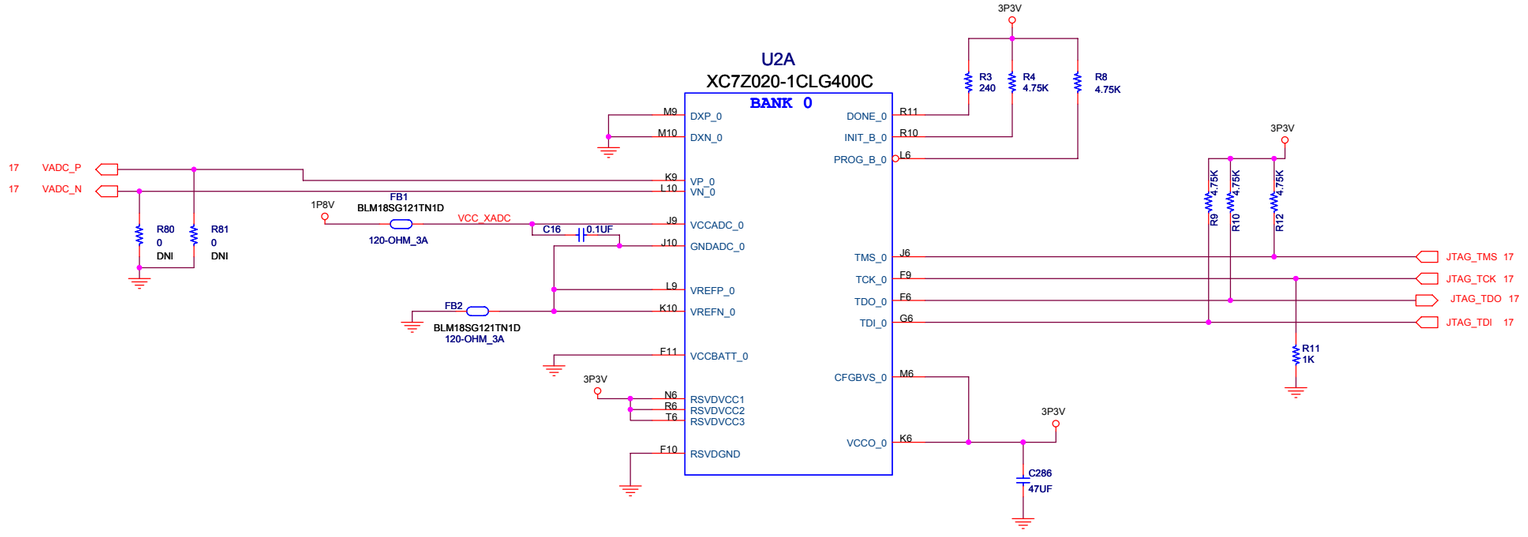
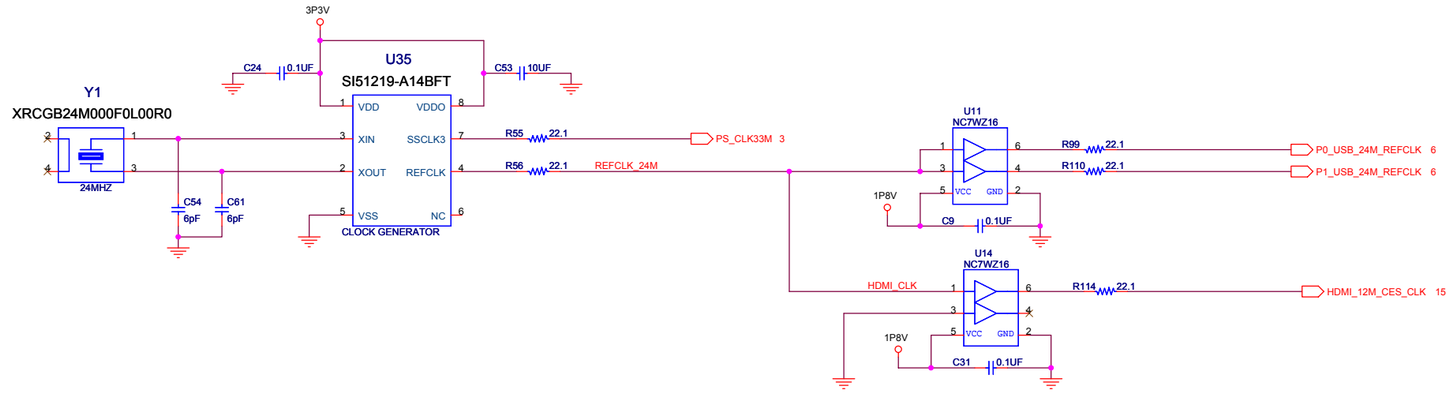
ZYNQ BANK0



BANK 0 OPERATING VOLTAGE = 3.3V

PROGRAMMABLE CLOCK GENERATOR

Place Close to U2



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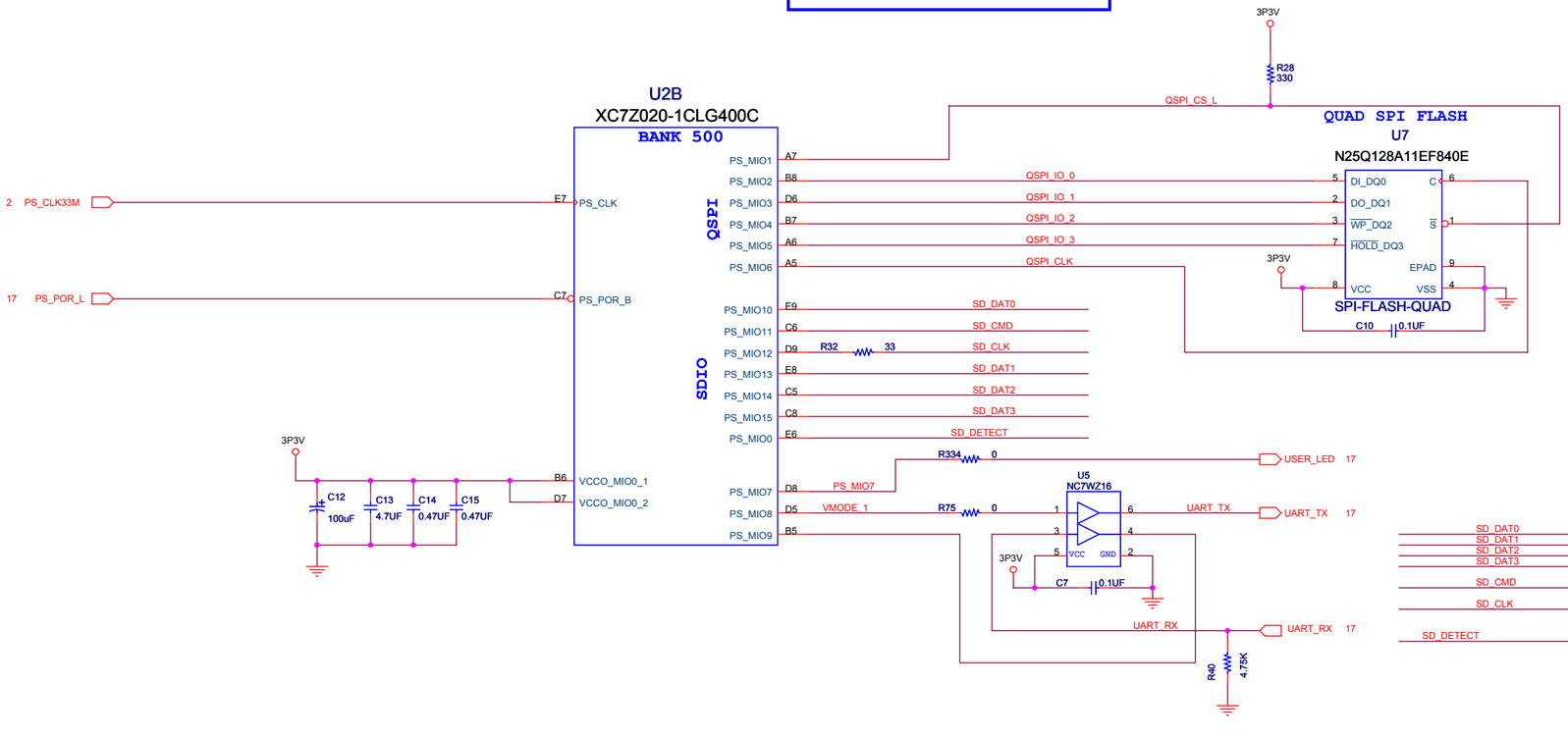
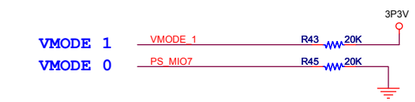
ZYNQ BANK 500

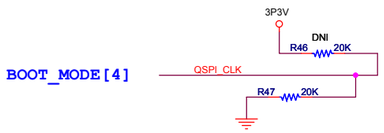


ZYNQ CONFIG MODE SELECT

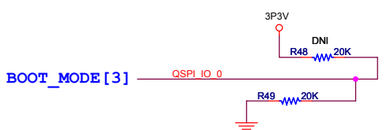
Layout Note:
Limit the Stub length to less than 10mm



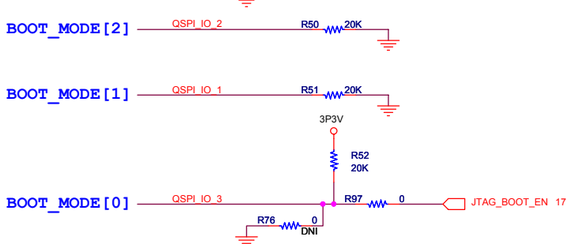
VMODE 1 = 0 --------> MIO Bank 1 Voltage = 1.8V
VMODE 0 = 0 --------> MIO Bank 0 Voltage = 3.3V



BOOT_MODE4 = 1 ---------> PLL Bypassed
BOOT_MODE4 = 0 ---------> PLL Used



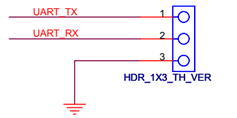
BOOT_MODE3 = 1 ---------> Independant JTAG
BOOT_MODE3 = 0 ---------> Cascaded JTAG



BOOT_MODE[0]	BOOT_MODE[1]	BOOT_MODE[2]	BOOT_MODE[3]	
0	0	0	0	Boot from JTAG
1	0	0	x	Boot from QSPI

UART HEADER

J2
PBC36SAAN



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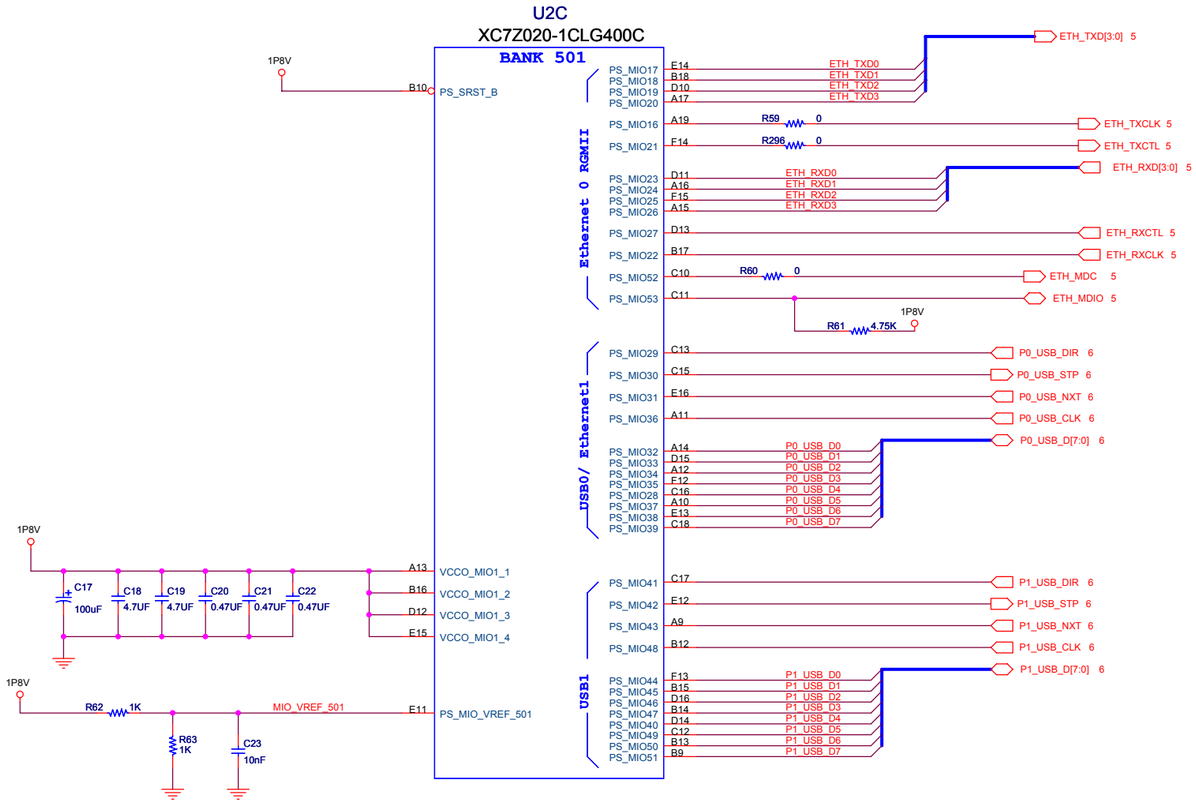
ZYNQ BANK 501



1.8V Interface IO

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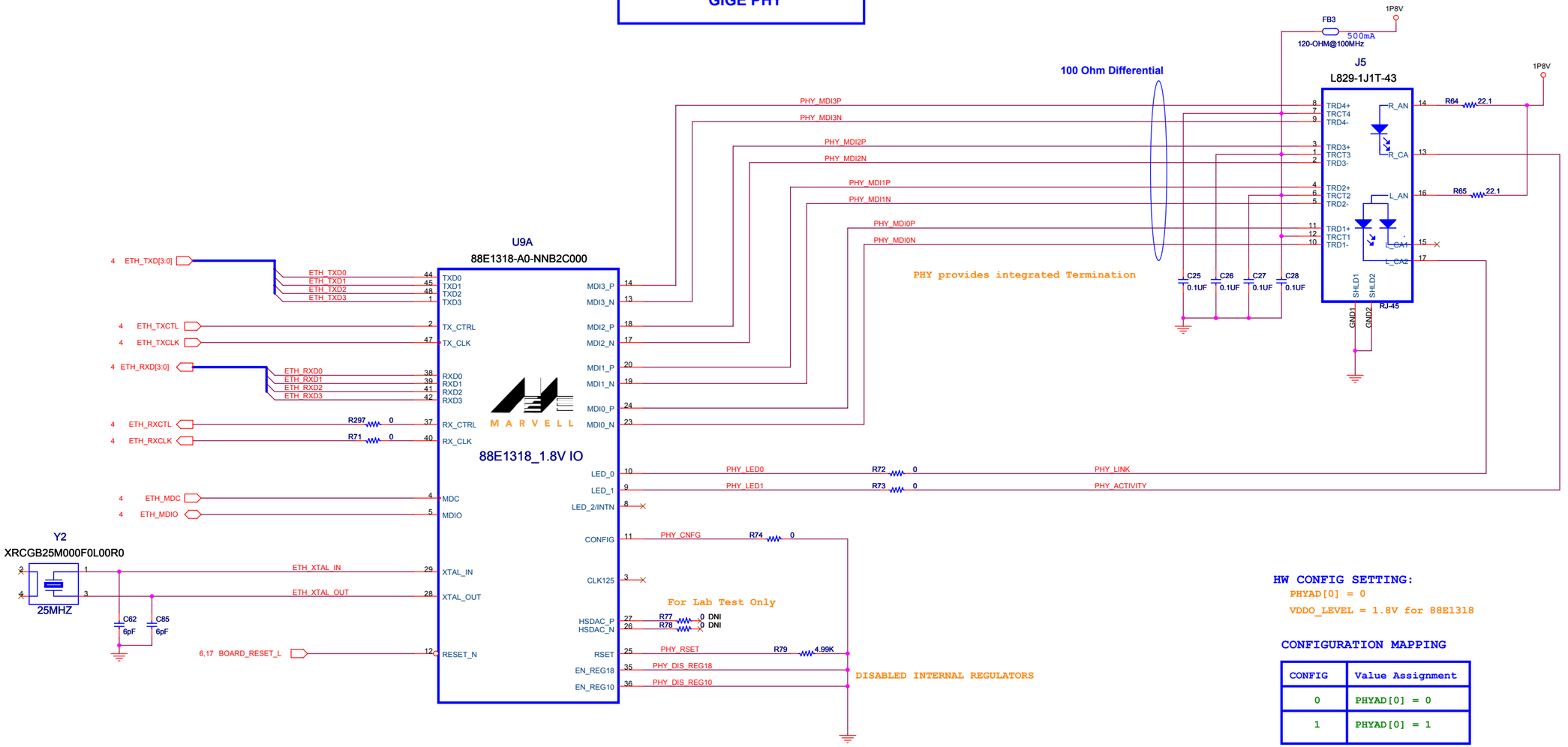
GIGE PHY



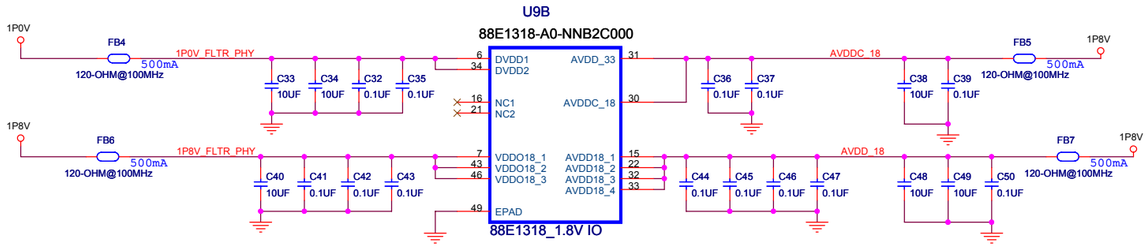
HW CONFIG SETTING:

PHYAD[0] = 0

VDDO_LEVEL = 1.8V for 88E1318

CONFIGURATION MAPPING

CONFIG	Value Assignment
0	PHYAD[0] = 0
1	PHYAD[0] = 1



USB PORTS

U12 — USB3320C-EZK-TR (USB_ULPI_XCVR)

4 P0_USB_D[7:0] → P0_USB_D0..D7 → DATA[0]..DATA[7]

4 P0_USB_DIR → R83 0 → DIR
4 P0_USB_STP → STP
4 P0_USB_NXT → R87 0 → NXT
4 P0_USB_CLK → R88 0 → CLKOUT
2 P0_USB_24M_REFCLK → REFCLK
XO
5,17 BOARD_RESET_L → RESETB
1P8V → R91 0, R92 0, R93 0 → REFSEL[0], REFSEL[1], REFSEL[2]
GND

DP ← P0_USB_DP
DM ← P0_USB_DN
ID → R85 0 → P0_USB_ID
VBUS → R86 1K → P0_VBUS_DET
SPK_R, SPK_L, CPEN → P0_USB_CPEN, NC
RBIAS → R90 8.06K
VDD18_1 → C55 0.1UF
VDD18_2 → C56 0.1UF
VDD33 → C57 2.2UF
VBAT ← SYS_5P0V
VDDIO ← 1P8V
C59 0.1UF
C60 0.1UF

100-ohm Differential

USB_PWR_GD
CR4 GREEN LTST-C193KGKT-5A
R84 620

TVS1 RCLAMP0502N.TCT
GND, VBUS, NC1, IO2, NC2, IO1

FB8 BLM18PG121SN1D 2A 120-OHM@100MHz
P0_VBUS

J6 10104111-0001LF
VBUS, D_N, D_P, ID, GND, SHLD1..SHLD4
USB_MICRO_AB_RA

FB9 BLM18PG121SN1D 2A 120-OHM@100MHz
C51 0.1UF
C260 0.1UF

USB HOST POWER

U13 MIC2025-1YM
EN, IN, FLAG, GND, OUT1, OUT2, NC2, NC1
USB PWR DIST

SYS_5P0V
C52 0.1UF
3P3V
R89 240
CR5 RED LTST-C193KRKT-5A
P0_USB_FLAG
USB_PWR_FAULT
C84 4.7UF 16V

USB PERIPHERAL CONNECTOR

U17 — USB3320C-EZK-TR (USB_ULPI_XCVR)

4 P1_USB_D[7:0] → P1_USB_D0..D7 → DATA[0]..DATA[7]

4 P1_USB_DIR → R102 0 → DIR
4 P1_USB_STP → STP
4 P1_USB_NXT → R104 0 → NXT
4 P1_USB_CLK → R105 0 → CLKOUT
2 P1_USB_24M_REFCLK → REFCLK
XO
5,17 BOARD_RESET_L → RESETB
1P8V → R107 0, R108 0, R109 0 → REFSEL[0], REFSEL[1], REFSEL[2]
GND

DP ← P1_USB_DP
DM ← P1_USB_DN
ID → R101 0
VBUS → R103 10K → P1_VBUS_DET
SPK_R, SPK_L, CPEN, NC
RBIAS → R106 8.06K
VDD18_1 → C64 0.1UF
VDD18_2 → C65 0.1UF
VDD33 → C66 2.2UF
VBAT ← USB_VBUS
VDDIO ← 1P8V
C68 0.1UF
C69 0.1UF

100-ohm Differential

USB_PWR_GD
CR6 GREEN LTST-C193KGKT-5A
R100 620

TVS2 RCLAMP0502N.TCT
USB_VBUS
GND, VBUS, NC1, IO2, NC2, IO1

FB10 BLM18PG121SN1D 2A 120-OHM@100MHz
P1_VBUS

USB PC CONNECTOR

J7 10118193-0001LF
VBUS, D_N, D_P, ID, GND, SHLD1..SHLD4
USB_MICRO_B_RA

FB11 BLM18PG121SN1D 2A 120-OHM@100MHz
C63 4.7UF 16V
C261 0.1UF

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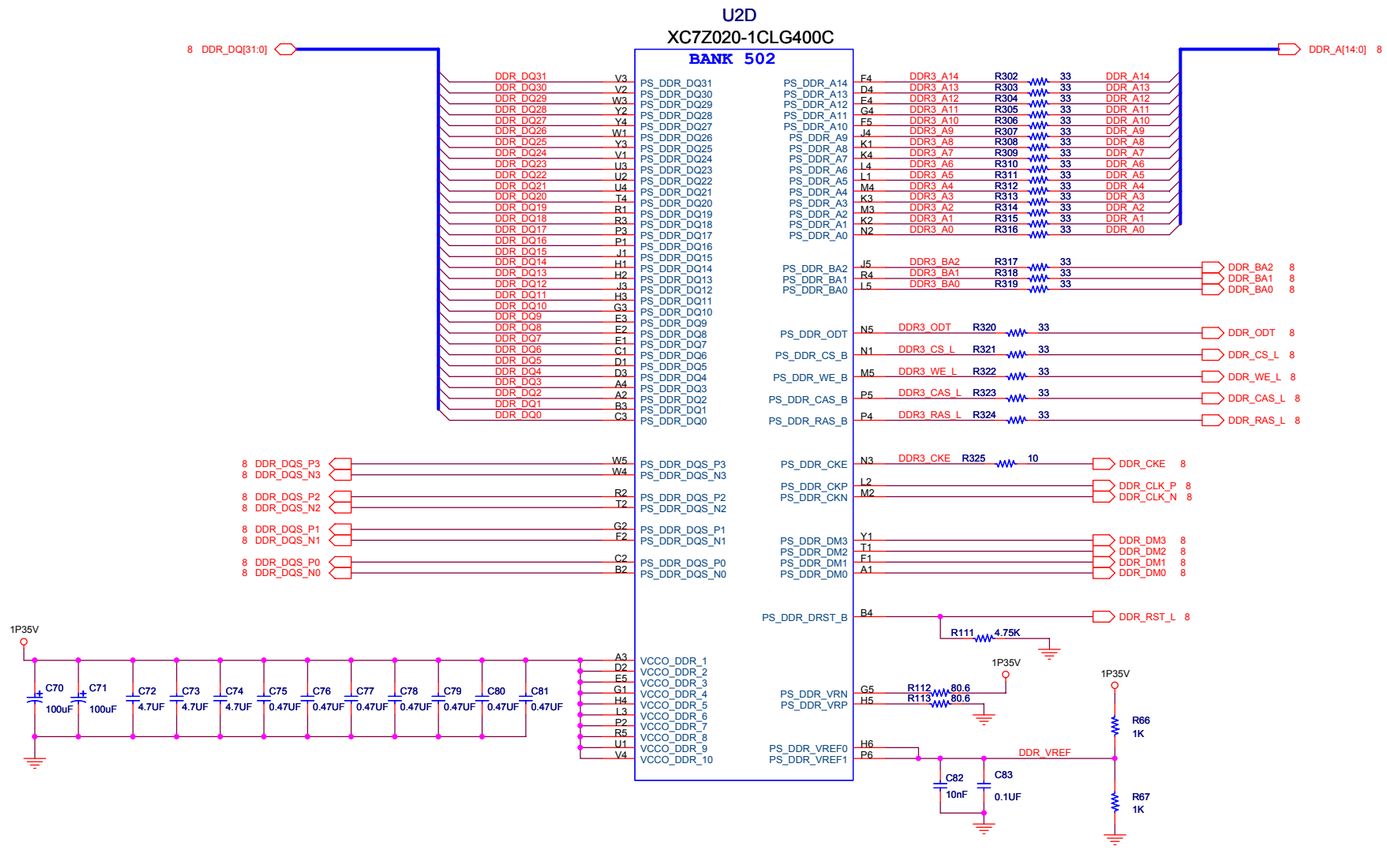
ZYNQ BANK 502



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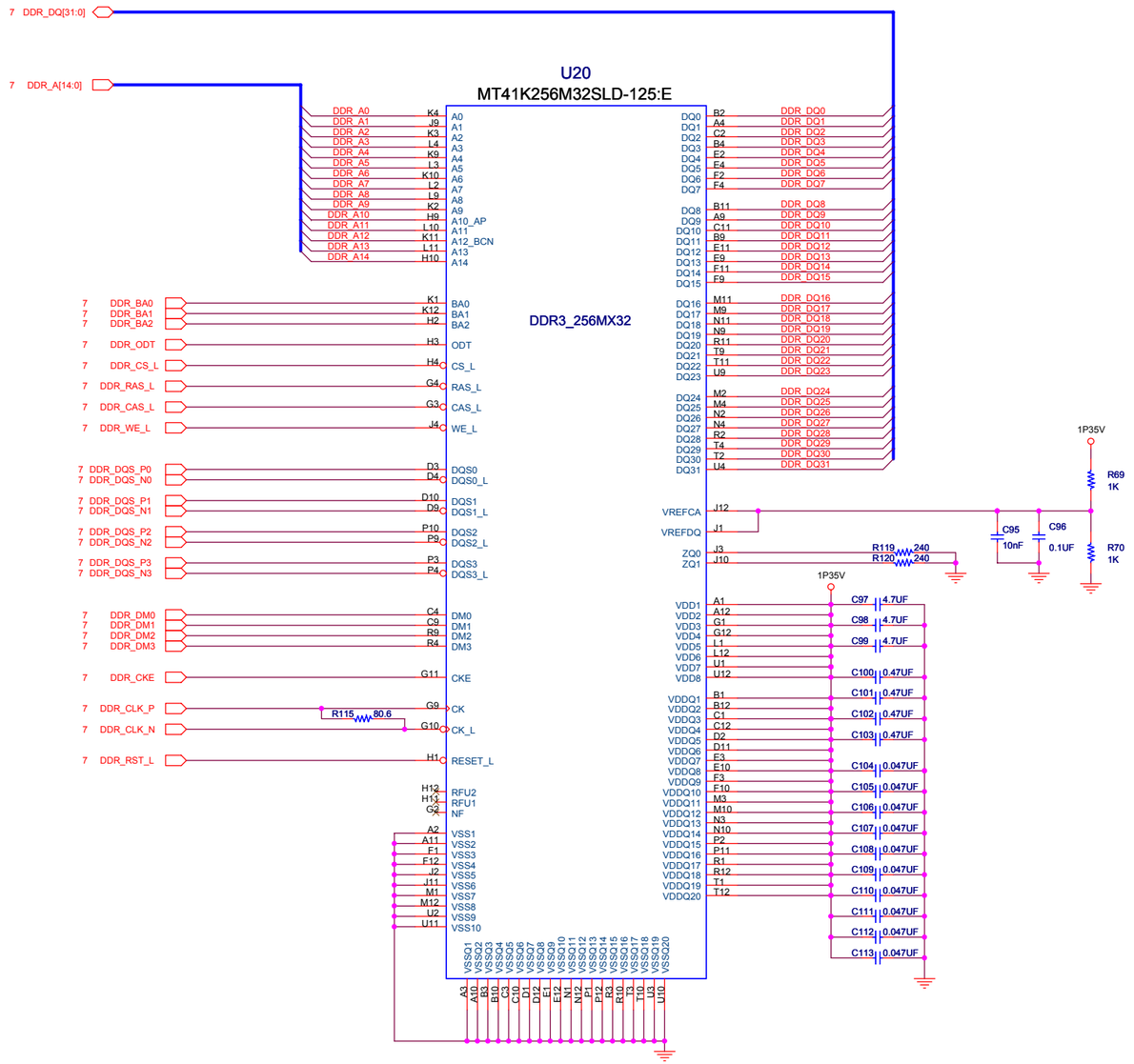
DDR3 - 256M X 32



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BANKS 34 & 35

Enable 100-ohm internal termination on all LVDS inputs

U2F
XC7Z020-1CLG400C

BANK 34

15 HDMI_D[23:8]

HDMI_D18	R19	IO_0_34	IO_25_34	T19	HDMI_D17
15 GPIO11_P	T11	IO_L1P_T0_34	IO_L13P_T2_MRCC_34	N18	
15 GPIO11_N	T10	IO_L1N_T0_34	IO_L13N_T2_MRCC_34	P19	HDMI_D19
15 GPIO10_P	T12	IO_L2P_T0_34	IO_L14P_T2_SRCC_34	N20	
15 GPIO10_N	U12	IO_L2N_T0_34	IO_L14N_T2_SRCC_34	P20	
15 GPIO8_P	U13	IO_L3P_T0_DQS_PUDC_B_34	IO_L15P_T2_DQS_34	T20	HDMI_D23
15 GPIO8_N	V13	IO_L3N_T0_DQS_34	IO_L15N_T2_DQS_34	U20	HDMI_D22
15 GPIO9_P	V12	IO_L4P_T0_34	IO_L16P_T2_34	V20	HDMI_D21
15 GPIO9_N	W13	IO_L4N_T0_34	IO_L16N_T2_34	W20	HDMI_D20
15 GPIO5_P	T14	IO_L5P_T0_34	IO_L17P_T2_34	Y18	HDMI_D8
15 GPIO5_N	T15	IO_L5N_T0_34	IO_L17N_T2_34	Y19	HDMI_D14
15 GPIO4_P	P14	IO_L6P_T0_34	IO_L18P_T2_34	V16	GPIO1_P 15
15 GPIO4_N	R14	IO_L6N_T0_VREF_34	IO_L18N_T2_34	W16	GPIO1_N 15
15,17 SPDIF	22.1 R82 Y16	IO_L7P_T1_34	IO_L19P_T3_34	R16	TURBO_MODE 16,17
15 HDMI_DE	22.1 R94 Y17	IO_L7N_T1_34	IO_L19N_T3_VREF_34	R17	R41 22.1 HDMI_CLK 15
15 GPIO7_P	W14	IO_L8P_T1_34	IO_L20P_T3_34	T17	R44 22.1 HDMI_HSYNC 15
15 GPIO7_N	Y14	IO_L8N_T1_34	IO_L20N_T3_34	R18	HDMI_D12
15 GPIO0_P	T16	IO_L9P_T1_DQS_34	IO_L21P_T3_DQS_34	V17	R42 22.1 HDMI_VSYNC 15
15 GPIO0_N	U17	IO_L9N_T1_DQS_34	IO_L21N_T3_DQS_34	V18	HDMI_D10
15 GPIO3_P	V15	IO_L10P_T1_34	IO_L22P_T3_34	W18	HDMI_D9
15 GPIO3_N	W15	IO_L10N_T1_34	IO_L22N_T3_34	W19	HDMI_D15
15 GPIO6_P	U14	IO_L11P_T1_SRCC_34	IO_L23P_T3_34	N17	R18 4.75K VDD_GPIO PS_I2C_SDA 15
15 GPIO6_N	U15	IO_L11N_T1_SRCC_34	IO_L23N_T3_34	P18	HDMI_D13
HDMI_D11	U18	IO_L12P_T1_MRCC_34	IO_L24P_T3_34	P15	GPIO2_P 15
HDMI_D16	U19	IO_L12N_T1_MRCC_34	IO_L24N_T3_34	P16	GPIO2_N 15

R20 4.75K VDD_GPIO PS_I2C_SCL 15

PROG_IO 17

HDMI_INT 15

R223 1K

VDD_GPIO

N19	VCCO_34_1
R15	VCCO_34_2
T18	VCCO_34_3
V14	VCCO_34_4
W17	VCCO_34_5
Y20	VCCO_34_6

C126 0.47UF, C127 0.47UF, C128 0.47UF, C129 0.47UF, C130 0.47UF, C131 4.7UF, C132 4.7UF, C133 4.7UF, C134 100uF

U2G
XC7Z020-1CLG400C

BANK 35

11 DSP_RESET_L	DSP_RESET_L R178 1K G14	IO_0_35	IO_25_34	J15	RXO_EA_RD_WAIT 11
11 RXI_EA_DATA1_P	C20	IO_L1P_T0_AD0P_35	IO_L13P_T2_MRCC_35	H16	RXI_CCLK_P 13
11 RXI_EA_DATA1_N	B20	IO_L1N_T0_AD0N_35	IO_L13N_T2_MRCC_35	H17	RXI_CCLK_N 13
11 RXI_EA_DATA0_P	B19	IO_L2P_T0_AD8P_35	IO_L14P_T2_AD4P_SRCC_35	J18	RXO_EA_WR_WAIT_P 11
11 RXI_EA_DATA0_N	A20	IO_L2N_T0_AD8N_35	IO_L14N_T2_AD4N_SRCC_35	H18	RXO_EA_WR_WAIT_N 11
11 RXI_EA_DATA4_P	E17	IO_L3P_T0_DQS_AD1P_35	IO_L15P_T2_DQS_AD12P_35	F19	RXI_EA_DATA5_P 11
11 RXI_EA_DATA4_N	D18	IO_L3N_T0_DQS_AD1N_35	IO_L15N_T2_DQS_AD12N_35	F20	RXI_EA_DATA5_N 11
11 RXI_EA_DATA2_P	D19	IO_L4P_T0_35	IO_L16P_T2_35	G17	RXI_EA_DATA6_P 11
11 RXI_EA_DATA2_N	D20	IO_L4N_T0_35	IO_L16N_T2_35	G18	RXI_EA_DATA6_N 11
11 RXI_EA_DATA3_P	E18	IO_L5P_T0_AD9P_35	IO_L17P_T2_AD5P_35	J20	TXO_EA_FRAME_P 11
11 RXI_EA_DATA3_N	E19	IO_L5N_T0_AD9N_35	IO_L17N_T2_AD5N_35	H20	TXO_EA_FRAME_N 11
11 RXI_EA_LCLK_P	F16	IO_L6P_T0_35	IO_L18P_T2_AD13P_35	G19	RXI_EA_DATA7_P 11
11 RXI_EA_LCLK_N	F17	IO_L6N_T0_VREF_35	IO_L18N_T2_AD13N_35	G20	RXI_EA_DATA7_N 11
11 TXO_EA_DATA5_P	M19	IO_L7P_T1_AD2P_35	IO_L19P_T3_35	H15	RXI_EA_FRAME_P 11
11 TXO_EA_DATA5_N	M20	IO_L7N_T1_AD2N_35	IO_L19N_T3_VREF_35	G15	RXI_EA_FRAME_N 11
11 TXO_EA_DATA6_P	M17	IO_L8P_T1_AD10P_35	IO_L20P_T3_AD6P_35	K14	TXI_EA_RD_WAIT_P 11
11 TXO_EA_DATA6_N	M18	IO_L8N_T1_AD10N_35	IO_L20N_T3_AD6N_35	J14	TXI_EA_RD_WAIT_N 11
11 TXO_EA_DATA4_P	L19	IO_L9P_T1_DQS_AD3P_35	IO_L21P_T3_DQS_AD14P_35	N15	TXO_EA_DATA7_P 11
11 TXO_EA_DATA4_N	L20	IO_L9N_T1_DQS_AD3N_35	IO_L21N_T3_DQS_AD14N_35	N16	TXO_EA_DATA7_N 11
11 TXO_EA_DATA0_P	K19	IO_L10P_T1_AD11P_35	IO_L22P_T3_AD7P_35	L14	TXO_EA_DATA1_P 11
11 TXO_EA_DATA0_N	J19	IO_L10N_T1_AD11N_35	IO_L22N_T3_AD7N_35	L15	TXO_EA_DATA1_N 11
11 TXO_EA_DATA2_P	L16	IO_L11P_T1_SRCC_35	IO_L23P_T3_35	M14	TXO_EA_DATA3_P 11
11 TXO_EA_DATA2_N	L17	IO_L11N_T1_SRCC_35	IO_L23N_T3_35	M15	TXO_EA_DATA3_N 11
11 TXO_EA_LCLK_P	K17	IO_L12P_T1_MRCC_35	IO_L24P_T3_AD15P_35	K16	TXI_EA_WR_WAIT_P 11
11 TXO_EA_LCLK_N	K18	IO_L12N_T1_MRCC_35	IO_L24N_T3_AD15N_35	J16	TXI_EA_WR_WAIT_N 11

2P5V

C19	VCCO_35_1
F18	VCCO_35_2
H14	VCCO_35_3
J17	VCCO_35_4
K20	VCCO_35_5
M16	VCCO_35_6

C135 0.47UF, C136 0.47UF, C137 0.47UF, C138 0.47UF, C139 0.47UF, C140 4.7UF, C141 4.7UF, C142 4.7UF, C143 100uF

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ZYNQ POWER & GROUND

U2H
XC7Z020-1CLG400C

PWR/GND

GND1 A8, GND2 A18, GND3 B1, GND4 B11, GND5 C4, GND6 C14, GND7 K11, GND8 D17, GND9 E10, GND10 E20, GND11 F3, GND12 F7, GND13 G10, GND14 G12, GND15 G16, GND16 H7, GND17 H9, GND18 H11, GND19 H13, GND20 H19, GND21 J2, GND22 J8, GND23 J12, GND24 K5, GND25 K7, GND26 C9, GND27 K13, GND28 K15, GND29 L8, GND30 L12, GND31 L18, GND32 M1, GND33 M7, GND34 M11, GND35 M13, GND36 N4, GND37 N8, GND38 N10, GND39 N12, GND40 N14, GND41 P7, GND42 P9, GND43 P11, GND44 P13, GND45 P17, GND46 R8, GND47 R12, GND48 R20, GND49 T3, GND50 T7, GND51 T13, GND52 U6, GND53 U16, GND54 V9, GND55 V19, GND56 W2, GND57 W12, GND58 Y5, GND59 Y15

VCCINT_1 G13, VCCINT_2 H12, VCCINT_3 J13, VCCINT_4 K12, VCCINT_5 L13, VCCINT_6 M12, VCCINT_7 N13, VCCINT_8 P12, VCCINT_9 R13

1P0V

C195 100uF, C214 100uF, C216 100uF, C149 4.7UF, C150 4.7UF, C151 4.7UF, C152 4.7UF, C153 4.7UF, C154 0.47UF, C155 0.47UF, C156 0.47UF, C157 0.47UF, C158 0.47UF, C159 0.47UF, C160 0.47UF

VCCAUX_1 J11, VCCAUX_2 L11, VCCAUX_3 N9, VCCAUX_4 P10, VCCAUX_5 R9, VCCAUX_6 N11

1P8V

C281 47UF, C162 4.7UF, C164 0.47UF, C165 0.47UF

VCCBRAM_1 G11, VCCBRAM_2 H10

1P0V

C168 100uF, C169 4.7UF, C282 4.7UF, C283 0.47UF, C170 0.47UF, C171 0.47UF

VCCPLL G8

ZYNQ_VCCPLL

FB12 BLM18SG121TN1D 120-OHM_3A

1P8V

C307 0.47UF, C172 10UF

VCCPAUX_1 G9, VCCPAUX_2 F8, VCCPAUX_3 H8, VCCPAUX_4 K8, VCCPAUX_5 M8

1P8V

C173 100uF, C174 4.7UF, C175 4.7UF, C176 0.47UF, C177 0.47UF, C178 0.47UF

VCCPINT_1 G7, VCCPINT_2 J7, VCCPINT_3 L7, VCCPINT_4 N7, VCCPINT_5 P8, VCCPINT_6 R7

1P0V

C179 100uF, C180 4.7UF, C181 4.7UF, C182 4.7UF, C183 0.47UF, C184 0.47UF, C185 0.47UF, C186 0.47UF, C187 0.47UF

U2E
XC7Z020-1CLG400C

BANK 13

15	GPIO21_P	U7	IO_L11P_T1_SRCC_13	IO_L16P_T2_13 W10	GPIO16_P 15
15	GPIO21_N	V7	IO_L11N_T1_SRCC_13	IO_L16N_T2_13 W9	GPIO16_N 15
15	GPIO15_P	T9	IO_L12P_T1_MRCC_13	IO_L17P_T2_13 U9	GPIO17_P 15
15	GPIO15_N	U10	IO_L12N_T1_MRCC_13	IO_L17N_T2_13 U8	GPIO17_N 15
15	GPIO20_P	Y7	IO_L13P_T2_MRCC_13	IO_L18P_T2_13 W11	GPIO13_P 15
15	GPIO20_N	Y6	IO_L13N_T2_MRCC_13	IO_L18N_T2_13 Y11	GPIO13_N 15
15	GPIO19_P	Y9	IO_L14P_T2_SRCC_13	IO_L19P_T3_13 T5	GPIO23_P 15
15	GPIO19_N	Y8	IO_L14N_T2_SRCC_13	IO_L19N_T3_VREF_13 U5	GPIO23_N 15
15	GPIO18_P	V8	IO_L15P_T2_DQS_13	IO_L20P_T3_13 Y12	GPIO12_P 15
15	GPIO18_N	W8	IO_L15N_T2_DQS_13	IO_L20N_T3_13 Y13	GPIO12_N 15
				IO_L21P_T3_DQS_13 V11	GPIO14_P 15
				IO_L21N_T3_DQS_13 V10	GPIO14_N 15
				IO_L22P_T3_13 V6	GPIO22_P 15
				IO_L22N_T3_13 W6	GPIO22_N 15

VDD_GPIO

VCCO_13_1 T8, VCCO_13_2 U11, VCCO_13_3 W7, VCCO_13_4 Y10

C285 0.47UF, C188 0.47UF, C189 0.47UF, C190 0.47UF, C191 0.47UF, C284 4.7UF, C192 4.7UF, C193 4.7UF, C194 100uF

Adapteva, Inc.		
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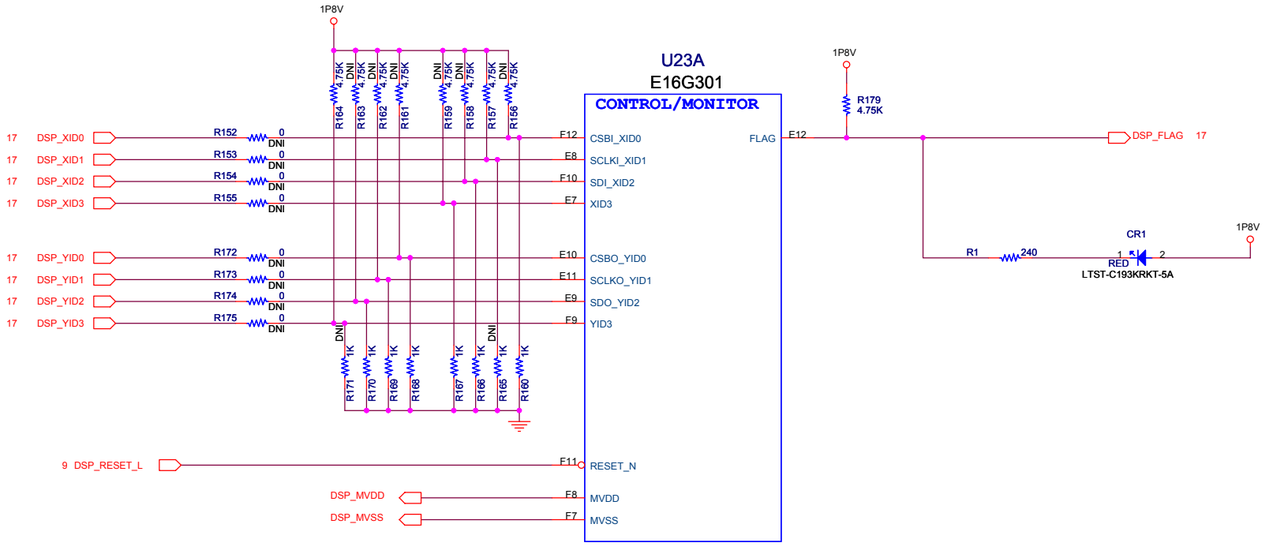
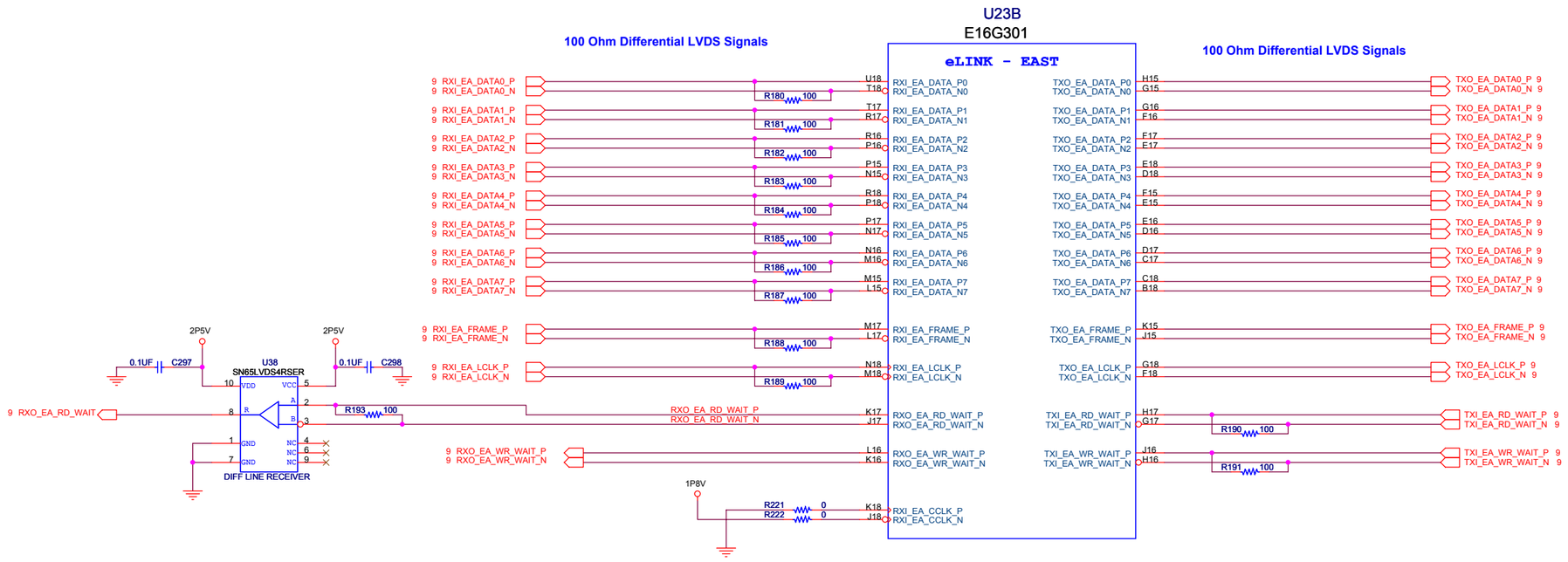
DSP PROCESSOR 1-OF-3





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DSP PROCESSOR 2-OF-3

U23C
E16G301

eLINK - NORTH

100 Ohm Differential LVDS Signals

14 RXI_NO_DATA0_P	R194 100	A3	RXI_NO_DATA_P0	TXO_NO_DATA_P0	D12	TXO_NO_DATA0_P 14
14 RXI_NO_DATA0_N		A2	RXI_NO_DATA_N0	TXO_NO_DATA_N0	D11	R233 100 DNI — TXO_NO_DATA0_N 14
14 RXI_NO_DATA1_P	R195 100	B4	RXI_NO_DATA_P1	TXO_NO_DATA_P1	C13	TXO_NO_DATA1_P 14
14 RXI_NO_DATA1_N		B3	RXI_NO_DATA_N1	TXO_NO_DATA_N1	C12	R232 100 DNI — TXO_NO_DATA1_N 14
14 RXI_NO_DATA2_P	R196 100	C5	RXI_NO_DATA_P2	TXO_NO_DATA_P2	B14	TXO_NO_DATA2_P 14
14 RXI_NO_DATA2_N		C4	RXI_NO_DATA_N2	TXO_NO_DATA_N2	B13	R231 100 DNI — TXO_NO_DATA2_N 14
14 RXI_NO_DATA3_P	R197 100	D6	RXI_NO_DATA_P3	TXO_NO_DATA_P3	A15	TXO_NO_DATA3_P 14
14 RXI_NO_DATA3_N		D5	RXI_NO_DATA_N3	TXO_NO_DATA_N3	A14	R230 100 DNI — TXO_NO_DATA3_N 14
14 RXI_NO_DATA4_P	R198 100	A5	RXI_NO_DATA_P4	TXO_NO_DATA_P4	D14	TXO_NO_DATA4_P 14
14 RXI_NO_DATA4_N		A4	RXI_NO_DATA_N4	TXO_NO_DATA_N4	D13	R229 100 DNI — TXO_NO_DATA4_N 14
14 RXI_NO_DATA5_P	R199 100	B6	RXI_NO_DATA_P5	TXO_NO_DATA_P5	C15	TXO_NO_DATA5_P 14
14 RXI_NO_DATA5_N		B5	RXI_NO_DATA_N5	TXO_NO_DATA_N5	C14	R228 100 DNI — TXO_NO_DATA5_N 14
14 RXI_NO_DATA6_P	R200 100	C7	RXI_NO_DATA_P6	TXO_NO_DATA_P6	B16	TXO_NO_DATA6_P 14
14 RXI_NO_DATA6_N		C6	RXI_NO_DATA_N6	TXO_NO_DATA_N6	B15	R227 100 DNI — TXO_NO_DATA6_N 14
14 RXI_NO_DATA7_P	R201 100	D8	RXI_NO_DATA_P7	TXO_NO_DATA_P7	A17	TXO_NO_DATA7_P 14
14 RXI_NO_DATA7_N		D7	RXI_NO_DATA_N7	TXO_NO_DATA_N7	A16	R226 100 DNI — TXO_NO_DATA7_N 14
R243 10K						
14 RXI_NO_FRAME_P	R202 100	B8	RXI_NO_FRAME_P	TXO_NO_FRAME_P	D10	TXO_NO_FRAME_P 14
14 RXI_NO_FRAME_N		B7	RXI_NO_FRAME_N	TXO_NO_FRAME_N	D9	TXO_NO_FRAME_N 14
1P8V R242 10K						
14 RXI_NO_LCLK_P	R203 100	A7	RXI_NO_LCLK_P	TXO_NO_LCLK_P	A13	TXO_NO_LCLK_P 14
14 RXI_NO_LCLK_N		A6	RXI_NO_LCLK_N	TXO_NO_LCLK_N	A12	R206 100 DNI — TXO_NO_LCLK_N 14
14 RXO_NO_RD_WAIT_P		B10	RXO_NO_RD_WAIT_P	TXI_NO_RD_WAIT_P	B12	R241 10K 1P8V — TXI_NO_RD_WAIT_P 14
14 RXO_NO_RD_WAIT_N		B9	RXO_NO_RD_WAIT_N	TXI_NO_RD_WAIT_N	B11	R204 100 — TXI_NO_RD_WAIT_N 14
14 RXO_NO_WR_WAIT_P		C9	RXO_NO_WR_WAIT_P	TXI_NO_WR_WAIT_P	C11	R240 10K — TXI_NO_WR_WAIT_P 14
14 RXO_NO_WR_WAIT_N		C8	RXO_NO_WR_WAIT_N	TXI_NO_WR_WAIT_N	C10	R205 100 — TXI_NO_WR_WAIT_N 14
1P8V R289 0 R290 0		A10	RXI_NO_CCLK_P			
		A9	RXI_NO_CCLK_N			

U23D
E16G301

eLINK - SOUTH

100 Ohm Differential LVDS Signals

14 RXI_SO_DATA0_P	R207 100	V2	RXI_SO_DATA_P0	TXO_SO_DATA_P0	R11	TXO_SO_DATA0_P 14
14 RXI_SO_DATA0_N		V3	RXI_SO_DATA_N0	TXO_SO_DATA_N0	R12	TXO_SO_DATA0_N 14
14 RXI_SO_DATA1_P	R208 100	U3	RXI_SO_DATA_P1	TXO_SO_DATA_P1	T12	TXO_SO_DATA1_P 14
14 RXI_SO_DATA1_N		U4	RXI_SO_DATA_N1	TXO_SO_DATA_N1	T13	TXO_SO_DATA1_N 14
14 RXI_SO_DATA2_P	R209 100	T4	RXI_SO_DATA_P2	TXO_SO_DATA_P2	U13	TXO_SO_DATA2_P 14
14 RXI_SO_DATA2_N		T5	RXI_SO_DATA_N2	TXO_SO_DATA_N2	U14	TXO_SO_DATA2_N 14
14 RXI_SO_DATA3_P	R210 100	R5	RXI_SO_DATA_P3	TXO_SO_DATA_P3	V14	TXO_SO_DATA3_P 14
14 RXI_SO_DATA3_N		R6	RXI_SO_DATA_N3	TXO_SO_DATA_N3	V15	TXO_SO_DATA3_N 14
14 RXI_SO_DATA4_P	R211 100	V4	RXI_SO_DATA_P4	TXO_SO_DATA_P4	R13	TXO_SO_DATA4_P 14
14 RXI_SO_DATA4_N		V5	RXI_SO_DATA_N4	TXO_SO_DATA_N4	R14	TXO_SO_DATA4_N 14
14 RXI_SO_DATA5_P	R212 100	U5	RXI_SO_DATA_P5	TXO_SO_DATA_P5	T14	TXO_SO_DATA5_P 14
14 RXI_SO_DATA5_N		U6	RXI_SO_DATA_N5	TXO_SO_DATA_N5	T15	TXO_SO_DATA5_N 14
14 RXI_SO_DATA6_P	R213 100	T6	RXI_SO_DATA_P6	TXO_SO_DATA_P6	U15	TXO_SO_DATA6_P 14
14 RXI_SO_DATA6_N		T7	RXI_SO_DATA_N6	TXO_SO_DATA_N6	U16	TXO_SO_DATA6_N 14
14 RXI_SO_DATA7_P	R214 100	R7	RXI_SO_DATA_P7	TXO_SO_DATA_P7	V16	TXO_SO_DATA7_P 14
14 RXI_SO_DATA7_N		R8	RXI_SO_DATA_N7	TXO_SO_DATA_N7	V17	TXO_SO_DATA7_N 14
R246 10K						
14 RXI_SO_FRAME_P	R215 100	U7	RXI_SO_FRAME_P	TXO_SO_FRAME_P	R9	R245 10K — TXO_SO_FRAME_P 14
14 RXI_SO_FRAME_N		U8	RXI_SO_FRAME_N	TXO_SO_FRAME_N	R10	R236 100 — R244 10K 1P8V — TXO_SO_FRAME_N 14
1P8V R247 10K						
14 RXI_SO_LCLK_P	R216 100	V6	RXI_SO_LCLK_P	TXO_SO_LCLK_P	V12	TXO_SO_LCLK_P 14
14 RXI_SO_LCLK_N		V7	RXI_SO_LCLK_N	TXO_SO_LCLK_N	V13	TXO_SO_LCLK_N 14
14 RXO_SO_RD_WAIT_P		U9	RXO_SO_RD_WAIT_P	TXI_SO_RD_WAIT_P	U11	TXI_SO_RD_WAIT_P 14
14 RXO_SO_RD_WAIT_N	R234 100 DNI	U10	RXO_SO_RD_WAIT_N	TXI_SO_RD_WAIT_N	U12	R217 100 — TXI_SO_RD_WAIT_N 14
14 RXO_SO_WR_WAIT_P		T8	RXO_SO_WR_WAIT_P	TXI_SO_WR_WAIT_P	T10	TXI_SO_WR_WAIT_P 14
14 RXO_SO_WR_WAIT_N	R235 100 DNI	T9	RXO_SO_WR_WAIT_N	TXI_SO_WR_WAIT_N	T11	R218 100 — TXI_SO_WR_WAIT_N 14
1P8V R291 0 R292 0		V9	RXI_SO_CCLK_P			
		V10	RXI_SO_CCLK_N			

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DSP PROCESSOR 3-OF-3

U23F
E16G301

POWER/GROUND

VDD_DSP

C213 0.1UF, C215 0.1UF, C217 0.1UF, C219 0.1UF, C221 0.1UF, C223 0.1UF, C225 0.1UF, C227 0.1UF

VDD1 H6, VDD2 H8, VDD3 H10, VDD4 H12, VDD5 J7, VDD6 J9, VDD7 J11, VDD8 J13, VDD9 K6, VDD10 K8, VDD11 K10, VDD12 K12, VDD13 L7, VDD14 L9, VDD15 L11, VDD16 L13, VDD17 M6, VDD18 M8, VDD19 M10, VDD20 M12, VDD21 N7, VDD22 N9, VDD23 N11, VDD24 N13

1P8V

C197 0.1UF, C198 10nF, C199 0.1UF, C200 10nF, C201 0.1UF, C202 10nF, C203 0.1UF, C204 10nF, C205 0.1UF, C206 10nF, C207 0.1UF, C208 10nF, C209 0.1UF, C210 10nF, C211 0.1UF, C212 10nF

DVDD1 G5, DVDD2 G7, DVDD3 G9, DVDD4 G11, DVDD5 G13, DVDD6 H14, DVDD7 J5, DVDD8 K14, DVDD9 L5, DVDD10 M14, DVDD11 N5, DVDD12 P6, DVDD13 P8, DVDD14 P10, DVDD15 P12, DVDD16 P14

VSS1 A1, VSS2 A8, VSS3 A11, VSS4 A18, VSS5 B2, VSS6 B17, VSS7 C3, VSS8 C16, VSS9 D4, VSS10 D15, VSS11 E5, VSS12 E6, VSS13 E13, VSS14 E14, VSS15 F5, VSS16 F6, VSS17 F13, VSS18 F14, VSS19 G6, VSS20 G8, VSS21 G10, VSS22 G12, VSS23 G14, VSS24 H1, VSS25 H5, VSS26 H7

VSS27 H9, VSS28 H11, VSS29 H13, VSS30 H18, VSS31 J6, VSS32 J8, VSS33 J10, VSS34 J12, VSS35 J14, VSS36 K5, VSS37 K7, VSS38 K9, VSS39 K11, VSS40 K13, VSS41 L1, VSS42 L6, VSS43 L8, VSS44 L10, VSS45 L12, VSS46 L14, VSS47 L18

VSS48 M5, VSS49 M7, VSS50 M9, VSS51 M11, VSS52 M13, VSS53 N6, VSS54 N8, VSS55 N10, VSS56 N12, VSS57 N14, VSS58 P5, VSS59 P7, VSS60 P9, VSS61 P11, VSS62 P13, VSS63 R4, VSS64 R5, VSS65 T3, VSS66 T16, VSS67 U2, VSS68 U17, VSS69 V1, VSS70 V8, VSS71 V11, VSS72 V18

U23E
E16G301

eLINK - WEST

RXI_WE_DATA_P0 T1, RXI_WE_DATA_N0 U1, RXI_WE_DATA_P1 R2, RXI_WE_DATA_N1 T2, RXI_WE_DATA_P2 P3, RXI_WE_DATA_N2 R3, RXI_WE_DATA_P3 N4, RXI_WE_DATA_N3 P4, RXI_WE_DATA_P4 P1, RXI_WE_DATA_N4 R1, RXI_WE_DATA_P5 N2, RXI_WE_DATA_N5 P2, RXI_WE_DATA_P6 M3, RXI_WE_DATA_N6 N3, RXI_WE_DATA_P7 L4, RXI_WE_DATA_N7 M4

TXO_WE_DATA_P0 G4, TXO_WE_DATA_N0 H4, TXO_WE_DATA_P1 F3, TXO_WE_DATA_N1 G3, TXO_WE_DATA_P2 E2, TXO_WE_DATA_N2 F2, TXO_WE_DATA_P3 D1, TXO_WE_DATA_N3 E1, TXO_WE_DATA_P4 E4, TXO_WE_DATA_N4 F4, TXO_WE_DATA_P5 D3, TXO_WE_DATA_N5 E3, TXO_WE_DATA_P6 C2, TXO_WE_DATA_N6 D2, TXO_WE_DATA_P7 B1, TXO_WE_DATA_N7 C1

1P8V

R219 0, R220 0 → RXI_WE_FRAME_P L2, RXI_WE_FRAME_N M2

TXO_WE_FRAME_P J4, TXO_WE_FRAME_N K4 → R238 0, R239 0 DNI

1P8V

DNI

RXI_WE_LCLK_P M1, RXI_WE_LCLK_N N1

TXO_WE_LCLK_P F1, TXO_WE_LCLK_N G1

RXO_WE_RD_WAIT_P J2, RXO_WE_RD_WAIT_N K2

TXI_WE_RD_WAIT_P G2, TXI_WE_RD_WAIT_N H2

RXO_WE_WR_WAIT_P K3, RXO_WE_WR_WAIT_N L3

TXI_WE_WR_WAIT_P H3, TXI_WE_WR_WAIT_N J3

9 RXI_CCLK_P, 9 RXI_CCLK_N → R192 100 → RXI_WE_CCLK_P J1, RXI_WE_CCLK_N K1

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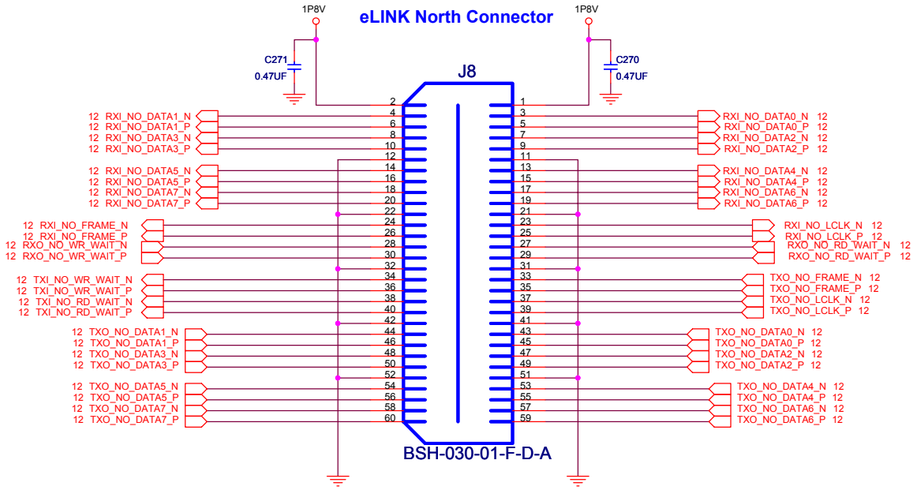
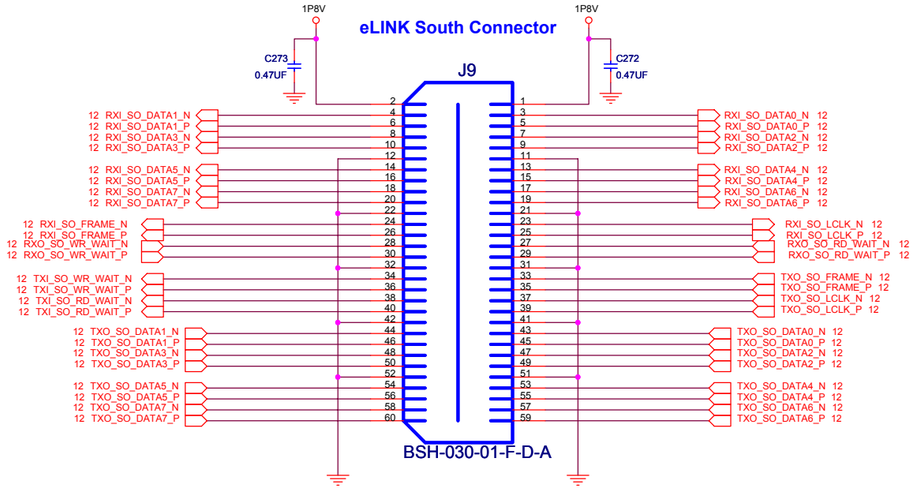
DSP eLINK CONNECTORS





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HDMI TRANSMITTER

U26
ADV7513BSWZ
HDMI/DVI XMTR

U37
TPD12S016PWR
ESD PROT & LEVEL SHIFT

J10
46765-1001
HDMI_MICRO_D_RA

GPIO EXPANSION Connector
J11
BSH-030-01-F-D-A

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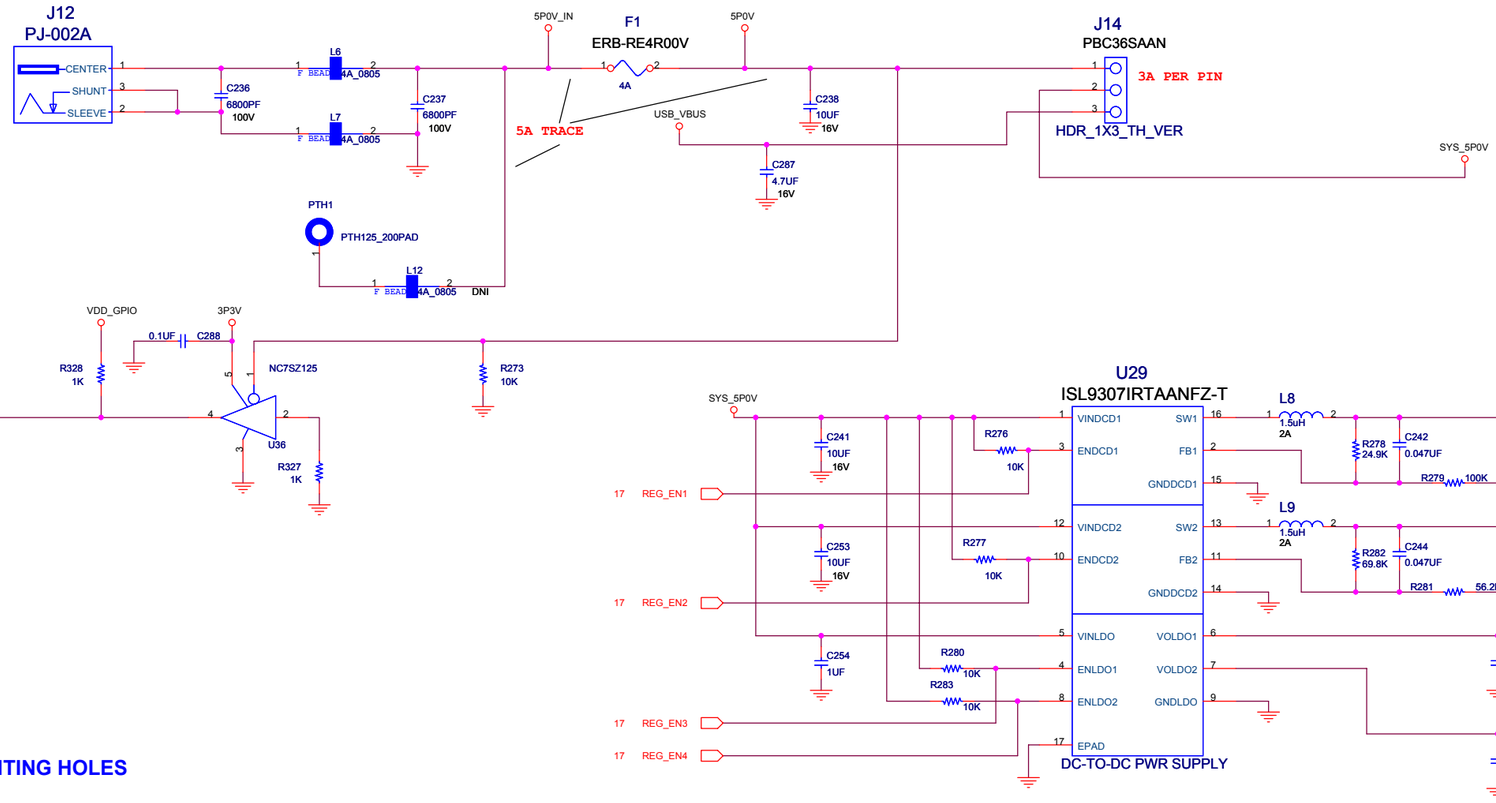
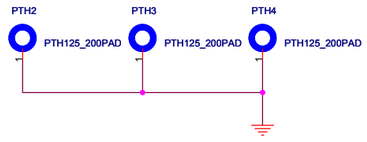
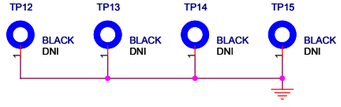
POWER MANAGEMENT

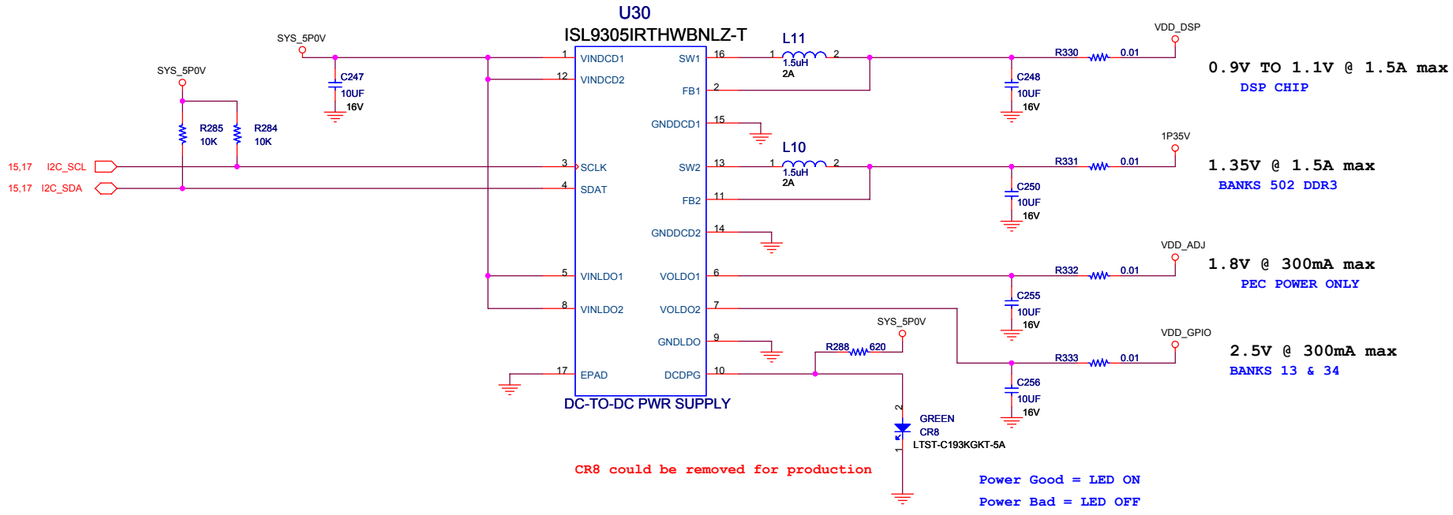


BOARD MOUNTING HOLES





Place in 4 quadrants of the board



CR8 could be removed for production

Power Good = LED ON
Power Bad = LED OFF

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RESET GENERATION

ZYNQ POWER-ON RESET

U34
STM6904TWEDS6F
VOLT_MONITOR

SW2
B3U-1000P
SW_PB_VERT

NC7SZ125
U33

C290 0.1UF
C291 0.1UF
C259 0.1UF
C275 0.47UF
C277 0.47UF
C276 0.47UF
C278 0.47UF
C292 0.47UF
C293 0.47UF
C294 0.47UF
C295 0.47UF

R326 10K
R96 0
R98 0
R298 10K
R300 4.75K
R301 10K
R299 10K
R295 1K
R294 1K
R95 0 DNI

RESET_N
PS_POR_L 3
BOARD_RESET_L 5,6
PB_RESET_L

populate R95 & remove R96 to bypass RESET circuit

PEC_POWER

J13
BSH-030-01-F-D-A

C279 0.47UF
C274 0.47UF

15,16 I2C_SDA
16 REG_EN2
16 REG_EN4
11 DSP_YID0
11 DSP_YID1
11 DSP_YID2
11 DSP_YID3
3 UART_RX
3 UART_TX
3 USER_LED
2 VADC_P
2 JTAG_TDI
2 JTAG_TDO

I2C_SCL 15,16
REG_EN1 16
REG_EN3 16
PROG_IO 9
DSP_XID0 11
DSP_XID1 11
DSP_XID2 11
DSP_XID3 11
DSP_FLAG 11
TURBO_MODE 9,16
SPDIF 9,15
JTAG_BOOT_EN 3
VADC_N 2
JTAG_TMS 2
JTAG_TCK 2

USER LED

CR10
GREEN
LTST-C193KGKT-5A

R30
240

Adapteva, Inc.	
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