HB01-AAFM Table of Contents

Rev.	Date	Rev. 1	Comments
1	7/19/11	E. Clark	Initial Release Major Rev. 1: Install Pull-Downs for CLK0_M2C_P/N, R12/13. Always install Pull-Up for CLK_DIR, R14. Remove Pull-Down for CLK_DIR, R15. Add Pull-Ups for FMC_CLK1_M2C_P/N, R306/307. Install Pull-Ups for XFMC_CLK_P/N, R53/60. Change PCB1 BWCPN HB00-AAFM -> HB01-AAFM. Install series resistor for XFMC_CLK_P/N - CLK0_M2C_P/N, R60/65. Updated FMC connections.
1.1	3/9/12	E. Clark	Connnect CPLD (TP19) to AD9520 SYNC_L pin (RWI-586)

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Title: HB01-AAFM		
Page Contents: AAFM Contents		
Size:B	DWG NO	Revision: 1.1
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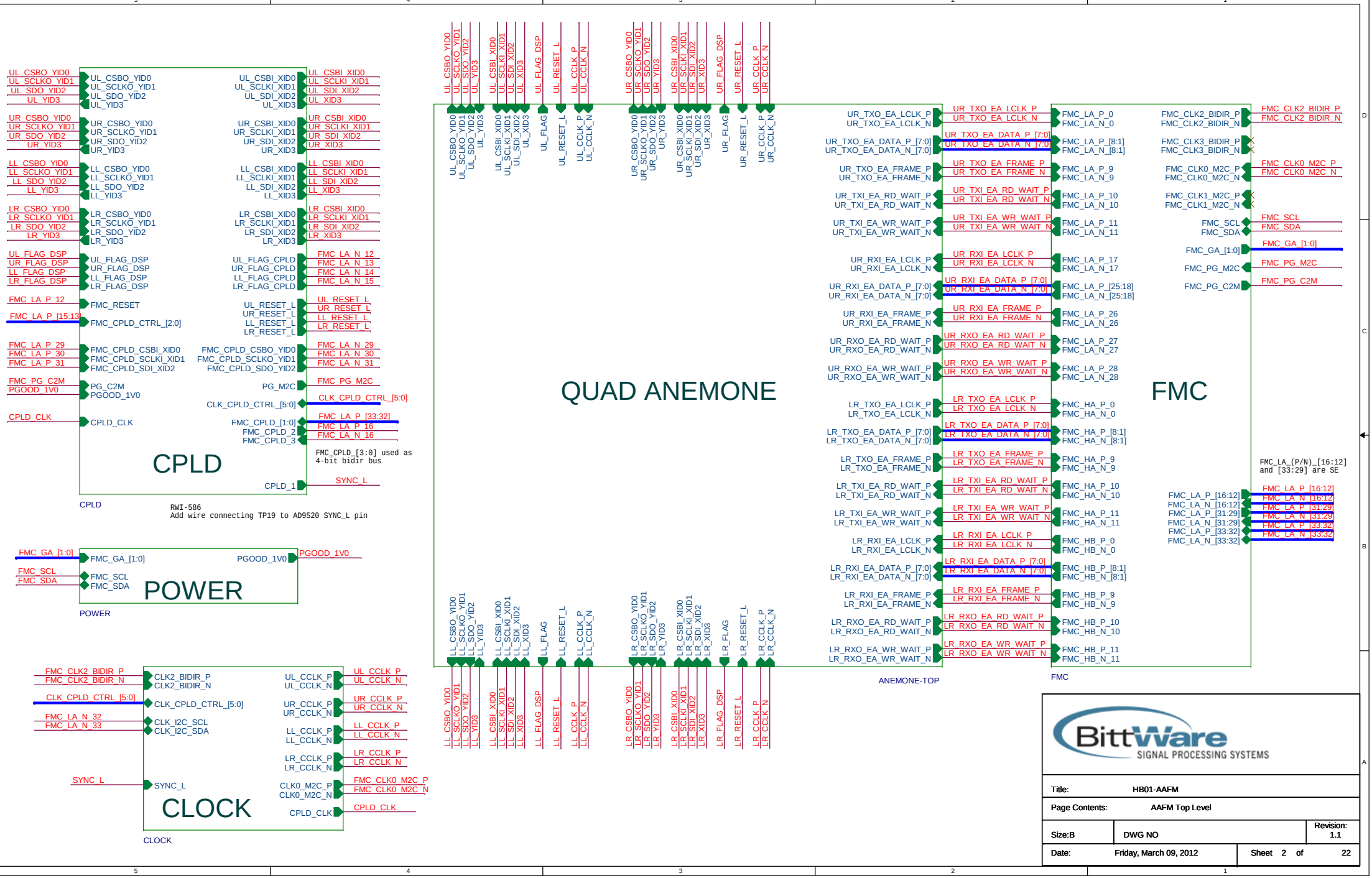
CPLD
POWER
CLOCK
QUAD ANEMONE
ANEMONE-TOP
FMC
FMC_CPLD_[3:0] used as 4-bit bidir bus
RWI-586
Add wire connecting TP19 to AD9520 SYNC_L pin
FMC_LA_(P/N)_[16:12] and [33:29] are SE
BittWare
SIGNAL PROCESSING SYSTEMS
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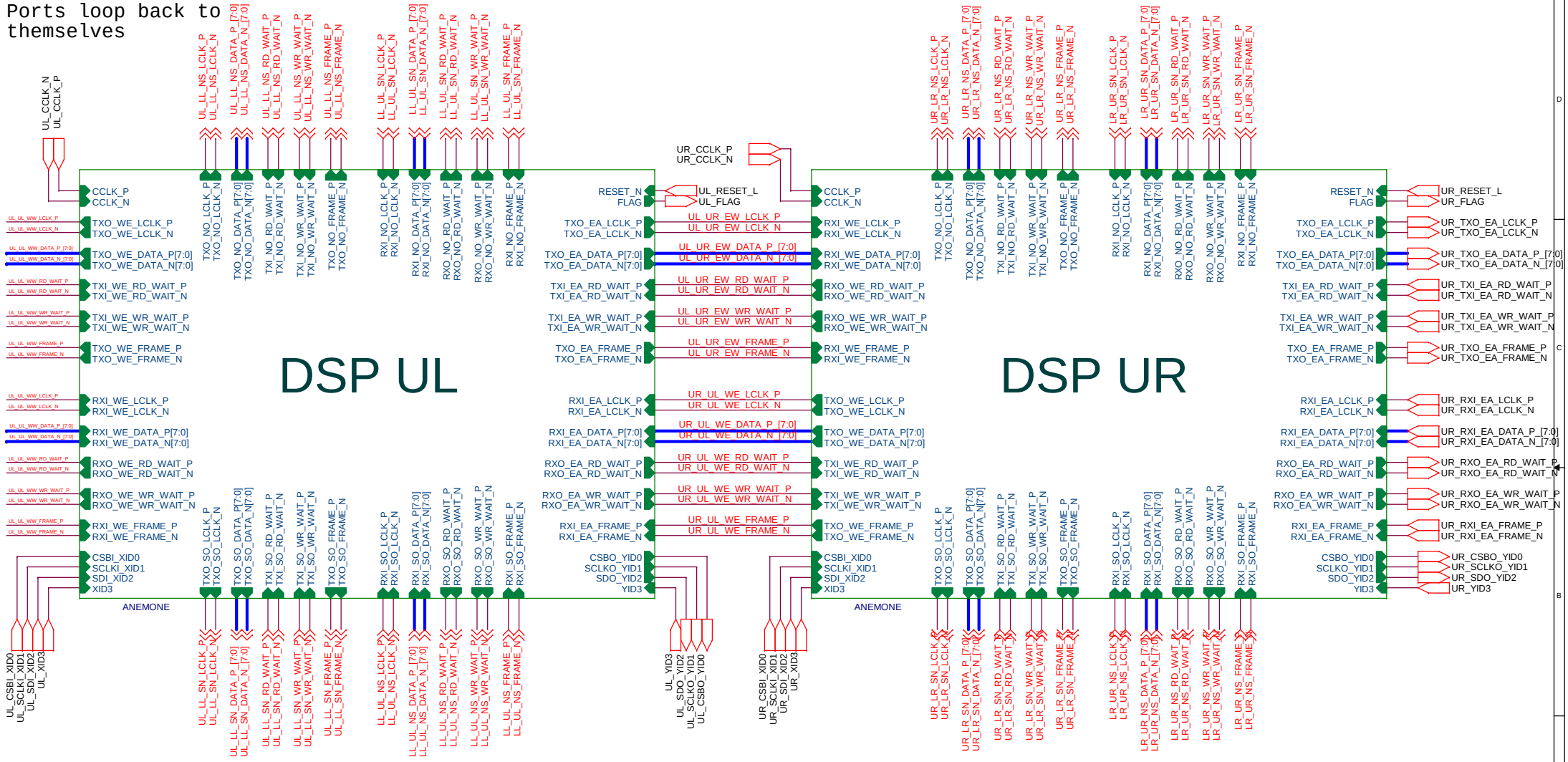
NOTE: UL/LL WEST Link Ports loop back to themselves



Note that for marketing/doc purposes, the following naming convention applies:

UL = NW (NorthWest)
UR = NE (NorthEast)
LL = SW (SouthWest)
LR = SE (SouthEast)

Inter-DSP Link Port Naming Convention:
AA_BB_CD_XXXX_Y

AA = Transmit DSP, UL | UR | LL | LR
BB = Receive DSP, UL | UR | LL | LR
C = Transmit Port, N | S | E | W
D = Receive Port, N | S | E | W
XXXX = Generic Signal Name, LCLK | DATA | WAIT | FRAME
Y = Polarity, P | N

BittWare SIGNAL PROCESSING SYSTEMS

Title:	HB01-AAFM	
Page Contents:	Anemone Top Level UL/UR	
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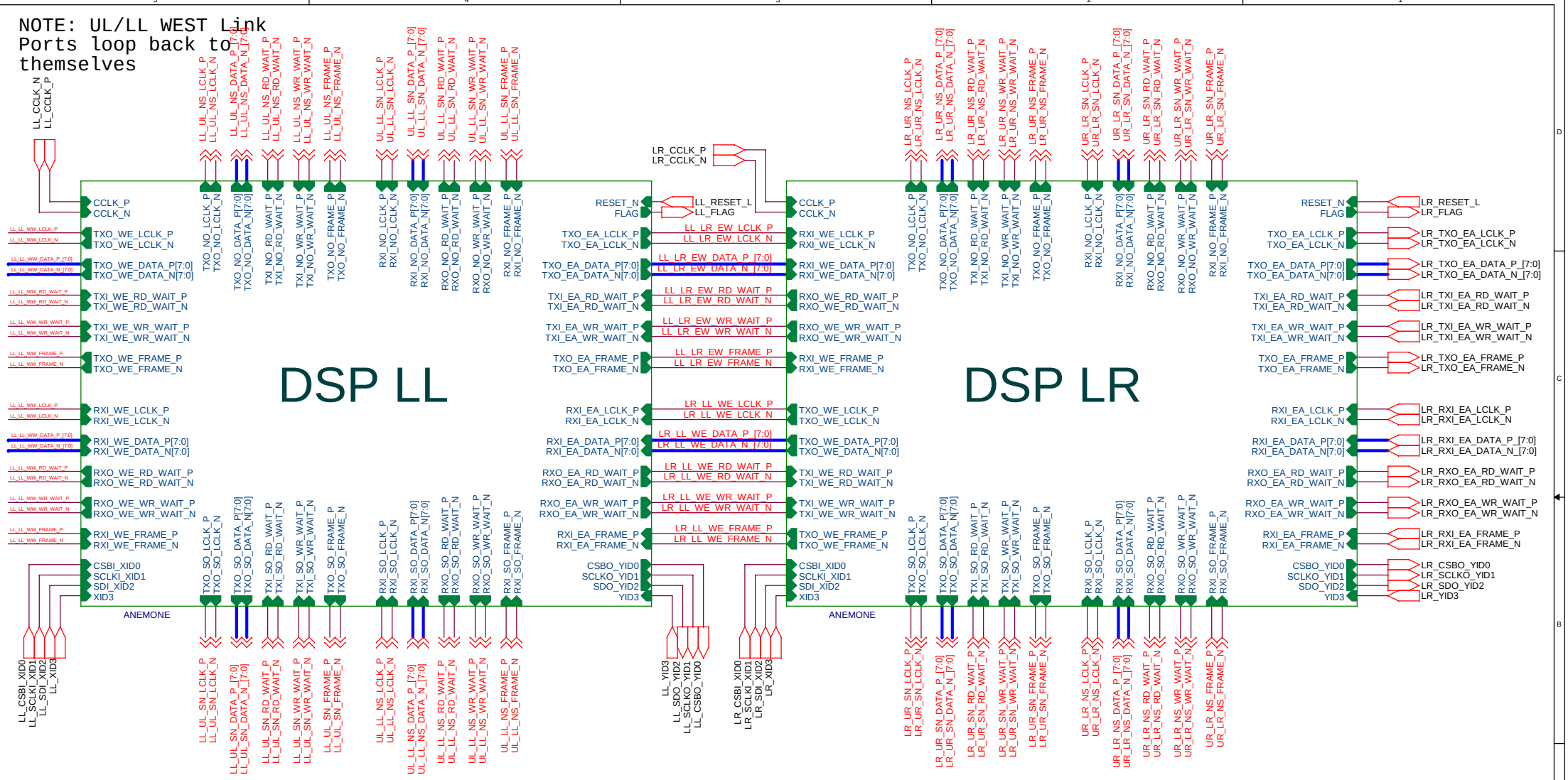

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Y = Polarity, P | N

BittWare SIGNAL PROCESSING SYSTEMS

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Page Contents:	Anemone Top Level LL/LR	
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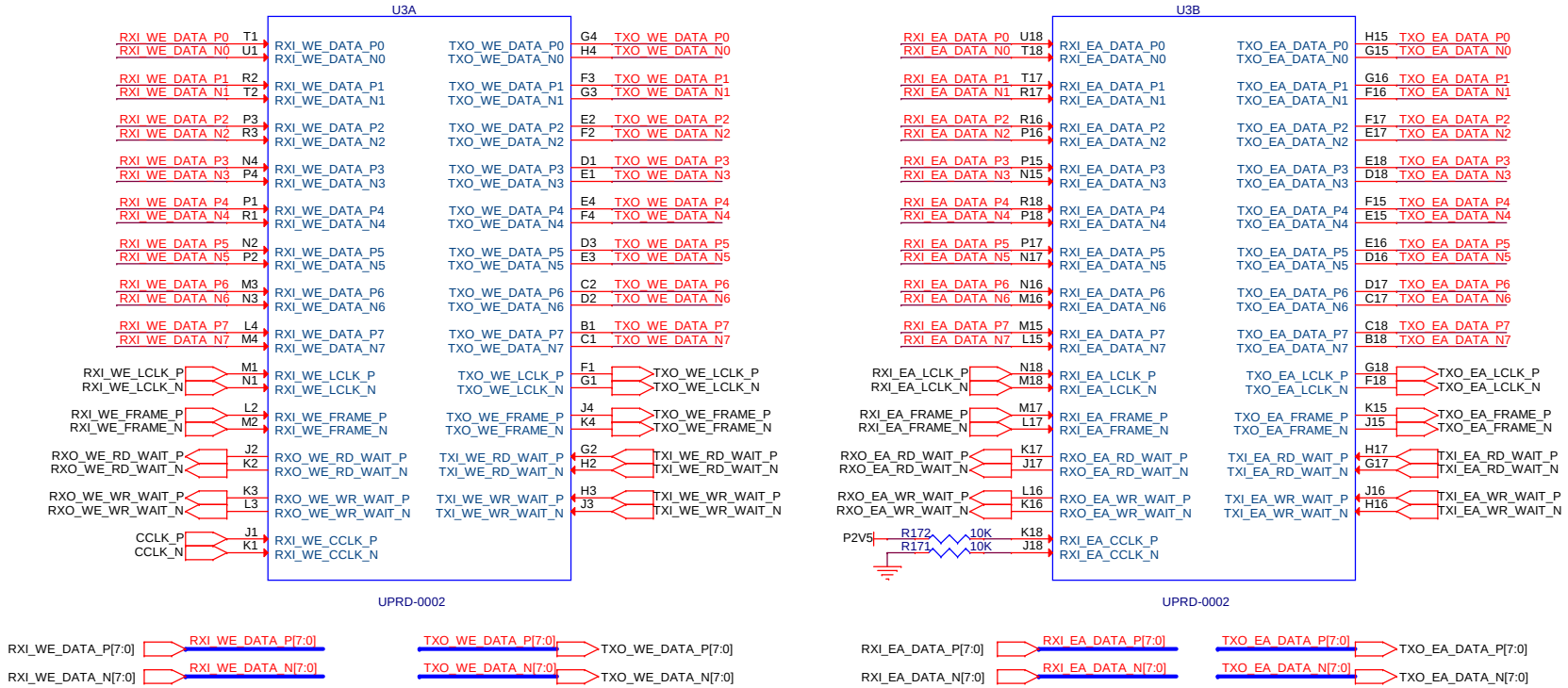
DSP Link Ports EAST/WEST



Place 100-ohm LVDS terminators close to DSP link receivers

BittWare SIGNAL PROCESSING SYSTEMS

Title:	HB01-AAFM	
Page Contents:	UL Anemone EAST/WEST Link Ports	
Size:B	DWG NO	Revision: 1.1
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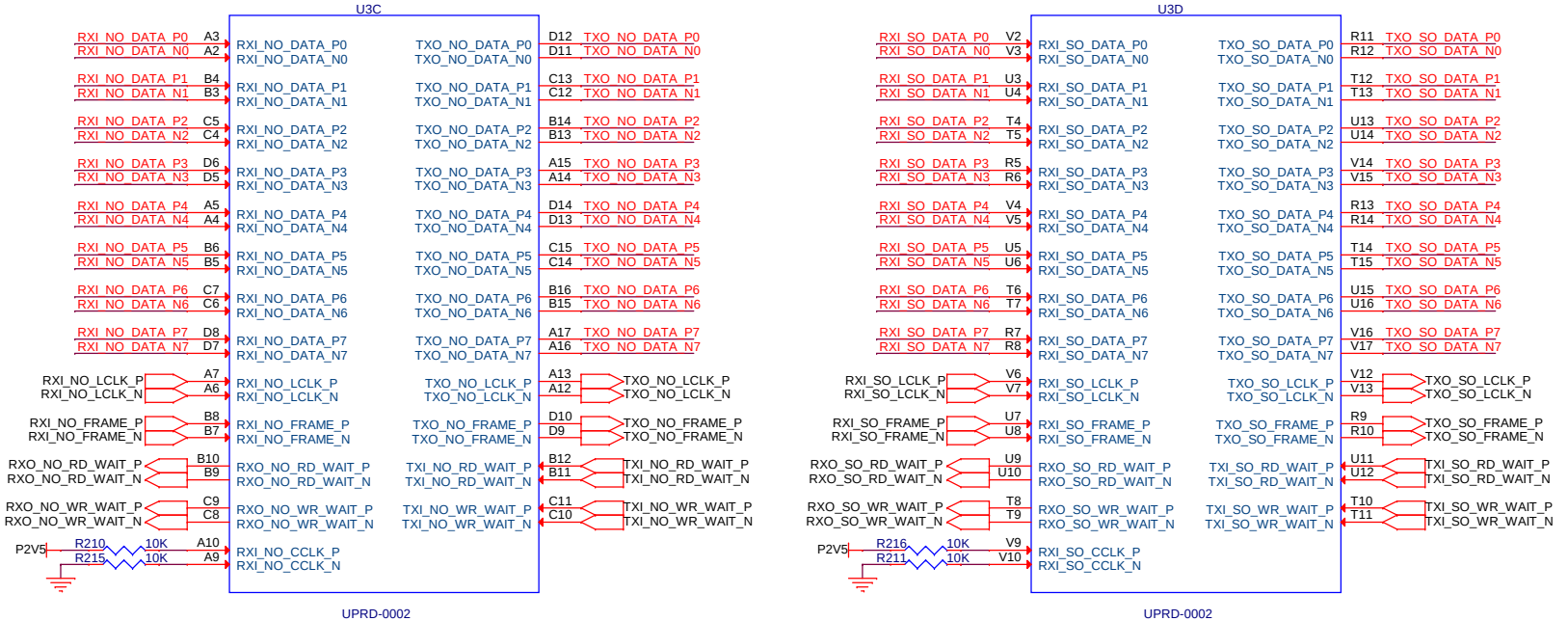
DSP Link Ports NORTH/SOUTH



Place 100-ohm LVDS terminators close to DSP link receivers

BittWare SIGNAL PROCESSING SYSTEMS

Title:	HB01-AAFM	
Page Contents:	UL Anemone NORTH/SOUTH Link Ports	
Size:B	DWG NO	Revision: 1.1
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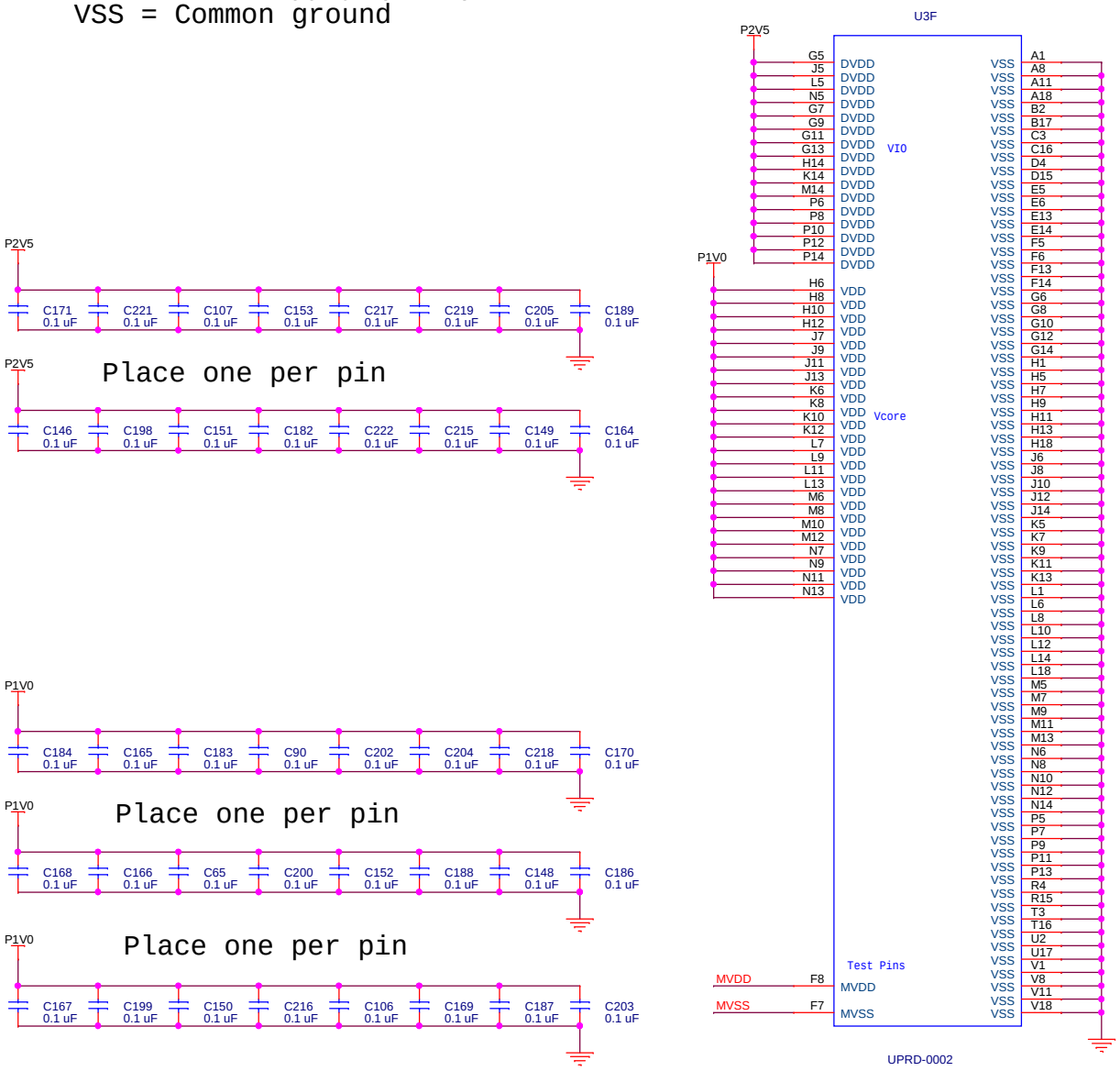
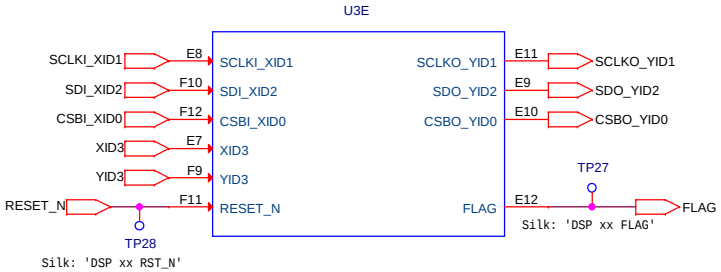
DVDD = IO supply (2.5V)
VDD = Core supply (1.0V)
VSS = Common ground

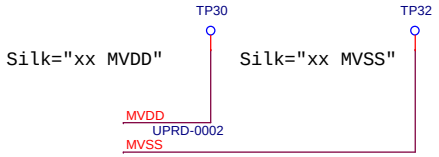
DSP Power



DSP Control



Layout note on TP silkscreen that xx corresponds to UL, UR, LL, LR



BittWare SIGNAL PROCESSING SYSTEMS

Title:	HB01-AAFM	
Page Contents:	UL Anemone Power & Control	
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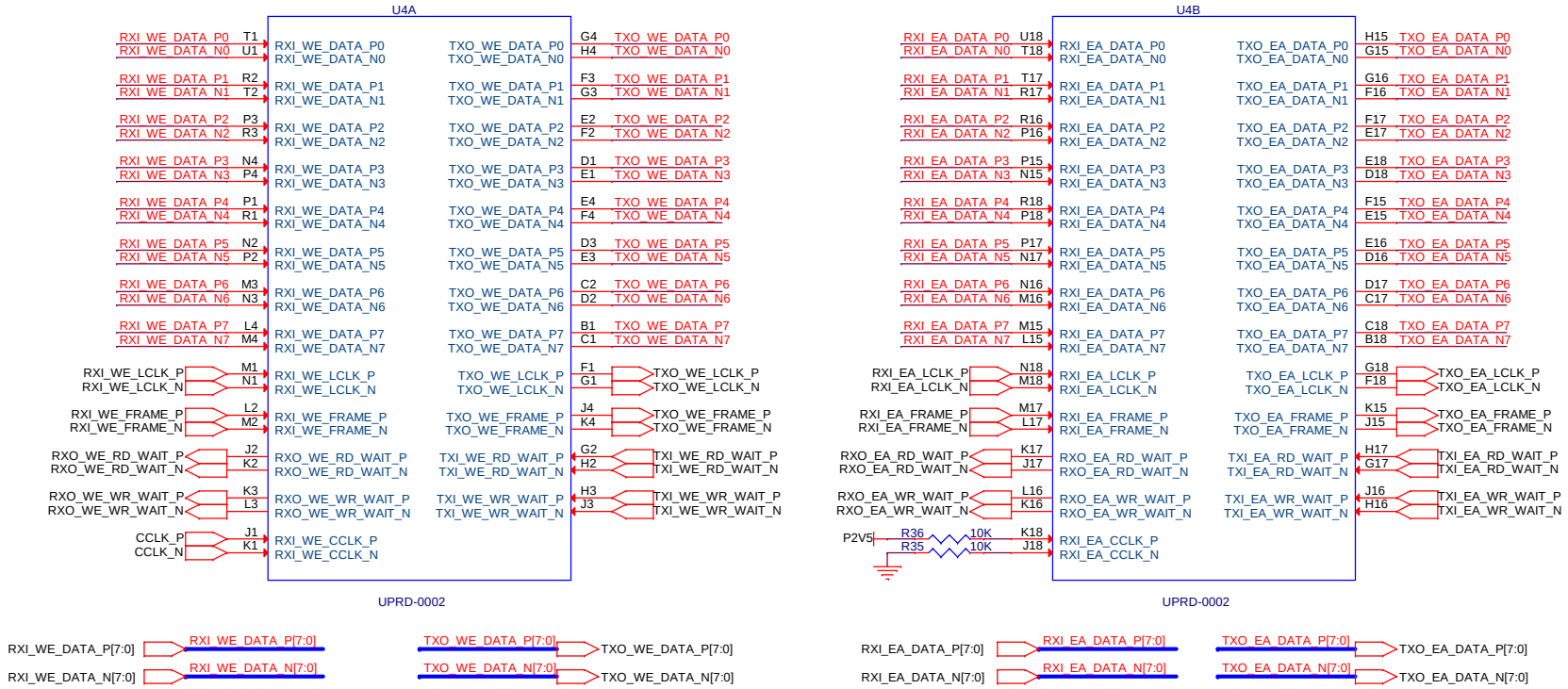
DSP Link Ports EAST/WEST



Place 100-ohm LVDS terminators close to DSP link receivers

BittWare SIGNAL PROCESSING SYSTEMS

Title:	HB01-AAFM	
Page Contents:	UR Anemone EAST/WEST Link Ports	
Size:B	DWG NO	Revision: 1.1
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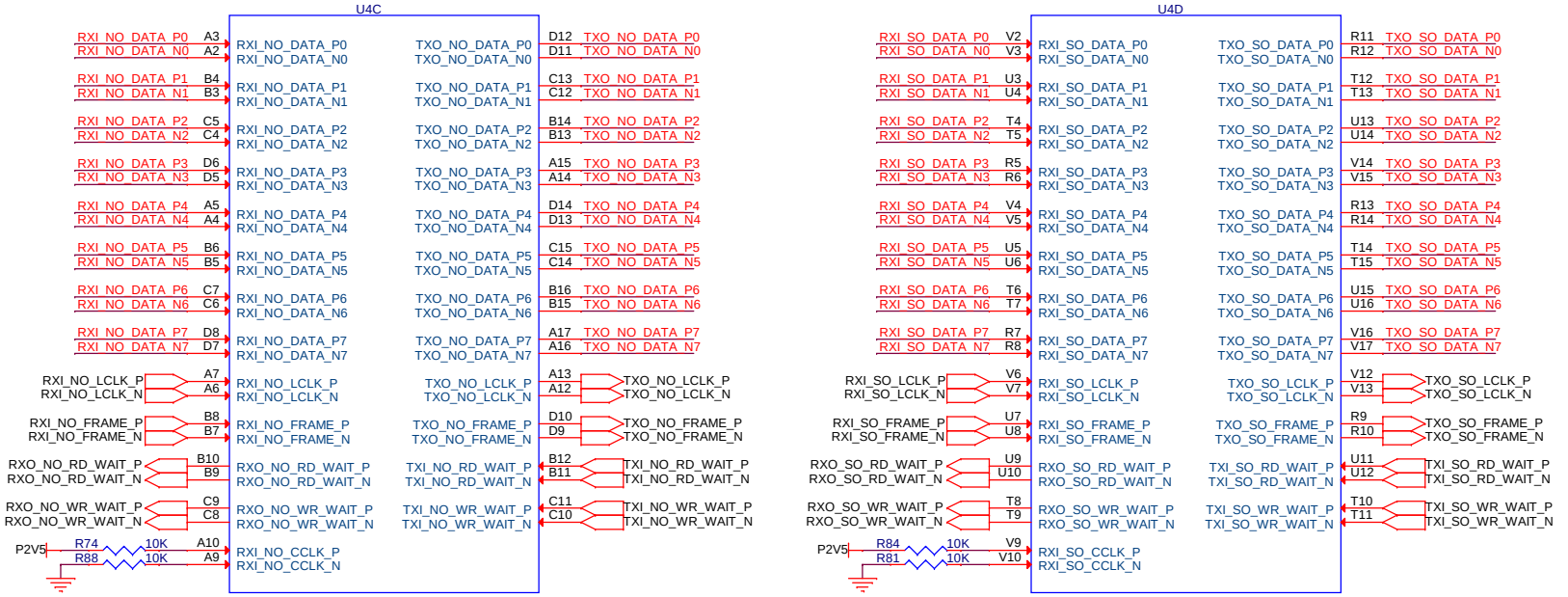
DSP Link Ports NORTH/SOUTH



Place 100-ohm LVDS terminators close to DSP link receivers

BittWare SIGNAL PROCESSING SYSTEMS

Title:	HB01-AAFM	
Page Contents:	UR Anemone NORTH/SOUTH Link Ports	
Size:B	DWG NO	Revision: 1.1
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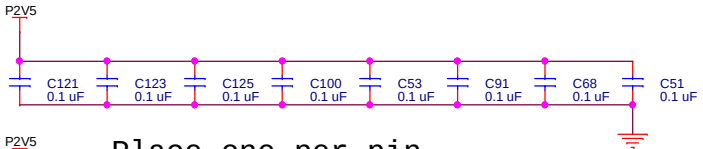
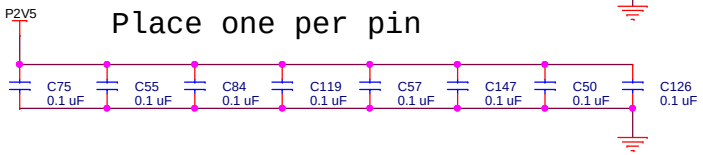
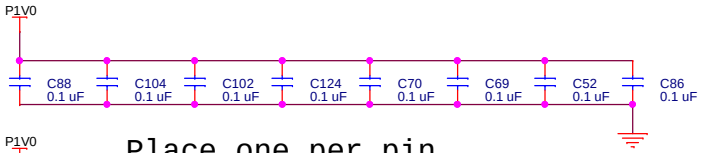
DVDD = IO supply (2.5V)
VDD = Core supply (1.0V)
VSS = Common ground

DSP Power

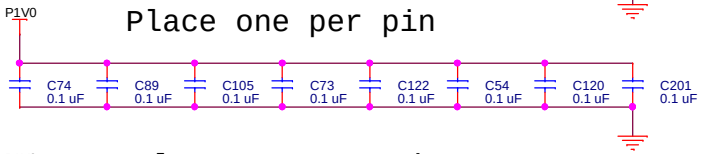


Place one per pin

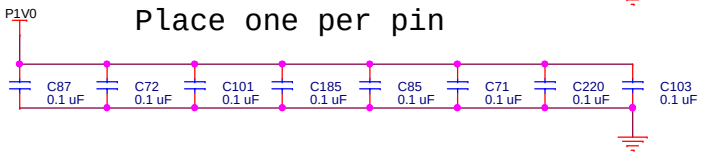


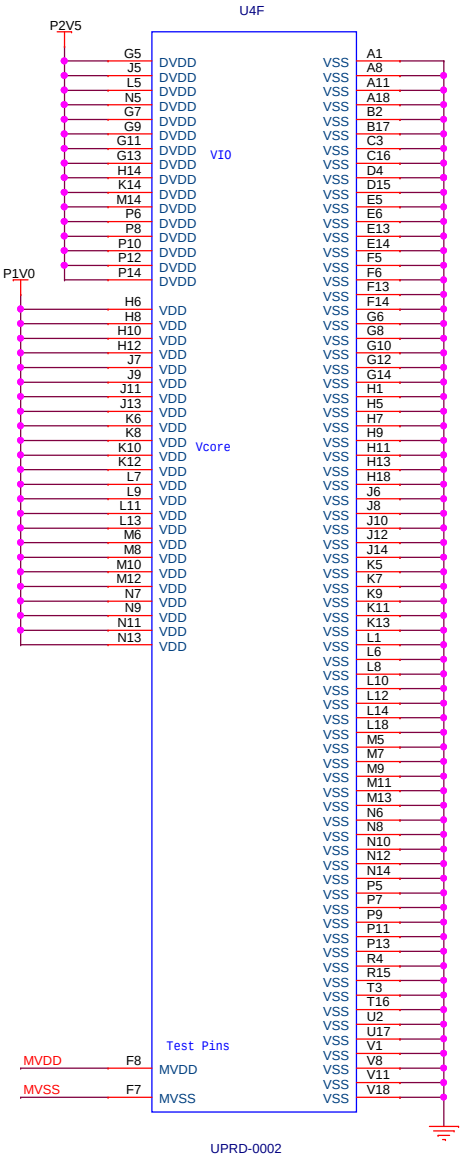


Place one per pin

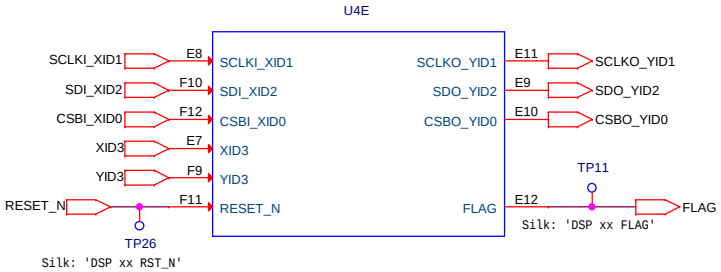


Place one per pin

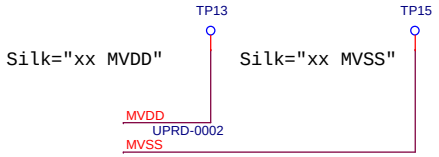




DSP Control



Layout note on TP silkscreen that xx corresponds to UL, UR, LL, LR



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Title: HB01-AAFM		
Page Contents: UR Anemone Power & Control		
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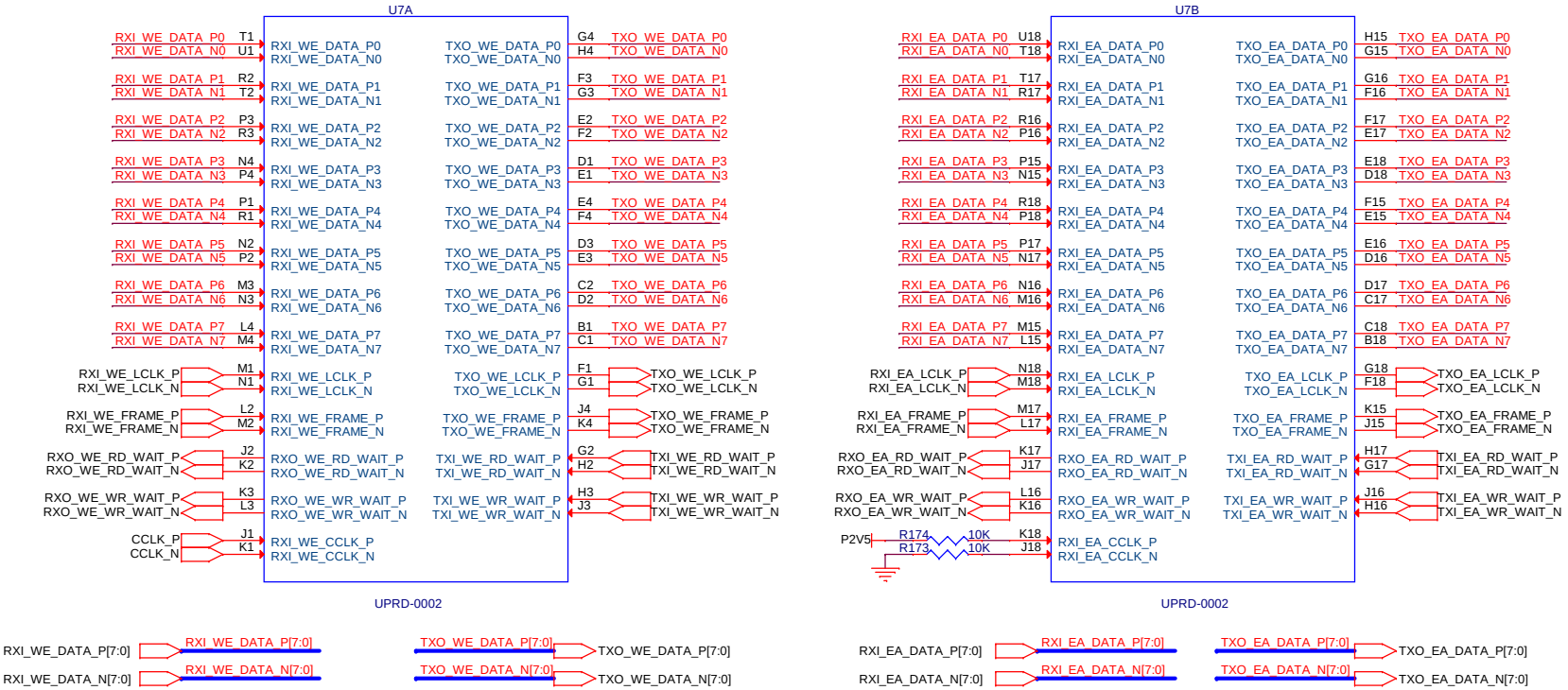
DSP Link Ports EAST/WEST



Place 100-ohm LVDS terminators close to DSP link receivers

BittWare SIGNAL PROCESSING SYSTEMS

Title:	HB01-AAFM	
Page Contents:	LL Anemone EAST/WEST Link Ports	
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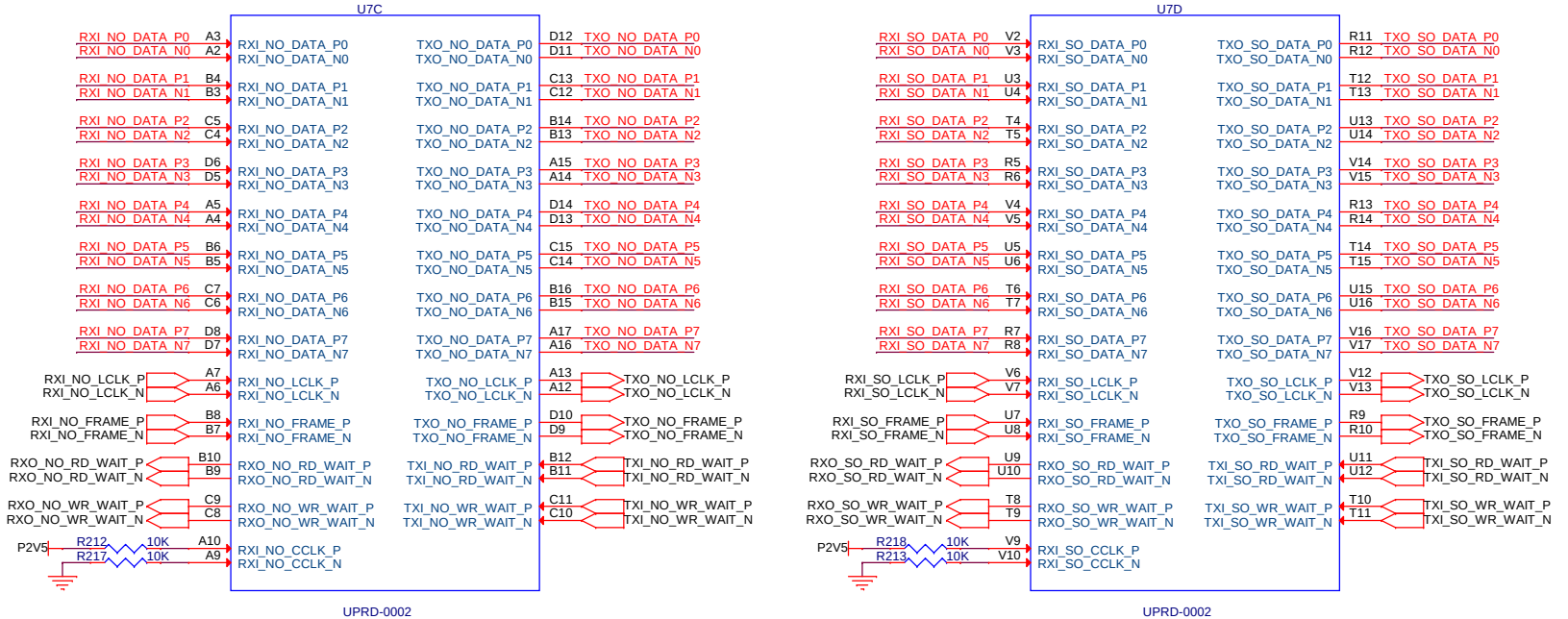
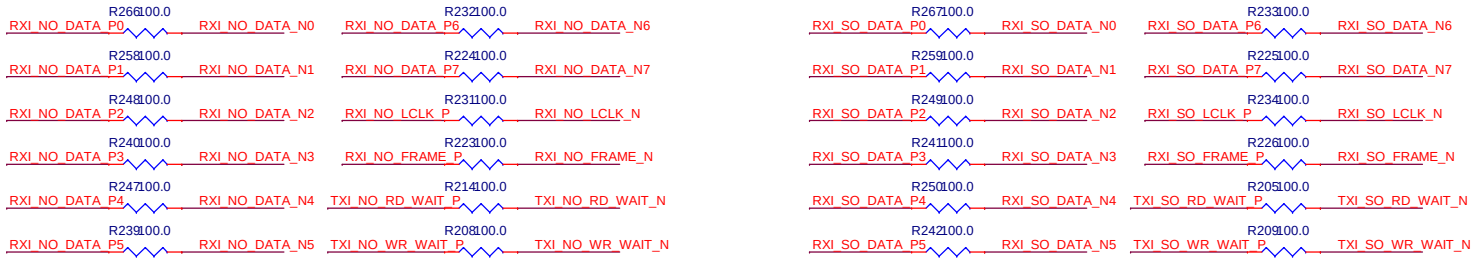
DSP Link Ports NORTH/SOUTH



Place 100-ohm LVDS terminators close to DSP link receivers



BittWare SIGNAL PROCESSING SYSTEMS

Title:	HB01-AAFM	
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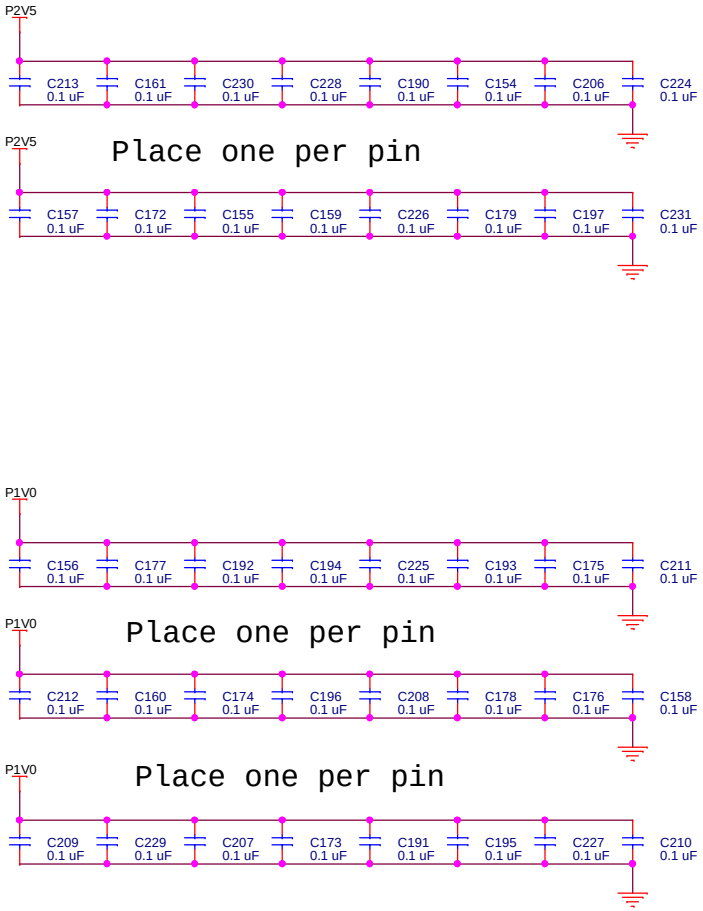
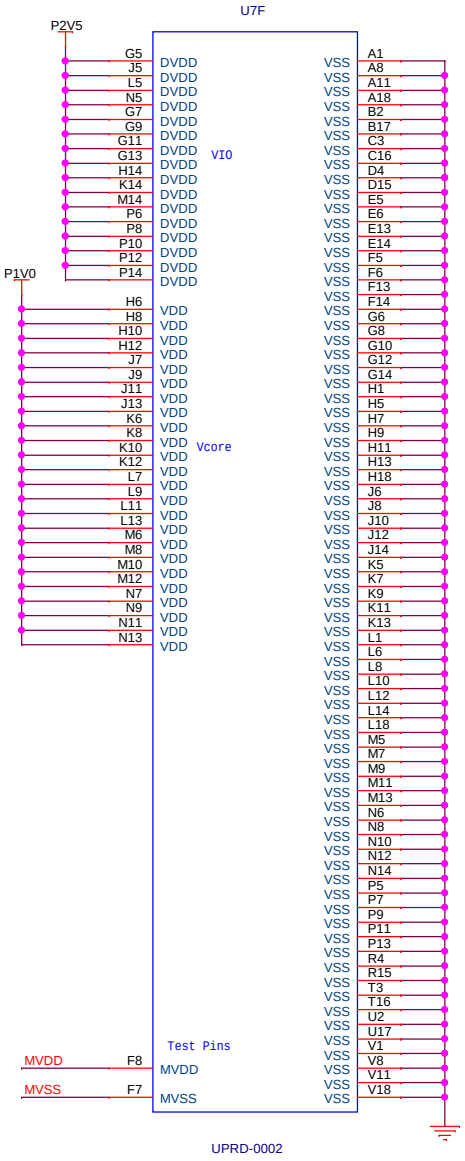
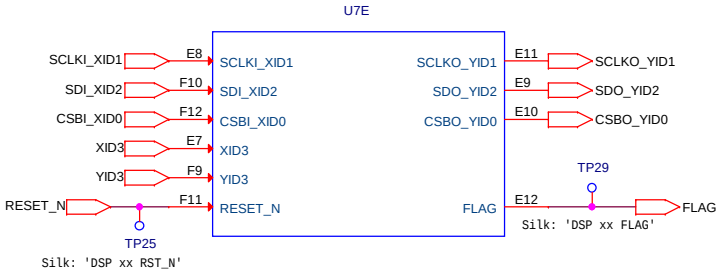
DVDD = IO supply (2.5V)
VDD = Core supply (1.0V)
VSS = Common ground

DSP Power

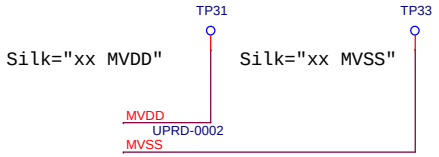




DSP Control



Layout note on TP silkscreen that xx corresponds to UL, UR, LL, LR



BittWare SIGNAL PROCESSING SYSTEMS

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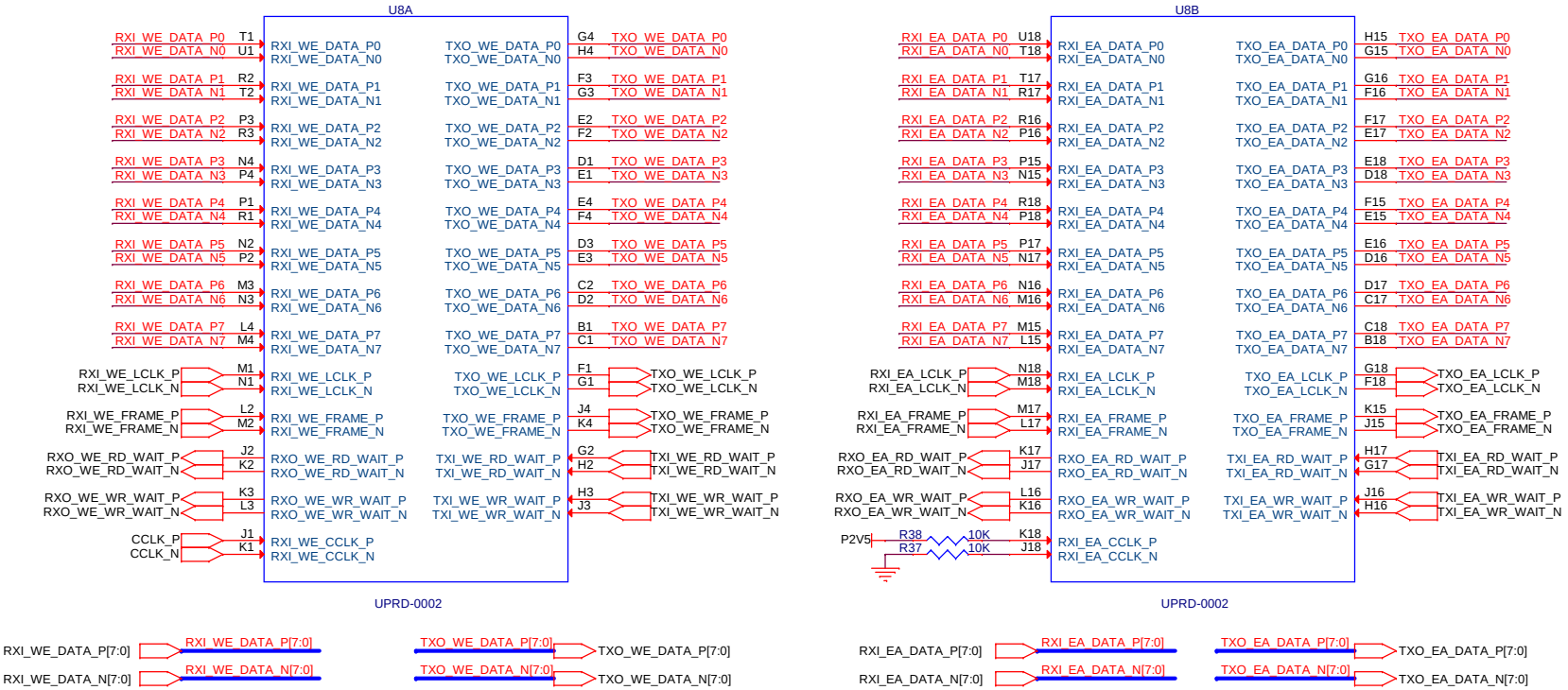
DSP Link Ports EAST/WEST



Place 100-ohm LVDS terminators close to DSP link receivers

BittWare SIGNAL PROCESSING SYSTEMS

Title:	HB01-AAFM	
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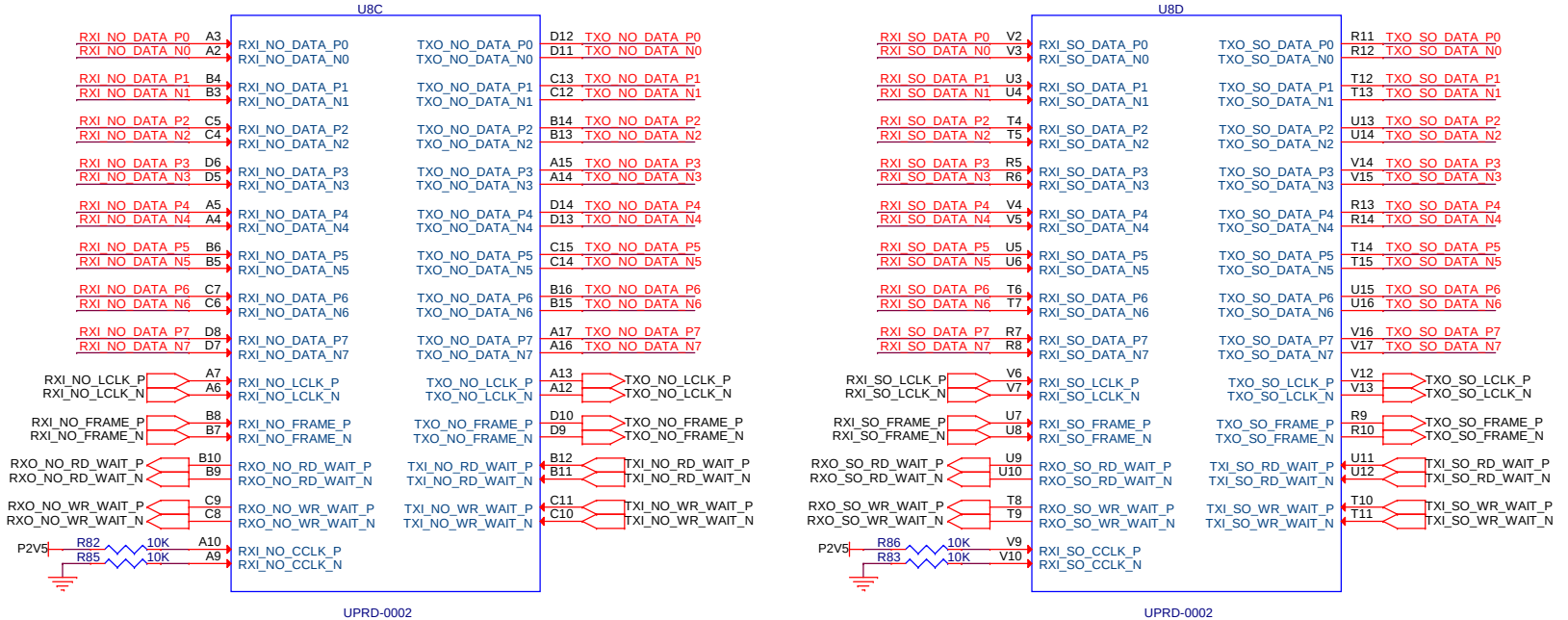
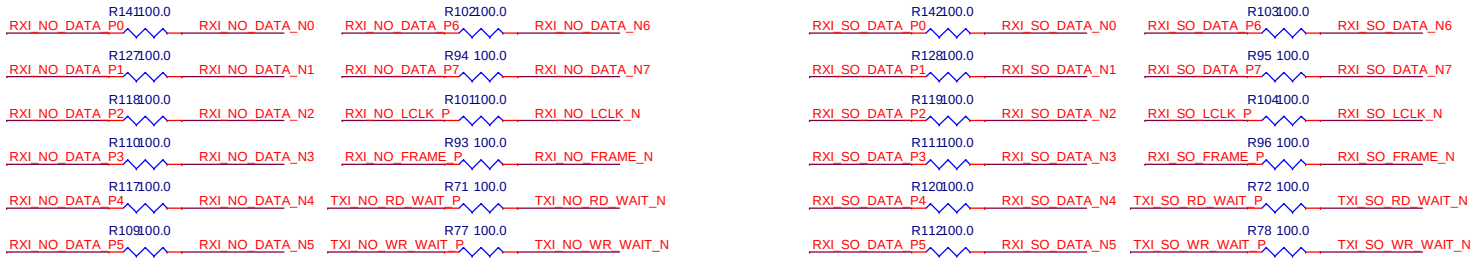
DSP Link Ports NORTH/SOUTH



Place 100-ohm LVDS terminators close to DSP link receivers



BittWare SIGNAL PROCESSING SYSTEMS

Title:	HB01-AAFM		
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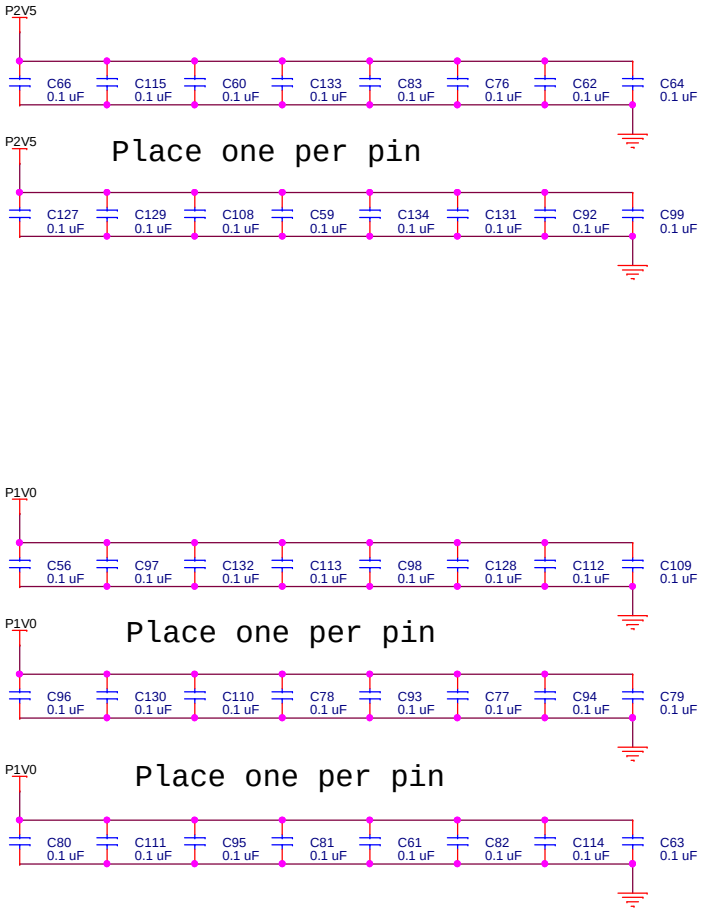
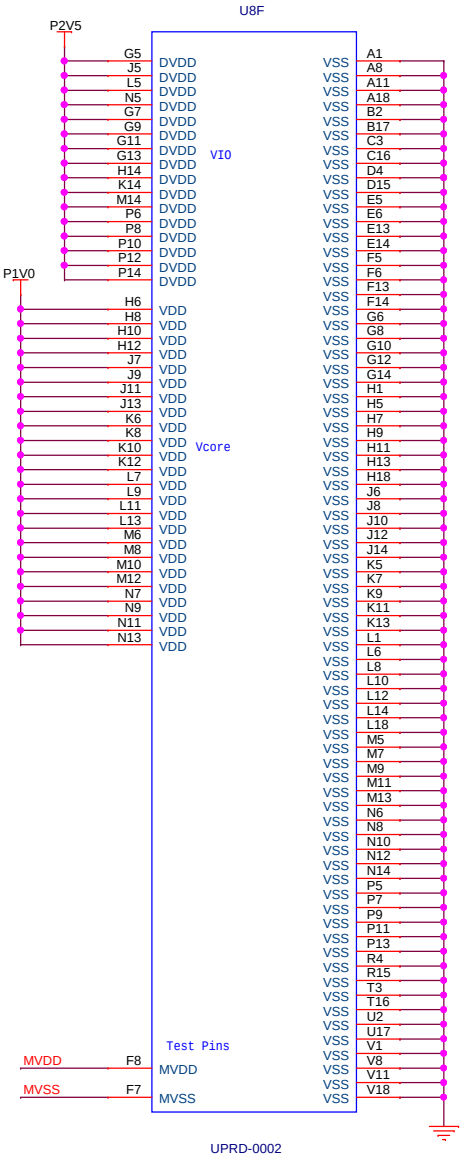
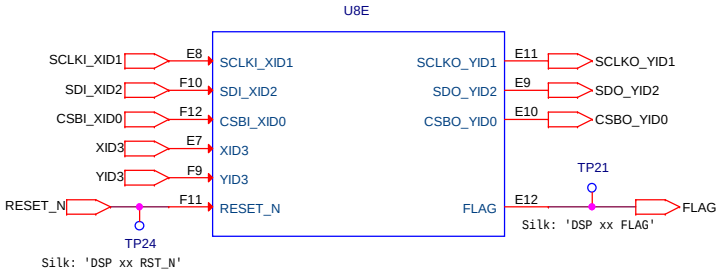
VDD = Core supply (1.0V)
VSS = Common ground

DSP Power

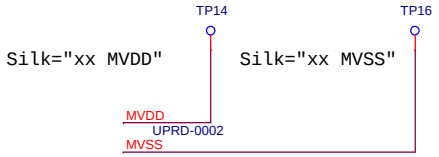




DSP Control



Layout note on TP silkscreen that xx corresponds to UL, UR, LL, LR



BittWare SIGNAL PROCESSING SYSTEMS

Title: HB01-AAFM		
Page Contents: LR Anemone Power & Control		
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Bank 1 VADJ

FMC_CPLD [1:0] → FMC_CPLD_[1:0]

U9A

UL_RESET_L, UR_RESET_L, LL_RESET_L, LR_RESET_L, UL_FLAG_DSP, UR_FLAG_DSP, LL_FLAG_DSP, LR_FLAG_DSP, FMC_CPLD_3, CPLD_0, CPLD_1, LED1, LED2, LED3, LED4, LED5, FMC_CPLD_CTRL_0

IO_B0_2 … IO_B0_28

IO_B0_29 … IO_B0_51

UL_FLAG_CPLD, UR_FLAG_CPLD, LL_FLAG_CPLD, LR_FLAG_CPLD

FMC_CPLD_0, FMC_CPLD_1 — Extra LA pins

PG_M2C, FMC_CPLD_2, FMC_CPLD_CSBI_XID0, FMC_CPLD_SCLKI_XID1, FMC_CPLD_SDI_XID2, FMC_CPLD_CSBO_YID0, FMC_CPLD_SCLKO_YID1, FMC_CPLD_SDO_YID2

FMC_CPLD_CTRL_1, FMC_CPLD_CTRL_2

FMC_RESET

TP20, TP19

FMC_CPLD is 4-bit wide bidir bus, but drawn as one 2-bit bus and two 1-bit buses

Bank 2 VADJ

U9B

UL_CSBI_XID0, UL_SCLKI_XID1, UL_SDI_XID2, UL_XID3, UL_CSBO_YID0, UL_SCLKO_YID1, UL_SDO_YID2, UL_YID3, UR_CSBI_XID0, UR_SCLKI_XID1, UR_SDI_XID2, UR_XID3, UR_CSBO_YID0, UR_SCLKO_YID1, UR_SDO_YID2, UR_YID3

CLK_CPLD_CTRL_0, CLK_CPLD_CTRL_1, CLK_CPLD_CTRL_2, CLK_CPLD_CTRL_3

IO_B1_1 … IO_B1_76

IO_B1_77 … IO_B1_100

LL_CSBI_XID0, LL_SCLKI_XID1, LL_SDI_XID2, LL_XID3, LL_CSBO_YID0, LL_SCLKO_YID1, LL_SDO_YID2, LL_YID3, LR_CSBI_XID0, LR_SCLKI_XID1, LR_SDI_XID2, LR_XID3, LR_CSBO_YID0, LR_SCLKO_YID1, LR_SDO_YID2, LR_YID3

PGOOD_1V0

CLK_CPLD_CTRL_4, CLK_CPLD_CTRL_5

PG_C2M used as CPLD reset

U9C

CPLD_GCLK_0, CPLD_GCLK_1, CPLD_CLK, PG_C2M

GCLK0p, GCLK1p, GCLK2p, GCLK3p, GNDINT, GNDINT, GNDIO …

PVADJ

VCCIO1, VCCIO1, VCCIO1, VCCIO2, VCCIO2, VCCIO2, VCCINT, VCCINT

TMS, TDO, TDI, TCK, DEV_OE, DEV_CLRn

FMC_TMS, FMC_TDO, FMC_TDI, FMC_TCK

MAX II JTAG VIO = VCCIO1 = VADJ = 2.5V

TP23 CPLD_GCLK_0 Silk = 'GCLK0'

TP22 CPLD_GCLK_1 Silk = 'GCLK1'

R202, R201, R200, R195 — 10K — UL_RESET_L, UR_RESET_L, LL_RESET_L, LR_RESET_L

FMC_CPLD_CTRL_[2:0] → FMC_CPLD_CTRL_[2:0]

CTRL Bus for FMC interface
Used to select active SPI port
Could also be used for sw control of active reset, DSP geo. address, AD9520 ref input

CLK_CPLD_CTRL_[5:0] → CLK_CPLD_CTRL_[5:0]

CTRL Bus for Clock Gen
[3:0] are CPLD Outputs
[5:4] are CPLD Inputs

0 REF_SEL
1 EEPROM
2 RST_L
3 PD_L
4 REFMON
5 LOCK

PVADJ

R297 DNI 10K, R298 DNI 10K

FMC_TCK D29, FMC_TDI D30, FMC_TDO D31, FMC_TMS D33, D34

FMC JTAG gate

P1L: TCK, TDI, TDO, TMS, TRST_L

J400-AV11

R299 1K DNI

RWI-586
Add wire connecting TP19 to AD9520 SYNC_L pin

CPLD_1 → CPLD_1

P3V3

Silk = 'Flag NW' DLED-0004 D5 LED1 100.0 R10

Silk = 'Flag NE' DLED-0004 D3 LED2 100.0 R11

Silk = 'Flag SW' DLED-0004 D4 LED3 100.0 R8

Silk = 'Flag SE' DLED-0004 D1 LED4 100.0 R6

Silk = 'Lock' DLED-0004 D2 LED5 100.0 R9

Vf = 2.2V typ.
Iled = 11mA

One 0402 per Max-II power pin

Bank 2 and VCCINT

PVADJ

C143 0.1 uF, C136 0.1 uF, C142 0.1 uF, C181 0.1 uF, C180 0.1 uF, C36 22.0 uF

GND

Bank 1

PVADJ

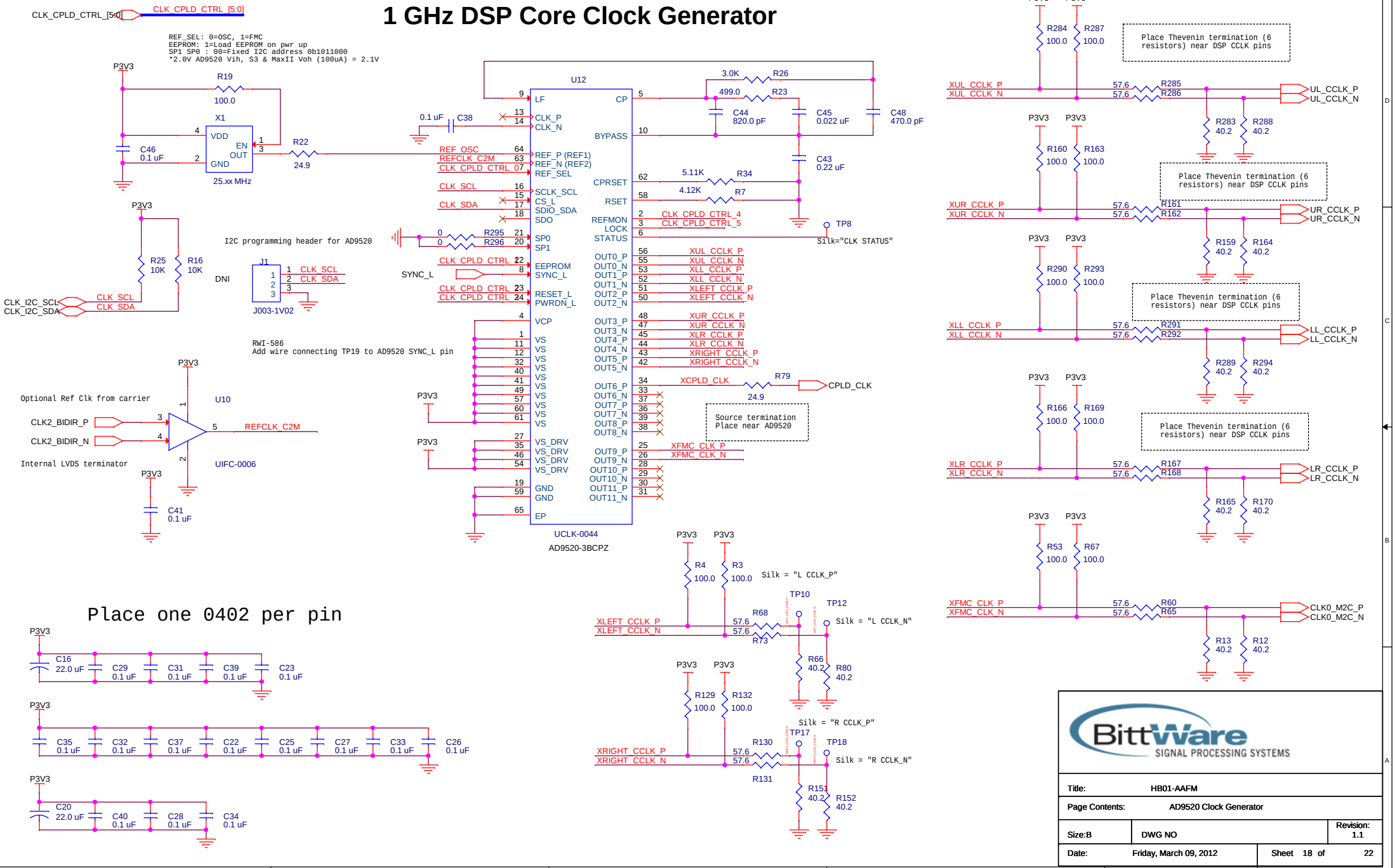
C139 0.1 uF, C118 0.1 uF, C141 0.1 uF, C30 22.0 uF

GND

BittWare SIGNAL PROCESSING SYSTEMS

Title:	HB01-AAFM	
Page Contents:	MAX II CPLD	
Size:B	DWG NO	Revision: 1.1
Date: Friday, March 09, 2012	Sheet 17 of 22	

1 GHz DSP Core Clock Generator



Title:	HB01-AAFM
Page Contents:	AD9520 Clock Generator
Size:B	DWG NO
Revision:	1.1
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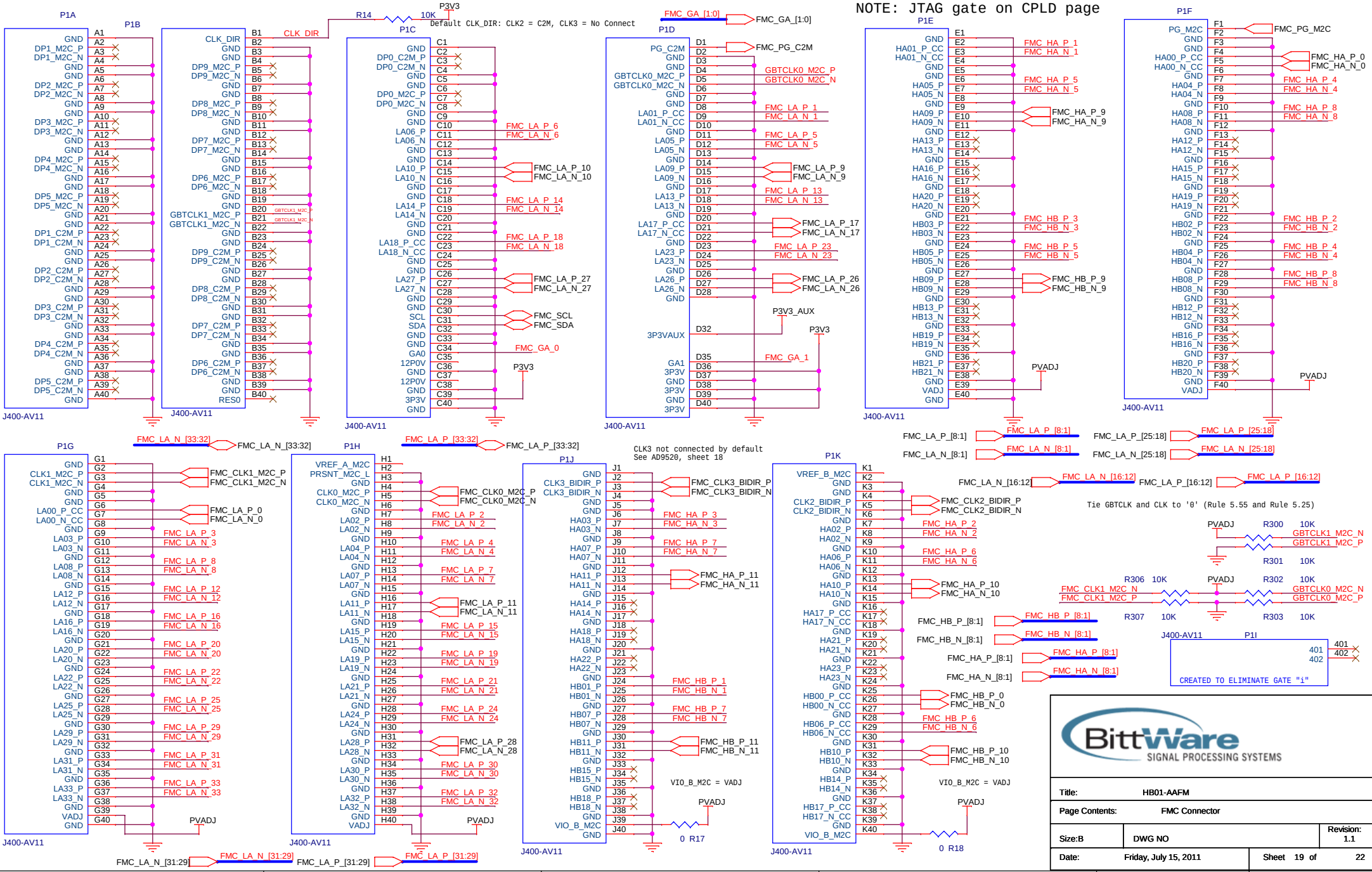
Sheet	18 of 22

NOTE: JTAG gate on CPLD page



BittWare SIGNAL PROCESSING SYSTEMS

Title:	HB01-AAFM	
Page Contents:	FMC Connector	
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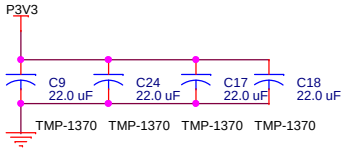
Default LTC3616 Settings:
RT/SYNC = SVIN: Internal 2.25MHz clock
MODE = 1.7V: Forced Continuous Mode
TRACK/SS = Track VADJ
ITH = SVIN: Internal compensation w/AVP mode
SLRM = GND: Max slew rate

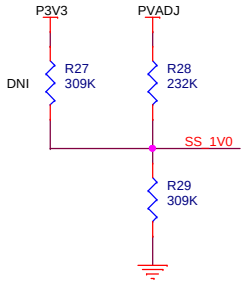
PGOOD_1V0 → PGOOD_1V0

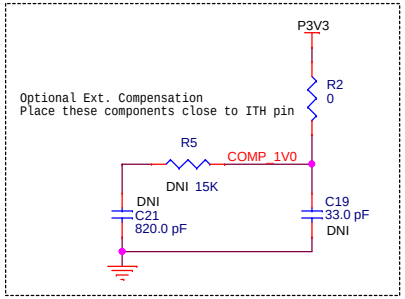
DSP Core Power: 1V @ 6A Max.

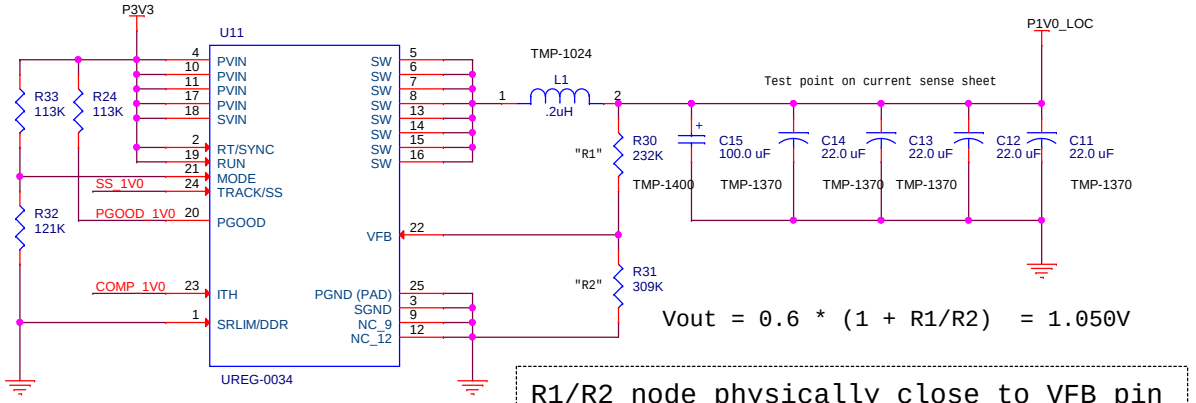
NOTE: Follow PC Board Layout Checklist on page 24 of LTC3616 Datasheet



Default tracks VADJ, but internal/external SS possible with component changes



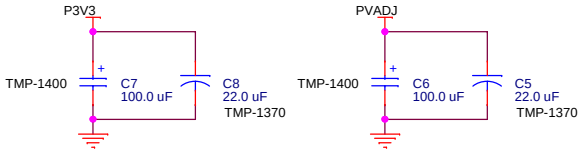


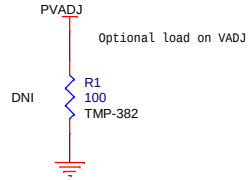


Vout = 0.6 * (1 + R1/R2) = 1.050V

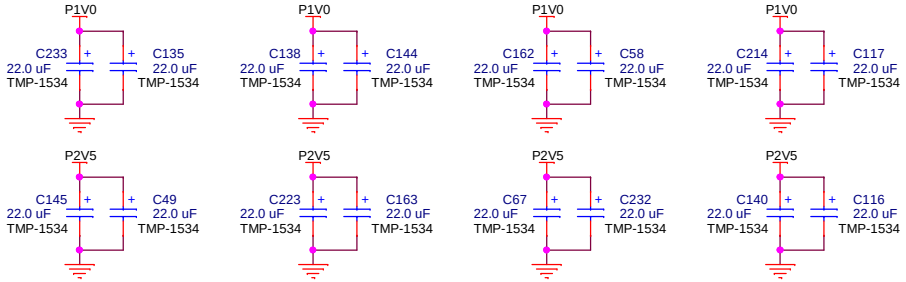
R1/R2 node physically close to VFB pin

Place bulk caps at FMC connector





Place bulk caps 2 per side of Anemone quad for each supply



BittWare SIGNAL PROCESSING SYSTEMS

Title:	HB01-AAFM	
Page Contents:	Local Power	
Size:B	DWG NO	Revision: 1.1
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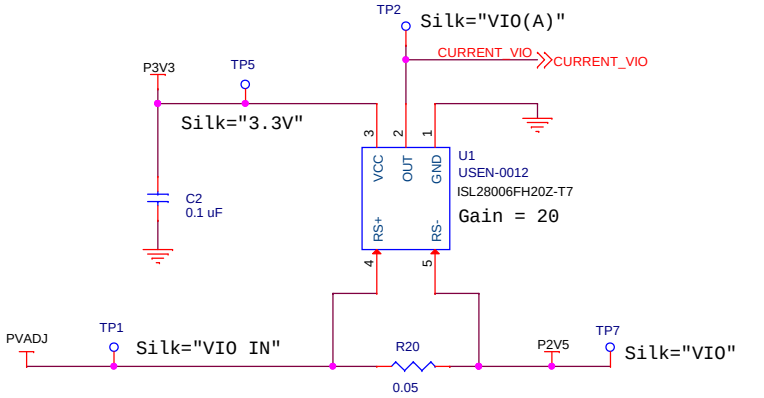
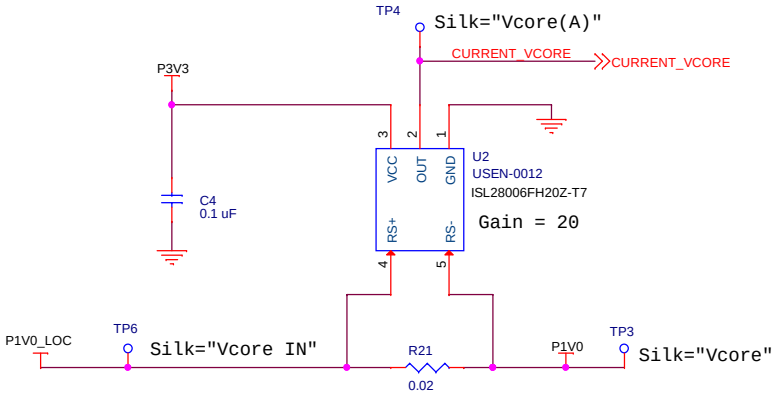
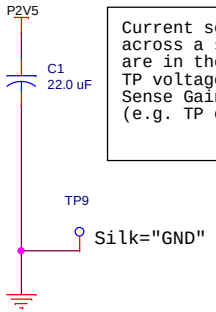
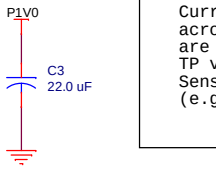
Current Sense Amplifiers







Current sense resistors (2512s) should be across a split plane. Layout guidelines are in the ISL28006 data sheet.
TP voltage will "equal" current since Sense Gain * Res = 20 * 0.05 = 1
(e.g. TP of 350mV means 350 mA)



Current sense resistors (2512s) should be across a split plane. Layout guidelines are in the ISL28006 data sheet.
TP voltage will "equal" 0.4 * current since Sense Gain * Res = 20 * 0.02 = 0.4
(e.g. TP of 350mV means 875mA or 1mV = 2.5mA)

BittWare SIGNAL PROCESSING SYSTEMS

Title: HB01-AAFM		
Page Contents: DSP Core and VIO Current Sense		
Size:B	DWG NO	Revision: 1.1
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FMC_GA_[1:0]

FMC_GA_[1:0]

I2C EEPROM
128k x 8-bits

P3V3_AUX

U5

GA_0 and GA_1 swapped as required by VITA 57.1

FMC_GA_1 1
FMC_GA_0 2
3
4

A0 VCC 8
A1 WP 7
A2 SCL 6
GND SDA 5

UMEM-0011

P3V3_AUX

C47
0.1 uF

ADDR = 0b10100xx
xx = GA_[0:1]

FMC_SCL
FMC_SDA

FMC_SCL
FMC_SDA

I2C pullups to P3V3_AUX on carrier

VREF=VDD

P3V3_AUX

PVADJ

U6

TMP-1370
C10
22.0 uF

C42
0.1 uF

8 VDD

CURRENT_VIO 3 VIN0
CURRENT_VCORE 4 VIN1
5 VIN2
6 VIN3/VREF

SCL 1 FMC_SCL
SDA 2 FMC_SDA

P1V0_LOC 7 GND

UADC-0005

AD7991-0 ADDR = 0b0101000 (default)
AD7991-1 ADDR = 0B0101001
Fixed address on ADC is spec violation

UADC-0005=ADC(0);UADC-0006=ADC(1)

Place LM75 temp sensor near middle of 4 DSPs

P3V3_AUX

U13

GA_0 and GA_1 swapped as required by VITA 57.1

FMC_SDA 1 SDA +Vs 8
FMC_SCL 2 SCL GND 4
FMC_GA_1 7 A0
FMC_GA_0 6 A1
5 A2 O.S. 3

C137
0.1 uF

USEN-0004

ADDR = 0b10010xx
xx = GA_[0:1]

4 holes for standoffs, connected to chassis GND

SO2 J001-1T01 DNI
SO1 J001-1T01 DNI
SO3 J001-1T01 DNI
SO4 J001-1T01 DNI

13 frame mounting holes, connected to chassis GND

FH1 J001-1T01 DNI
FH2 J001-1T01 DNI
FH3 J001-1T01 DNI
FH4 J001-1T01 DNI
FH5 J001-1T01 DNI
FH6 J001-1T01 DNI
FH7 J001-1T01 DNI
FH8 J001-1T01 DNI
FH9 J001-1T01 DNI
FH10 J001-1T01 DNI
FH11 J001-1T01 DNI
FH13 J001-1T01 DNI
FH12 J001-1T01 DNI

Isolates signal and chassis GND

R87 1M

Minimum of 500Vdc and 1M ohm
Rule 3.20

Mechanical Parts

PCB1
1 1

AAFM PCB Revision 01
TMP-1606
PCB AAFM Rev. 1

BittWare SIGNAL PROCESSING SYSTEMS

Title:	HB01-AAFM		
Page Contents:	I2C PROM/Temp Sensor & Misc		
Size:B	DWG NO		Revision: 1.1
Date:	Tuesday, July 19, 2011	Sheet 22 of	22