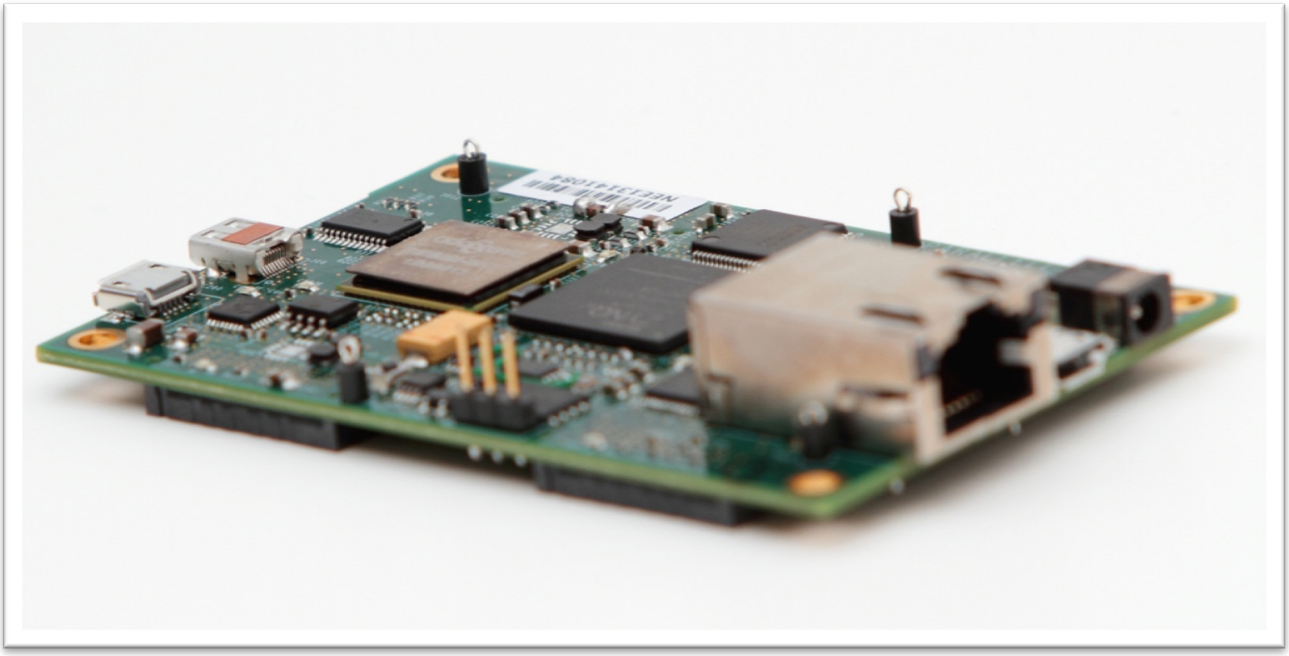
Parallella Reference Manual

Gen1

1.13.06.29

(PRELIMINARY, FOR REVIEW PURPOSES ONLY!)



Revision History

Version	Comments
0.13.2.13	Initial release
1.13.6.24	Updated PEC_POWER Pin outs Part Numbers Added + Document Links Changed flash to 128Mb Replaced 5V DC/USB power mux with pin header Changed power sub-system Epiphany now uses 1.8V IO voltage Added UART 2-pin header Changed license to creative common

Related Documents:

Epiphany Architecture Reference Manual:

http://www.adapteva.com/support/docs/e3-reference-manual

Epiphany SDK Reference Manual:

http://www.adapteva.com/support/docs/esdk3-manual

Epiphany-III Datasheet:

http://www.adapteva.com/products/silicon-devices/e16g301/

Epiphany-IV Datasheet:

http://www.adapteva.com/products/silicon-devices/e16g401/

Software Repositories:

Parallella Hardware and Software Repository

https://github.com/parallella/

Epiphany SDK Software Repository

https://github.com/adapteva

SD Card Images:

ftp://ftp.parallella.org

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1 Overview

The Parallella board is a high performance computing platform based on a dual-core ARM-A9 Zynq System-On-Chip and Adapteva's Epiphany multicore coprocessor.

Feature	Specification
CPU	Xilinx Zynq7000 Series (Z-7010 or Z-7020) Dual-Core ARM-A9 with 512KB L2 Shared Cache
Coprocessor	Epiphany Multicore Coprocessor The Parallella-16 board includes the 16-core Epiphany-III processor The Parallella-64 board includes the 64-cire Epiphany-IV processor
Memory	1024MB DDR3L
Boot Flash	128Mb QSPI Flash
Indicators	2 User controlled LEDs
USB 2.0 Port (0)	Connects to a host machine (PC/tablet/smartphone)
USB 2.0 Port (1)	Connect peripheral devices
Ethernet	10/100/1000 Ethernet, RJ45 with magnetics, LEDs
SD Connector	MicroSD, 3.3V
Video	Micro HDMI connector
Expansion Connectors	Four 60-pin high speed Samtec connectors for: • Epiphany link expansion connector(s) • Zynq programmable logic extension connector • Power, JTAG, debug connector
Power Source	USB or 5.0V DC
PCB	86.36mm x 53.34mm (3.4'' x 2.15'')

Table 1: Parallella Feature Summary

The Parallella is a dense credit card sized board. The active components and the majority of the standard connectors are placed on the top side of the board while the expansion connectors and uSD card connector are placed at the bottom side of the board. Standard interface connectors on opposite sides of the cards to allow easy access when sitting in a rack or closed box.

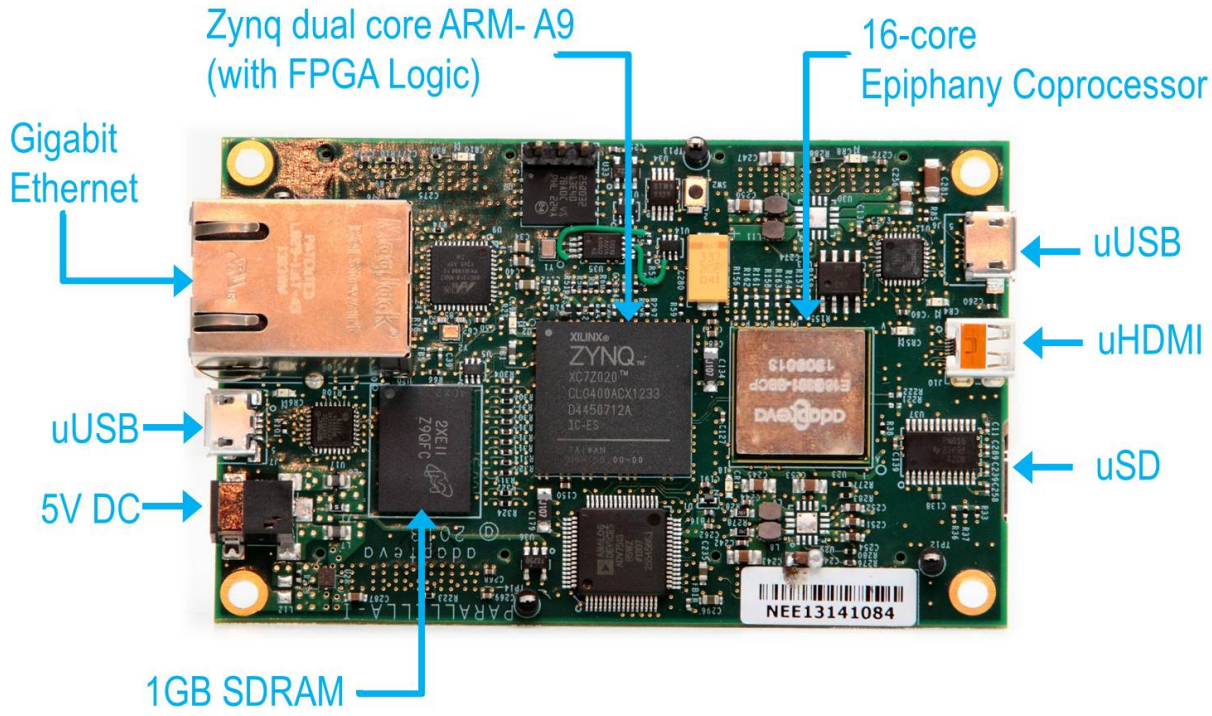


Figure 1: The Parallella Board

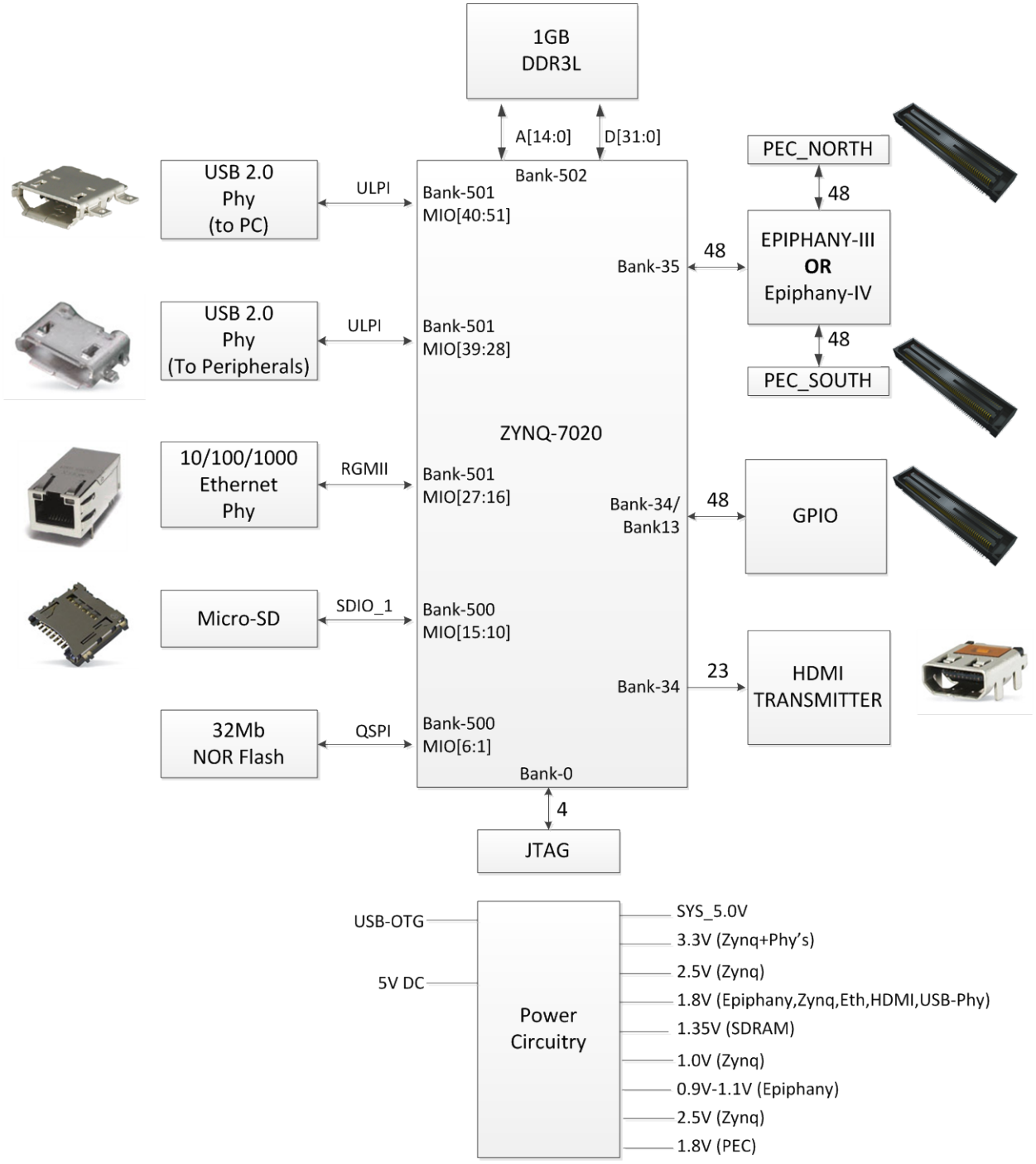


Figure 2: Zynq Connectivity Diagram

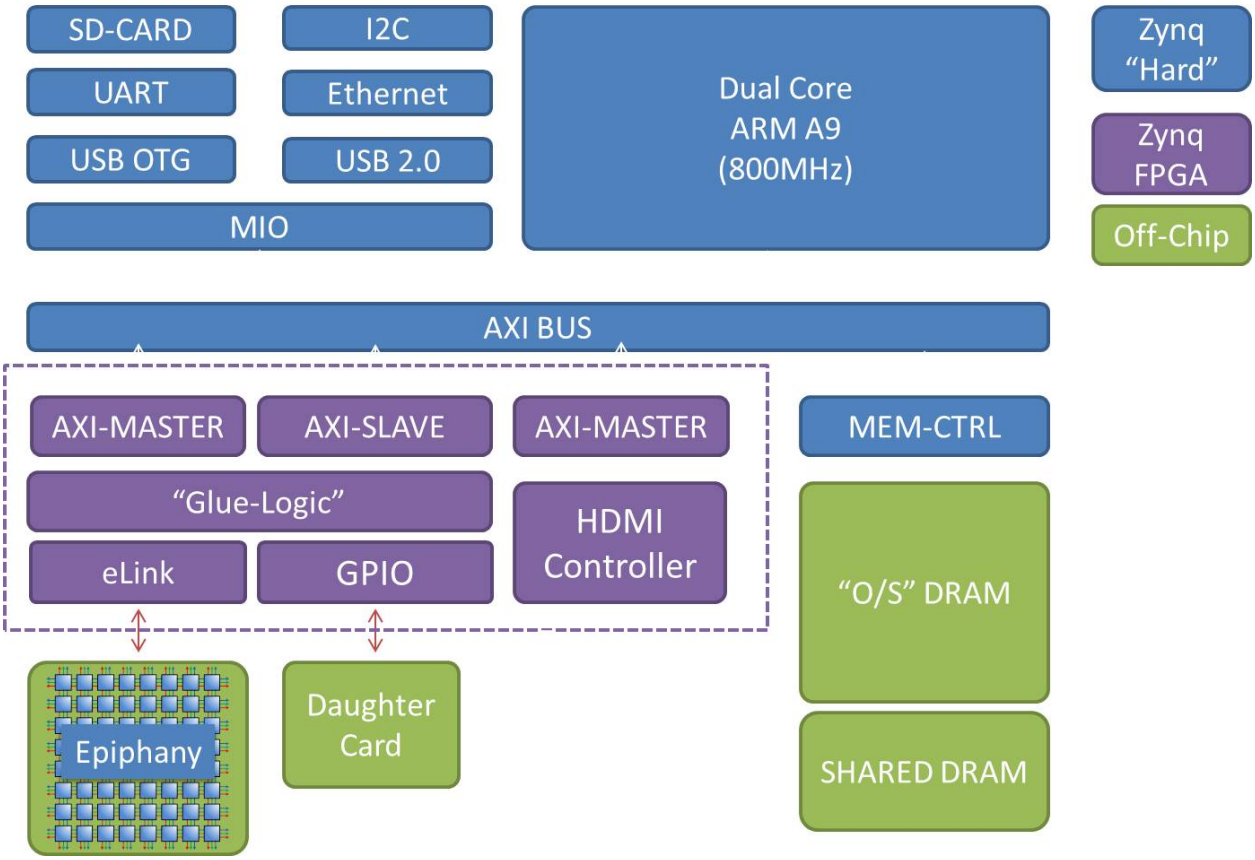


Figure 3: Parallella High Level Architecture

2 Parallella Features

2.1 Introduction

The Parallella board uses the components listed in the table below.

Type	Part Number	Documentation
CPU	Z-7010 OR Z-7020	http://www.xilinx.com/support/index.html/content/xilinx/en/supportNav/silicon_devices/soc/zynq-7000.html
Epiphany	E16G301 OR E64G401	http://www.adapteva.com/products/silicon-devices/e16g301/ http://www.adapteva.com/products/silicon-devices/e16g401/
Eth PHY	88E1318	N/A
USB PHY	USB3320C-EZK-TR	http://www.smsc.com/Products/USB/USB_Transceivers/USB3320/Download
HDMI PHY	ADV7513BSWZ	http://www.analog.com/en/audiovideo-products/analoghdmidvi-interfaces/adv7513/products/product.html
SDRAM	MT41K256M32SLD	http://www.micron.com/~/media/Documents/Products/Data%20Sheet/DRAM/DDR3L_8Gb_x32_1CS_TwinDie_V70S_V80A.pdf
Flash	N25Q128A13EF840E	http://www.micron.com/parts/nor-flash/serial-nor-flash/n25q128a13ef840e
PMIC #1	ISL9307	http://www.intersil.com/content/dam/Intersil/documents/fn79/fn7931.pdf
PMIC #2	ISL9305	http://www.intersil.com/content/dam/Intersil/documents/fn76/fn7605.pdf

Table 2: Parallella Component Summary

2.2 CPU

The central processor on the Parallella board is the Zynq™-7000 AP SoC. The Zynq represents a new class of processor product which combines an industry-standard ARM® dual-core Cortex™-A9 MPCore™ processing system with Xilinx 28nm programmable logic. The Zynq SoC includes the following set of features:

Dual-core ARM® Cortex™-A9 CPU:

- Coherent multiprocessor support
- ARMv7-A architecture
- 32 KB Level 1 4-way set-associative instruction/data caches (independent for each CPU)
- 512 KB 8-way set-associative Level 2 cache shared between CPUs
- TrustZone® security
- Jazelle® RCT execution Environment Architecture
- NEON™ media-processing engine
- Single and double precision Vector Floating Point Unit (VFPU)
- CoreSight™ and Program Trace Macrocell (PTM)
- Three watchdog timers, one global timer, two triple-timer counters

I/O Peripherals and Interfaces:

- 10/100/1000 tri-speed Ethernet MAC peripherals GMII, RGMII, and SGMII interfaces
- Two USB 2.0 OTG peripherals
- Two full CAN 2.0B compliant CAN bus interfaces
- Two SD/SDIO 2.0/MMC3.31 compliant controllers
- Two full-duplex SPI ports with three peripheral chip selects
- Two high-speed UARTs (up to 1 Mb/s)
- Two master and slave I2C interfaces
- 8-Channel DMA Controller with scatter/gather capability
- JTAG port for ARM debugging and FPGA programming
- 12 bit ADC input
- On-chip voltage and temperature sensing

Programmable Logic:

- LVCMOS, LVDS, and SSTL signaling with 1.2V to 3.3V IO
- Easily accessible from ARM cores through AXI bus(master or slave)
- Up to 125 programmable IO pins (Z-7020)
- Up to 85K programmable logics cells (Z-7020)
- Up to 560 KB distributed RAM (Z-7020)
- Up to 220 DSP slice and (Z-7020)

The Parallella board can be built with two different pin compatible Zynq devices: the Zynq Z-7010 and Zynq Z-7020. The major differences between the Z-7010 and Z-7020 are summarized in Table 4:

	Z-7010	Z-7020
Programmable Logic Cells	28K	85K
Look-Up Tables	17,600	53,200
Flip-flops	35,200	106,400
Extensible Block RAM	240KB	560KB
Programmable DSP Slices	80	220
Bank-13 IO Pins	No	Yes

Table 3: Parallella Zynq Versions

2.3 Epiphany Coprocessor

The Parallella-16 includes the E16G301 device with 16 CPU cores and the Parallella-64 includes the E64G401 device with 64 CPU cores. Both devices have the following basic features:

Epiphany Core (eCore):

- 32-bit RISC core
- Dual-issue superscalar architecture
- Quad-bank 32KB local single cycle access memory
- Floating point instruction set (IEEE754)
- 64-entry register file
- Dual channel DMA engine
- Two 32-bit timers
- Nested interrupt controller
- Memory protection unit
- Debug unit

Network-On-Chip (eMesh):

- Three separate networks:
    - rMesh for read transactions
    - xMesh for off-chip write transactions
    - cMesh for on-chip write transactions
- "API-less" network that processes regular load/store transactions
- All transactions are complete and atomic 104 bit transactions (32 bit address, 64 bit data, and 8 control bits)
- Round robin arbitration at every mesh node
- Mesh network extends off chip enabling glue-less multi-chip design

Chip-To-Chip Links (eLink):

- North, east, west, south links for connecting to other Epiphany chips, FPGAs, or ASICs
- Muxes and serializes 104 bit eMesh transactions
- Source synchronous LVDS links with transmit clock aligned in the middle of the data eye
- Dual data rate communication (positive and negative edge transfers)
- Max transfer of 2 bytes transferred in and out simultaneously per link per clock cycle
- Automatic bursting for sequential 64-bit write transactions

2.4 SDRAM

1GB 32-bit wide DDR3L SDRAM

2.5 Flash

128Mb QSPI Flash Memory

2.6 Gigabit Ethernet

10/100/1000 Ethernet, RJ45 connector with magnetics.

2.7 USB 2.0 (0) PC Connection

Connects to a host PC. Connector can be used to power the Parallella board.

2.8 USB 2.0 (1) OTG connection

Connects to peripheral devices such as mice, keyboard, camera, etc.

2.9 Micro SD

Primary boot source and main Parallella board storage medium.

2.10 HDMI Port

A high quality connection to modern DVI/HDMI monitors and TVs through a micro-HDMI connector.

2.11 LED Indicators

- Two green user controlled LEDs. One controlled by Zynq and one by the Epiphany.
- Two LEDs on the RJ45. The left LED indicates link speed.(amber=1Gb, green=100Mb,off=10Mb). The right indicates that there is activity on the port.

2.12 Reset Button

Pushing the reset button resets all components on board including the Zynq CPU.

2.13 Serial Port

Two-pin header for 3.3V UART output from the Zynq.

2.14 JTAG Debugging

FPGA programming and debugging of programs running on the Zynq is possible through the JTAG connections on the PEC_POWER connector.

2.15 Parallella Power Sub-System

The Parallella board is powered from a 5V DC supply through the 2.1mm barrel connector jack Under light loads it will also be possible to power the board directly from the USB (0) connector. The power rails are regulated by the Intersil PMICs ISL9307 and ISL9305 as shown in the following Figure.

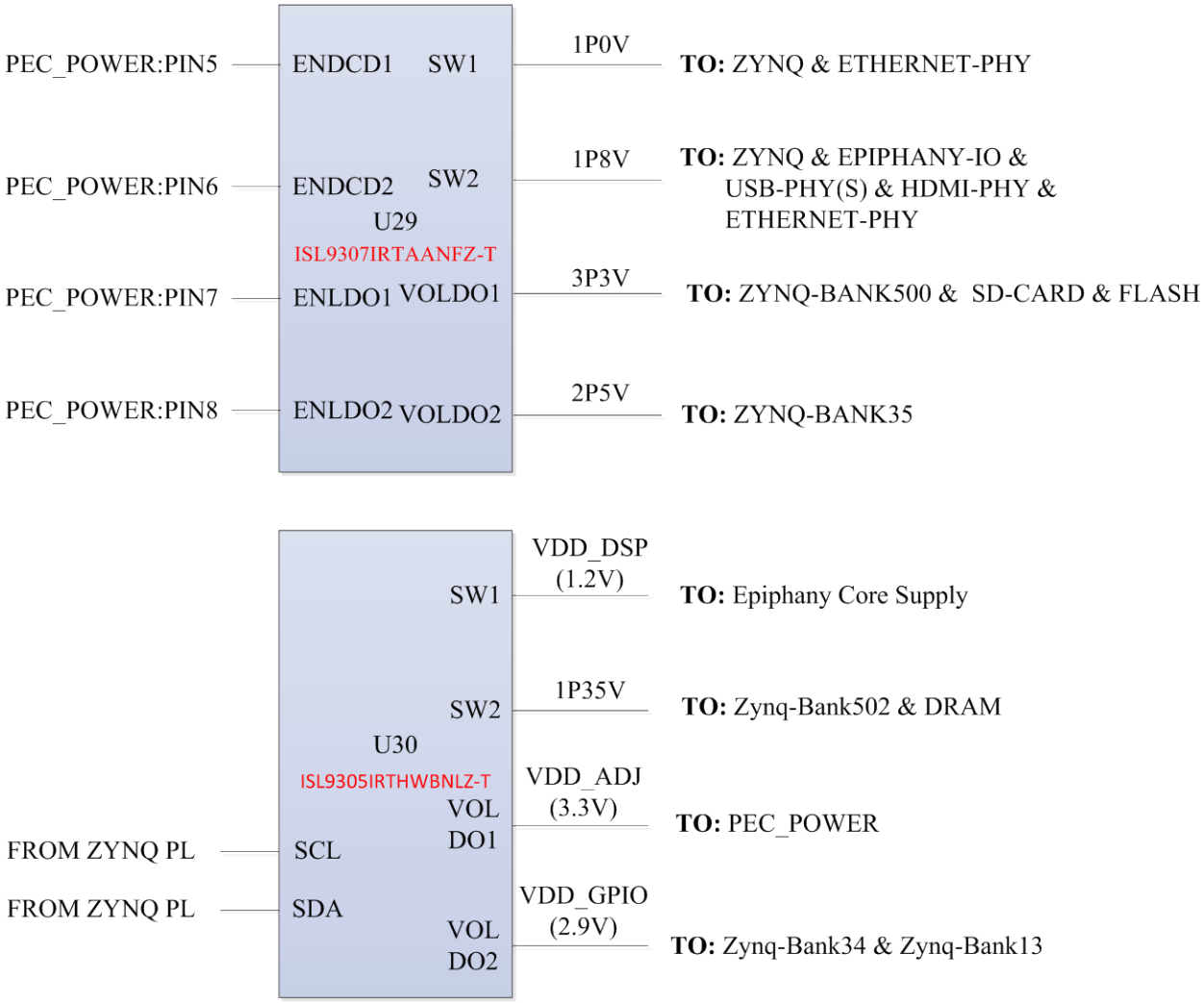


Figure 4: Power Sub-System

All four voltage rail outputs on the ISL9305 can be set by programming the appropriate registers within the chip using the I2C interface. The Parallella on-board flash will contain the appropriate programming sequence to set the VDD_DSP rail to 1.0V and the VDD_GPIO rail to 2.5V automatically at boot time.

The Parallella can power expansion cards directly using the PEC_POWER connector. The two on-board PMICs can deliver 1.5A on each step-down converter output and 300MA on each general purpose LDO output. The amount of current drawn by the Parallella board will depend on the level of activity on the board and the amount of current left over for the expansion card is yet to be characterised.

NOTE: At this time, the PEC_POWER feature should be considered experimental. The safest power solution for expansion cards is to: 1.) Have a completely independent power sub system or 2.) To use the 5V PEC_POWER rail.

Each one of the Parallella rails can also be powered directly from the PEC_POWER connector instead of from the on board power management ICs. Each rail to be driven from an external connector would first need to be powered down appropriately to avoid damaging the circuitry. To disable one of the ISL7307 outputs, pull down the corresponding REG_EN* signal available on the PEC_POWER connector. To disable one of the ISL9305 outputs, program the appropriate registers using the I2C interface.

NOTE: There WILL be permanent damage to the board the power rails are driven incorrectly. Please exercise extreme care!

2.16 Parallella Expansion Connectors

The Parallella board has four expansions connectors placed on the opposite edges of the bottom side of the board shown in Figure 4. For exact connector and placement information, please refer to the Parallella mechanical drawings. The following figure shows the expansion connector placements as seen from the bottom side of the board.

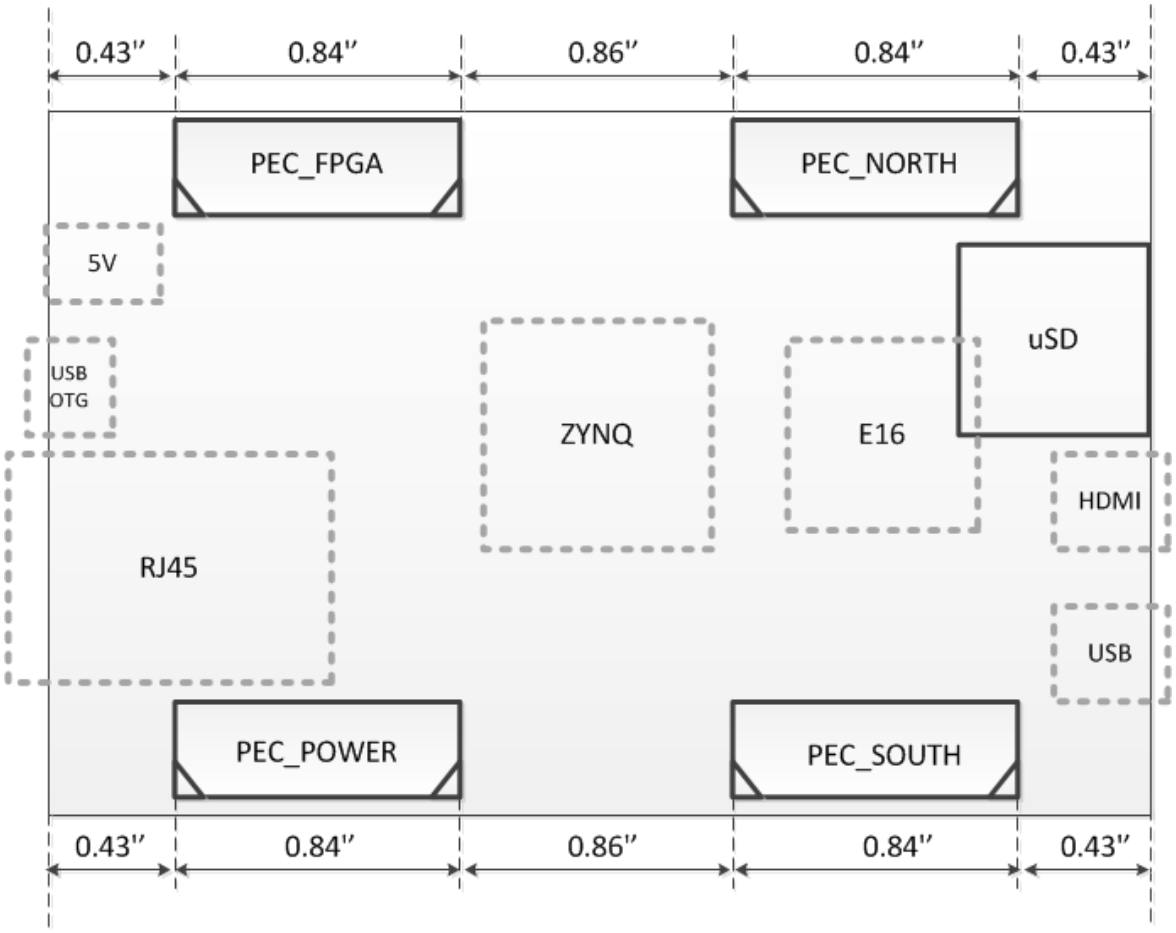


Figure 5: PEC Placement

The Parallella Expansion Connectors uses the 60 pin BSH-030-01-FDA high speed connector from Samtec. The corresponding mating connector to be placed on the expansion card is BTH-030-01-FDA. The complete data sheets can be found at:

https://www.samtec.com/technical-specifications/Default.aspx?SeriesMaster=BSH

A complete characterization report for the Samtec connectors can be found at:

http://www.samtec.com/Documents/WebFiles/TestRpt/172630_report_rev_2_qua.pdf

Connector	Functions
PEC_POWER	Power and control signal expansion connector
PEC_FPGA	Zynq programmable logic expansion connector
PEC_NORTH	Epiphany north link expansion connector
PEC_SOUTH	Epiphany south link expansion connector

Table 4: Parallella Expansion Connectors (PEC)

The four symmetrically placed connectors allow for robust mating of expansion cards and the Parallella board using matching BTH-030-01-FDA connectors. As shown in Figure 5, it is possible to connect a single full length credit card sized expansion cards or two half-length expansion cards. The left side shows two half-length expansion boards (pink/green transparent) connected to the backside of the Parallella board and the right side shows a full length (blue transparent) expansion board connected to the backside of the Parallella board.

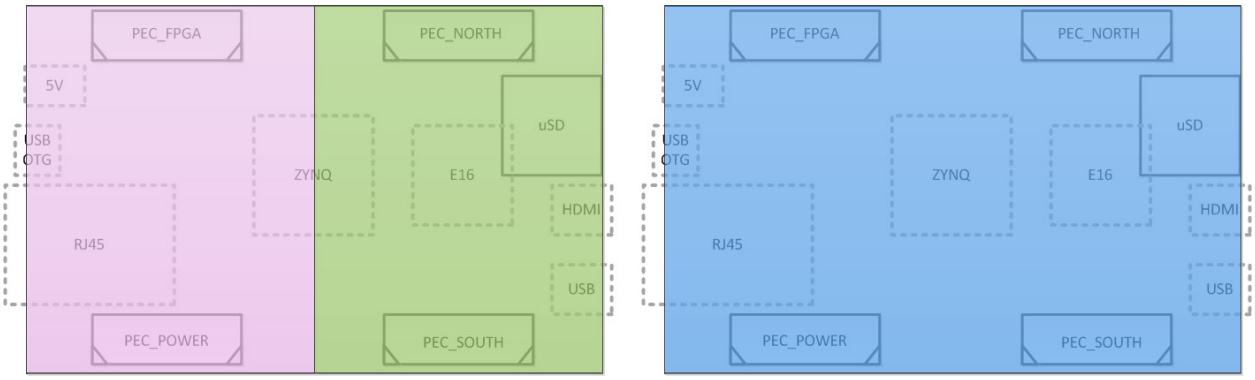


Figure 6: Expansion Card Configuration

2.17 Mounting Holes

The board has four symmetrically placed mounting holes, one in each corner. The mounting holes have a diameter of 0.125".

Three of the mounting holes are connected to ground while the fourth mounting hole is floating. This floating mounting hole can be connected to the 5V supply as a build or solder option, allowing power to be easily applied to a stack of Parallella boards without the need for extensive 5V DC cabling.

3 Parallella System Architecture

3.1 Zynq Memory Map

The following Table shows the hard-coded memory architecture of the Zynq architecture most relevant to the Parallella architecture. For a complete description of the Zynq of the memory architecture, please refer to the Architecture Reference manual for the Zynq.

Address Start	Address End	Size	Function	Note
0x0010_0000	0x3FFF_FFFF	1GB	DRAM	Accessible to all interconnect masters
0x4000_0000	0x7FFF_FFFF	1GB	PL	Custom logic address range
0x8000_0000	0xBFFF_FFFF	1GB	PL	Epiphany address range
0xFC00_0000	0xFCFF_FFFF	16MB	FLASH	Quad-SPI linear address for linear mode
0xFFFC_0000	0xFFFF_FFFF	252KB	OCM	OCM upper address range

Table 5: Zynq Memory Map

The ARM communicates with programmable logic, GPIO connected to the programmable logic, and the Epiphany by accessing the memory ranges shown in the table.

The Epiphany 32-bit memory space is mapped into the Zynq memory space allowing for easy sharing of data and resources between the ARM and the Epiphany. The Epiphany address range is a matter of convention and depends on the appropriate AXI master and slave interfaces being implemented within the programmable logic on the Zynq.

3.2 Epiphany Memory Map

The Epiphany chip is situated within a 1GB section within the Zynq host processor memory map. The offset within the 1GB space occupied by an Epiphany coprocessor is set by the ROWID and COLID pins on the Epiphany chip. The ROWID and COLID can be individually set on boards through the PEC_POWER connector enabling direct board to board connection through the PEC_NORTH and PEC_SOUTH connectors. By default the address locations of the Epiphany cores on Parallella-16 are as shown in the Table below.

Chip Core Number	Start Address	End Address	Size
(32,8)	80800000	80807FFF	32KB
(32,9)	80900000	80907FFF	32KB
(32,10)	80A00000	80A07FFF	32KB
(32,11)	80B00000	80B07FFF	32KB
(33,8)	84800000	84807FFF	32KB
(33,9)	84900000	84907FFF	32KB
(33,10)	84A00000	84A07FFF	32KB
(33,11)	84B00000	84B07FFF	32KB
(34,8)	88800000	88807FFF	32KB
(34,9)	88900000	88907FFF	32KB
(34,10)	88A00000	88A07FFF	32KB
(34,11)	88B00000	88B07FFF	32KB
(35,8)	8C800000	8C807FFF	32KB
(35,9)	8C900000	8C907FFF	32KB
(35,10)	8CA00000	8CA07FFF	32KB
(35,11)	8CB00000	9CB07FFF	32KB

Table 6: Epiphany System Registers

3.3 Parallella FPGA Design

NOTE: Developers that modify the FPGA logic or create designs from scratch should be aware that there is a very real danger of causing permanent damage to the board if incorrect pin constraints are used.

3.4 Epiphany Specific FPGA Resources

Developers that want leverage the Epiphany co-processors should use the Parallella programmable logic reference design with minimal changes for best results. The following registers must be accessible by the Epiphany drivers from the ARM for correct operation.

Register	Address	Details
REG_SYSCFG	0x808f0f00	[31:28] - Control mode for eMesh transaction [27:3] - Reserved [2:1] - Filter enable 00: Filter disable 01: Inclusive range. Block transactions inside REG_FILTERL and REG_FILTERH range) 10: Exclusive range. Block transactions outside REG_FILTERL and REG_FILTERH range) 11: Reserved [0] - Reserved
REG_RESET	0x808f0f04	A write transaction to this register resets "resetable" fpga logic and the Epiphany chip.
REG_VERSION	0x808f0f08	Read only register containing the version number for the FPGA logic
REG_FILTERL	0x808f0f0c	32-bit Transaction Filter Register (Low), [1:0] are ignored
REG_FILTERH	0x808f0f10	32-bit Transaction Filter Register (High), [1:0] are ignored
REG_FILTERC	0x808f0f14	[31:2] - Captured address of a filter violation [1:0] - Status 00 - not a valid value 01 - First violating transaction 10 - Second violating transaction 11 - There are more than 3 violating transactions A write to this register clears value to zero

Table 7: Epiphany System Registers

The Epiphany coprocessor is connected to the Zynq SOC via the 48-pin eLink. An Epiphany eLink protocol is implemented in the programmable logic portion of the Zynq SOC. In addition to the eLink interface, the programmable logic block shipped with the Parallella board includes an AXI master interface, an AXI slave interface, and an HDMI controller.

4 Parallella Expansion Connector Details

4.1 PEC_POWER

The PEC_POWER provides convenient access to various key Parallella board signals and can provide power to expansion boards with modest current requirements. Expansion boards with substantial current requirements should draw power from the SYS_5P0V connection or generate supply rails from a completely independent DC supply.

Signal	Direction	Max	Notes
SYS_5P0V	Inout	5.0V	Parallella expansion board supply. Driven by output of power selector 3-pin header that selects between DC power and USB power.
1P0V	Inout	1.0V	Core voltage for Zynq and Ethernet PHY. Driven by 1.5A switching regulator output of PMIC.
VDD_DSP	Inout	1.0V	Core voltage for Epiphany coprocessor. Driven by 1.5A switching regulator output of PMIC.
1P35V	Inout	1.35V	Supply shared by Zynq and DDR3L SDRAM. Driven by 1.5A switching regulator output of PMIC.
1P8V	Inout	1.8V	General purpose voltage shared by USB PHY, Ethernet PHY, Epiphany, Zynq, and HDMI. Driven by 1.5A switching regulator output of PMIC.
2P5V	Inout	2.5V	IO voltage for Zynq LVDS interface that communicates with the Epiphany coprocessor. Driven by 300mA LDO output of PMIC.
3.3V	Inout	3.3V	IO voltage for Zynq, HDMI, and flash chip. Driven by 300mA LDO output of PMIC.
VDD_GPIO	Inout	3.3V	IO voltage for Zynq, HDMI, and flash chip. Driven by 300mA LDO output of PMIC.
VDD_ADJ	Inout	3.3V	Independent supply output for expansion cards. Driven by 300mA LDO output on PMIC.
GND	Inout	0.0V	System Ground
I2C_SDA	Inout	5.0V	I2C bidirectional open-drain Serial Data Line
I2C_SCL	Inout	5.0V	I2C bidirectional open-drain Serial Clock Line
UART_TX	Output	3.3V	UART transmit signal
UART_RX	Input	3.3V	UART receive signal
SPDIF	Output	2.5V	Single bit SPDIF audio interface output

RESET_N	Output	3.3V	Active low Parallella board reset signal
USER_LED	Output	3.3V	On board LED signal driven by Zynq
DSP_XID[3:0]	Input	1.8V	Sets the relative chip column ID of the Epiphany chip on the Parallella board, overriding the default board settings. These signals must be driven correctly in systems that utilize the PEC_NORTH/PEC_SOUTH to connect multiple Parallella boards.
DSP_YID[3:0]	Input	1.8V	Sets the relative chip row ID of the Epiphany chip on the Parallella board, overriding the default board settings. These signals must be driven correctly in systems that utilize the PEC_NORTH/PEC_SOUTH to connect multiple Parallella boards.
DSP_FLAG	Output	1.8V	Flag signal driven by the Epiphany.
TURBO_MODE	Output	3.3V	Driven high when the Parallella board is powered from a 5V DC supply.
JTAG_BOOT	Input	3.3V	Pull down to zero for JTAG boot
JTAG_TCK	Input	3.3V	JTAG Clock
JTAG_TMS	Input	3.3V	JTAG Test Mode
JTAG_TDI	Input	3.3V	JTAG Data Input
JTAG_TDO	Output	3.3V	JTAG Data Output
REG_EN1	Input	5V	Drive low to disable on-board 1V regulator output
REG_EN2	Input	5V	Drive low to disable on-board 1.8V regulator output
REG_EN3	Input	5V	Drive low to disable on-board 3.3V regulator output
REG_EN4	Input	5V	Drive low to disable on-board 2.5V regulator output

Table 8: PEC_POWER Signal Summary

Signal	Pin	Pin	Signal
SYS_5P0V	1	2	SYS_5P0V
I2C_SCL	3	4	I2C_SDA
REG_EN1	5	6	REG_EN2
REG_EN3	7	8	REG_EN3
PROG_IO	9	10	NC
GND	11	12	GND
DSP_XID[0]	13	14	DSP_YID[0]
DSP_XID[1]	15	16	DSP_YID[1]
DSP_XID[2]	17	18	DSP_YID[2]
DSP_XID[3]	19	20	DSP_YID[3]
GND	21	22	GND
DSP_FLAG	23	24	UART_RX
TURBO_MODE	25	26	UART_TX
SPDIF	27	28	USER_LED
JTAG_BOOT_EN	29	30	RESET_N
GND	31	32	GND
VADC_N	33	34	VADC_P
GND	35	36	GND
JTAG_TMS	37	38	JTAG_TDI
TAG_TCK	39	40	JTAG_TDO
GND	41	42	GND
1P0V	43	44	1P0V
VDD_DSP	45	46	VDD_DSP
1P35V	47	48	1P35V
1P8V	49	50	1P8V
GND	51	52	GND
VDD_ADJ	53	54	VDD_ADJ
VDD_GPIO	55	56	VDD_GPIO
2P5V	57	58	2P5V
3P3V	59	60	3P3V

Table 9: PEC_POWER Pin Mapping

4.2 PEC_FPGA

The PEC_FPGA can be used to connect the Zynq programmable logic to expansion cards or other PEC_FPGA interfaces on another Parallella boards. The PEC_FPGA includes 48 bidirectional signals that can be configured within the Zynq device to support a number of different signal standards, including LVCMOS and LVDS.

Signal	Direction	Notes
VDD_GPIO	Output	Supply driven by power management IC on the Parallella board. Nominal voltage is 2.5V. The PMIC output voltage can be reprogrammed in software through I2C from the Zynq.
GND	Inout	System Ground
GPIOx_{N,P}	Inout	A differential pair or two single ended signals that connect between an expansion card and the Zynq device on the Parallella board.

Table 10: PEC_FPGA Signal Summary

Signal	Pin	Pin	Signal
VDD_GPIO	1	2	VDD_GPIO
GPIO0_N	3	4	GPIO1_N
GPIO0_P	5	6	GPIO1_P
GPIO2_N	7	8	GPIO3_N
GPIO2_P	9	10	GPIO3_P
GND	11	12	GND
GPIO4_N	13	14	GPIO5_N
GPIO4_P	15	16	GPIO5_P
GPIO6_N	17	18	GPIO7_N
GPIO6_P	19	20	GPIO7_P
GND	21	22	GND
GPIO8_N	23	24	GPIO9_N
GPIO8_P	25	26	GPIO9_P
GPIO10_N	27	28	GPIO11_N
GPIO10_P	29	30	GPIO11_P
GND	31	32	GND
GPIO12_N	33	34	GPIO13_N
GPIO12_P	35	36	GPIO13_P
GPIO14_N	37	38	GPIO15_N
GPIO14_P	39	40	GPIO15_P
GND	41	42	GND
GPIO16_N	43	44	GPIO17_N
GPIO16_P	45	46	GPIO17_P
GPIO18_N	47	48	GPIO19_N
GPIO18_P	49	50	GPIO19_P
GND	51	52	GND
GPIO20_N	53	54	GPIO21_N
GPIO20_P	55	56	GPIO21_P
GPIO22_N	57	58	GPIO23_N
GPIO22_P	59	60	GPIO23_P

Table 11: PEC_FPGA Pin Mapping

4.3 PEC_NORTH/PEC_SOUTH

The PEC_NORTH and PEC_SOUTH are connected to the north and south link of the Epiphany chip on the Parallella board. These expansion connectors can be used to connect multiple Parallella boards in a bidirectional line or ring configuration or they can be connected to an FPGA device with an Epiphany eLink interface implemented in RTL. The Parallella board support standard differential LVDS signaling.

Signal Name	Direction	Signal Description
1P8V	Output	1.8V supply driven by power management IC on the Parallella board.
GND	Inout	System ground
RXI_{NO,SO}_DATA_{P,N}[7:0]	Input	Receiver data
RXI_{NO,SO}_FRAME_{P,N}	Input	Receiver packet framing signal
RXI_{NO,SO}_LCLK_{P,N}	Input	Receiver clock
RXO_{NO,SO}_WR_WAIT_{P,N}	Output	Push-back for transmitter indicating that device must hold off on sending another write packet.
RXO_{NO,SO}_RD_WAIT_{P,N}	Output	Push-back for transmitter indicating that device must hold off on sending another read packet.
TXO_{NO,SO}_DATA_{P,N}[7:0]	Output	Transmitter data
TXO_{NO,SO}_FRAME_{P,N}	Output	Transmitter packet framing signal
TXO_{NO,SO}_LCLK_{P,N}	Output	Transmitter clock
TXI_{NO,SO}_WR_WAIT_{P,N}	Input	Push-back from receiver indicating that transmitter must hold off on sending another write packet.
TXI_{NO,SO}_RD_WAIT_{P,N}	Input	Push-back from transmitter indicating that transmitter must hold off on sending another read packet.

Table 12: PEC_NORTH/PEC_SOUTH Signal Summary

Signal	Pin	Pin	Signal
1P8V	1	2	1P8V
RXI_NO_DATA_N[0]	3	4	RXI_NO_DATA_N[1]
RXI_NO_DATA_P[0]	5	6	RXI_NO_DATA_P[1]
RXI_NO_DATA_N[2]	7	8	RXI_NO_DATA_N[3]
RXI_NO_DATA_P[2]	9	10	RXI_NO_DATA_P[3]
GND	11	12	GND
RXI_NO_DATA_N[4]	13	14	RXI_NO_DATA_N[5]
RXI_NO_DATA_P[4]	15	16	RXI_NO_DATA_P[5]
RXI_NO_DATA_N[6]	17	18	RXI_NO_DATA_N[7]
RXI_NO_DATA_P[6]	19	20	RXI_NO_DATA_P[7]
GND	21	22	GND
RXI_NO_LCLK_N	23	24	RXI_NO_FRAME_N
RXI_NO_LCLK_P	25	26	RXI_NO_FRAME_P
RXO_NO_RD_WAIT_N	27	28	RXO_SO_WR_WAIT_N
RXO_NO_RD_WAIT_P	29	30	RXO_NO_WR_WAIT_P
GND	31	32	GND
TXO_NO_FRAME_N	33	34	TXI_NO_WR_WAIT_N
TXO_NO_FRAME_P	35	36	TXI_NO_WR_WAIT_P
TXO_NO_LCLK_N	37	38	TXI_NO_RD_WAIT_N
TXO_NO_LCLK_P	39	40	TXI_NO_RD_WAIT_P
GND	41	42	GND
TXO_NO_DATA_N[0]	43	44	TXO_NO_DATA_N[1]
TXO_NO_DATA_P[0]	45	46	TXO_NO_DATA_P[1]
TXO_NO_DATA_N[2]	47	48	TXO_NO_DATA_N[3]
TXO_NO_DATA_P[2]	49	50	TXO_NO_DATA_P[3]
GND	51	52	GND
TXO_NO_DATA_N[4]	53	54	TXO_NO_DATA_N[5]
TXO_NO_DATA_P[4]	55	56	TXO_NO_DATA_P[5]
TXO_NO_DATA_N[6]	57	58	TXO_NO_DATA_N[7]
TXO_NO_DATA_P[6]	59	60	TXO_NO_DATA_P[7]

Table 13: PEC_NORTH Pin Mapping for Parallella-16

Signal	Pin	Pin	Signal
1P8V	1	2	1P8V
TXO_NO_DATA_P[7]	3	4	TXO_NO_DATA_P[6]
TXO_NO_DATA_N[7]	5	6	TXO_NO_DATA_N[6]
TXO_NO_DATA_P[5]	7	8	TXO_NO_DATA_P[4]
TXO_NO_DATA_N[5]	9	10	TXO_NO_DATA_N[4]
GND	11	12	GND
TXO_NO_DATA_P[3]	13	14	TXO_NO_DATA_P[2]
TXO_NO_DATA_N[3]	15	16	TXO_NO_DATA_N[2]
TXO_NO_DATA_P[1]	17	18	TXO_NO_DATA_P[0]
TXO_NO_DATA_N[1]	19	20	TXO_NO_DATA_N[0]
GND	21	22	GND
TXO_NO_LCLK_P	23	24	TXI_NO_RD_WAIT_P
TXO_NO_LCLK_N	25	26	TXI_NO_RD_WAIT_N
RXO_NO_WR_WAIT_P	27	28	RXO_NO_RD_WAIT_P
RXO_NO_WR_WAIT_N	29	30	RXO_NO_RD_WAIT_N
GND	31	32	GND
TXO_NO_FRAME_P	33	34	TXI_NO_WR_WAIT_N
TXO_NO_FRAME_N	35	36	TXI_NO_WR_WAIT_P
RXI_NO_LCLK_P	37	38	RXI_NO_FRAME_P
RXI_NO_LCLK_N	39	40	RXI_NO_FRAME_N
GND	41	42	GND
RXI_NO_DATA_P[7]	43	44	RXI_NO_DATA_P[6]
RXI_NO_DATA_N[7]	45	46	RXI_NO_DATA_N[6]
RXI_NO_DATA_P[5]	47	48	RXI_NO_DATA_P[4]
RXI_NO_DATA_N[5]	49	50	RXI_NO_DATA_N[4]
GND	51	52	GND
RXI_NO_DATA_P[3]	53	54	RXI_NO_DATA_P[2]
RXI_NO_DATA_N[3]	55	56	RXI_NO_DATA_N[2]
RXI_NO_DATA_P[1]	57	58	RXI_NO_DATA_P[0]
RXI_NO_DATA_N[1]	59	60	RXI_NO_DATA_N[0]

Table 14: PEC_NORTH Pin Mapping for Parallella-64

Signal	Pin	Pin	Signal
1P8V	1	2	1P8V
RXI_SO_DATA_N[0]	3	4	RXI_SO_DATA_N[1]
RXI_SO_DATA_P[0]	5	6	RXI_SO_DATA_P[1]
RXI_SO_DATA_N[2]	7	8	RXI_SO_DATA_N[3]
RXI_SO_DATA_P[2]	9	10	RXI_SO_DATA_P[3]
GND	11	12	GND
RXI_SO_DATA_N[4]	13	14	RXI_SO_DATA_N[5]
RXI_SO_DATA_P[4]	15	16	RXI_SO_DATA_P[5]
RXI_SO_DATA_N[6]	17	18	RXI_SO_DATA_N[7]
RXI_SO_DATA_P[6]	19	20	RXI_SO_DATA_P[7]
GND	21	22	GND
RXI_SO_LCLK_N	23	24	RXI_SO_FRAME_N
RXI_SO_LCLK_P	25	26	RXI_SO_FRAME_P
RXO_SO_RD_WAIT_N	27	28	RXO_SO_WR_WAIT_N
RXO_SO_RD_WAIT_P	29	30	RXO_SO_WR_WAIT_P
GND	31	32	GND
TXO_SO_FRAME_N	33	34	TXI_SO_WR_WAIT_N
TXO_SO_FRAME_P	35	36	TXI_SO_WR_WAIT_P
TXO_SO_LCLK_N	37	38	TXI_SO_RD_WAIT_N
TXO_SO_LCLK_P	39	40	TXI_SO_RD_WAIT_P
GND	41	42	GND
TXO_SO_DATA_N[0]	43	44	TXO_SO_DATA_N[1]
TXO_SO_DATA_P[0]	45	46	TXO_SO_DATA_P[1]
TXO_SO_DATA_N[2]	47	48	TXO_SO_DATA_N[3]
TXO_SO_DATA_P[2]	49	50	TXO_SO_DATA_P[3]
GND	51	52	GND
TXO_SO_DATA_N[4]	53	54	TXO_SO_DATA_N[5]
TXO_SO_DATA_P[4]	55	56	TXO_SO_DATA_P[5]
TXO_SO_DATA_N[6]	57	58	TXO_SO_DATA_N[7]
TXO_SO_DATA_P[6]	59	60	TXO_SO_DATA_P[7]

Table 15: PEC_SOUTH Pin Mapping for Parallella-16

Signal	Pin	Pin	Signal
1P8V	1	2	1P8V
RXI_SO_DATA_N[7]	3	4	RXI_SO_DATA_N[6]
RXI_SO_DATA_P[7]	5	6	RXI_SO_DATA_P[6]
RXI_SO_DATA_N[5]	7	8	RXI_SO_DATA_N[4]
RXI_SO_DATA_P[5]	9	10	RXI_SO_DATA_P[4]
GND	11	12	GND
RXI_SO_DATA_N[3]	13	14	RXI_SO_DATA_N[2]
RXI_SO_DATA_P[3]	15	16	RXI_SO_DATA_P[2]
RXI_SO_DATA_N[1]	17	18	RXI_SO_DATA_N[0]
RXI_SO_DATA_P[1]	19	20	RXI_SO_DATA_P[0]
GND	21	22	GND
RXI_SO_LCLK_N	23	24	RXO_SO_RD_WAIT_N
RXI_SO_LCLK_P	25	26	RXO_SO_RD_WAIT_P
TXI_SO_WR_WAIT_N	27	28	TXI_SO_RD_WAIT_N
TXI_SO_WR_WAIT_P	29	30	TXI_SO_RD_WAIT_P
GND	31	32	GND
RXI_SO_FRAME_N	33	34	RXO_SO_WR_WAIT_N
RXI_SO_FRAME_P	35	36	RXO_SO_WR_WAIT_P
TXO_SO_LCLK_N	37	38	TXO_SO_FRAME_N
TXO_SO_LCLK_P	39	40	TXO_SO_FRAME_P
GND	41	42	GND
TXO_SO_DATA_N[7]	43	44	TXO_SO_DATA_N[6]
TXO_SO_DATA_P[7]	45	46	TXO_SO_DATA_P[6]
TXO_SO_DATA_N[5]	47	48	TXO_SO_DATA_N[4]
TXO_SO_DATA_P[5]	49	50	TXO_SO_DATA_P[3]
GND	51	52	GND
TXO_SO_DATA_N[3]	53	54	TXO_SO_DATA_N[2]
TXO_SO_DATA_P[3]	55	56	TXO_SO_DATA_P[2]
TXO_SO_DATA_N[1]	57	58	TXO_SO_DATA_N[0]
TXO_SO_DATA_P[1]	59	60	TXO_SO_DATA_P[0]

Table 16: PEC_SOUTH Pin Mapping for Parallella-64

5 Parallella Specifications

5.1 Dimensions and Weight

Feature	
Size	3.4'' x 2.15''
Max Height **(with RJ45, PEC)**	TBD
Min Height **(without RJ45, PEC, 0.1'' header pins)**	TBD
PCB Layers	12
PCB Thickness	0.62''
Weight	TBD

Table 17: Dimension and Weight

5.2 Power Consumption

The following table will contain the power consumption for typical Parallella use cases. Once documented, each use case will include all sources needed to repeat the experiments.

Workload	1P0V	1P8V	3P3V	2P5V	VDD_DSP	1P35	VDD_ADJ	VDD_GPIO
Idle	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD
Boot	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD
Nominal	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD
Max	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD

Table 18: Power Consumption

5.3 Performance Metrics

The following table shows the performance specifications of the Parallella board at the time of publication of this reference manual. Give more time for optimization and testing most of these metrics should improve.

Performance Goal	Value
Peak Zynq Frequency	667MHz
Peak Epiphany Instruction Issue Rate	21 GIPS (Parallella-16) 85 GIPS (Parallella-64)
Peak Epiphany Frequency	667 MHz (Parallella-16) 667 MHz (Parallella-64)
Peak Floating Point Performance	21 GFLOPS (Parallella-16) 85 GFLOPS (Parallella-64)
Peak Bandwidth between Zynq and Epiphany	1.3GB/s
PEC_FPGA Peak Bandwidth	2.85GB/s (22.8 Gbps)
PEC_NORTH/PEC_SOUTH Peak Bandwidth	2.6GB/s (25.6 Gbps)

Table 19: Parallella Performance Goals

6 Parallella Quick Start Guides (TBD)

6.1 Desktop Evaluation System

6.2 Embedded Platform

6.3 Wireless Computer

6.4 Stacked clusters

7 About the Parallella Board

7.1 Design Information

The board is open source hardware and the Parallella project provides all the files required to study, modify and manufacture the design.

The design resources provided include:

- Complete reference manual
- Schematic sources in OrCAD format
- PCB layout sources in Allegro format
- PCB manufacturing files in Gerber format
- Assembled board 3D CAD model(s)
- Bill of material

Design files for this board will be available at:

http://github.com/parallella/parallella-hw/gen1

7.2 Build Options

The following Parallella assembly options will be supported in manufacturing:

- **Zynq Device**: Z-7010 or Z-7020
- **Epiphany Device:** E16G301 or E64G401
- **IO:** With our without Samtec expansion connectors
- **Ethernet:** With or without Ethernet (RJ45 and Ethernet Phy)

7.3 Contributors

- **Adapteva:** (http://www.adapteva.com)
  - Parallella architecture and board design (Andreas Olofsson)
  - FPGA design (Roman Trogan)
  - Linux distribution (Roman Trogan)
  - Board bringup (Roman Trogan, Andreas Olofsson)
  - Reference manuals (Andreas Olofsson)

- **Boston Design Solutions:** (http://www.bostondesignsolutions.com/)
  - Schematic and board layout (Mike Bakhtiari, Mike Damiano)
  - Board bringup (Joe Galibois)

- **Review and Feedback:**
  - Andrew Back
  - Flemming Christensen
  - Gunnar Hillerström
  - Al Wood
  - @trioflex
  - @tschaboo
  - @hamster
  - @psupine
  - @tnt

7.4 Attributions

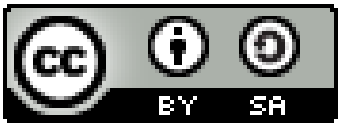
- Warranty notice and Disclaimers based on those found in the Beaglebone Black System Reference Manual Rev A5.2, authored by Gerald Coley of Texas Instruments and published under the Creative Commons Attribution Share-Alike 3.0 Unported License.

- The Parallella project benefited greatly from being able to study the design of the following open source hardware projects:
    - Arduino
    - Beaglebone

- The Parallella project also drew inspiration from the following projects:
    - Zedboard
    - Raspberry Pi

7.5 Licensing

Send all comments and errors concerning this document to andreas@adapteva.com



7.6 Disclaimers

These design materials referred to in this document are ***NOT SUPPORTED*** and **DO NOT** constitute a reference design. Only "community" support is allowed via resources at http://forums.parallella.org

THERE IS NO WARRANTY FOR THE DESIGN MATERIALS DESCRIBED IN THIS REFERENCE MANUAL, TO THE EXTENT PERMITTED BY APPLICABLE LAW. EXCEPT WHEN OTHERWISE STATED IN WRITING THE COPYRIGHT HOLDERS AND/OR OTHER PARTIES PROVIDE THE DESIGN MATERIALS "AS IS" WITHOUT WARRANTY OF ANY KIND, EITHER EXPRESSED OR IMPLIED, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. THE ENTIRE RISK AS TO THE QUALITY AND PERFORMANCE OF THE DESIGN MATERIALS IS WITH YOU. SHOULD THE DESIGN MATERIALS PROVE DEFECTIVE, YOU ASSUME THE COST OF ALL NECESSARY SERVICING, REPAIR OR
CORRECTION

This Parallella board was designed as an evaluation and development tool. It was not designed with any other application in mind. As such, these design materials may or may not be suitable for any other purposes. If used, the design material becomes your responsibility as to whether or not it meets your specific needs or your specific applications and may require changes to meet your requirements.

For Feasibility Evaluation Only, in Laboratory/Development Environments: The Parallella Board is not a complete product. It is intended solely for use for preliminary feasibility evaluation in laboratory/development environments by technically qualified electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems and subsystems. It should not be used as all or part of a finished end product.

Your Sole Responsibility and Risk you acknowledge, represent, and agree that:

1. You have unique knowledge concerning Federal, State and local regulatory requirements (including but not limited to Food and Drug Administration regulations, if applicable) which relate to your products and which relate to your use (and/or that of your employees, affiliates, contractors or designees) of the Parallella for evaluation, testing and other purposes.
2. You have full and exclusive responsibility to assure the safety and compliance of your products with all such laws and other applicable regulatory requirements, and also to

assure the safety of any activities to be conducted by you and/or your employees, affiliates, contractors or designees, using the Parallella. Further, you are responsible to assure that any interfaces (electronic and/or mechanical) between the\Parallella and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard.

3. Since the Parallella is not a completed product, it may not meet all applicable regulatory and safety compliance standards which may normally be associated with similar items. You assume full responsibility to determine and/or assure compliance with any such standards and related certifications as may be applicable. You will employ reasonable safeguards to ensure that your use of the Parallella will not result in any property damage, injury or death, even if the Parallella should fail to perform as described or expected.

Certain Instructions: It is important to operate the Parallella Black within Supplier's recommended specifications and environmental considerations per the user guidelines. Exceeding the specified Parallella ratings (including but not limited to input and output voltage, current, power, and environmental ranges) may cause property damage, personal injury or death. If there are questions concerning these ratings please contact the Supplie representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may result in unintended and/or inaccurate operation and/or possible permanent damage to the Parallella and/or interface electronics. Please consult the System Reference Manual prior to connecting any load to the Parallella output. If there is uncertainty as to the load specification, please contact the Supplier representative. During normal operation, some circuit components may have case temperatures greater than 60 C as long as the input and output are maintained at a normal ambient operating temperature. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors which can be identified using the Parallella schematic located at the link in the Parallella System Reference Manual. When placing measurement probes near these devices during normal operation, please be aware that these devices may be very warm to the touch. As with all electronic evaluation tools, only qualified personnel knowledgeable in electronic measurement and diagnostics normally found in development environments should use the Parallella.

Agreement to Defend, Indemnify and Hold Harmless: You agree to defend, indemnify and hold the Suppliers, its licensors and their representatives harmless from and against any and all claims, damages, losses, expenses, costs and liabilities (collectively, "Claims") arising out of or in connection with any use of the Parallella that is not in accordance with the terms of the agreement. This obligation shall apply whether Claims arise under law of tort or contract or any other legal theory, and even if the Parallella fails to perform as described or expected.

Safety-Critical or Life-Critical Applications: If you intend to evaluate the components for possible use in safety critical applications (such as life support) where a failure of the Supplier's product would reasonably be expected to cause severe personal injury or death, such as devices which are classified as FDA Class III or similar classification, then you must specifically notify Suppliers of such intent and enter into a separate Assurance and Indemnity Agreement.

7.7 Warranty

Parallella.org and Adapteva, Inc (Supplier) provide the Parallella board under the following conditions:

- The user assumes all responsibility and liability for proper and safe handling of the goods. Further, the user indemnifies Supplier from all claims arising from the handling or use of the goods.
- Should the Parallella not meet the specifications indicated in the Parallella Reference Manual, the Parallella may be returned within 90 days from the date of delivery to the distributor of purchase for a full refund.

THE FOREGOING LIMITED WARRANTY IS THE EXCLUSIVE WARRANTY MADE BY SELLER TO BUYER AND IS IN LIEU OF ALL OTHER WARRANTIES, EXPRESSED, IMPLIED, OR STATUTORY, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PARTICULAR PURPOSE. EXCEPT TO THE EXTENT OF THE INDEMNITY SET FORTH ABOVE, NEITHER PARTY SHALL BE LIABLE TO THE OTHER FOR ANY INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES.

For up to date board information, please refer to:
http://github.com/parallella/parallella-hw

All support for this board is provided via community support at
http://forums.parallella.org

Before returning the board, please request an RMA at:
www.parallella.org/support/rma

Please DO NOT return the board without approval from the Parallella RMA team first. All boards received without RMA approval will not be worked on.