Hardware-Software Systems Design
1st Lab.

Vitis HLS

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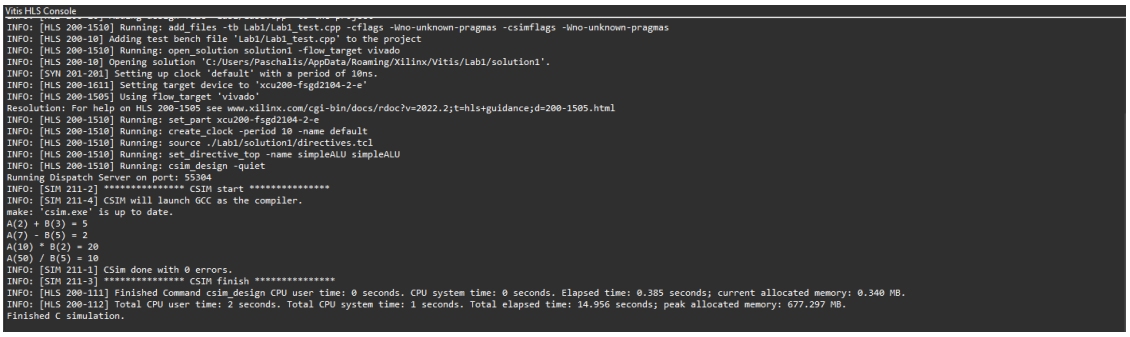
Contents

Lab Description:

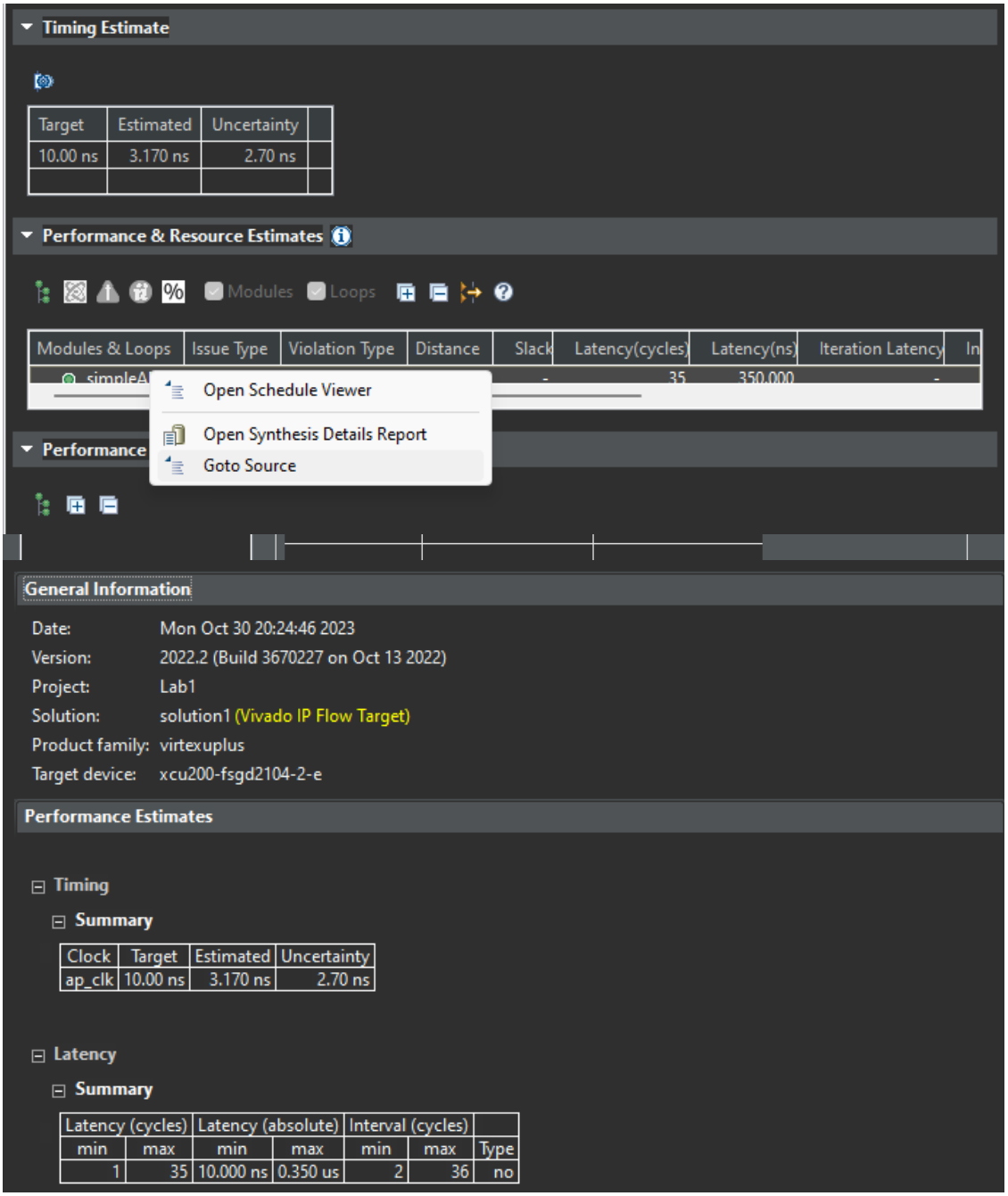
In the first Lab of the course, we got familiar with VITIS HLS. Our goal was to implement a 2D matrix multiplication function, and later try to use Vivado HLS directives, top achieve a good acceleration.

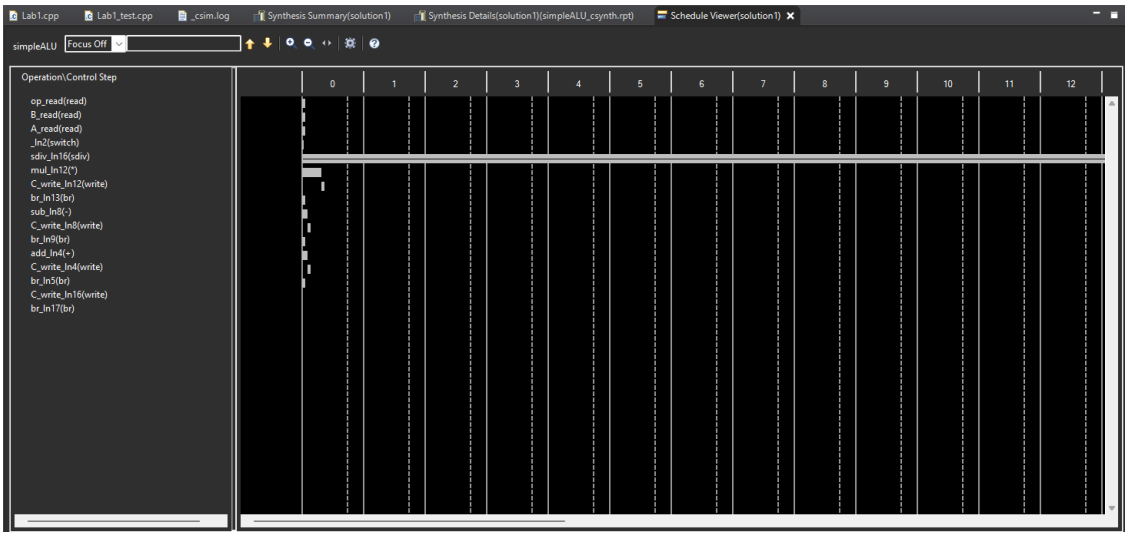
Introduction to VITIS (20%):

- Run C Simulation:



- Run C Synthesis:





Summary

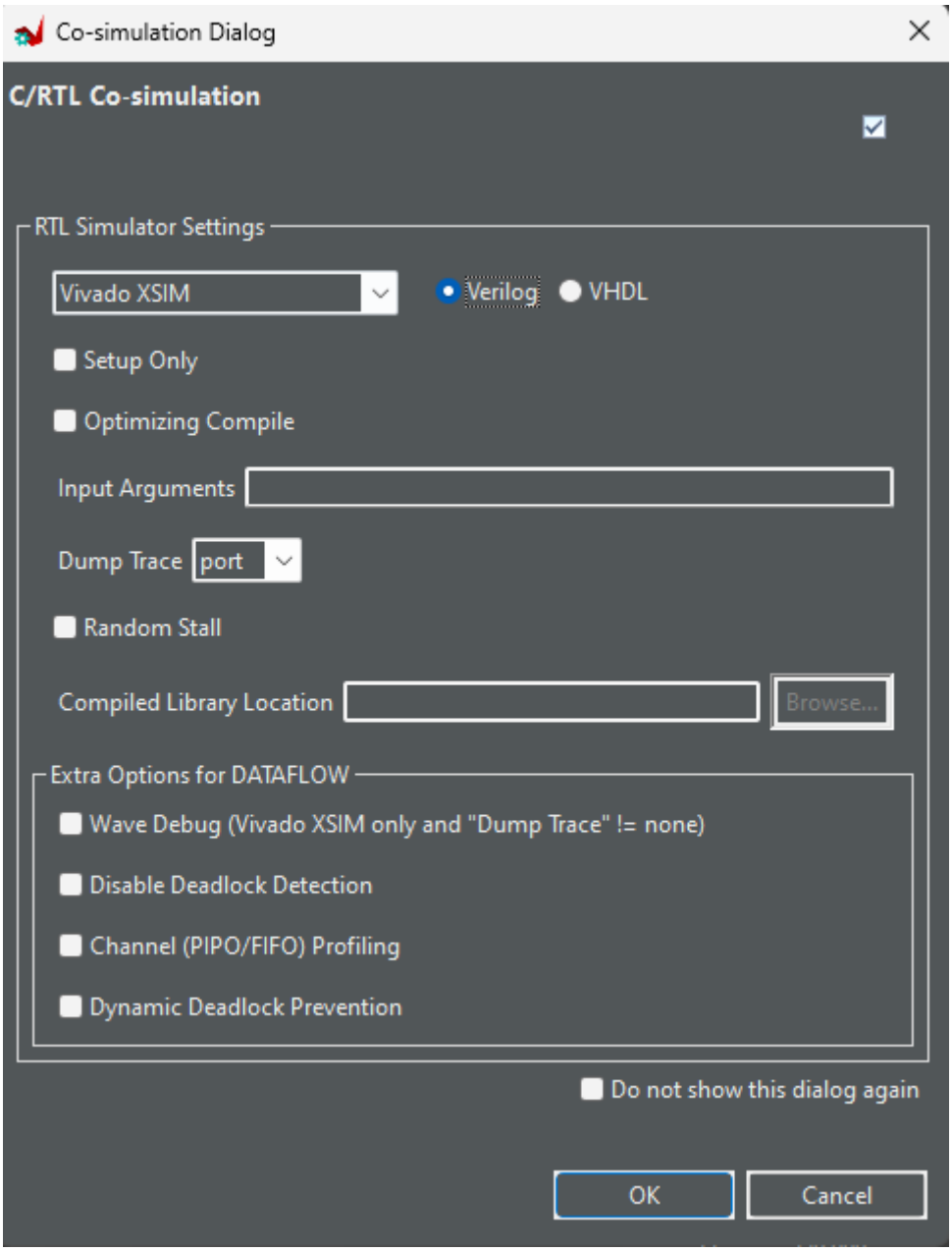
Name	BRAM_18K	DSP	FF	LUT	URAM
DSP	-	-	-	-	-
Expression	-	-	0	78	-
FIFO	-	-	-	-	-
Instance	-	3	394	258	-
Memory	-	-	-	-	-
Multiplexer	-	-	-	192	-
Register	-	-	36	-	-
Total	0	3	430	528	0
Available	4320	6840	2364480	1182240	960
Available SLR	1440	2280	788160	394080	320
Utilization (%)	0	~0	~0	~0	0
Utilization SLR (%)	0	~0	~0	~0	0

Interface

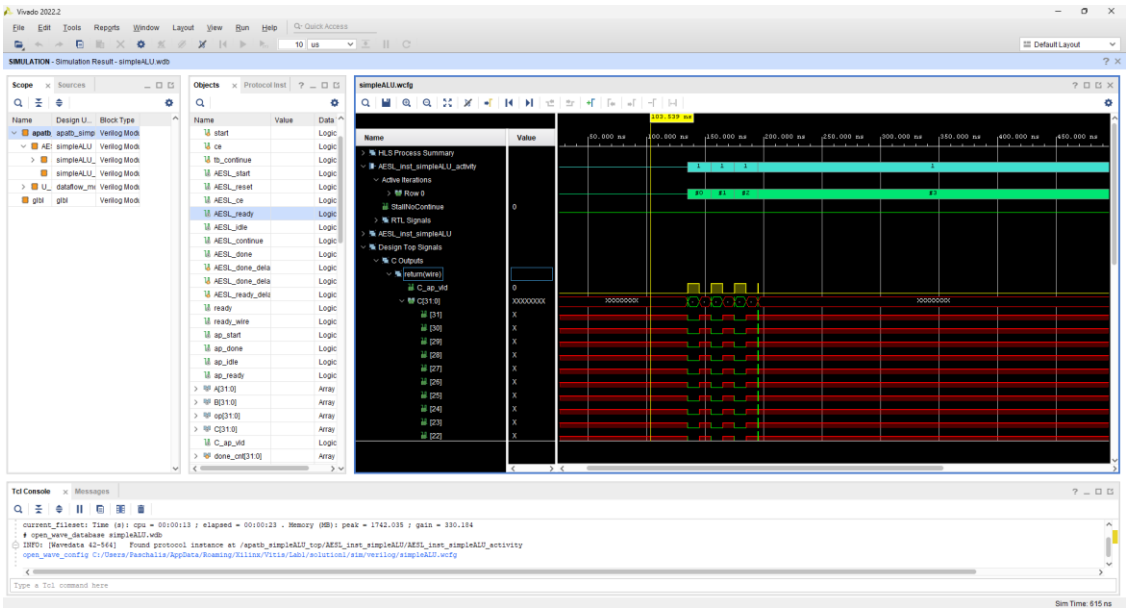
Summary

RTL Ports	Dir	Bits	Protocol	Source Object	C Type
ap_clk	in	1	ap_ctrl_hs	simpleALU	return value
ap_rst	in	1	ap_ctrl_hs	simpleALU	return value
ap_start	in	1	ap_ctrl_hs	simpleALU	return value
ap_done	out	1	ap_ctrl_hs	simpleALU	return value
ap_idle	out	1	ap_ctrl_hs	simpleALU	return value
ap_ready	out	1	ap_ctrl_hs	simpleALU	return value
A	in	32	ap_none	A	scalar
B	in	32	ap_none	B	scalar
op	in	32	ap_none	op	scalar
C	out	32	ap_vld	C	pointer
C_ap_vld	out	1	ap_vld	C	pointer

- Run C/RTL Cosimulation:




```
$finish called at time : 615 ns : File "C:/Users/Paschalis/AppData/Roa
## quit
INFO: [Common 17-206] Exiting xsim at Mon Oct 30 20:32:43 2023...
INFO: [COSIM 212-316] Starting C post checking ...
A(2) + B(3) = 5
A(7) - B(5) = 2
A(10) * B(2) = 20
A(50) / B(5) = 10
INFO: [COSIM 212-1000] *** C/RTL co-simulation finished: PASS ***
```



H/W accelerator design using Vivado HLS (80%):

- *Question 1(30%).*

```
void MATRIX_MUL_SW(uint8_t A[n][m], uint8_t B[m][p], uint32_t C[n][p]){

    for(int i = 0; i < n; i++){
        for(int j = 0; j < p; j++){
            int res = 0;
            for(int k = 0; k < m; k++){
                res += A[i][k] * B[k][j];
            }
            C[i][j] = res;
        }
    }
}
```

- *Question 2(5%).*

(για lm=ln=lp=6):

Estimated clock period: 6.304ns.

Worst case latency: 131091 cycles.

Number of DSP48E used: 32.

Number of BRAMs used: 0.

Number of FFs used: 1491.

Number of LUTs used: 4420.

Target	Estimated	Uncertainty	
10.00 ns	6.304 ns	2.70 ns	

Latency

Summary

Latency (cycles)		Latency (absolute)		Interval (cycles)		
min	max	min	max	min	max	Type
131091	131091	1.311 ms	1.311 ms	131092	131092	no

Detail

Summary

Name	BRAM_18K	DSP	FF	LUT	URAM
DSP	-	32	-	-	-
Expression	-	-	0	2080	-
FIFO	-	-	-	-	-
Instance	-	0	0	1280	-
Memory	-	-	-	-	-
Multiplexer	-	-	-	1060	-
Register	-	-	1491	-	-
Total	0	32	1491	4420	0
Available	4320	6840	2364480	1182240	960
Available SLR	1440	2280	788160	394080	320
Utilization (%)	0	~0	~0	~0	0
Utilization SLR (%)	0	1	~0	1	0

- *Question 3(5%):*

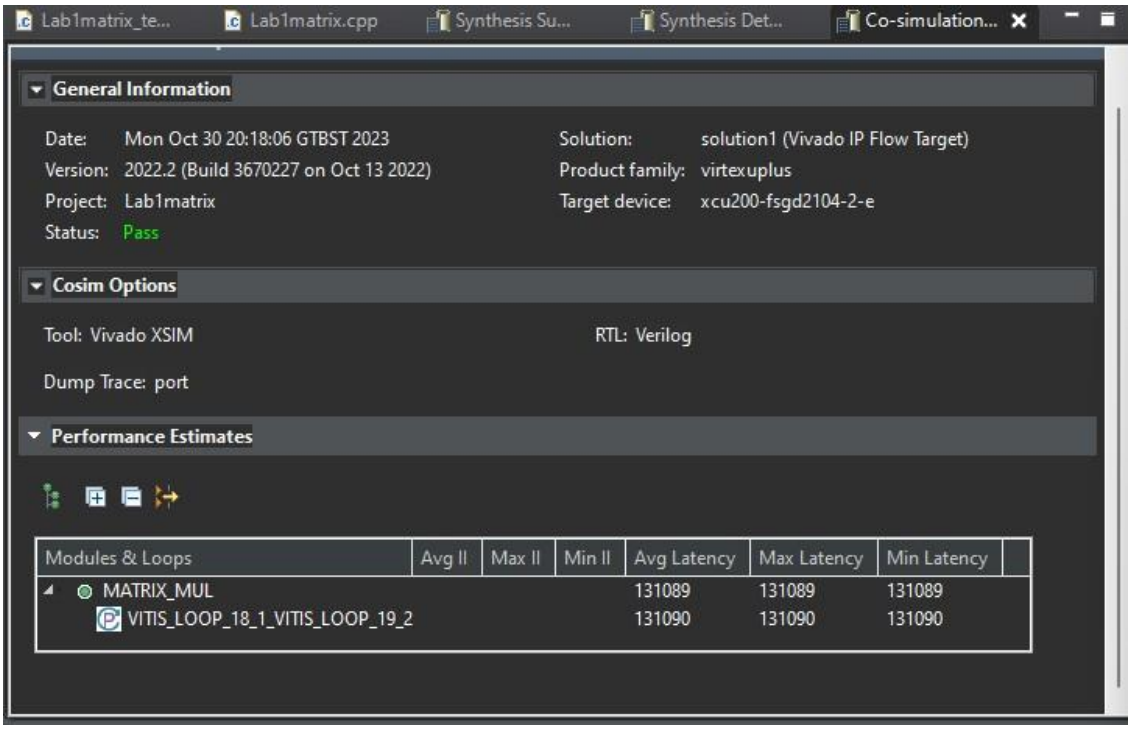
για τις τιμές lm=ln=lp=6:

Total Execution Time: 1311095ns.

Min latency: 131089.

Avg. latency: 131089.

Max latency: 131089.




```
$finish called at time : 1311095 ns : File "C:/Users/Paschalis/AppData/Roaming/Xilinx/Vitis/Lab1matrix
run: Time (s): cpu = 00:00:03 ; elapsed = 00:00:05 . Memory (MB): peak = 238.996 ; gain = 0.000
## quit
INFO: [Common 17-206] Exiting xsim at Mon Oct 30 20:18:06 2023...
INFO: [COSIM 212-316] Starting C post checking ...
```

- *Question 4(40%):*

1.

Keeping lm = constant and changing ln and lp, it was observed that the number of DSPs dropped. Also, no BRAMs where used at all. Additionally, the number of FFs and LUTs was also reduced. This happened probably because

the arrays weren’t symmetrical and the data couldn’t be treated in same size “blocks”, thus less hardware was used.

2.

για τις τιμές lm=ln=lp=6:

Estimated clock period: 5.259ns

Number of DSP48E used: 2048.

Number of BRAMs used: 64.

Number of FFs used: 66738.

Number of LUTs used: 158828.

Total Execution Time: 46985ns.

Min latency: 4678.

Avg. latency: 4678.

Max latency: 4678.

Summary

Clock	Target	Estimated	Uncertainty
ap_clk	10.00 ns	5.259 ns	2.70 ns

Latency

Summary

Latency (cycles)		Latency (absolute)		Interval (cycles)		
min	max	min	max	min	max	Type
4682	4682	46.820 us	46.820 us	4683	4683	no

Detail

Instance

Loop

Utilization Estimates

Summary

Name	BRAM_18K	DSP	FF	LUT	URAM
DSP	-	-	-	-	-
Expression	-	-	0	2	-
FIFO	-	-	-	-	-
Instance	-	2048	33451	133809	-
Memory	64	-	0	0	0
Multiplexer	-	-	-	25017	-
Register	-	-	33287	-	-
Total	64	2048	66738	158828	0
Available	4320	6840	2364480	1182240	960
Available SLR	1440	2280	788160	394080	320
Utilization (%)	1	29	2	13	0
Utilization SLR (%)	4	89	8	40	0

```
$finish called at time : 46985 ns : File "C:/Users/Paschalis/AppData/Roaming/Xilinx/Vitis/Matrix/solution1/sim/verilog/MATRIX_MUL_HW.autotb.v" Line 2502
run: Time (s): cpu = 00:00:00 ; elapsed = 00:00:12 . Memory (MB): peak = 326.055 ; gain = 0.000
## quit
INFO: [Common 17-206] Exiting xsim at Sat Nov  4 18:41:28 2023...
INFO: [COSIM 212-316] Starting C post checking ...
```

3.

speedup = 1311095/46985 =28.