

Hardware-Software Systems Design

1st Lab.

Vitis HLS

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Lab Description:

In the first Lab of the course, we got familiar with VITIS HLS. Our goal was to implement a 2D matrix multiplication function, and later try to use Vivado HLS directives, top achieve a good acceleration.

Introduction to VITIS (20%):

- Run C Simulation:

```
Vitis HLS Console
INFO: [HLS 200-1510] Running: add_files -tb Lab1/Lab1_test.cpp -cflags -Wno-unknown-pragmas -csimflags -Wno-unknown-pragmas
INFO: [HLS 200-10] Adding test bench file 'Lab1/Lab1_test.cpp' to the project
INFO: [HLS 200-1510] Running: open_solution solution1 -flow_target vivado
INFO: [HLS 200-10] Opening solution 'c:/Users/Paschalis/AppData/Roaming/Xilinx/Vitis/Lab1/solution1'.
INFO: [SVN 201-201] Setting up clock 'default' with a period of 10ns.
INFO: [HLS 200-1611] Setting target device to 'xcu200-fsgd2104-2-e'
INFO: [HLS 200-1505] Using flow target: 'vivado'
Resolution: For help on HLS 200-1505 see www.xilinx.com/cgi-bin/docs/rdoc?v=2022.2;t=hls+guidance;d=200-1505.html
INFO: [HLS 200-1510] Running: set_part xcu200-fsgd2104-2-e
INFO: [HLS 200-1510] Running: create_clock -period 10 -name default
INFO: [HLS 200-1510] Running: source /Lab1/solution1/directives.tcl
INFO: [HLS 200-1510] Running: set_directive_top -name simpleALU simpleALU
INFO: [HLS 200-1510] Running: csim_design -quiet
Running Dispatch Server on port: 55304
INFO: [SIM 211-2] ***** CSDM start *****
INFO: [SIM 211-4] CSDM will launch GCC as the compiler.
make: 'csim.exe' is up to date.
A(2) * B(3) = 5
A(7) - B(5) = 2
A(10) * B(2) = 20
A(50) / B(5) = 10
INFO: [SIM 211-1] CSDM done with 0 errors.
INFO: [SIM 211-3] ***** CSDM finish *****
INFO: [HLS 200-111] Finished Command csim_design CPU user time: 0 seconds. CPU system time: 0 seconds. Elapsed time: 0.385 seconds; current allocated memory: 0.340 MB.
INFO: [HLS 200-112] Total CPU user time: 2 seconds. Total CPU system time: 1 seconds. Total elapsed time: 14.956 seconds; peak allocated memory: 677.297 MB.
Finished C simulation.
```

- Run C Synthesis:

Timing Estimate

Target	Estimated	Uncertainty
10.00 ns	3.170 ns	2.70 ns

Performance & Resource Estimates

Modules & Loops

Issue Type

Violation Type

Distance

Slack

Latency(cycles)

Latency(ns)

Iteration Latency

In

simpleA					35	350.000	
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Open Schedule Viewer
Open Synthesis Details Report
Goto Source

Performance

General Information

Date: Mon Oct 30 20:24:46 2023
Version: 2022.2 (Build 3670227 on Oct 13 2022)
Project: Lab1
Solution: solution1 (Vivado IP Flow Target)
Product family: virtexuplus
Target device: xcu200-fsgd2104-2-e

Performance Estimates

Timing

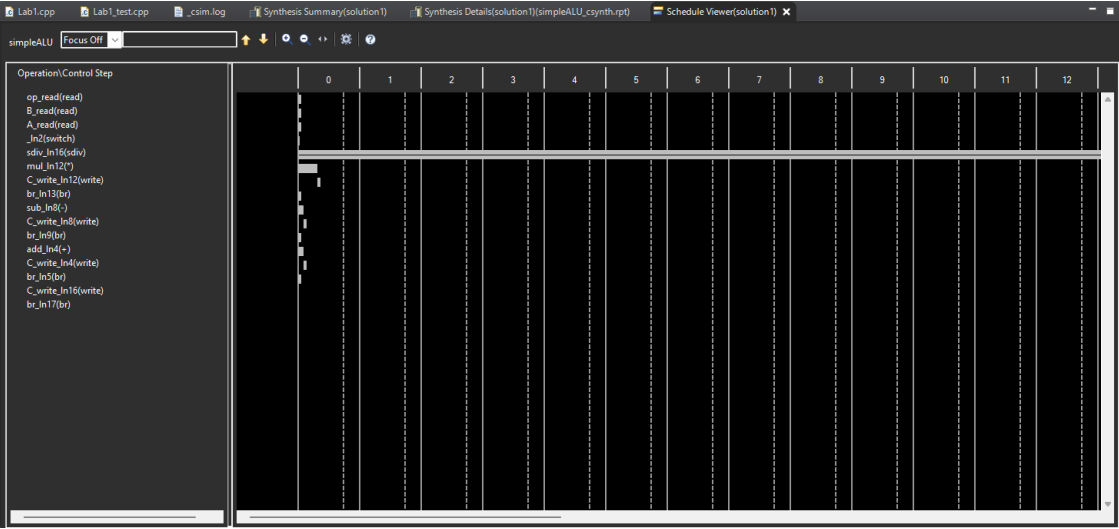
Summary

Clock	Target	Estimated	Uncertainty
ap_clk	10.00 ns	3.170 ns	2.70 ns

Latency

Summary

Latency (cycles)		Latency (absolute)		Interval (cycles)		
min	max	min	max	min	max	Type
1	35	10.000 ns	0.350 us	2	36	no



Summary

Name	BRAM_18K	DSP	FF	LUT	URAM
DSP	-	-	-	-	-
Expression	-	-	0	78	-
FIFO	-	-	-	-	-
Instance	-	3	394	258	-
Memory	-	-	-	-	-
Multiplexer	-	-	-	192	-
Register	-	-	36	-	-
Total	0	3	430	528	0
Available	4320	6840	2364480	1182240	960
Available SLR	1440	2280	788160	394080	320
Utilization (%)	0	~0	~0	~0	0
Utilization SLR (%)	0	~0	~0	~0	0

Interface

Summary

RTL Ports	Dir	Bits	Protocol	Source Object	C Type
ap_clk	in	1	ap_ctrl_hs	simpleALU	return value
ap_rst	in	1	ap_ctrl_hs	simpleALU	return value
ap_start	in	1	ap_ctrl_hs	simpleALU	return value
ap_done	out	1	ap_ctrl_hs	simpleALU	return value
ap_idle	out	1	ap_ctrl_hs	simpleALU	return value
ap_ready	out	1	ap_ctrl_hs	simpleALU	return value
A	in	32	ap_none	A	scalar
B	in	32	ap_none	B	scalar
op	in	32	ap_none	op	scalar
C	out	32	ap_vld	C	pointer
C_ap_vld	out	1	ap_vld	C	pointer

- Run C/RTL Cosimulation:

Co-simulation Dialog

C/RTL Co-simulation ☒

RTL Simulator Settings

Vivado XSIM Verilog ☐ VHDL

☐ Setup Only

☐ Optimizing Compile

Input Arguments

Dump Trace

☐ Random Stall

Compiled Library Location

Extra Options for DATAFLOW

☐ Wave Debug (Vivado XSIM only and "Dump Trace" != none)

☐ Disable Deadlock Detection

☐ Channel (PIPO/FIFO) Profiling

☐ Dynamic Deadlock Prevention

☐ Do not show this dialog again

```
$finish called at time : 615 ns : File "C:/Users/Paschalis/AppData/Roaming/Xilinx/Vivado/2023.1/Scripts/RunCRTLCoSimulation.tcl"
## quit
INFO: [Common 17-206] Exiting xsim at Mon Oct 30 20:32:43 2023...
INFO: [COSIM 212-316] Starting C post checking ...
A(2) + B(3) = 5
A(7) - B(5) = 2
A(10) * B(2) = 20
A(50) / B(5) = 10
INFO: [COSIM 212-1000] *** C/RTL co-simulation finished: PASS ***
```


- Question 2(5%).

($\gamma \propto I_m = I_n = I_p = 6$):

Estimated clock period: 6.304ns.

Worst case latency: 131091 cycles.

Number of DSP48E used: 32.

Number of BRAMs used: 0.

Number of FFs used: 1491.

Number of LUTs used: 4420.

Target	Estimated	Uncertainty	
10.00 ns	6.304 ns	2.70 ns	

Latency

Summary

Latency (cycles)		Latency (absolute)		Interval (cycles)		Type
min	max	min	max	min	max	
131091	131091	1.311 ms	1.311 ms	131092	131092	no

Detail

Summary

Name	BRAM_18K	DSP	FF	LUT	URAM
DSP	-	32	-	-	-
Expression	-	-	0	2080	-
FIFO	-	-	-	-	-
Instance	-	0	0	1280	-
Memory	-	-	-	-	-
Multiplexer	-	-	-	1060	-
Register	-	-	1491	-	-
Total	0	32	1491	4420	0
Available	4320	6840	2364480	1182240	960
Available SLR	1440	2280	788160	394080	320
Utilization (%)	0	~0	~0	~0	0
Utilization SLR (%)	0	1	~0	1	0

- Question 3(5%):

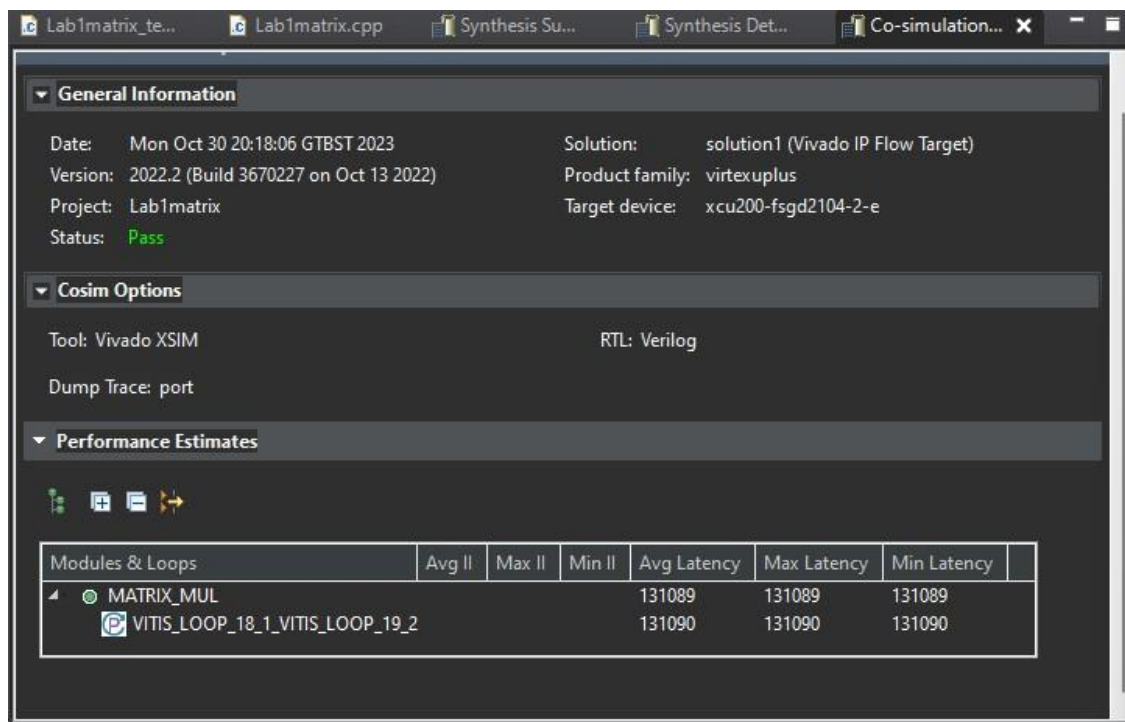
για τις τιμές $l_m=l_n=l_p=6$:

Total Execution Time: 1311095ns.

Min latency: 131089.

Avg. latency: 131089.

Max latency: 131089.



General Information

Date:	Mon Oct 30 20:18:06 GTBST 2023	Solution:	solution1 (Vivado IP Flow Target)
Version:	2022.2 (Build 3670227 on Oct 13 2022)	Product family:	virtexuplus
Project:	Lab1matrix	Target device:	xcu200-fsgd2104-2-e
Status:	Pass		

Cosim Options

Tool: Vivado XSIM RTL: Verilog

Dump Trace: port

Performance Estimates

Modules & Loops	Avg II	Max II	Min II	Avg Latency	Max Latency	Min Latency
MATRIX_MUL				131089	131089	131089
VITIS_LOOP_18_1_VITIS_LOOP_19_2				131090	131090	131090

```
$finish called at time : 1311095 ns : File "C:/Users/Paschalis/AppData/Roaming/Xilinx/Vitis/Lab1matrix/
run: Time (s): cpu = 00:00:03 ; elapsed = 00:00:05 . Memory (MB): peak = 238.996 ; gain = 0.000
## quit
INFO: [Common 17-206] Exiting xsim at Mon Oct 30 20:18:06 2023...
INFO: [COSIM 212-316] Starting C post checking ...
```

- Question 4(40%):

1.

Keeping l_m = constant and changing l_n and l_p , it was observed that the number of DSPs dropped. Also, no BRAMs were used at all. Additionally, the number of FFs and LUTs was also reduced. This happened probably because

the arrays weren't symmetrical and the data couldn't be treated in same size "blocks", thus less hardware was used.

2.

για τις τιμές $l_m=l_n=l_p=6$:

Estimated clock period: 5.259ns

Number of DSP48E used: 2048.

Number of BRAMs used: 64.

Number of FFs used: 66738.

Number of LUTs used: 158828.

Total Execution Time: 46985ns.

Min latency: 4678.

Avg. latency: 4678.

Max latency: 4678.

Summary

Clock	Target	Estimated	Uncertainty
ap_clk	10.00 ns	5.259 ns	2.70 ns

Latency

Summary

Latency (cycles)		Latency (absolute)		Interval (cycles)		Type
min	max	min	max	min	max	
4682	4682	46.820 us	46.820 us	4683	4683	no

Detail

Instance

Loop

Utilization Estimates

Summary

Name	BRAM_18K	DSP	FF	LUT	URAM
DSP	-	-	-	-	-
Expression	-	-	0	2	-
FIFO	-	-	-	-	-
Instance	-	2048	33451	133809	-
Memory	64	-	0	0	0
Multiplexer	-	-	-	25017	-
Register	-	-	33287	-	-
Total	64	2048	66738	158828	0
Available	4320	6840	2364480	1182240	960
Available SLR	1440	2280	788160	394080	320
Utilization (%)	1	29	2	13	0
Utilization SLR (%)	4	89	8	40	0

```

$finish called at time : 46985 ns : File "C:/Users/Paschalis/AppData/Roaming/Xilinx/Vitis/Matrix/solution1/sim/verilog/MATRIX_MUL_HW.autotb.v" Line 2502
run: Time (s): cpu = 00:00:00 ; elapsed = 00:00:12 . Memory (MB): peak = 326.055 ; gain = 0.000
## quit
INFO: [Common 17-206] Exiting xsim at Sat Nov  4 18:41:28 2023...
INFO: [COSIM 212-316] Starting C post checking ...

```

3.

$$\text{speedup} = 1311095/46985 = 28.$$