## Wire + void update() + void set signal(int signal) + int get signal() const #inputs #output Component + virtual void update()=0 #wires + virtual void write (Wire \*base address, std::ostream &os=std ::cout)=0 #components

## LogicNetwork

- + LogicNetwork(size
  \_t wires\_size, std::
  ostream &os=std::cout)
- + void update()
- + void bulk\_update(size
   \_t update\_count)
- + Wire \* get\_wire(size \_t wire\_id)
- + void add\_component (Component \*component)
- + std::ostream & get\_os()