## LogicNetwork

+ LogicNetwork(size t wires size, std::

ostream &os=std::cout) + void update()

+ void bulk update(size t update count) + Wire \* get wire(size

t wire id) + void add component (Component \*component)

+ std::ostream & get\_os()



LogicNetworkConfigurer

+ void read logic network (std::istream &is) + void write logic network (std::ostream &os)