4 Bit Bi-directional Shift Register with Parallel Load

Naga Ganesh Kurapati

University of Massachusetts Lowell
ECE Department

Instructor: Kanti Prasad

Table of contents **Page No.**

1. Introduction

4-bit bidirectional shift register can be used to shift-left or shift-right the serial data to produce parallel data. And can hold parallel data for next clock-period. It is built with two main types of basic components, D-flip flop and multiplexer. The schematic, layout of the circuit is developed using Cadence software. Initially, layout of the basic components is developed and tested for variable inputs. And then integrating those components to form the shift register. Finally, waveforms of output for given inputs are produced. To produce desired results, the components in the schematic, layout should match. And this can be done using LVS feature in the software.

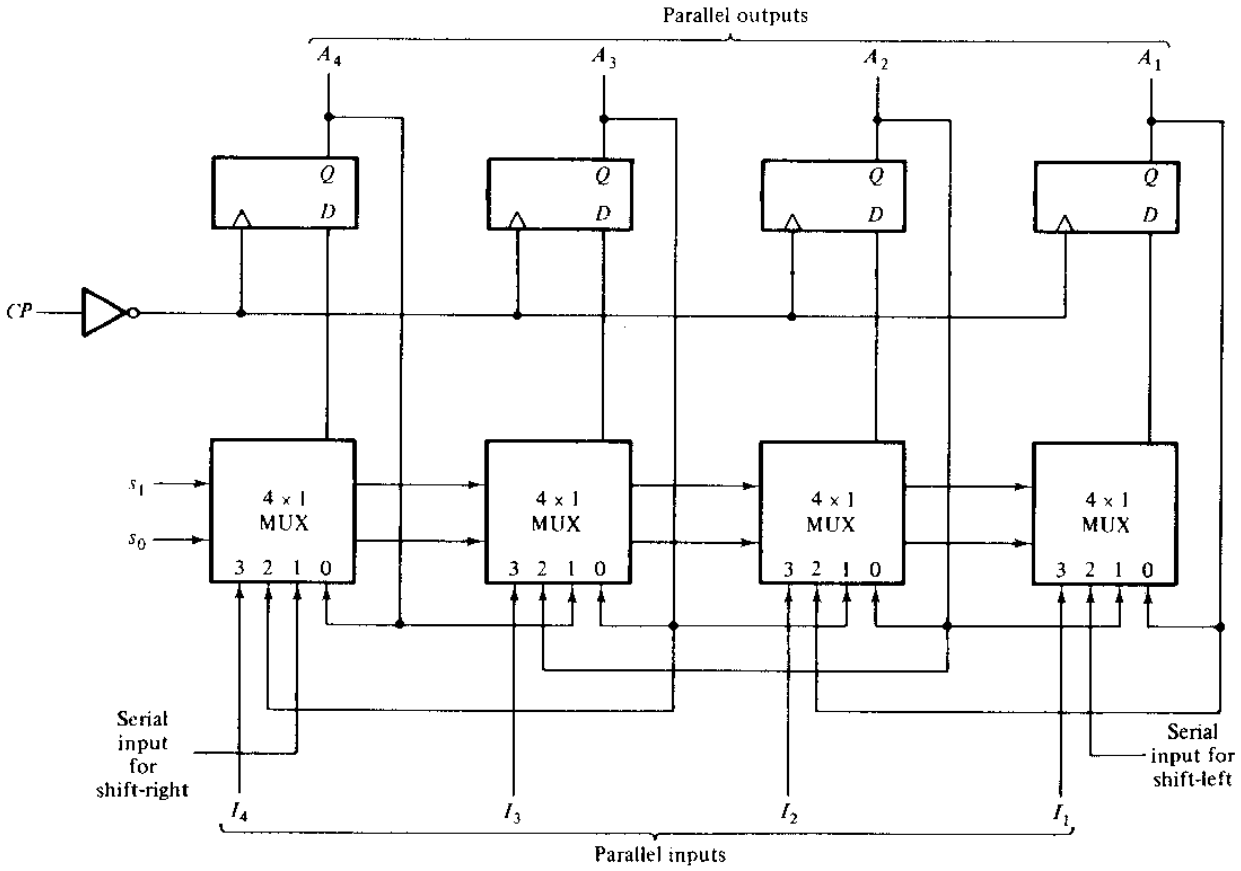
2. Problem Formulation

A bidirectional shift register can shift the data both left and right. It has also parallel load capabilities. So, it is called shift register with parallel load. Fig.-1 is a bidirectional shift register with parallel load consists of four D flip-flops and 4:1 Multiplexers each. The Multiplexers having select lines S1, S2 and they help to switch the operations as shown in the Table-1.

Mode of operation of bidirectional shift register

S1	**S2**	**Operation**
0	0	No change
0	1	Shift right
1	0	Shift left
1	1	Parallel Load

Table-1



Source: Digital Design Book 3rd edition by M. Morris Mano

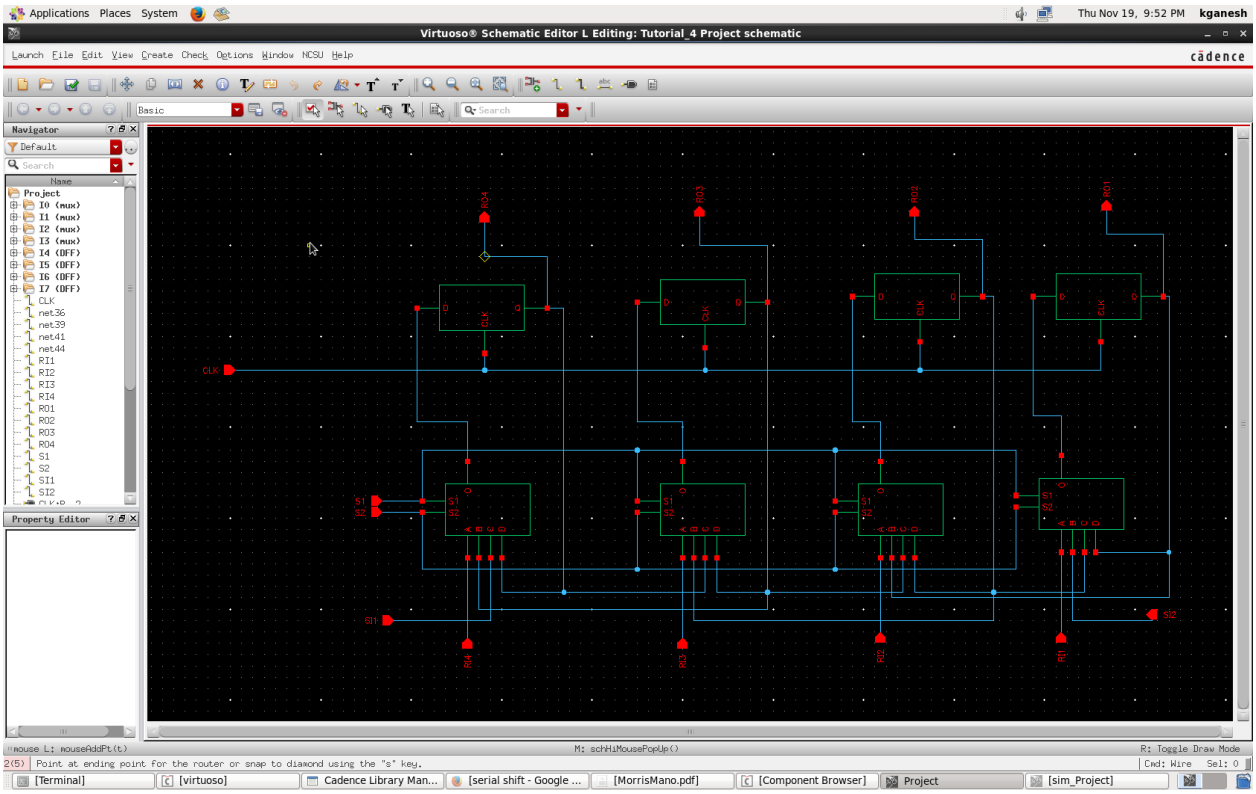
Fig.-1

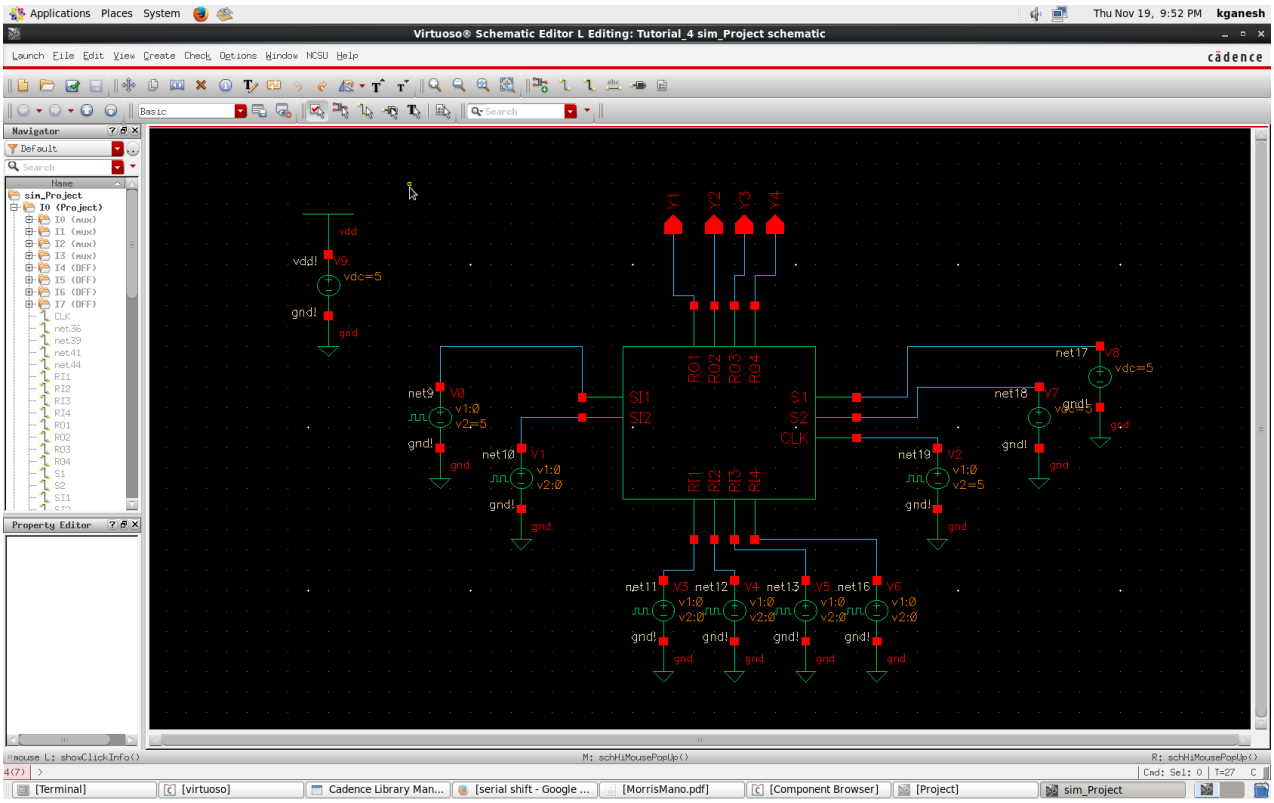
The operations can be explained as below:

1. When shift-right operation is selected, Serial input send through the pin *serial input for shift-right* and output received through parallel outputs.
2. When shift-left operation is selected, Serial input send through the pin *serial input for shift-left* and output received through parallel outputs.
3. When parallel mode is selected, parallel input is given through I1, I2, I3, I4 and output received through parallel outputs A1, A2, A3, and A4.

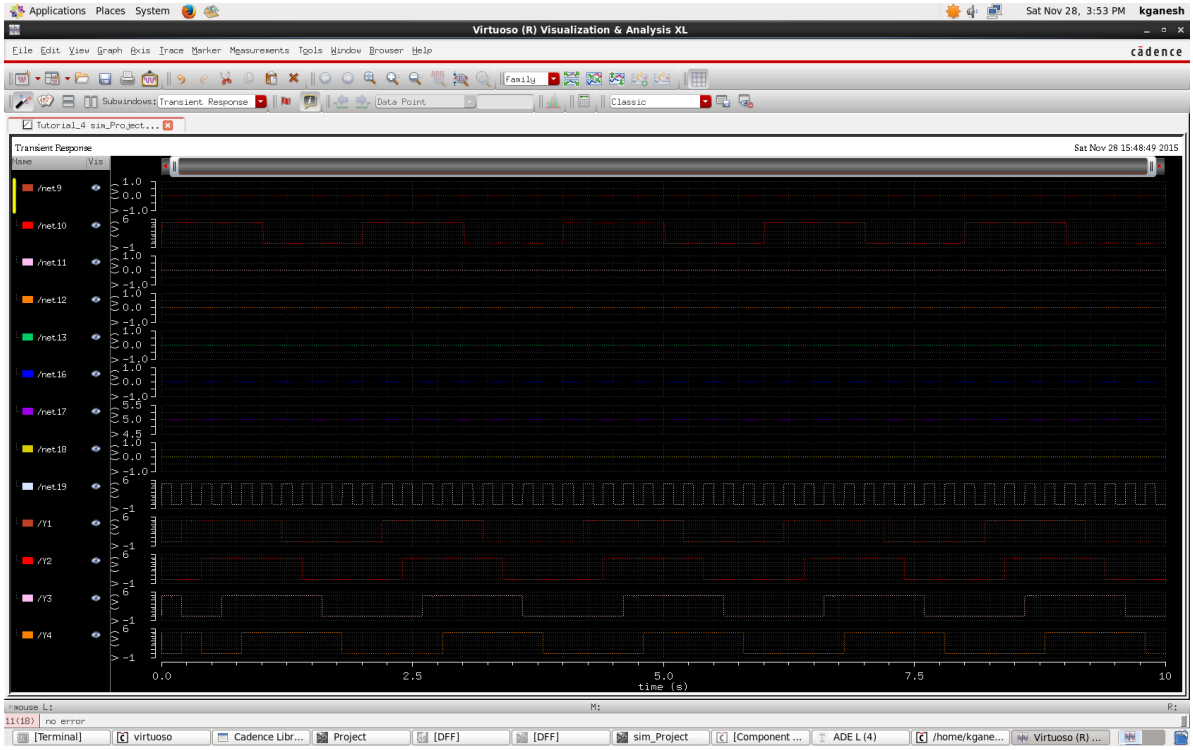
3. CMOS Design

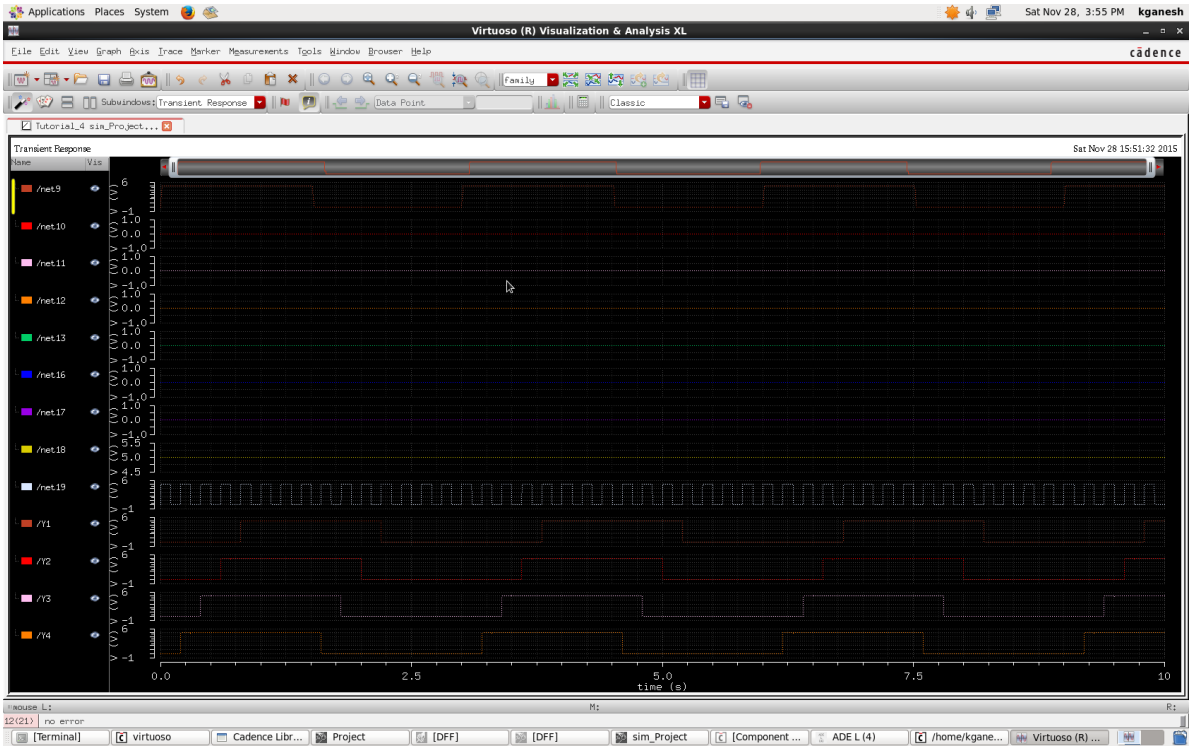
3.1 Schematic of 4-bit shift register



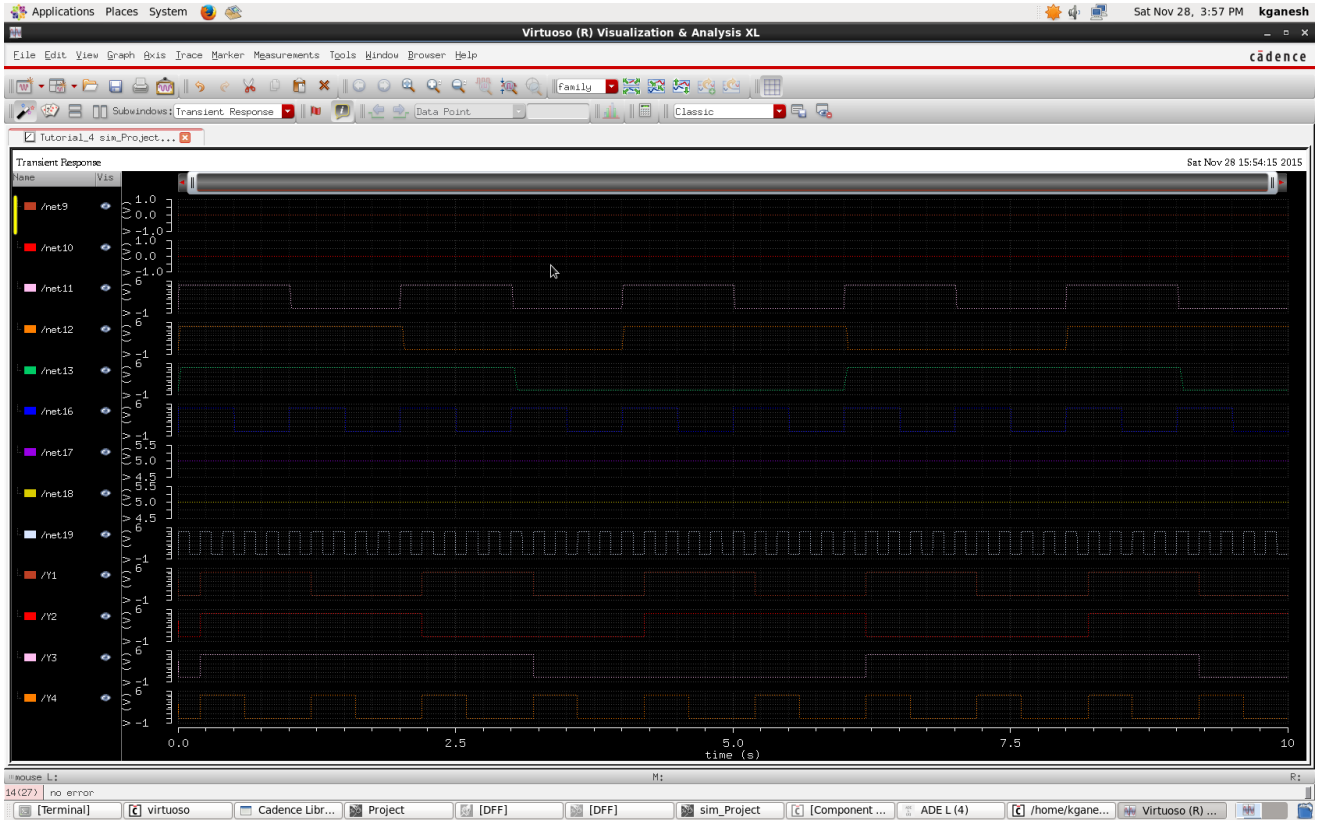


3.2 Output waveforms of shift-right and shift-left operation

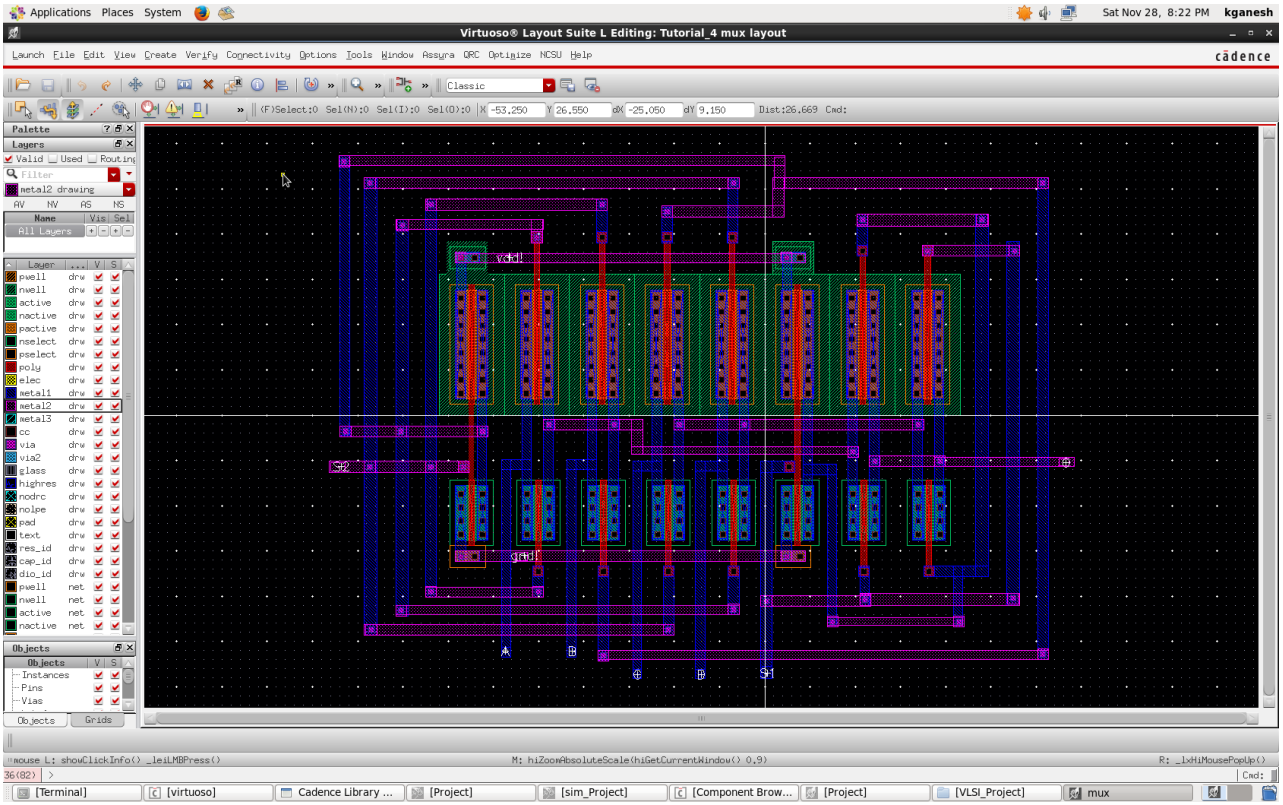


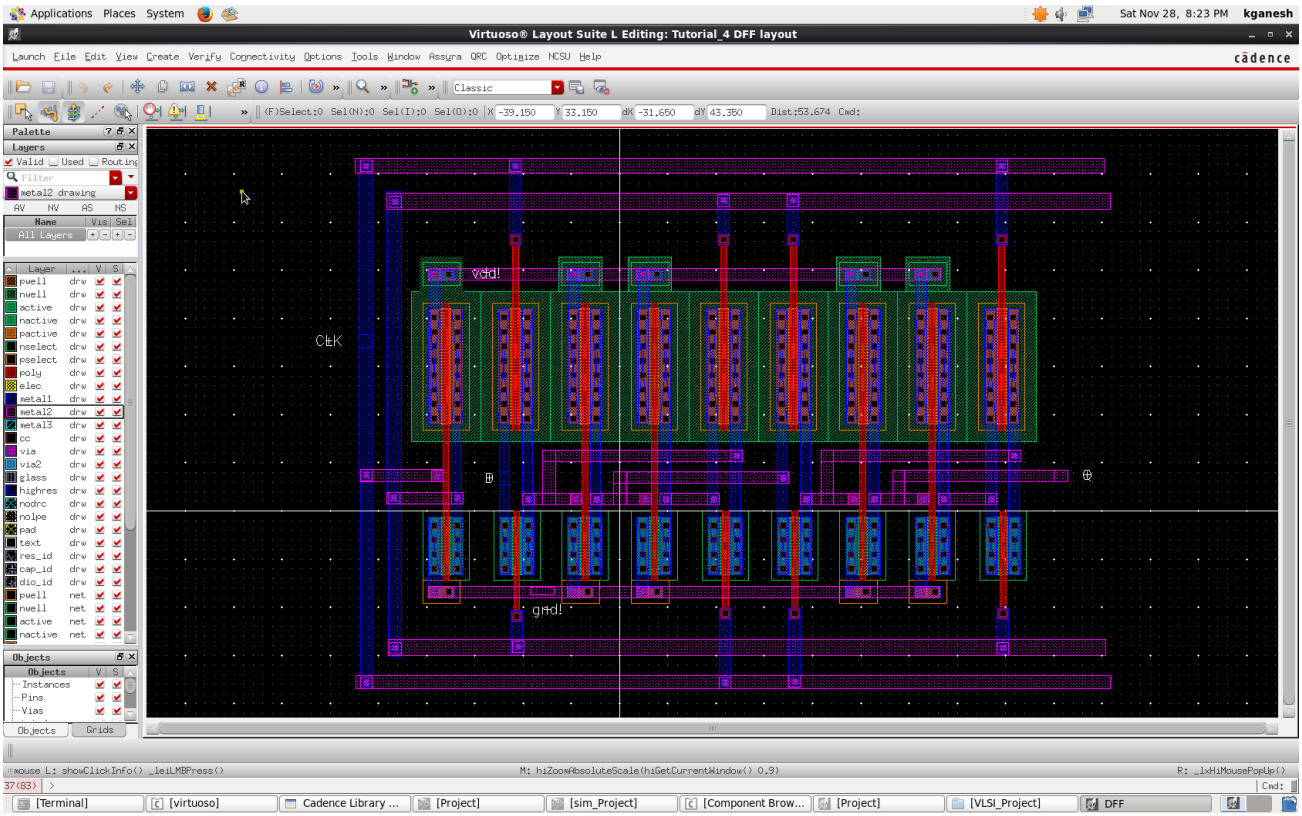


3.3 Output waveform of parallel data operation



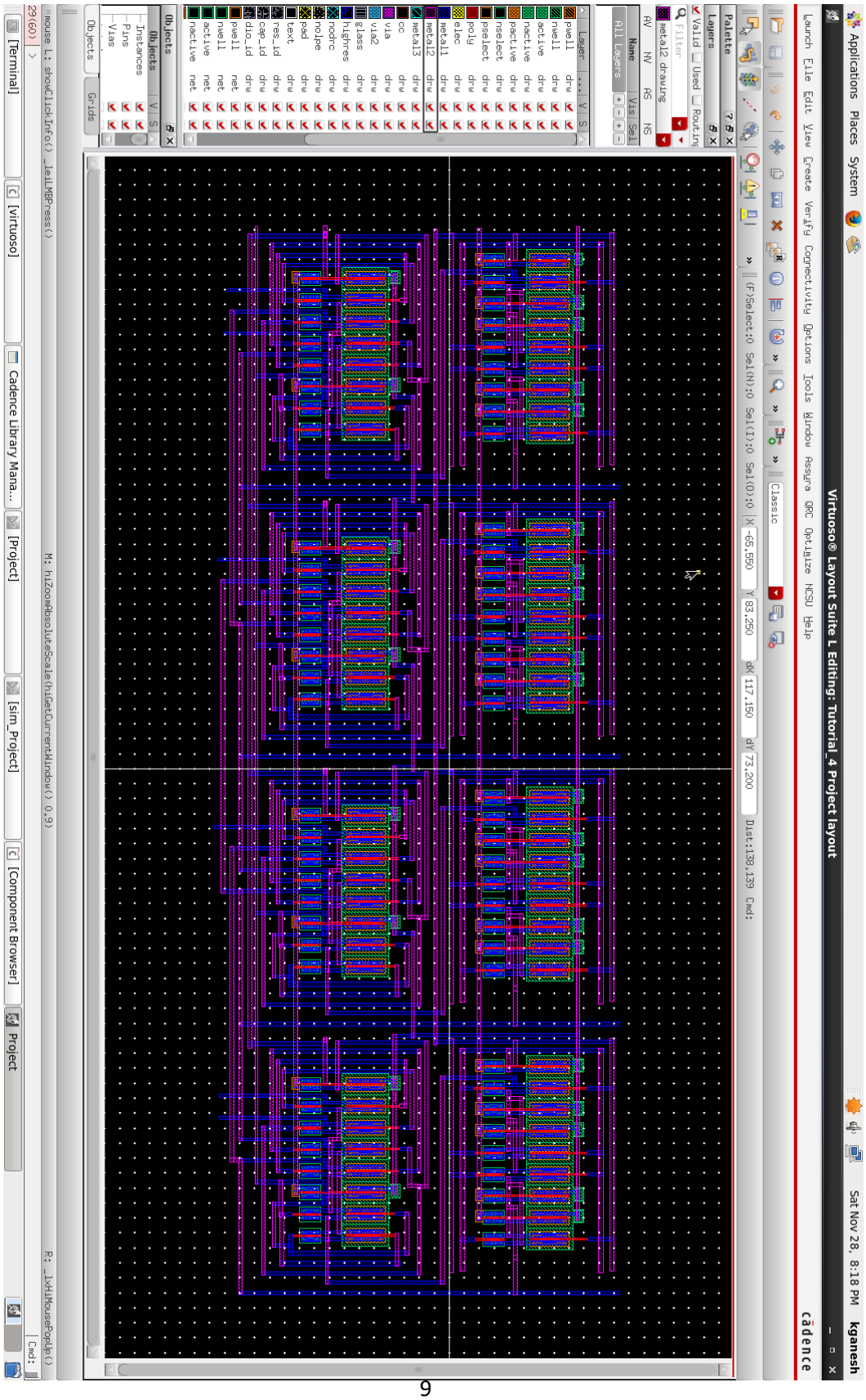
3.4 Layout of 4:1 multiplexer and D flip-flop





3.5

Layout of 4-bit Bidirectional Shift register with parallel load



Cadence Virtuoso Software is used to design the schematic and layout. Initially, they are generated for D flip-flop, Multiplexer separately and are integrated to form shift register as shown in the section 3.5. The layout for D flip-flop and mux can be seen in the section 3.4. The output waveforms for Shift-right, Shift-left and parallel operation can be seen in section 3.2, 3.3 respectively.

4. Trouble Shooting

1. To utilize the minimum area, pre-planning of connections should be made. Otherwise, you will end up with complex metal connection and larger area.
2. Make sure that m2-m1 cell is placed on ploy cell if your connecting m2-type metal with ploy cell.

5. Conclusion

Successfully designed the schematic and layout of 4 bit bidirectional shift register using cadence virtuoso software. The output waveforms for shift-right, shift-left and parallel operations is obtained.

6. References

1. Seok Chang Kim and Byeong Gi Lee, “Realizations of Parallel and Multibit-Parallel Shift Register Generators,” IEEE transactions on communications, vol. 45, no. 9, september 1997.
2. Page No.268, Digital Design Book 3rd edition by M. Morris Mano.