1. Description

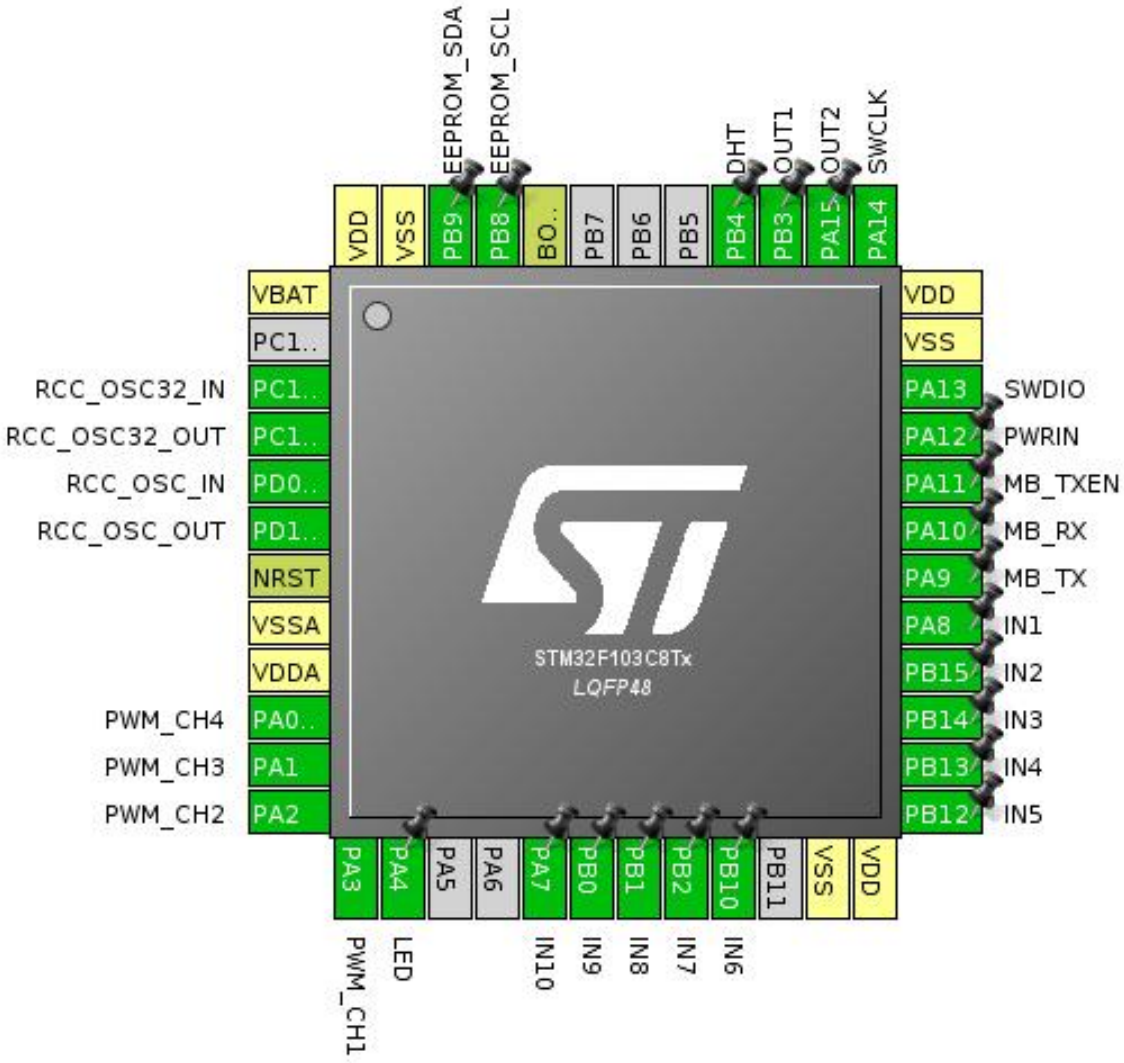
1.1. Project

Project Name	stm32F103-bath
Board Name	custom
Generated with:	STM32CubeMX 4.9.0
Date	07/23/2020

1.2. MCU

MCU Series	STM32F1
MCU Line	STM32F103
MCU name	STM32F103C8Tx
MCU Package	LQFP48
MCU Pin number	48

2. Pinout Configuration



3. Pins Configuration

Pin Number LQFP48	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VBAT	Power		
3	PC14-OSC32_IN	I/O	RCC_OSC32_IN	
4	PC15-OSC32_OUT	I/O	RCC_OSC32_OUT	
5	PD0-OSC_IN	I/O	RCC_OSC_IN	
6	PD1-OSC_OUT	I/O	RCC_OSC_OUT	
7	NRST	Reset		
8	VSSA	Power		
9	VDDA	Power		
10	PA0-WKUP	I/O	TIM2_CH1	PWM_CH4
11	PA1	I/O	TIM2_CH2	PWM_CH3
12	PA2	I/O	TIM2_CH3	PWM_CH2
13	PA3	I/O	TIM2_CH4	PWM_CH1
14	PA4 *	I/O	GPIO_Output	LED
17	PA7 *	I/O	GPIO_Input	IN10
18	PB0 *	I/O	GPIO_Input	IN9
19	PB1 *	I/O	GPIO_Input	IN8
20	PB2 *	I/O	GPIO_Input	IN7
21	PB10 *	I/O	GPIO_Input	IN6
23	VSS	Power		
24	VDD	Power		
25	PB12 *	I/O	GPIO_Input	IN5
26	PB13 *	I/O	GPIO_Input	IN4
27	PB14 *	I/O	GPIO_Input	IN3
28	PB15 *	I/O	GPIO_Input	IN2
29	PA8 *	I/O	GPIO_Input	IN1
30	PA9	I/O	USART1_TX	MB_TX
31	PA10	I/O	USART1_RX	MB_RX
32	PA11 *	I/O	GPIO_Output	MB_TXEN
33	PA12 *	I/O	GPIO_Input	PWRIN
34	PA13	I/O	SYS_JTMS-SWDIO	SWDIO
35	VSS	Power		
36	VDD	Power		
37	PA14	I/O	SYS_JTCK-SWCLK	SWCLK
38	PA15 *	I/O	GPIO_Output	OUT2
39	PB3 *	I/O	GPIO_Output	OUT1
40	PB4	I/O	TIM3_CH1	DHT

Pin Number LQFP48	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
44	BOOT0	Boot		
45	PB8	I/O	I2C1_SCL	EEPROM_SCL
46	PB9	I/O	I2C1_SDA	EEPROM_SDA
47	VSS	Power		
48	VDD	Power		

* The pin is affected with an I/O function

4. IPs and Middleware Configuration

4.1. ADC1

mode: Temperature Sensor Channel

mode: Vrefint Channel

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Data Alignment	Right alignment
Scan Conversion Mode	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Enable Regular Conversions	Enable
Rank	1
Channel	**Channel Temperature Sensor ***
Sampling Time	1.5 Cycles

ADCgroup:

Number Of Conversion	1
External Trigger Conversion Edge	None
Number Of Conversions	0
Number Of Conversion	1
External Trigger Conversion Edge	None

WatchDog:

Enable Analog WatchDog Mode	false

4.2. I2C1

I2C: I2C

Master Features:

I2C Speed Mode	Standard Mode
I2C Clock Speed (Hz)	100000

Slave Features:

Clock No Stretch Mode	Disabled

Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0
General Call address detection	Disabled

4.3. IWDG

mode: Activated

Clocking:

IWDG counter clock prescaler	4
IWDG down-counter reload value	4095

4.4. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

Low Speed Clock (LSE) : Crystal/Ceramic Resonator

System Parameters:

VDD voltage (V)	3.3
Prefetch Buffer	Enabled
Flash Latency(WS)	2 WS (3 CPU cycle)

RCC Parameters:

HSI Calibration Value	16

4.5. RTC

RTC OUT: No RTC Output

General:

Auto Predivider Calculation	Enabled
Asynchronous Predivider value	Automatic Predivider Calculation Enabled
Output	No output on the TAMPER pin

Calendar Time:

Data Format	BCD data format

4.6. SYS

Debug: Serial-Wire

4.7. TIM1

Clock Source : Internal Clock

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	0
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

4.8. TIM2

Clock Source : Internal Clock

Channel1: PWM Generation CH1

Channel2: PWM Generation CH2

Channel3: PWM Generation CH3

Channel4: PWM Generation CH4

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	0
Internal Clock Division (CKD)	No Division

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable

CH Polarity	High

PWM Generation Channel 3:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 4:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High

4.9. TIM3

mode: Clock Source

Channel1: Input Capture direct mode

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	0
Internal Clock Division (CKD)	No Division

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Input Capture Channel 1:

Polarity Selection	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

4.10. USART1

Mode: Asynchronous

Basic Parameters:

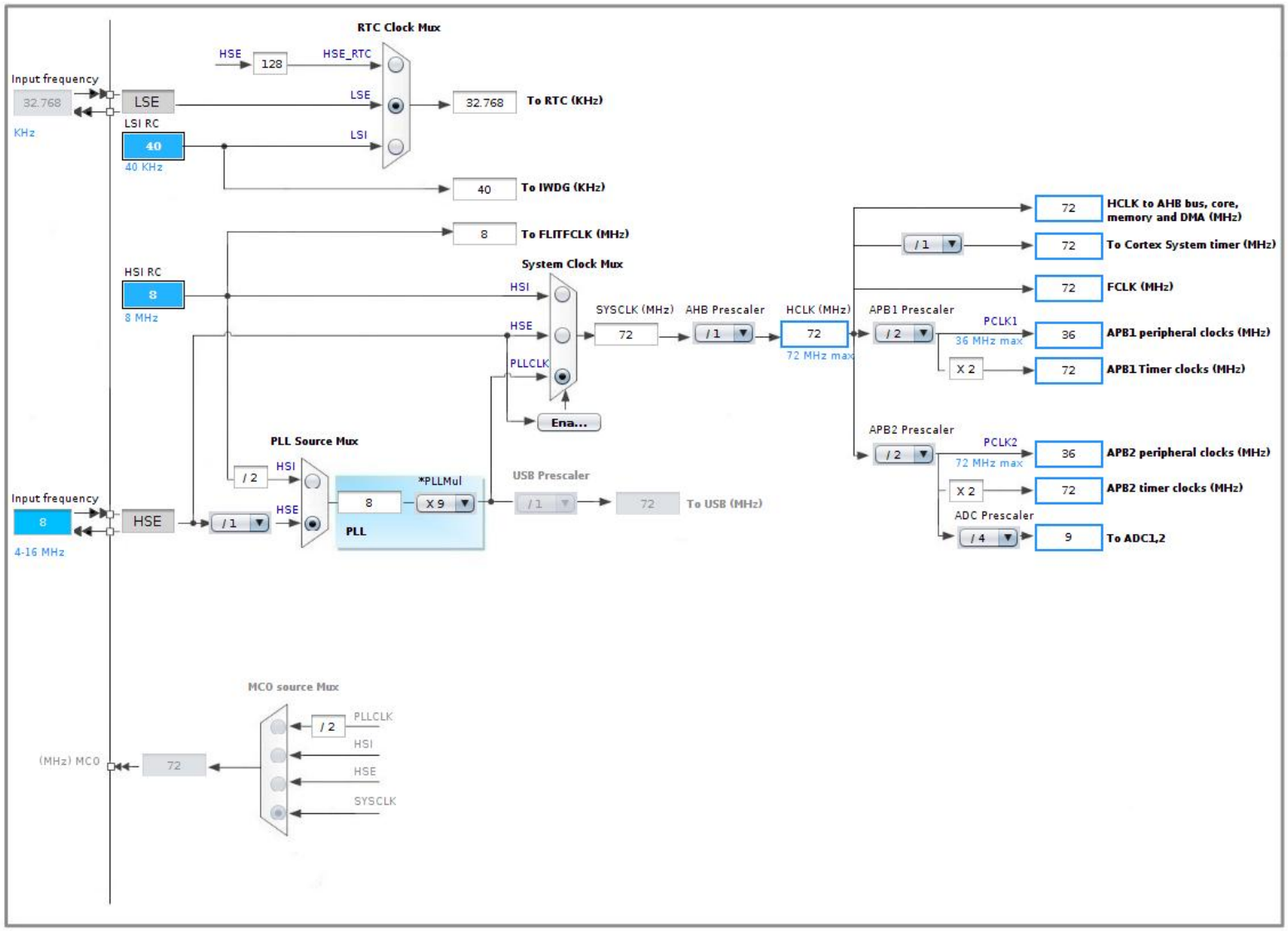
Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

* User modified value

2. Clock Tree Configuration



3. Power Plugin report

3.1. Microcontroller Selection

Series	STM32F1
Line	STM32F103
MCU	STM32F103C8Tx
Datasheet	13587_Rev16

3.2. Parameter Selection

Temperature	25
Vdd	3.3

3.3. Battery Selection

Battery	Alkaline(AA LR6)
Capacity	2850.0 mAh
Self discharge	0.3 %/month
Nominal voltage	1.5 V
Max Cont Current	1000.0 mA
Max Pulse Current	0.0 mA
Cells in series	1
Cells in parallel	1

3.4. Sequence

Step	STEP1
Mode	RUN
Range	No Scale
Fetch type	FLASH

Clock Config.	HSE PLL
Clock Source Freq.	8.0 MHz
CPU Freq.	72.0 MHz
Periph.	ADC1 GPIOA GPIOB GPIOC I2C1 IWDG RTC TIM2 TIM3 TIM4 USART1
Additional Cons.	0 mA
Average Current	35.44 mA
Duration	1 ms
DMIPS	90.0

3.5. Results

Sequence time	1 ms	Average current	35.44 mA
Battery Life	3 days & 8 hours	Average DMIPS	90.0 DMIPS

3.6. Chart