XILINX
ALL PROGRAMMABLE™

Digital Design Tutorial

Xilinx University Program

XILINX
ALL PROGRAMMABLE™

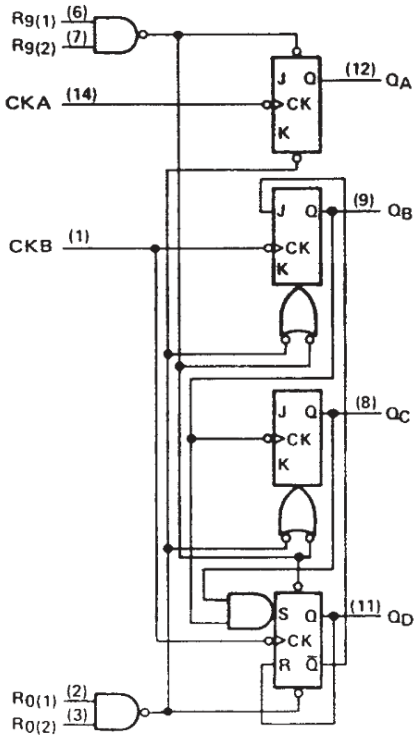
Digital Clock

- 实验介绍
- 演示

实验介绍

数字钟是一个以秒为单位的计时器，可以在数码管上显示“秒”和“分”。通过将FPGA时钟分频，得到1秒为周期的时钟信号作为脉冲激励。同时使用计数电路74LS90和与门电路74LS08搭建模60计数器。并将最终的时间通过数码管模块显示在板卡的数码管上。

SN74LS90



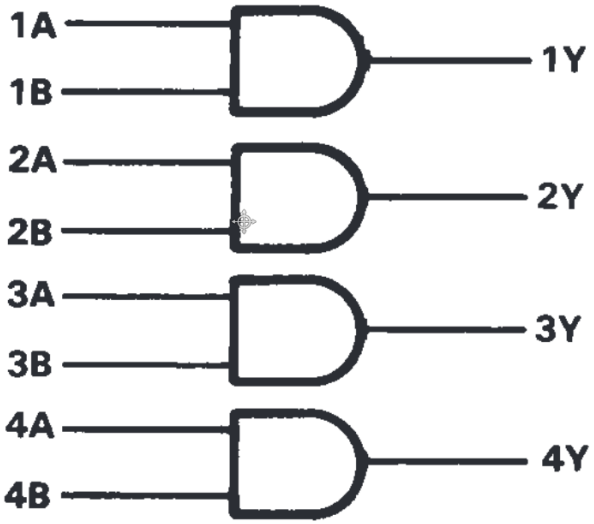
Input				Output			
R0_1	R0_2	R9_1	R9_2	qa	qb	qc	qd
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
X	L	X	L	Count			
L	X	L	X				
L	L	X	X				
X	X	L	L				

H=High-Level L=Low-Level X=Don’t Care

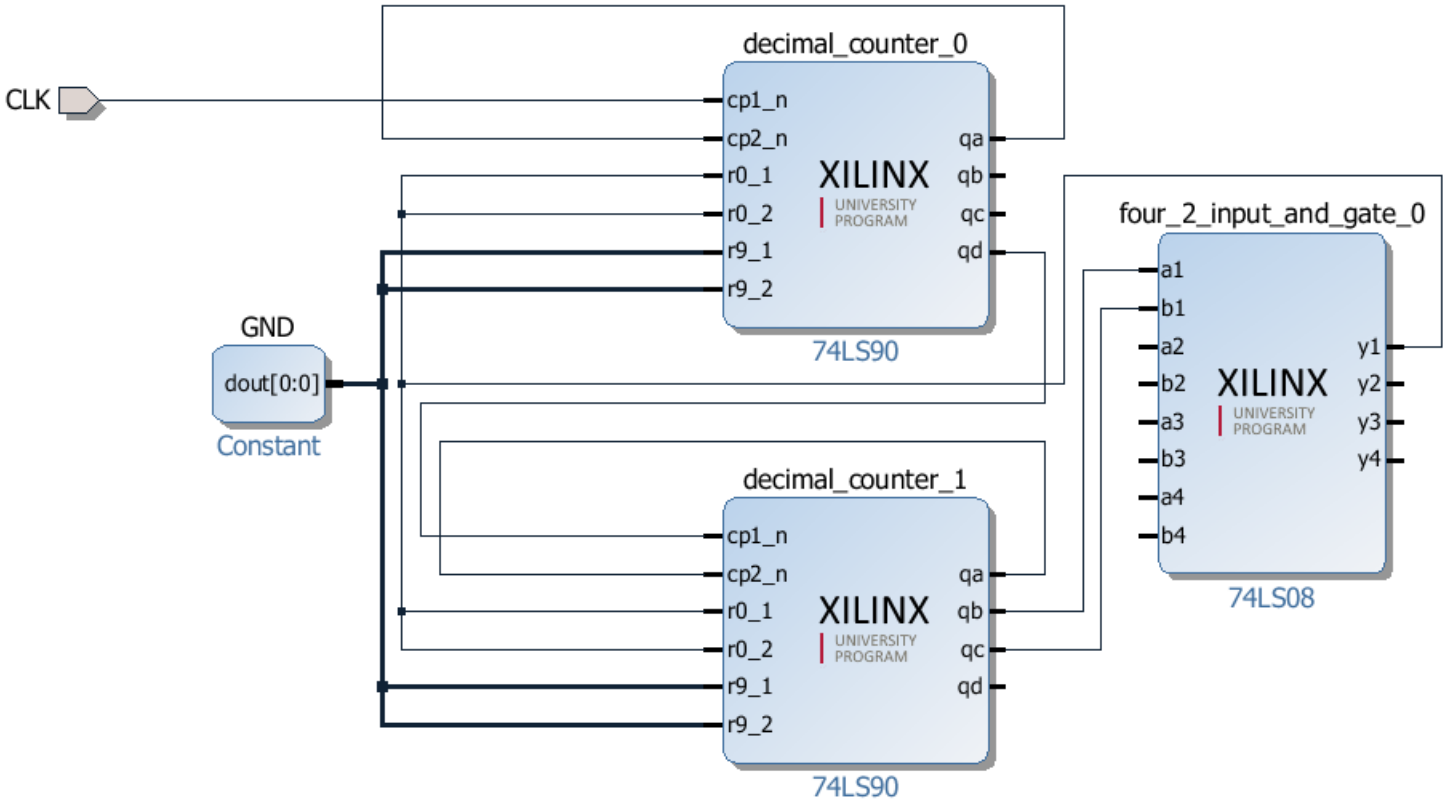
SN74LS08

Input		Output
a1	b1	y1
L	X	L
X	L	L
H	H	H

H=High-Level L=Low-Level X=Don’t Care



模60计数器



Vivado Flow Overview

- Step 1: Create New Project
- Step 2: Add Source Files and IP
- Step 3: Generate Bitstream
- Step 4: Download Bitstream and Verify Functionality

Step 1: Create New Project

- **Specify Project Name**
- **Specify Project Type**
- **Import/Create Source files**
- **Specify Device to be used**

Step 2: Add Source Files and IP

- **Create Block Design**
- **Open IP Catalog**
- **Add IP Repository**
- **Add IP to the project**
- **Create HDL wrapper**

Step 3: Generate Bitstream

- **Add Pin Constraints**
- **Generate Bitstream**
- **Check your Timing in Design Runs Window**

Step 4: Download Bitstream and Verify Functionality

- Make sure your board is connected to your PC
- Turn on your FPGA board
- Open Hardware Manager
- Program Device
- Verify Functionality on Hardware

总结

- 创建Block Design
- 在Block Design内添加IP
- 74LS90和74LS08