SoC Design Laboratory Lab3 Report

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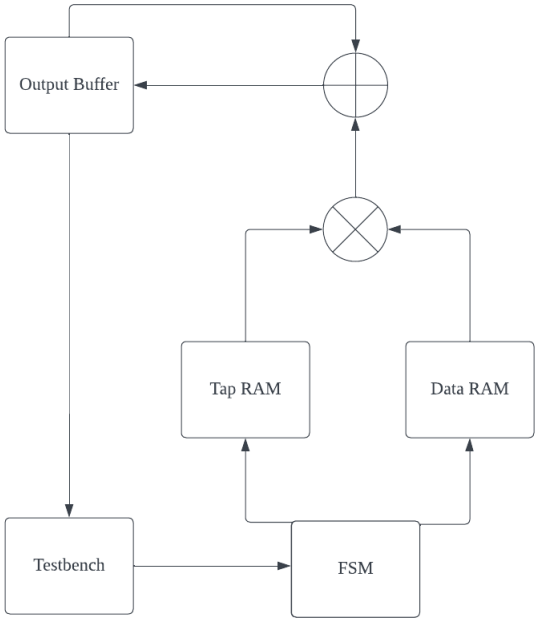
1. Block Diagram
   - Datapath



   - Control signals
     FSM to Tap RAM: tap_A, tap_WE, tap_EN, tap_Di
     FSM to Data RAM: data_A, data_WE, data_EN, data_Di
     Output handling: sm_tvalid, sm_tready, sm_tlast
2. Operation
   - How to receive data-in and tap parameters and place into SRAM
     i. Data RAM: Implemented as a queue. I shift the address and place the new data in the address the originally stored the oldest data.
     ii. Tap RAM: Set tap_EN to 1 to access the RAM and set tap_WE to 1111 when writing tap parameter to BRAM.
   - How to access shiftram and tapRAM to do computation
     Since there is one cycle delay from we set an address to get the corresponding data, we need to set the desired address at cycle k-1 if we want to get data at cycle k. Also, we need to set EN to 1 and WE to 0000 if we want to access data from BRAM.
   - How ap_done is generated.
     In my design, I set a 32-bit variable called config_r. When sm_tready && sm_tvalid && sm_tlast is 1, I set the config_r to 32'h0000_0006. After one cycle, the config_r would send to r_data and got received by testbench.

3. Resource Usage

1. Slice Logic

Site Type	Used	Fixed	Prohibited	Available	Util%
Slice LUTs*	281	0	0	53200	0.53
LUT as Logic	281	0	0	53200	0.53
LUT as Memory	0	0	0	17400	0.00
Slice Registers	278	0	0	106400	0.26
Register as Flip Flop	278	0	0	106400	0.26
Register as Latch	0	0	0	106400	0.00
F7 Muxes	0	0	0	26600	0.00
F8 Muxes	0	0	0	13300	0.00

2. Memory

Site Type	Used	Fixed	Prohibited	Available	Util%
Block RAM Tile	0	0	0	140	0.00
RAMB36/FIFO*	0	0	0	140	0.00
RAMB18	0	0	0	280	0.00

4. Timing Report
   - Synthesis Frequency

     66.67MHz
   - Timing on longest path and slack

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Max Delay Paths
--------------------------------------------------------------------------------------
Slack (MET) :             1.261ns  (required time - arrival time)
  Source:                 data_length_reg[1]/C
                            (rising edge-triggered cell FDCE clocked by axis_clk  {rise@0.000ns fall@7.500ns period=15.000ns})
  Destination:            accumulated_result_reg[29]/D
                            (rising edge-triggered cell FDCE clocked by axis_clk  {rise@0.000ns fall@7.500ns period=15.000ns})
  Path Group:             axis_clk
  Path Type:              Setup (Max at Slow Process Corner)
  Requirement:            15.000ns  (axis_clk rise@15.000ns - axis_clk rise@0.000ns)
  Data Path Delay:        13.634ns  (logic 9.575ns (70.227%)  route 4.059ns (29.773%))
  Logic Levels:           15  (CARRY4=9 DSP48E1=2 LUT2=1 LUT3=1 LUT4=1 LUT5=1)
  Clock Path Skew:        -0.145ns (DCD - SCD + CPR)
    Destination Clock Delay (DCD):    2.128ns = ( 17.128 - 15.000 )
    Source Clock Delay      (SCD):    2.456ns
    Clock Pessimism Removal (CPR):    0.184ns
  Clock Uncertainty:      0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter     (TSJ):    0.071ns
    Total Input Jitter      (TIJ):    0.000ns
    Discrete Jitter          (DJ):    0.000ns
    Phase Error              (PE):    0.000ns
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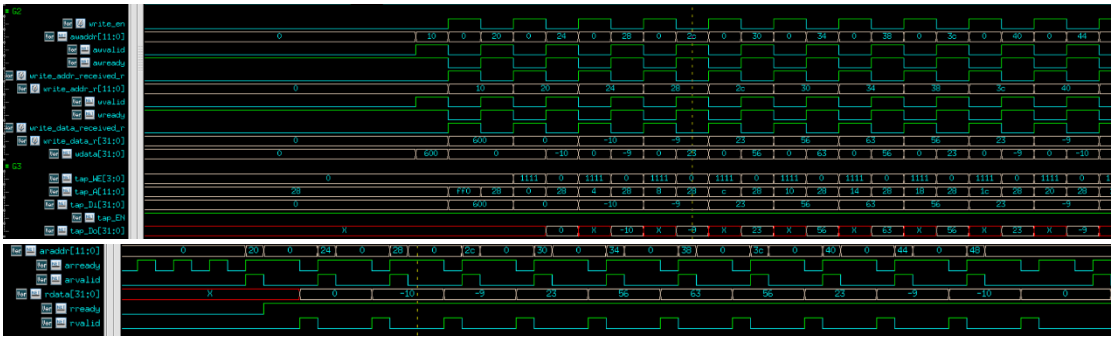
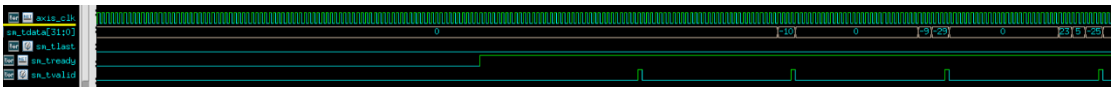
5. Simulation Waveform
   - Coefficient program, and read back



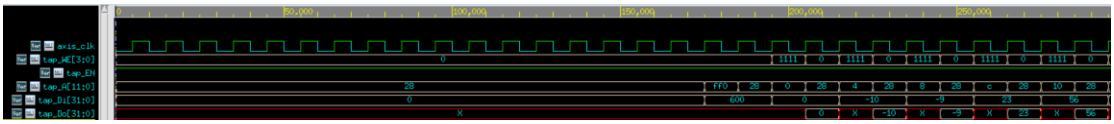
- Data-in stream-in

- Data-out stream-out

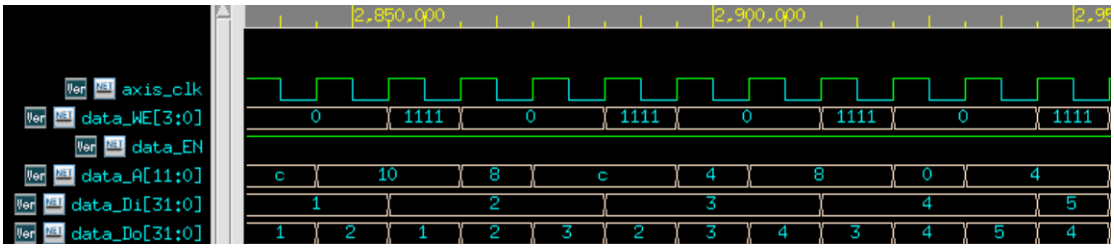


- RAM access control

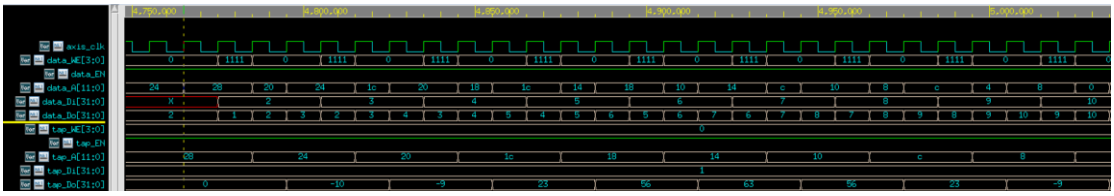
  Tap Write



  Data Write



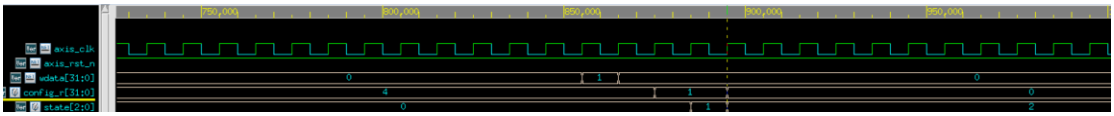
  Tap & Data Read



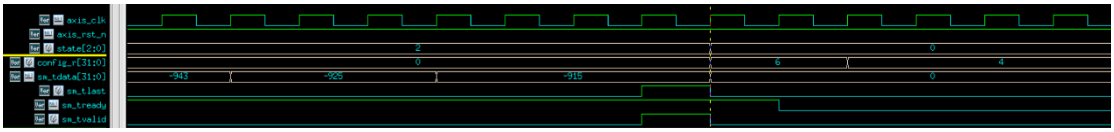
- FSM

```
always @(*) begin
    case (state)
        IDLE: state_next = config_r[0] ? SET_UP : IDLE;
        SET_UP:  begin
            state_next = ss_tvalid ? COMPUTE : SET_UP;
        end
        COMPUTE: begin
            state_next = !(sm_tlast && sm_tready && sm_tvalid) ? COMPUTE : IDLE;
        end
        default: state_next = IDLE;
    endcase
end
```

ap_start



ap_done



ap_start to ap_done: 21005 cycles.