8K x 8 Bit Mask ROM

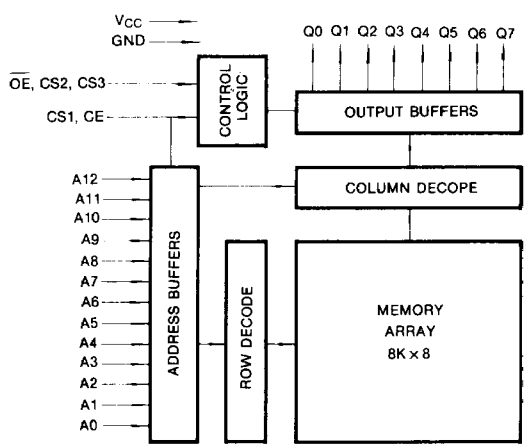
FEATURES

- **2364/65: Non-power down**
- **2364S/65S: Automatic power down**
- **Fully static operation**
- **Silicon gate NMOS technology**
- **Maximum access time**
  2364/65-20: 200 ns
  2364/65-25: 250 ns
  2364/65-30: 300 ns
- **Programmable chip selects**
- **3-State outputs**
- **Fully TTL compatible**
- **Single ±10% 5 volt supply**
- **Pin compatible with 2564 EPROM's**
- **Available in 3 temperature ranges**
  2364/65 (Commercial): 0°C to 70°C
  2364I/65I (Industrial): −40°C to 85°C
  2364HR/65HR (Military): −55°C to 125°C

GENERAL DESCRIPTION

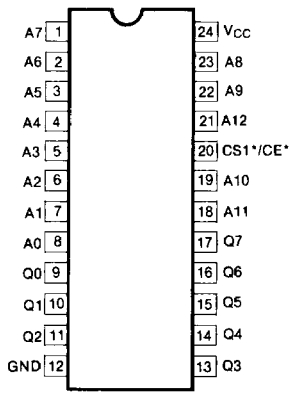
The KM2365/65 are mask programmable read only memories with 8K word by 8 bit organizations. Designed for ease of use, these devices require only a 5-volt supply, are TTL compatible, and because of their totally static (asynchronous) operation require no clock. These memory devices are available in two versions. The 2364/65 are non-power down versions where the active level of chip selects CS1 (on the 2364), and CS2 and CS3 (on the 2365) are programmable and defined by the user to facilitate system memory expansion. The 2364S and 2365S are standby versions offering an automatic power-down feature controlled by the chip enable CE input. When CE goes high, the device automatically powers down and remains in a low power standby mode as long as CE remains high. Also to provide easier system implementation, the active level of chip enable CE (on the 2364S), and chip selects CS2 and CS3 (on the 2365S) is programmable. The KM2364 is packaged in a 24 pin DIP, and the 2365 is packaged in a 28 pin DIP, both with industry standard byte-wide JEDEC pin-outs. Optionally, the 2365 is available in a space saving 28 pin surface mounted plastic leaded chip carrier.

FUNCTIONAL BLOCK DIAGRAM

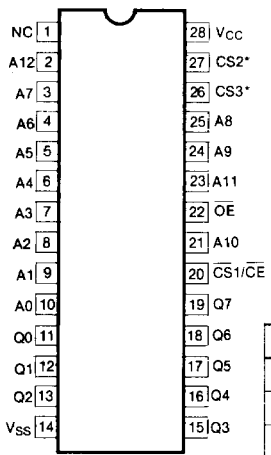


PIN CONFIGURATION

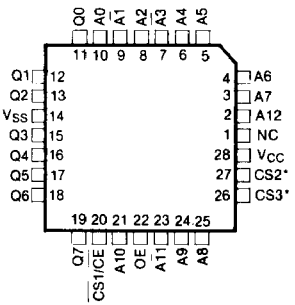
KM2364/S



KM2365/S



*Active Level (Hi, Low or Don't Care) defined by user.



Pin Name	Pin Function
A_0-A_{12}	Address Inputs
Q_0-Q_7	Data Outputs
CS1, $\overline{CS1}$ CS2, CS3	Programmable Chip Select
CE, $\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
V_{CC}	5V ± 10% Supply Voltage

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Voltage on Any Pin with Respect to Ground	V_{CC}	−0.5 to +7V	V
Storage Temperature	T_{stg}	−65 to +150	°C

Stresses above "absolute maximum ratings" may result in damage to the device. Functional operation of devices at the "absolute maximum ratings" or above the recommended operating conditions stipulated elsewhere in this specification is not implied.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	KM2364/65			KM2364I/65I			KM2364HR/65HR			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Supply Voltage*	V_{CC}	4.5	5.0	5.5	4.5	5.0	5.5	4.5	5.0	5.5	Volts
Input High Level Voltage	V_{IH}	2.0		V_{CC}	2.0		V_{CC}	2.2		V_{CC}	Volts
Input Low Level Voltage	V_{IL}	−0.5		0.8	−0.5		0.8	−0.5		0.8	Volts
Operating Ambient Temperature	T_A	0		70	−40		85	−55		125	°C

*V_{CC} must be applied at least 100μs before proper device operation is achieved.

STATIC ELECTRICAL CHARACTERISTICS OVER RECOMMENDED OPERATING CONDITIONS (UNLESS OTHERWISE NOTED)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Input Leakage Current	I_{IN}	V_{IN} = 0V to V_{CC} max			10	μA
Output Leakage Current	I_O	V_O = 0.2 to V_{CC} max Chip Deselected			±10	μA
Output High Voltage	V_{OH}	I_{OH} = −200μA	2.4			Volts
Output Low Voltage	V_{OL}	I_{OL} = 3.2mA			0.4	Volts
Supply Current-Active	I_{CC}	Outputs Open			60	mA
Supply Current-Standby	I_{SB}*	Chip Deselected			10	μA

*Applies to KM2364S/65S Power Down Versions only.

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CAPACITANCE (Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Input Capacitance	C_{IN}	All pins except pin under test are tied to ground			7	pF
Output Capacitance	C_O				12.5	pF

Notes: Characteristics are the same for all Operating Temperature Ranges.

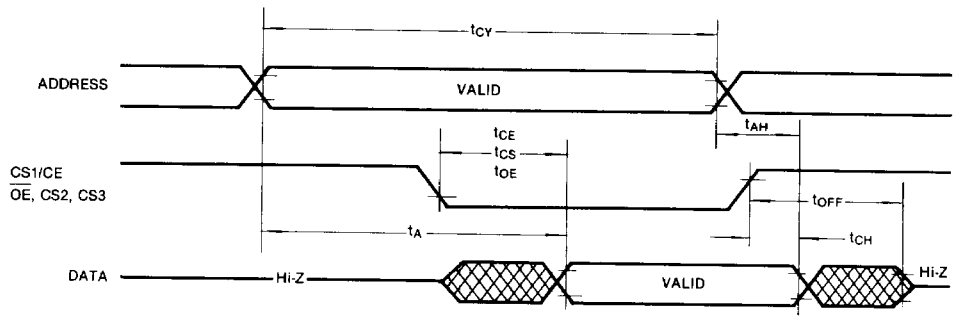
AC CHARACTERISTICS

AC CHARACTERISTICS OVER RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	2364/65-20, 2364I/65I-20, 2364HR/65HR-20		2364/65-25, 2364I/65I-25, 2364HR/65HR-25		2364/65-30, 2364I/65I-35, 2364HR/65HR-30		Units
		Min	Max	Min	Max	Min	Max	
Cycle Time	t_{CY}	200			250		300	ns
Address Access Time	t_A		300	200		250		ns
Chip Enable Access Time	t_{CE}	200			250		300	ns
Chip Select Access Time	t_{CS}		150	100		120		ns
Chip Select to Data Off (Hi Z)	t_{OFF}		150	100		120		ns
Data Hold Time from Control	t_{CH}	0			0		0	ns
Data Hold Time from Address	t_{AH}	0				0		ns

TIMING DIAGRAMS

AC WAVEFORMS

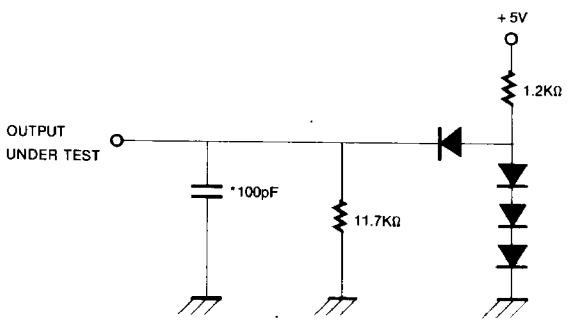


The chip select line is assumed to be active low.

AC CONDITION OF TESTS

Input Pulse Levels ..... 0.8 Volts to 2.0 Volts
Input Rise & Fall Times ..... 10 ns
Output Timing Levels ..... 0.8 Volts to 2.0 Volts

AC TEST LOAD CIRCUIT

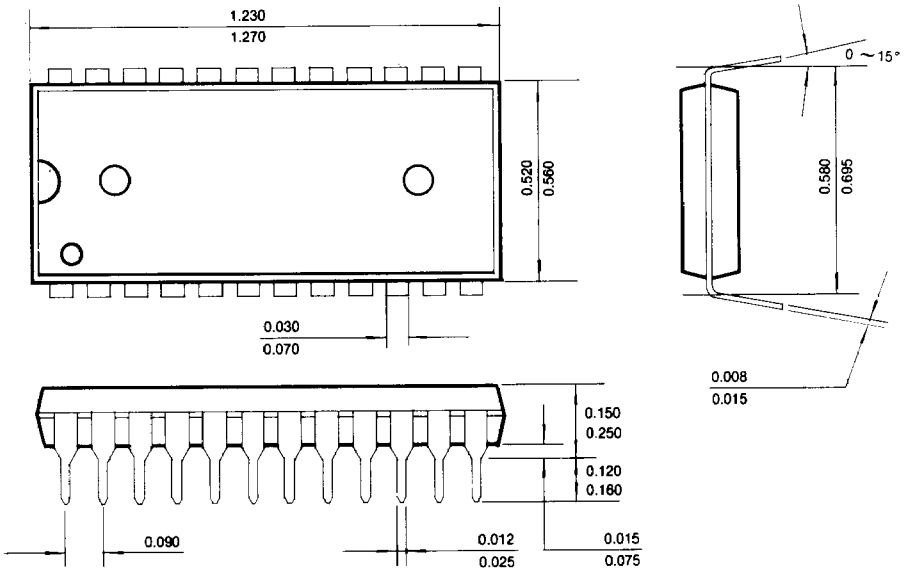


*includes jig capacitance.
All diodes 1N3064 or equivalent.

PACKAGE DIMENSIONS (Continued)

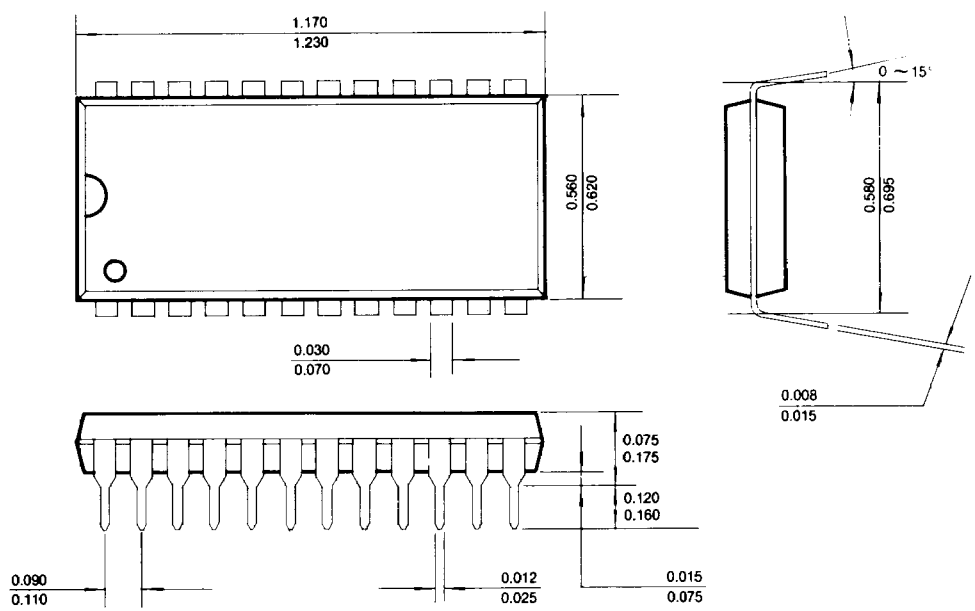
24 LEAD PLASTIC DUAL IN LINE PACKAGE

Unit: Inches



24 LEAD CERAMIC DUAL IN LINE PACKAGE

Unit: Inches



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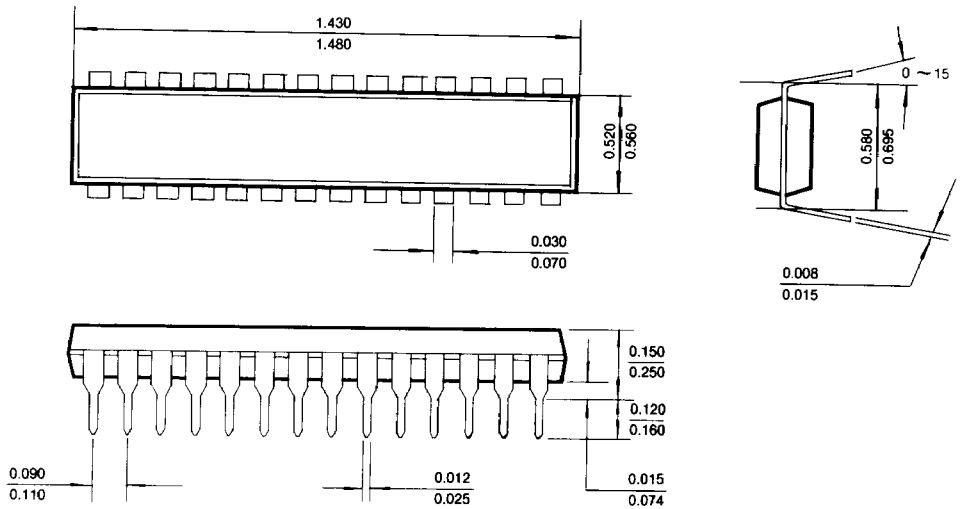
PACKAGE DIMENSIONS

28 LEAD PLASTIC DUAL IN LINE PACKAGE

Unit: Inches



28 LEAD CERAMIC DUAL IN LINE PACKAGE

Unit: Inches