6500/11, 6500/12, 6500/13 and 6500/11E
SINGLE-CHIP MICROCOMPUTER

- Enhanced 6502 CPU
  - 8-bit pipelined architecture
  - 4 new bit manipulation instructions (set memory bit, reset memory bit, branch on bit set, branch on bit reset)
  - 13 addressing modes
  - Decimal and binary arithmetic
  - True indexing capability
- Up to 3K bytes mask-programmable ROM
- 192-byte static RAM (12 mw standby power for 32 bytes)
- Up to 56 bidirectional, TTL - compatible I/O lines
- 2 16-bit programmable counter / timers with latches, each with 4 independent operating modes
- Up to four external bus modes for expansion
- Serial port
  - Full duplex, buffered UART
  - Receiver wake-up and transmitter end of transmission features
  - Synchronous shift register alternate mode (250 KHz @ 2MHz)
- 10 interrupts, 4 internal and 6 external
- 68% of instructions have execution times less than 2 μs @ 2 MHz
- 3 μm. NMOS silicon gate, depletion load technology
- Single +5V power supply
- Emulator device available (NCR 6500/11E)

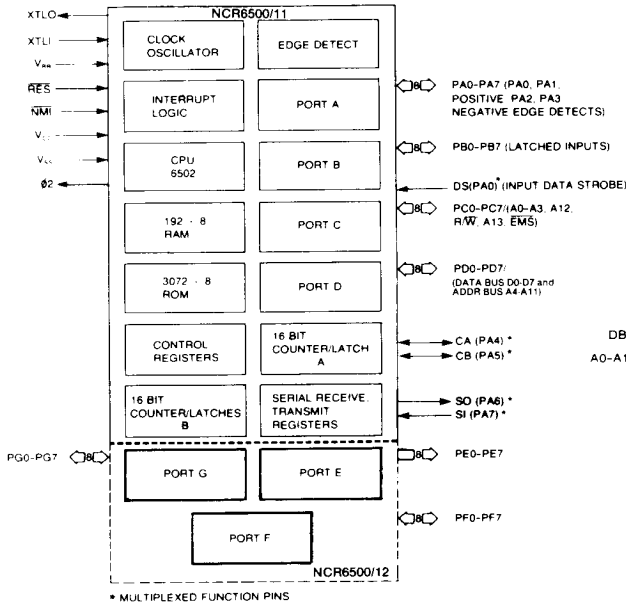
The NCR 6500/11, NCR 6500/12, NCR 6500/13 and NCR 6500/11E are each complete, high-performance 8-bit microcomputers on a single chip. All four models contain an enhanced 6502 CPU, an internal clock oscillator, 192 bytes of RAM, and versatile interface circuitry. The interface circuitry includes two 16-bit programmable timer/counters; at least 32 bidirectional I/O lines (including four edge-sensitive lines and input latching on one 8-bit port); a full-duplex serial I/O channel; 10 interrupts; and bus expandability.

The NCR 6500/11 has 3072 bytes of ROM and four 8-bit I/O ports. The NCR 6500/12 also has 3072 bytes of ROM, plus three additional 8-bit ports. The NCR 6500/13 contains 256 bytes of ROM, four 8-bit I/O ports, plus a full 16-bit address bus and 8-bit data bus to access 64K bytes of external memory. The NCR 6500/13 may be used in multichip systems as a CPU—RAM—I/O counter device that includes 256 bytes of bootstrap ROM. The NCR 6500/11E has all the features of the NCR 6500/13 except that it has no ROM and can thus be used as an emulator device for the NCR 6500/11 family of microcomputers.

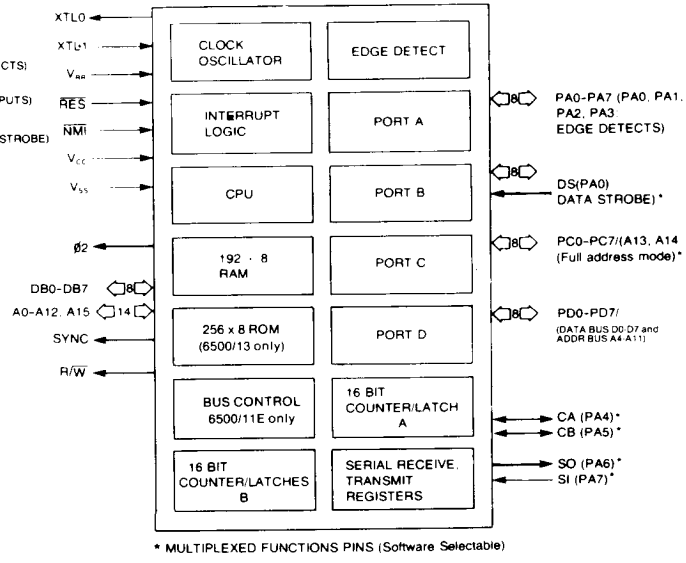
FAMILY DIFFERENCES

MODEL	ON-CHIP ROM	EXPANSION BUS	I/O LINES
NCR 6500/11	3K bytes	Access to 16K bytes via multiplexed I/O ports	32
NCR 6500/12	3K bytes	Access to 16K bytes via multiplexed I/O ports	56
NCR 6500/13	256 bytes	Access to additional 64K bytes via address bus and data bus	32
NCR 6500/11E	None	Access to additional 64K bytes via address bus and data bus	32

FUNCTIONAL BLOCK DIAGRAMS

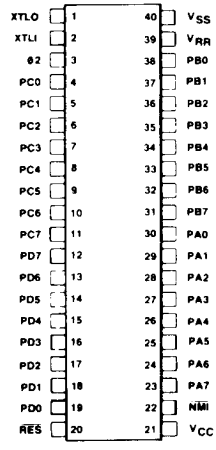


NCR 6500/11 & NCR 6500/12



NCR 6500/13 & NCR 6500/11E

PIN CONFIGURATION



NCR6500/11 Pin Out

PIN DESCRIPTIONS

PIN	DESCRIPTION
VCC	Main Power Supply +5V.
VRR	Separate power pin for RAM. In the event that VCC power is lost, this power retains the lowest 32 bytes of RAM data.
VSS	Signal and power ground (0V).
XTLI	Crystal or clock input for internal clock oscillator. Also allows input of X1 clock signal if XTLO is connected to VSS, or X2, or X4 clock if XTLO is floated.
XTLO	Crystal output from internal clock oscillator.
$\overline{RES}$	The Reset input is used to initialize the microcomputer. This signal must not transition from low to high for at least eight cycles after VCC reaches operating range and the internal oscillator has stabilized.
$\phi 2$	Clock signal output at internal frequency.
$\overline{NMI}$	A negative going edge on the Non-Maskable Interrupt signal requests that a non-maskable interrupt be generated within the CPU.
PA0-PA7 PB0-PB7 PC0-PC7 PD0-PD7	Four 8-bit ports used for either input or outputs. Each line of Ports A, B, and C consist of an active transistor to VSS and an optional pullup to VCC. In the abbreviated or multiplexed modes of operation, Port C has active pull-up transistors. Port D functions as either an 8-bit input or 8-bit output port. It has active pull-up and pull-down transistors.
SYNC	A positive going signal for the full clock cycle whenever the CPU is performing an op code fetch. Available on the NCR 6500/13 and NCR 6500/11E only.
R/$\overline{W}$	Dedicated read/write output line for NCR 6500/13 and NCR 6500/11E. Controls the direction of data transfer between the CPU and the external 64K address space. R/$\overline{W}$ is available on NCR 6500/11 and NCR 6500/12 via Port C operating in abbreviated or multiplexed mode.
A0-A12, A15	Fourteen dedicated address bus lines for NCR 6500/13 and NCR 6500/11E are used to address external memory. Note that A13 and A14 are sourced through PC6 and PC7, respectively, when in full address mode. (Some of these lines are available on the NCR 6500/11 and NCR 6500/12 via Port C operations in abbreviated mode and Port C and Port D operating in multiplexed mode.)
DB0-DB7	Eight dedicated data bus lines for NCR 6500/13 and NCR 6500/11E used to transmit data to and from external memory. These lines are also available on NCR 6500/11 and NCR 6500/12 via Port D operating in abbreviated or multiplexed mode.
PE0-PE7 PF0-PF7 PG0-PG7	Additional ports available on NCR 6500/12. Port E may be used as an output port only. Ports F and G can be configured to be inputs or outputs in any combination.

DEVICE OPERATION

CENTRAL PROCESSING UNIT (CPU)

The 6502 CPU in each of these four microcomputers executes instructions in 2 to 7 clock cycles. The automatic increment/decrement feature of the stack pointer facilitates rapid and flexible subroutines and interrupts, including context switching. Two 8-bit index registers permit pre- and post indexing of indirect addresses. (For details on the CPU operation, see NCR 6500/11 - 13 Data Sheet, Publication No. MC - 701.) The standard 6502 instruction set is available in each model; additionally, four new bit manipulation instructions have been added to improve memory utilization efficiency and performance. These bit manipulation instructions include:

- **Set Memory Bit (SMB)** - This instruction sets to "1" one bit of the 8-bit data field specified by the zero page address (memory or I/O port.) The first byte of the instruction specifies the SMB operation and which one of 8 bits is to be set. The second byte of the instruction designates the address (0-255) of the byte to be operated upon.
- **Reset Memory Bit (RMB)** - The RMB instruction is the same operation and in the same format as the SMB instruction, except a reset to "0" of the bit results.
- **Branch on Bit Set Relative (BBS)** - This instruction tests one of 8-bits designated by a 3-bit immediate field within the first byte of the instruction. The second byte is used to designate the location of the byte to be tested within the zero page address range (memory of I/O ports). The third byte of the instruction is used to specify the 8-bit relative address to which the instruction branches if the bit tested is a "1". If the bit tested is not set, the next sequential instruction is executed.
- **Branch on Bit Reset Relative (BBR)** - This instruction is the same operation and in the same format as the BBS instruction except that a branch takes place if the bit tested is a "0".

READ ONLY MEMORY (ROM)

The ROM for the NCR 6500/11 and NCR 6500/12 consists of 3072 by 8-bits (3K) of mask-programmable memory with an address space from F400 to FFFF. ROM locations FFFA through FFFF are assigned to interrupt and reset vectors. The ROM for the NCR 6500/13 consists of 256 by 8 bits of mask-progammable memory with an address space from 7F00 to 7FFF. Address locations FFFA, FFFB, FFFE and FFFF are assigned to interrupt vectors. The reset vector is assigned to memory locations FFFC and FFFD. For the NCR 6500/13, the reset vector can be optionally assigned to these locations, but is normally at memory locations 7FFE and 7FFF. The NCR 6500/11E has no ROM.

RANDOM ACCESS MEMORY (RAM)

The RAM consists of 192 by 8 bits of read/write memory with an assigned page zero address of 0040 through 00FF. A separate power pin (VRR) may be used for standby power. In the event of the loss of VCC power, the lowest 32 bytes of RAM data will be retained if standby power is supplied to the VRR pin.

CLOCK OSCILLATOR

The clock oscillator provides the basic timing signals. The reference frequency can be generated with the on board oscillator (with external crystal) or an external source can be driven into the XTLI pin. If the XTLO pin is left floating, the reference frequency is internally divided by two (divide by four is a mask option) to obtain the internal clock. The internal clock is then available as an output at the Ø2 pin. The XTLI pin may be used as an undivided clock input by connecting XTLO to VSS, in which case the internal division circuitry is bypassed and the device operates at the reference frequency.

MODE CONTROL REGISTER (MCR)

The Mode Control Register contains control bits for the multifunction I/O ports and mode select bits for Counter A and Counter B.

PARALLEL INPUT/OUTPUT PORTS

The NCR 6500/11, NCR 6500/13 and NCR 6500/11E have 32 I/O lines grouped into four 8-bit ports (PA, PB, PC and PD). The NCR 6500/12 has 56 I/O lines grouped into seven 8-bit ports (PA, PB, PC, PD, PE, PF and PG).

- **Port A (PA)** - Port A can be programmed via the Mode Control and the Serial Communications Control Register as a standard parallel 8-bit, bit-independent I/O port or as serial channel I/O lines, counter I/O lines, or an input data strobe for the Port B input latch option. In addition to their normal I/O functions, PA0 and PA1 can detect positive going edges, and PA2 and PA3 can detect negative going edges.

- **Port B (PB)** - Port B can be programmed as an 8-bit, bit-independent I/O port. It has a latched input capability which may be enabled or disabled via the Mode Control Register.
- **Port C and Port D (PC and PD)** - Port C can be programmed in one of three modes. The first mode is as an 8-bit, bit-independent I/O port. A second mode uses Port D in conjunction with the Mode Control Register as an abbreviated bus to address an additional 64K bytes of nonmultiplexed address and data space. In a third mode Port C uses Port D to effect a multiplexed bus which addresses an additional 16K bytes of multiplexed address and data space.

  Port D can be programmed as an I/O port, an 8-bit tri-state data bus, or as a multplexed bus. Mode selection for Port D is made by the Mode Control Register.

  In addition to the I/O modes of the NCR 6500/11 and NCR 6500/12, the NCR 6500/13 and NCR 6500/11E have an additional full address mode which allows emulation of the NCR 6500/11 or addressing of up to 64K bytes of memory.
- **Ports E,F,G (PE, PF, PG)** - Port E may be used for output only. PF and PG can be configured to be inputs or outputs in any combination.

SERIAL I/O CHANNEL — UART

Each microcomputer model provides a full-duplex asynchronous serial I/O channel with programmable baud rates covering all standard baud rates from 50 to 125K bits/sec, including the SMPTE 422 Standard at 38.4K bits/sec. Character lengths of 5 to 8 bits, with or without parity, are programmable. A full complement of flags provides for Receiver Wake-Up; Receiver Buffer Full; Receiver Error Conditions detecting Framing, Parity and Overrun errors; Transmitter End of Transmission and Transmitter Buffer Empty. In addition, a synchronous shift register mode to 250 KHz @ 2 MHz is available.

WAKE-UP FEATURE

In a multidistributed microcomputer application, a destination address is usually included at the beginning of the message. The wake-up feature allows non-selected CPU's to ignore the remainder of the message until the beginning of the next message by setting the wake-up bit.

COUNTER/LATCH LOGIC

Each microcomputer model contains two 16-bit counters and three 16-bit latches associated with the counters. Counter A has one 16-bit latch and Counter B has two 16-bit latches. Each counter can be indepently programmed to operate in one of four modes:

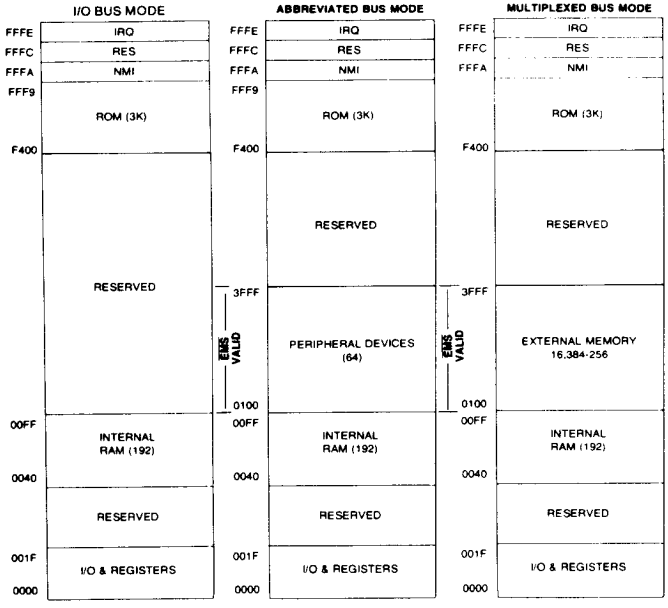
Counter A	Counter B
— Pulse Width Measurement	— Retriggerable Interval Counter
— Pulse Generation	— Asymetrical Pulse Generation
— Interval Timer	— Interval Timer
— Event Counter	— Event Counter

INTERRUPT FLAG REGISTER (IFR) AND INTERRUPT ENABLE REGISTER (IER)

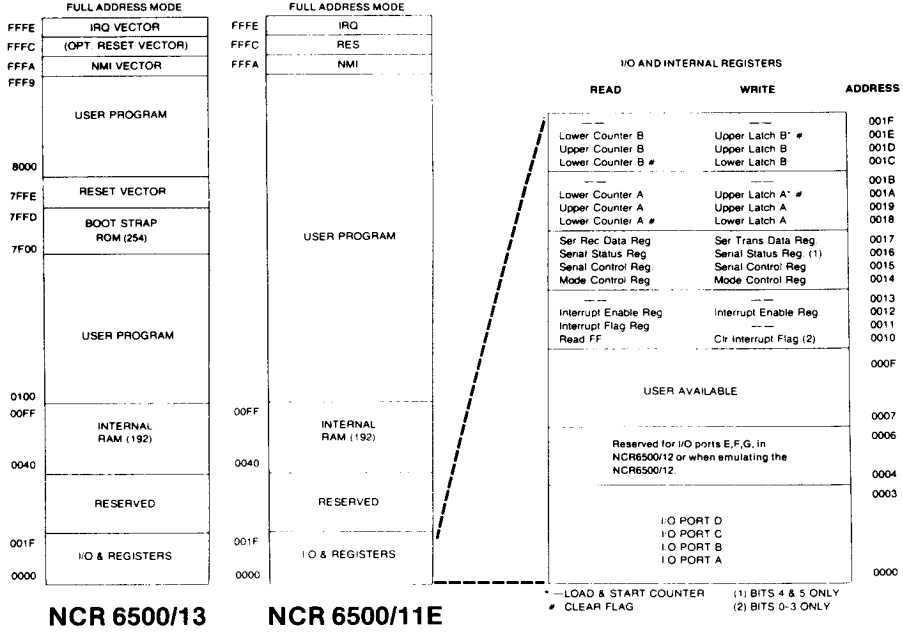
Each microcomputer model includes an IFR and IER which flags and controls I/O and counter status. Each model has ten interrupts: four edge-sensitive lines, two counter underflows, a serial data received, a serial data transmitted, a non-maskable interrupt, and a reset interrupt.

SYSTEM MEMORY MAPS

NCR 6500/11 and NCR 6500/12

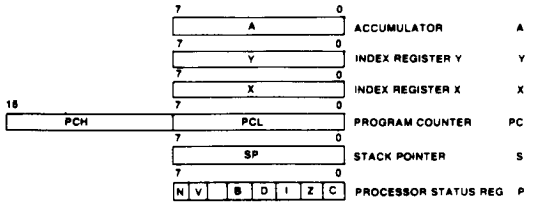


For additional details on the NCR 6500/13 and /11E, see Pub. No. MC-701.

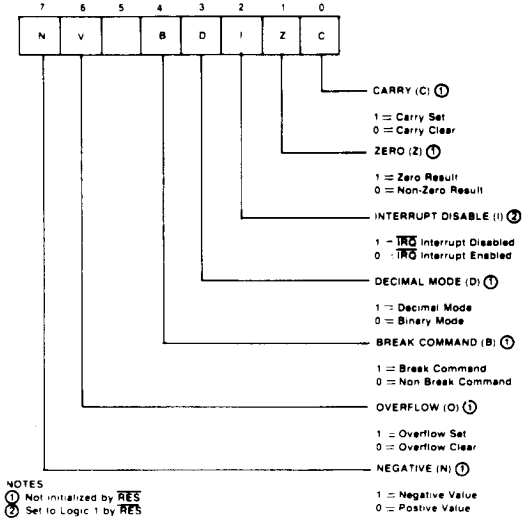


NCR 6500/13 **NCR 6500/11E**

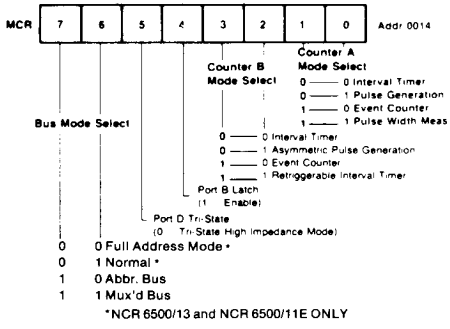
KEY REGISTER SUMMARY



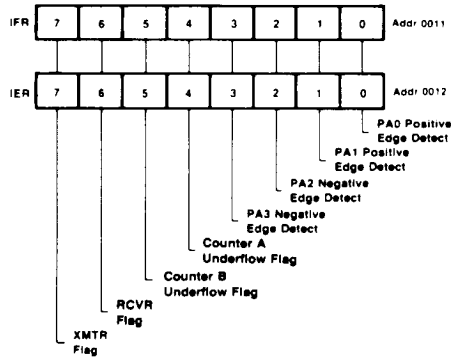
CPU Registers



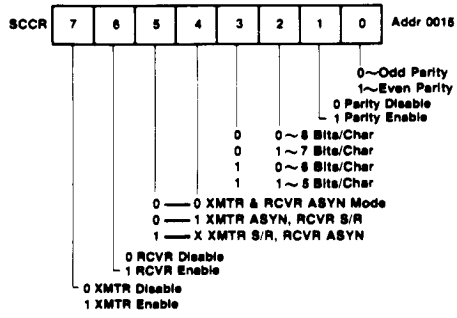
Processor Status Register



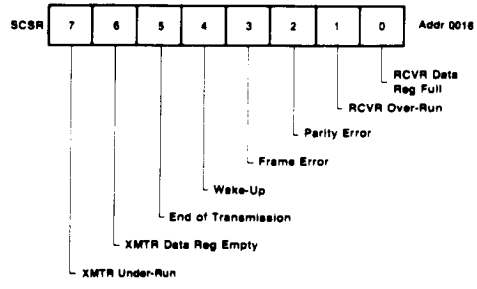
Mode Control Register



Interrupt Enable and Flag Registers



Serial Communications Control Register



Serial Communications Status Register

ELECTRICAL SPECIFICATIONS

Maximum Ratings

RATING	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC} & V_{RR}	0.3 to +7.0	Vdc
Input Voltage	V_{in}	0.3 to +7.0	Vdc
Operating Temperature Range, Commercial	T	0 to +70	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this circuit.

D.C. Characteristics (V_{CC} = 5V ±5%, V_{SS} = 0)

CHARACTERISTIC	SYMBOL	MIN	TYP	MAX	UNIT
Power Dissipation (Outputs High) Commercial @ 25 C	P_D	—		1200	mW
RAM Standby Voltage (Retention Mode)	V_{RR}	3.0	—	V_{CC}	Vdc
RAM Standby Current (Retention Mode) Commercial @ 25 C	I_{RR}	—	4	—	mAdc
Input High Voltage Except XTLI	V_{IH}	+2.0	—	V_{CC}	Vdc
Input High Voltage (XTLI)	V_{IH}	+4.0	—	V_{CC}	Vdc
Input Low Voltage	V_{IL}	-0.3	—	+0.8	Vdc
Input Leakage Current (RES, NMI) V_{in} = 0 to 5.0 Vdc	I_{IN}	—	—	±10	μAdc
Input Low Current PA, PB, PC, PF, and PG (V_{IL} = 0.4 Vdc)	I_{IL}	—	1.0	1.6	mAdc
Output High Voltage Except XTLO (I_{Load} = -100 μAdc)	V_{OH}	+2.4	—	V_{CC}	Vdc
Output Low Voltage (I_{Load} = 1.6 mAdc)	V_{OL}	—	—	+0.4	Vdc
Darlington Current Drive, PE (V_o = 1.5 Vdc)	I_{OH}	1.0	—	—	mAdc
Output Low Voltage, PE (I_{Load} = 1.6 mAdc sink)	V_{OL}	—	—	+0.4	Vdc
Input Capacitance (V_{in} = 0, T_A = 25 C, f = 1.0 MHz)	C_{in}				pF
PA, PB, PC, PD, PF, and PG		—	—	10	
XTLI, XTLO		—	—	50	
I/O Port Pull-Up Resistance PA0-PA7, PB0-PB7, PC0-PC7, PF0-PF7 & PG0-PG7	R_L	3.0	6.0	11.5	KΩ

NOTE: Negative sign indicates outward current flow, positive indicates inward flow.

AC CHARACTERISTICS (V_{CC} = 5V ± 5% V_{SS} = 0)

PARAMETER	SYMBOL	1 MHz MIN	1 MHz MAX	2 MHz MIN	2 MHz MAX	UNIT
XTLI Input Clock Cycle Time	T_{cyc}	1.0	10.0	0.500	10.0	μ sec
Internal Write to Peripheral Data Valid (TTL)	T_{PDW}	1.0		0.5		μ sec
Peripheral Data Setup Time	T_{PDSU}	500		500		nsec
Count and Edge Detect Pulse Width	T_{PW}	1.0		0.5		μ sec

NCR

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