20.2 External signal description

There are no ICS signals that connect off chip.

20.3 Register definition

ICS memory map

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
4006_4000	ICS Control Register 1 (ICS_C1)	8	R/W	04h	20.3.1/292
4006_4001	ICS Control Register 2 (ICS_C2)	8	R/W	20h	20.3.2/293
4006_4002	ICS Control Register 3 (ICS_C3)	8	R/W	Undefined	20.3.3/294
4006_4003	ICS Control Register 4 (ICS_C4)	8	R/W	See section	20.3.4/295
4006_4004	ICS Status Register (ICS_S)	8	R	10h	20.3.5/296

20.3.1 ICS Control Register 1 (ICS_C1)

Address: 4006_4000h base + 0h offset = 4006_4000h

Bit	7	6	5	4	3	2	1	0
Read Write	CLKS		RDIV			IREFS	IRCLKEN	IREFSTEN
Reset	0	0	0	0	0	1	0	0

ICS_C1 field descriptions

Field	Description
7–6 CLKS	Clock Source Select Selects the clock source that controls the bus frequency. The actual bus frequency depends on the value of ICS_C2[BDIV]. 00 Output of FLL is selected. 01 Internal reference clock is selected. 10 External reference clock is selected. 11 Reserved, defaults to 00.
5–3 RDIV	Reference Divider Changing RDIV will cause the change of reference clock frequency of FLL, RDIV is not allowed to be changed in FEE/FBE mode. Selects the amount to divide down the FLL reference clock selected by the IREFS bits. Resulting frequency must be in the range 31.25 kHz to 39.0625 kHz.

Table continues on the next page...