Simulated timing (ns)：

clock cycle = 5.5(ns)

```
`timescale 1 ns/10 ps
`define H_CYCLE 2.75
`define CYCLE 5.5
```

```
ncsim> source /usr/cad/cadence/INCISIV/cur/tools/inca/files/ncsimrc
ncsim> run
Your lw instruction is correct!
Your lw instruction is correct!
Your add instruction is correct!
Your sub instruction is correct!
Your and instruction is correct!
Your beq instruction is correct!
Your or instruction is correct!
Your slt instruction is correct!
Your sw instruction is correct!
Your jump instruction is correct!
Your jal instruction is correct!
Your jr instruction is correct!
Your beq instruction is correct!

-------------------------------------------------------

  Congratulations!! Your design has passed all the test!!

-------------------------------------------------------
```

Area(um^2) ：67249.289711

```
Combinational area:                34224.676429
Buf/Inv area:                       5175.372520
Noncombinational area:             33024.613281
Macro/Black Box area:                  0.000000
Net Interconnect area:      undefined  (No wire load specified)

Total cell area:                   67249.289711
Total area:                 undefined
```

Cost(A*T)：369871.093411(um^2*ns)