DSD Final Project Scores

1. Baseline

(1) Area: (um^2)

截圖:

```
Number of ports:                         4014
Number of nets:                         23466
Number of cells:                        19744
Number of combinational cells:          15078
Number of sequential cells:              4647
Number of macros/black boxes:               0
Number of buf/inv:                       2829
Number of references:                       7

Combinational area:            144747.482378
Buf/Inv area:                   22030.554472
Noncombinational area:         145640.310276
Macro/Black Box area:               0.000000
Net Interconnect area:        2797727.592407

Total cell area:               290387.792654
Total area:                   3088115.385061
```

290388 (um^2)

(2) Total Simulation Time (hasHazard testbench): (ns)

截圖:

```
FSDB Dumper for IUS, Release Verdi_N-2017.12, Linux, 11/12/2017
(C) 1996 - 2017 by Synopsys, Inc.
*Verdi* FSDB WARNING: The FSDB file already exists. Overwriting the FSDB file
 may crash the programs that are using this file.
*Verdi* : Create FSDB file 'Final.fsdb'
*Verdi* : Begin traversing the scope (Final_tb), layer (0).
*Verdi* : Enable +mda dumping.
*Verdi* : End of traversing.
-------------------------- Simulation FINISH !!--------------------------
==============================================================================

 \(^o^)/ CONGRATULATIONS!!  The simulation result is PASS!!!

==============================================================================
Simulation complete via $finish(1) at time 8741400 PS + 0
```

8741 (ns)

(3) Area*Total Simulation Time: (um^2 * ns)

2.538 * 10^9 (um^2 x ns)

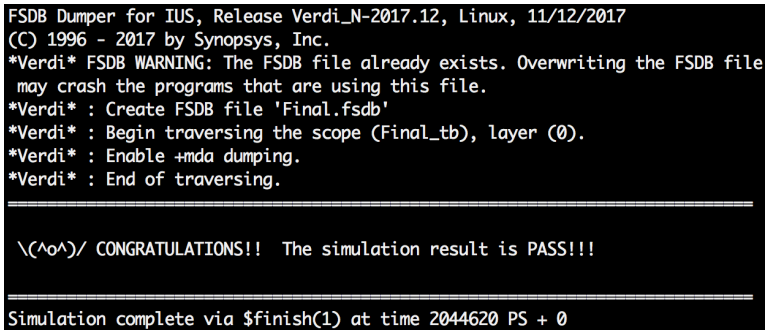
(4) Clock cycle for post-syn simulation: (ns)

4.08 (ns)

2. BrPred

(1) Total execution cycles of I_mem_BrPred:

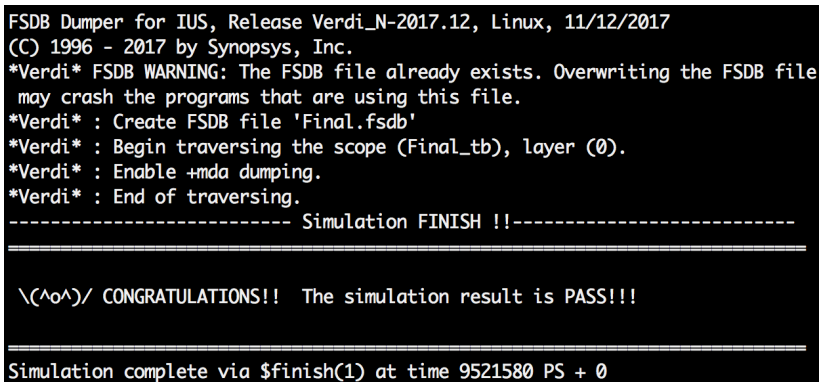
截圖:



2045 ns / 4.44 = **460 (cycles)**

(2) Total execution cycles of I_mem_hasHazard:

截圖:



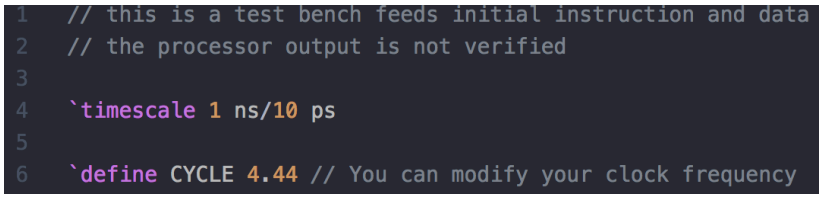
9522 / 4.44 = **2145 (cycles)**

(3) Synthesis area of BPU(Total area of BrPred minus baseline design, two design clock cycle need to be same): (um^2)

12410 (um^2)

(4) Clock cycle for post-syn simulation: (ns)

截圖:



```
1  // this is a test bench feeds initial instruction and data
2  // the processor output is not verified
3
4  `timescale 1 ns/10 ps
5
6  `define CYCLE 4.44 // You can modify your clock frequency
```

4.44 (ns)

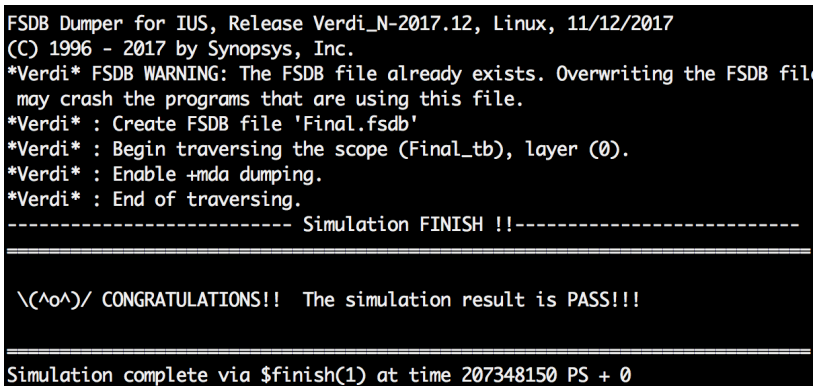
3. L2Cache

(1) Avg. memory access time: (ns)

6.46 (ns)

(2) Total execution time: (ns)

截圖:



207348 / 6.1 = **33991 (cycles)**

(3) Clock cycle for post-syn simulation: (ns)

6.1 (ns)

4. MultDiv

(1) Total synthesis area: (um^2)

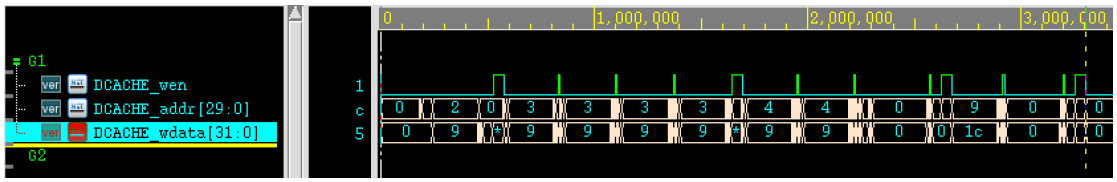
截圖:

```
Number of ports:                          5070
Number of nets:                          26883
Number of cells:                         21851
Number of combinational cells:           16405
Number of sequential cells:               5418
Number of macros/black boxes:                0
Number of buf/inv:                        3455
Number of references:                        9

Combinational area:                164849.790415
Buf/Inv area:                       24690.380075
Noncombinational area:             161904.796623
Macro/Black Box area:                   0.000000
Net Interconnect area:             3050055.562897

Total cell area:                   326754.587038
Total area:                        3376810.149935
```

326755 (um^2)

(2) Total execution time: (ns)

截圖:



3300 (ns)

(3) Minimum clock period: (ns)

截圖:

```
1  // this is a test bench feeds initial instruction and data
2  // the processor output is not verified
3
4  `timescale 1 ns/10 ps
5
6  `define CYCLE 6.1 // You can modify your clock frequency
```

6.1 (ns)