1.(3)

The output went wrong when I set the CYCLE to 15.0. Input 00 00 and FF 01 right after will arise the worst case delay. So the sum of delay of the critical path is 16 ns.

This path started from the input of the least significant full adder, went all the way from the path formed by the carries to the most significant full adder, and finally to the output of the most significant full adder.

2.(3)

The output went wrong when I set the CYCLE to 6.0. So the sum of delay of the critical path is 7 ns.

The MUX of the first level should delay at most 3 ns. When the MUX of the second level receive the input from the first level, it should delay at most 2 ns. When the MUX of the third level receive the input from the second level, it should delay at most 2 ns. Therefore, the shifter should delay at most 7 ns.

3.(3)

The sum of delay of the critical path is 18.5 ns. Which is the worst case delay from the plus 2.5 ns.

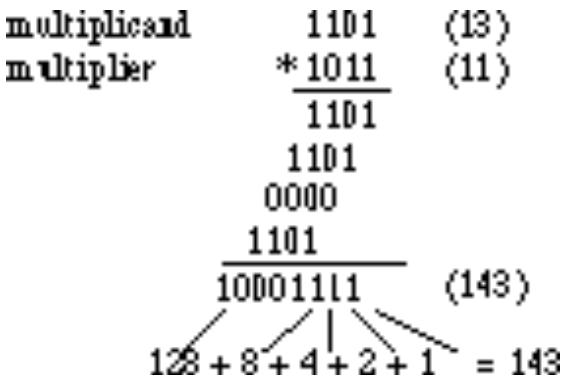
3.(4)

The main cause of delay of the adder is the carry. The full adder of the MSB has to wait for the the other full adder to operate completely to get the carry. And this may cause a lot of time in some cases.

A solution to this is to build a carry computation circuit aside from the full adders. This carry computation circuit can compute the carries in a short time, and feed the carries into the full adders simultaneously. This can lead to a considerable reduction of worst case delay time of the adder, and also minimize that of the add-shifter unit.

3.(5)

The process of binary multiplication can be illustrated with an example. In this case, the multiplicand is 11012 and the multiplier is 10112 :



Each bit of the multiplier is multiplied against the multiplicand, the product is aligned according to the position of the bit within the multiplier, and the resulting products are then summed to form the final result.

We can connect eight registers at the input [7:0]y to store the value temporarily. We can perform either adding or shifting to the result generated by the add-shifter unit in the previous clock cycle. By using a finite state machine controller, we can perform the calculation described above and equally, do multiplication with the circuit.