Delay incrementing PC the first clock cycle out of reset.
This is to allow memory location $0000 to be read. Otherwise,
PC would be incremented to $0001 before instruction at $0000
is loaded into IR.

Program Counter - PC

U8 — MC74HC74AN
- 1 RESET1
- 2 DATA1
- 3 CLOCK1
- 4 SET1
- 5 Q1
- 6 Q1#
- 7 GND
- 14 VCC
- 13 RESET2
- 12 DATA2
- 11 CLOCK2
- 10 SET2
- 9 Q2
- 8 Q2#

EXT_RST*
EXT_CLK

U9 — SN74HC32N
- 1 1A
- 2 1B
- 3 1Y
- 4 2A
- 5 2B
- 6 2Y
- 7 GND
- 14 VCC
- 13 4B
- 12 4A
- 11 4Y
- 10 3B
- 9 3A
- 8 3Y

U10 — SN74HC00N
- 1 1A
- 2 1B
- 3 1Y
- 4 2A
- 5 2B
- 6 2Y
- 7 GND
- 14 VCC
- 13 4B
- 12 4A
- 11 4Y
- 10 3B
- 9 3A
- 8 3Y

RST*
CLK
CLK*

U6 — SN74HC161D (PC Bits 4 - 0 (lsb))
- 1 CLR#
- 2 CLK
- 3 A (PC_IN0)
- 4 B (PC_IN1)
- 5 C (PC_IN2)
- 6 D (PC_IN3)
- 7 ENP
- 8 GND
- 16 VCC
- 15 RCO
- 14 QA (PC_ADDR_OUT0)
- 13 QB (PC_ADDR_OUT1)
- 12 QC (PC_ADDR_OUT2)
- 11 QD (PC_ADDR_OUT3)
- 10 ENT
- 9 LOAD#

U7 — SN74HC161D
- 1 CLR#
- 2 CLK
- 3 A (PC_IN4)
- 4 B (PC_IN5)
- 5 C (PC_IN6)
- 6 D (PC_IN7)
- 7 ENP
- 8 GND
- 16 VCC
- 15 RCO
- 14 QA (PC_ADDR_OUT4)
- 13 QB (PC_ADDR_OUT5)
- 12 QC (PC_ADDR_OUT6)
- 11 QD (PC_ADDR_OUT7)
- 10 ENT
- 9 LOAD#

U3 — SN74HC161D
- 1 CLR#
- 2 CLK
- 3 A (PC_IN8)
- 4 B (PC_IN9)
- 5 C (PC_IN10)
- 6 D (PC_IN11)
- 7 ENP
- 8 GND
- 16 VCC
- 15 RCO
- 14 QA (PC_ADDR_OUT8)
- 13 QB (PC_ADDR_OUT9)
- 12 QC (PC_ADDR_OUT10)
- 11 QD (PC_ADDR_OUT11)
- 10 ENT
- 9 LOAD#

U4 — SN74HC161D (PC Bits 15 - 12 (msb))
- 1 CLR#
- 2 CLK
- 3 A (PC_IN12)
- 4 B (PC_IN13)
- 5 C (PC_IN14)
- 6 D (PC_IN15)
- 7 ENP
- 8 GND
- 16 VCC
- 15 RCO
- 14 QA (PC_ADDR_OUT12)
- 13 QB (PC_ADDR_OUT13)
- 12 QC (PC_ADDR_OUT14)
- 11 QD (PC_ADDR_OUT15)
- 10 ENT
- 9 LOAD#

PC_INC_EN
PC_LOAD

PC_IN[0:15]
PC_ADDR_OUT[0:15]

+5V
GND

Schematic		Homemade CPU	Create at 2025-11-05
			Update at 2025-11-07
Board			Page Reset-Pgm Counter
Drawn		Homemade CPU	
Reviewed			

Version	Size	Page 2 Total 4
V1.0	A4	Andy4495

EasyEDA