19-5724; Rev 0; 12/10

EVALUATION KIT AVAILABLE

4-Channel, High-Voltage, Liquid Lens Driver for OIS/AF Systems

MAX14574

General Description

The MAX14574 high-voltage liquid lens driver features four high-voltage PWM outputs controlled through an I²C interface. The device uses an inductive-based boost converter and integrated H-bridges to provide a multiple-output optical image stabilization/auto focus (OIS/AF) lens-driver solution in a small overall footprint.

The device features a 10-bit monotonic DAC with high-voltage outputs controlled by a 2-wire I²C interface to set the RMS output value. The high-voltage outputs can deliver up to +70V_{RMS} into a 75pF liquid lens load at 5kHz.

The device also features two power-saving modes (shutdown mode and sleep mode) to minimize power consumption when the device is inactive. Shutdown mode places the device in a shutdown state that resets all registers and disables the I²C input buffers to reduce current below 100nA. In sleep mode, register data remains intact, and, if no activity is detected on the I²C interface, current consumption is less than 3µA.

The device operates over the +2.7V to +5.5V supply voltage range, ideal for portable applications using lithium-ion (Li+) battery sources. The device is specified over the -40°C to +85°C extended temperature range, and is available in a small (1.6mm x 2.6mm x 0.5mm pitch), 15-bump wafer-level package (WLP).

Applications

OIS/AF Cellular Phone Camera Modules

Ordering Information

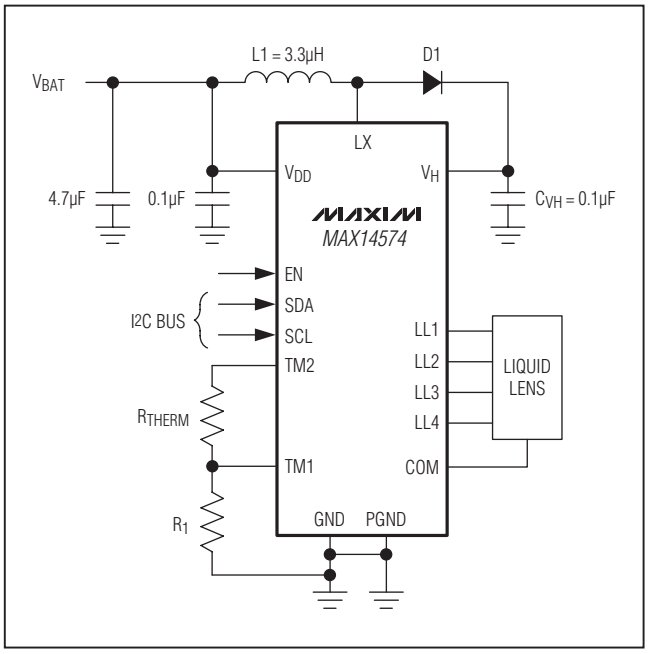
PART	TEMP RANGE	BUMP-PACKAGE
MAX14574EWL+	-40°C to +85°C	15 WLP

+Denotes a lead(Pb)-free/RoHS-compliant package.

Features

- Inductor-Based Boost Topology
- +2.7V to +5.5V Input Voltage Range
- +70V_{RMS} Maximum Output (C_{LOAD} = 75pF, 5kHz)
- I²C-Compatible Interface for Setting Output Voltage
- 10-Bit (typ) Output V_{RMS} Voltage Resolution
- Guaranteed Monotonic Output
- Low 100nA Shutdown Current (Shutdown Mode)
- Space-Saving 15-Bump WLP (1.6mm x 2.6mm x 0.5mm Pitch)

Typical Application Circuit



4-Channel, High-Voltage, Liquid Lens Driver for OIS/AF Systems

ABSOLUTE MAXIMUM RATINGS

(All Voltages Referenced to GND)

V_{DD} ..... -0.3V to +5.5V
LX ..... -0.3V to +85V
V_H ..... -0.3V to +75V
LL1–LL4, COM ..... -0.3V to the lesser of (75V, V_H + 0.3V)
SDA, SCL, EN, TM1 ..... -0.3V to +5.5V
TM2 ..... -0.3V to (V_{DD} + 0.3V)

Continuous Power Dissipation (T_A = +70°C):
WLP (derate 19.2mW/°C above +70°C) 1536mW
Operating Temperature Range ..... -40°C to +85°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Soldering Temperature (reflow) ..... +260°C

PACKAGE THERMAL CHARACTERISTICS (Note 1)

WLP
Junction-to-Ambient Thermal Resistance (θ_{JA}) ..... 52°C/W
Junction-to-Case Thermal Resistance (θ_{JC}) ..... 12°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +2.7V to +5.5V, total C_{LL} = 75pF, C_{VH} = 100nF, inductor = 3.3µH, maximum V_{RMS} difference between any electrodes = +27V_{RMS}, maximum V_{RMS} difference between adjacent electrodes = 19V_{RMS}, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{DD} = 3.3V and T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage	V_{DD}			2.7		5.5	V
Input Supply Current	I_{DD}	Peak output voltage register (V_[9:0]) = 0x3FF, TS_EXT = 0				5	mA
Shutdown Supply Current	I_{SHDN}	EN = low	T_A = +25°C		25	100	nA
			T_A = -40°C to +85°C			300	
Sleep Supply Current	I_{SLEEP}	SCL = SDA = high, SM = 0	V_{EN} = V_{DD} = +2.8V			3	µA
			V_{EN} = +1.8V, V_{DD} = +4.2V		3	6.5	
Shutdown-Inductor Supply Current	I_{LX_SHDN}					1	µA
POR Threshold	V_{TH_POR}					2.6	V
POR Threshold Hysteresis	$V_{TH\_POR\_HYS}$				150		mV
Thermal Shutdown					+155		°C
Thermal Shutdown Hysteresis					20		°C
LIQUID LENS OUTPUTS (LL_, COM)							
Peak-to-Peak Output Voltage	V_{PK-PK}	Figure 1 (Note 3)		137.5	141	144.5	V
Output RMS Voltage (Note 4)	V_{RMS}	V_[9:0] = 0x000		23.8	24.4	25	V_{RMS}
		V_[9:0] = 0x3FF		68	69.7	71.5	
Max RMS Output Mismatch	V_{MATCH}	V_[9:0] = 0x000		-1		+1	%
Max DC Output Voltage	V_{OFFS}			-500		+500	mV
Resolution	N	(Note 5)			10		Bits
LSB	LSB			0	44	80	mV_{RMS}
Output RMS Voltage Error				-2.5		+2.5	%

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +2.7V to +5.5V, total C_{LL} = 75pF, C_{VH} = 100nF, inductor = 3.3µH, maximum V_{RMS} difference between any electrodes = +27V_{RMS}, maximum V_{RMS} difference between adjacent electrodes = 19V_{RMS}, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{DD} = 3.3V and T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Shutdown Pulldown Resistor	$R_{SHPD\_LL\_}$				50	Ω
COM/LL_ High-Side Switch On-Resistance	$R_{ONHS\_LL\_}$				50	Ω
COM/LL_ Low-Side Switch On-Resistance	$R_{ONLS\_LL\_}$				50	Ω
COM/LL_ High-Side Switch Off-Leakage	$I_{LKHS\_LL\_}$		-1		+1	µA
COM/LL_ Low-Side Switch Off-Leakage	$I_{LKLS\_LL\_}$		-1		+1	µA
Liquid Lens Switching Frequency	f_{LL_SWTICH}		4.5	5.0	5.5	kHz
Edges Time	t_{EDGE}	Figure 1	0.15	0.5	2.5	µs
Startup Time	t_{STU}	FSTU[1:0] = 10			5	ms
Settling Time	t_{SET}			0.1		ms
Shutdown Time	t_{SHDN}			0.1		ms
BOOST CONVERTER						
Peak Output Voltage	V_{PEAK}	(Note 3)	68.7	70.5	72.3	V
V_H Output Ripple	V_{RIPPLE}			±1		%
Switch On-Resistance	R_{LX}	I_{SINK} = 250mA		1.1	2.6	Ω
LX Leakage Current	I_{LEAK_LX}	V_{LX} = 70V	-1		+1	µA
TEMPERATURE SENSOR, INTERNAL (Note 6)						
Resolution	N			8		Bits
LSB	LSB			1.6		°C
Offset	$T25_{OFF}$	T_J = +25°C	-18		+18	LSB
Gain Error	$G25_{ERR}$	T_J = -40°C, T_J = +85°C (Note 7)	-6		+6	LSB
Integral Nonlinearity	INL		-7		+7	LSB
Differential Nonlinearity	DNL		-2		+2	LSB
TEMPERATURE SENSOR, EXTERNAL						
TM_ Output Voltage		I_{LOAD} = 10µA	0.9	1	1.1	V
TM_ Current Load					100	µA
Resolution	N			8		Bits
LSB	LSB			3.9		mV
Offset	V_{TOFF}		-10		+10	LSB
Gain Error	G_{TERR}		-6		+6	LSB
Integral Nonlinearity	INL		-7		+7	LSB
Differential Nonlinearity	DNL		-2		+2	LSB
CONTROL INPUTS (EN)						
Input Logic-High Voltage	V_{IH}		1.4			V
Input Logic-Low Voltage	V_{IL}				0.4	V

4-Channel, High-Voltage, Liquid Lens Driver for OIS/AF Systems

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +2.7V to +5.5V, total C_{LL} = 75pF, C_{VH} = 100nF, inductor = 3.3µH, maximum V_{RMS} difference between any electrodes = +27V_{RMS}, maximum V_{RMS} difference between adjacent electrodes = 19V_{RMS}, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{DD} = 3.3V and T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Leakage Current	I_{IH}		-1		+1	µA
Input Low Leakage Current	I_{IL}		-1		+1	µA
CONTROL INPUTS (SDA, SCL)						
Input Logic-High Voltage	V_{IH}		1.4			V
Input Logic-Low Voltage	V_{IL}				0.4	V
Input Logic Hysteresis	V_{IHYS}			100		mV
Output Logic-Low Voltage	V_{OL}	I_{SINK} = 20mA			0.4	V
Input Low Leakage Current	I_{IL}	EN = V_{CC}	-6		+6	µA
		EN = GND	-1		+1	
Input High Leakage Current	I_{IH}	EN = V_{CC}	-1		+1	µA
Input Capacitance	C_{IN}			10		pF
I²C INTERFACE (Figure 3)						
Serial-Clock Frequency	f_{SCL}				1000	kHz
Bus Free Time Between START and STOP Condition	t_{BUF}		0.5			µs
Hold Time for Repeated START Condition	$t_{HD:STA}$		0.26			µs
Low Period for SCL Clock	t_{LOW}		0.5			µs
High Period for SCL Clock	t_{HIGH}		0.26			µs
Setup Time for Repeated START Condition	$t_{SU:STA}$		0.26			µs
Data Hold Time	$t_{HD:DAT}$		0			µs
Data Setup Time	$t_{SU:DAT}$		50			ns
Rise Time of Both SDA and SCL Signals	t_R				120	ns
Fall Time of Both SDA and SCL Signals	t_F				120	ns
Setup Time for STOP Condition	$t_{SU:STO}$		0.26			µs
Capacitive Load for Each Bus Line	C_B				550	pF

Note 2: All units are tested at T_A = +25°C. Specification limits over temperature are guaranteed by design.
Note 3: V_{PEAK} is the average peak voltage of the output waveform ($V_{LL\_}$ - V_{COM}).
Note 4: Output RMS voltage is defined as the RMS voltage of the output waveform ($V_{LL\_}$ - V_{COM}).
Note 5: Output RMS voltage is configured for each output with 10-bit resolution by internally setting the duty cycle of the output waveform ($V_{LL\_}$ - V_{COM}) to have V_{RMS} = 24.4V_{RMS} + 44mV_{RMS} x code, where code = [0 to 1023].
Note 6: Internal temperature sensor senses silicon temperature T_J, that is T_J = T_A + θ_{JA} x PWR, where T_A is ambient temperature, PWR is the power dissipated inside the device, and θ_{JA} is the junction-to-ambient thermal resistance. In typical conditions with no power delivered to the liquid lens, T_J - T_A < +1°C. Gain error is defined as the error at T_J = -40°C (or T_J = +85°C) minus the offset error measured for T_J = +25°C.
Note 7: Gain error guaranteed by design.

Timing Diagram

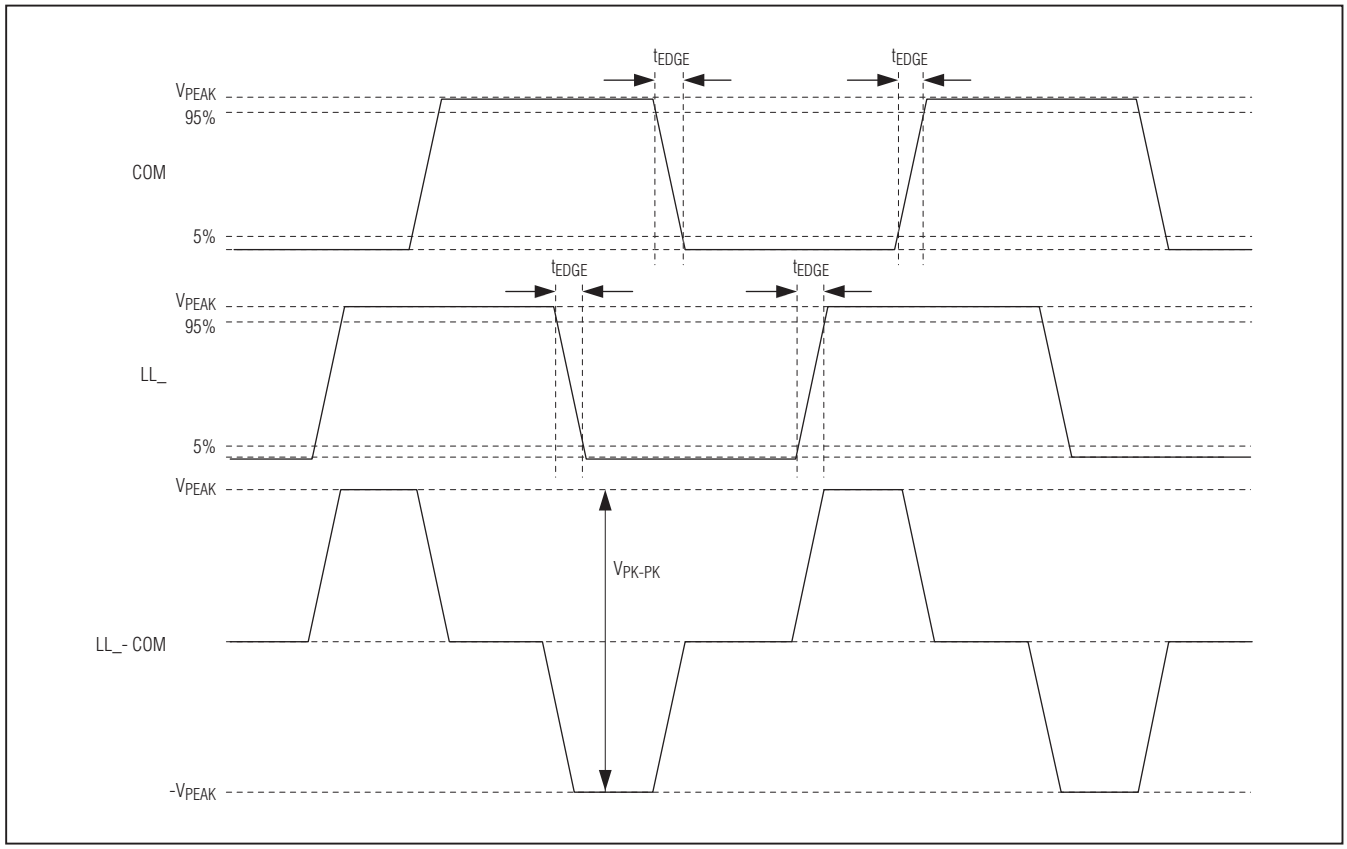


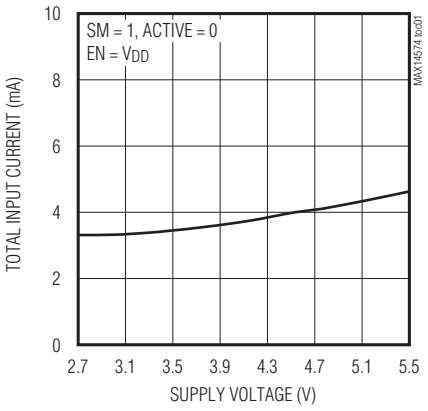
Figure 1. Output Waveforms Timing Details

4-Channel, High-Voltage, Liquid Lens Driver for OIS/AF Systems

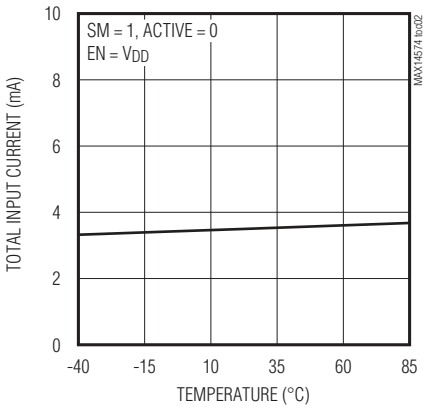
Typical Operating Characteristics

(V_{DD} = +3.6V, T_A = +25°C, inductor 3.3µH, I_{SAT} = 0.7A, C_{VH} = 100nF, IL[1:0] = 01, FSTU[1:0] = 10, see Figure 2 where C_{LENS} = 75pF, R_{IJ} = 150kΩ, unless otherwise noted.)

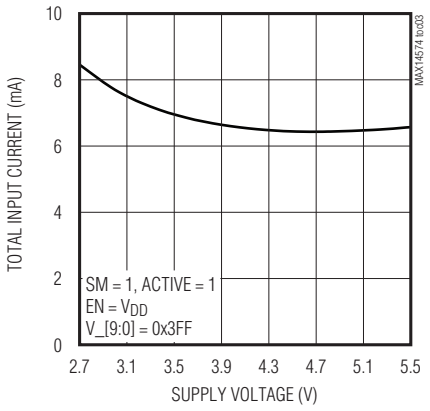
TOTAL INPUT CURRENT (I_{DD} + I_{LX}) vs. SUPPLY VOLTAGE



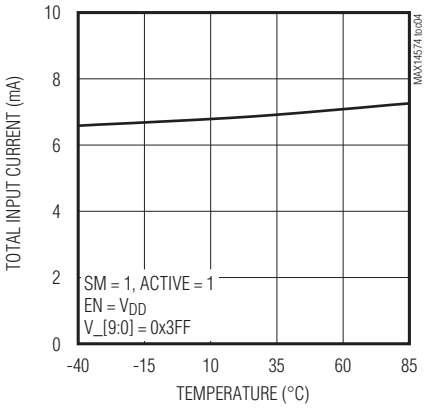
TOTAL INPUT CURRENT (I_{DD} + I_{LX}) vs. TEMPERATURE



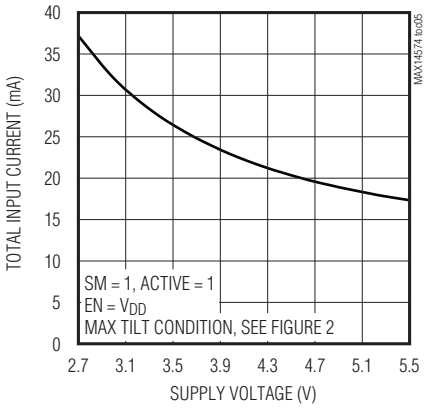
TOTAL INPUT CURRENT (I_{DD} + I_{LX}) vs. SUPPLY VOLTAGE



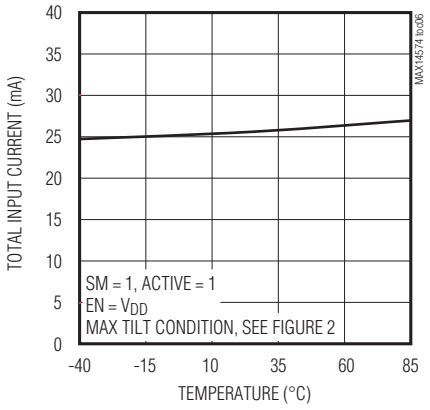
TOTAL INPUT CURRENT (I_{DD} + I_{LX}) vs. TEMPERATURE



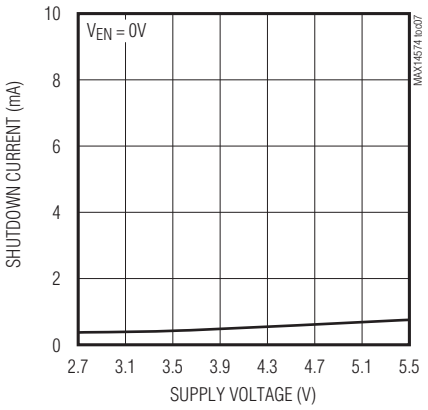
TOTAL INPUT CURRENT (I_{DD} + I_{LX}) vs. SUPPLY VOLTAGE



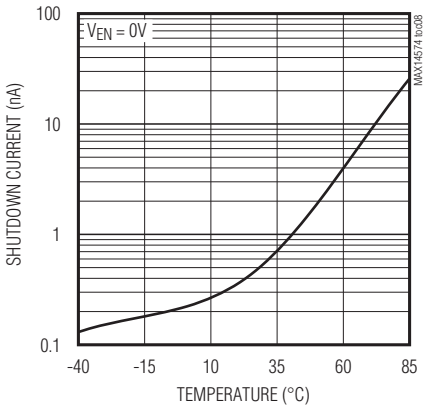
TOTAL INPUT CURRENT (I_{DD} + I_{LX}) vs. TEMPERATURE



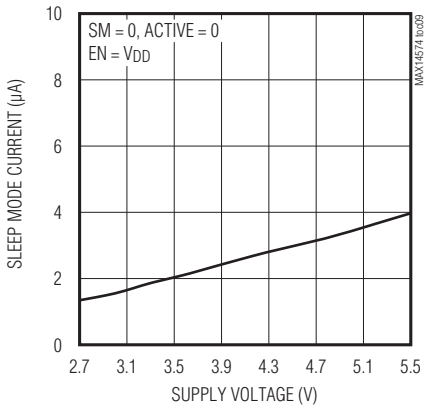
SHUTDOWN CURRENT (I_{DD}) vs. SUPPLY VOLTAGE



SHUTDOWN CURRENT (I_{DD}) vs. TEMPERATURE



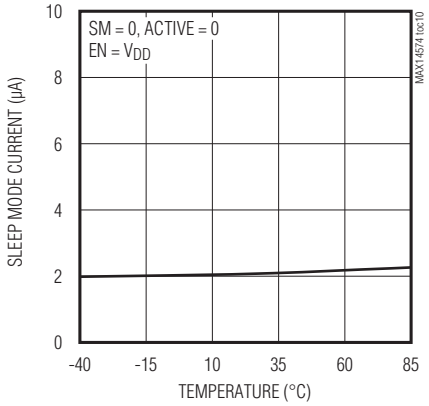
SLEEP MODE CURRENT (I_{DD} + I_{LX}) vs. SUPPLY VOLTAGE



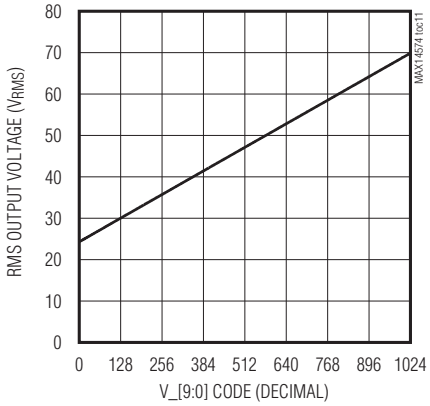
Typical Operating Characteristics (continued)

(V_{DD} = +3.6V, T_A = +25°C, inductor 3.3µH, I_{SAT} = 0.7A, C_{VH} = 100nF, IL[1:0] = 01, FSTU[1:0] = 10, see Figure 2 where C_{LENS} = 75pF, R_{IJ} = 150kΩ, unless otherwise noted.)

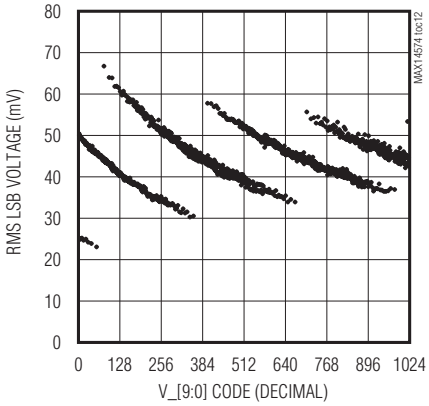
SLEEP MODE CURRENT (I_{DD} + I_{LX}) vs. TEMPERATURE



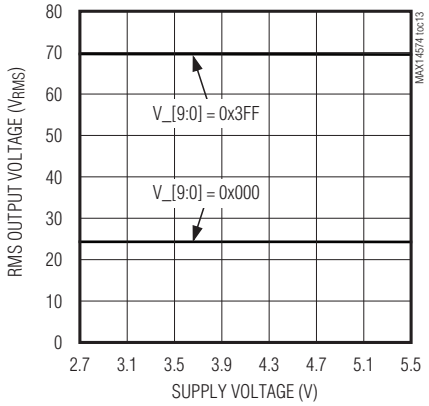
RMS OUTPUT VOLTAGE vs. CODE



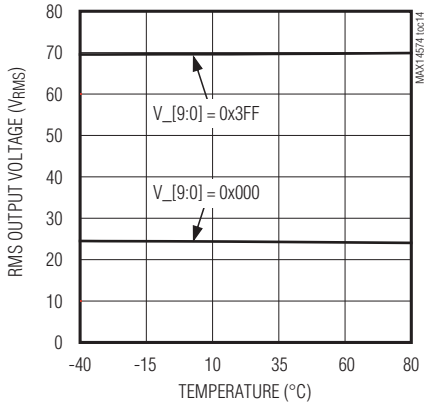
RMS LSB VOLTAGE vs. CODE



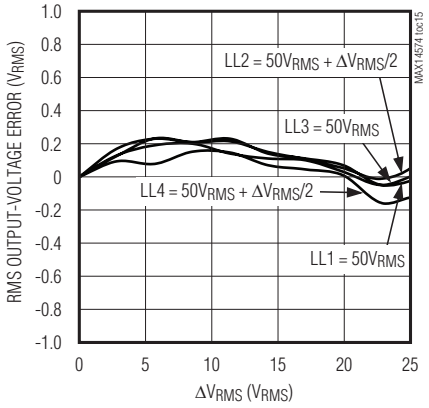
RMS OUTPUT VOLTAGE vs. SUPPLY VOLTAGE



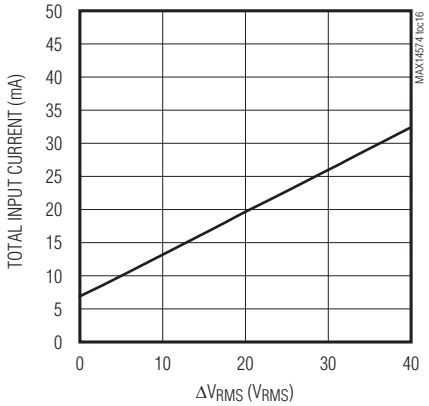
RMS OUTPUT VOLTAGE vs. TEMPERATURE



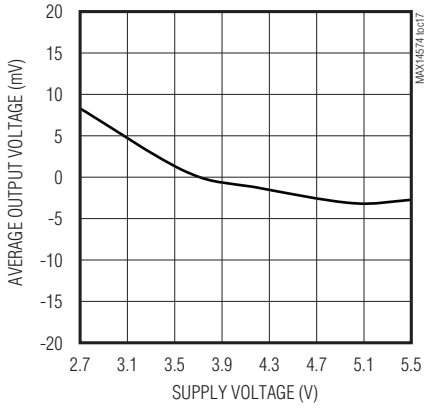
RMS OUTPUT-VOLTAGE ERROR vs. ΔVRMS



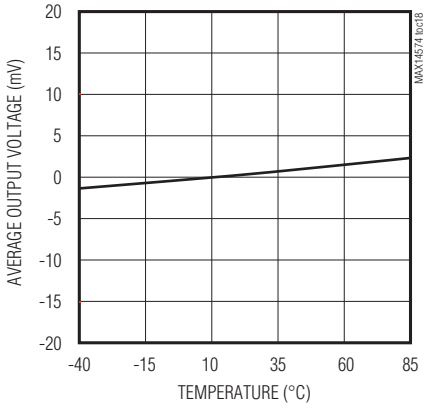
TOTAL INPUT CURRENT (I_{DD} + I_{LX}) vs. ΔVRMS



AVERAGE DC OUTPUT VOLTAGE vs. SUPPLY VOLTAGE



AVERAGE DC OUTPUT VOLTAGE vs. TEMPERATURE

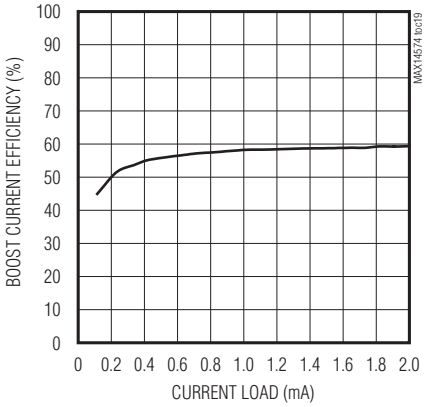


4-Channel, High-Voltage, Liquid Lens Driver for OIS/AF Systems

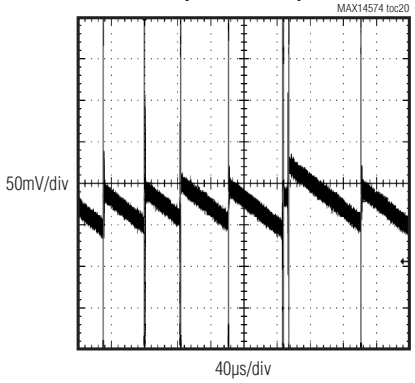
Typical Operating Characteristics (continued)

(V_{DD} = +3.6V, T_A = +25°C, inductor 3.3µH, I_{SAT} = 0.7A, C_{VH} = 100nF, IL[1:0] = 01, FSTU[1:0] = 10, see Figure 2 where C_{LENS} = 75pF, R_{IJ} = 150kΩ, unless otherwise noted.)

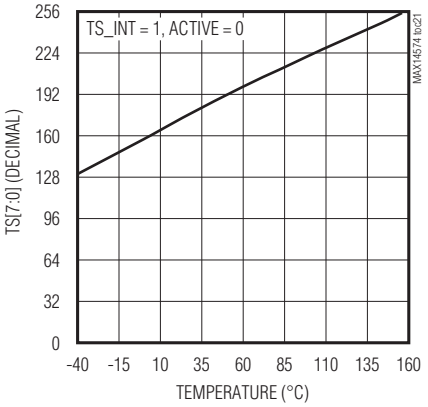
BOOST CURRENT EFFICIENCY vs. CURRENT LOAD



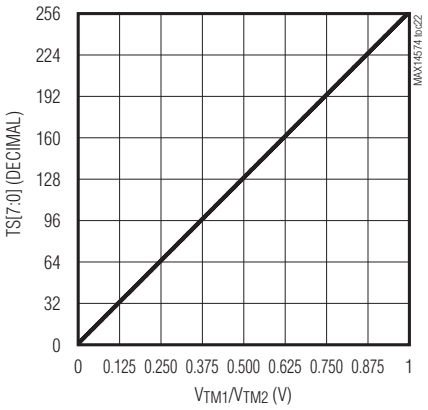
V_H OUTPUT-VOLTAGE RIPPLE (C_{VH} = 100nF)



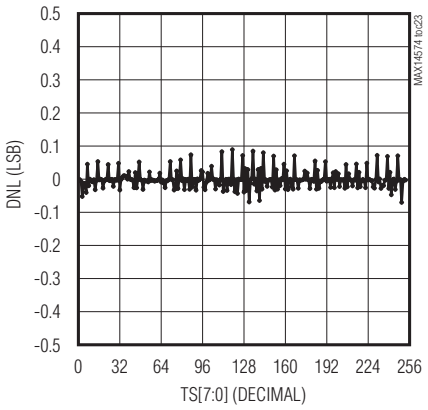
TEMPSENSE INTERNAL CODE vs. TEMPERATURE



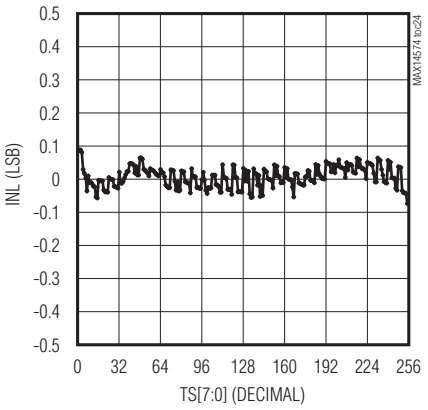
TEMPSENSE EXTERNAL CODE vs. V_{TM1}/V_{TM2}



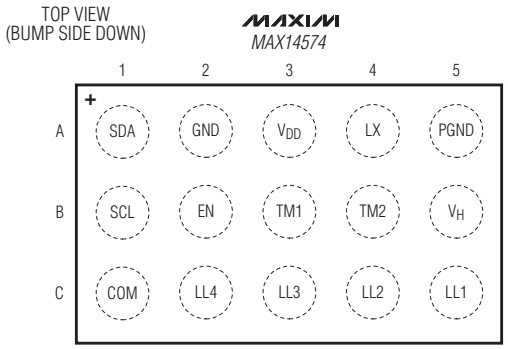
TEMPSENSE EXTERNAL DNL



TEMPSENSE EXTERNAL INL



Bump Configuration

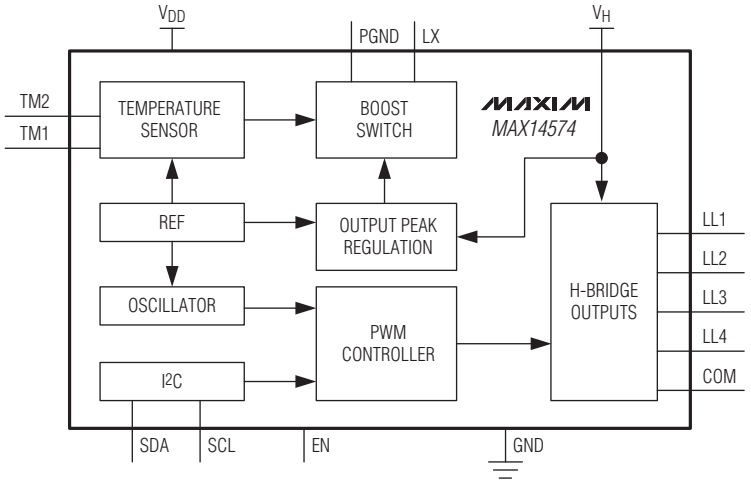


WLP
(1.6mm x 2.6mm x 0.5mm)

Bump Description

BUMP	NAME	FUNCTION
A1	SDA	I²C Open-Drain Serial-Data Input/Output
A2	GND	Ground
A3	V_{DD}	Input Supply Voltage. Bypass V_{DD} to GND with a 0.1µF capacitor as close as possible to the part and a 4.7µF capacitor as close as possible to the inductor.
A4	LX	Switching Transistor Node. Connect a 3.3µH (I_{SAT} > 0.6A) inductor from LX to V_{DD}.
A5	PGND	Ground for Boost Converter Switch
B1	SCL	I²C Open-Drain Serial-Clock Input
B2	EN	Enable Input. Drive EN high for normal operation. Drive EN low to enter shutdown mode.
B3	TM1	Temperature Sensor Terminal 1. If using external temperature sensing, connect a partition resistor between TM1 and GND.
B4	TM2	Temperature Sensor Terminal 2. If using external temperature sensing, connect a partition resistor between TM1 and TM2.
B5	V_H	High-Voltage Supply. Connect V_H to the output of the boost converter. Bypass V_H to PGND with a 0.1µF (> 75V) capacitor.
C1	COM	Liquid Lens OIS/AF Voltage Output COM. Connect COM to the COM terminal of a liquid lens module.
C2	LL4	Liquid Lens OIS/AF Voltage Output 4. Connect LL4 to the LL4 terminal 4 of a liquid lens module.
C3	LL3	Liquid Lens OIS/AF Voltage Output 3. Connect LL3 to the LL3 terminal 3 of a liquid lens module.
C4	LL2	Liquid Lens OIS/AF Voltage Output 2. Connect LL2 to the LL2 terminal 2 of a liquid lens module.
C5	LL1	Liquid Lens OIS/AF Voltage Output 1. Connect LL1 to the LL1 terminal 1 of a liquid lens module.

Functional Diagram



4-Channel, High-Voltage, Liquid Lens Driver for OIS/AF Systems

Detailed Description

The MAX14574 4-channel, high-voltage liquid lens driver uses an inductor-based boost converter and integrated H-bridges to provide a lens driver solution. This device features a 10-bit monotonic DAC controlled by a simple 2-wire I²C interface to set the peak-to-peak amplitude of the high-voltage outputs.

Power-On Reset

When the device initially powers up, all the registers are cleared and the device is in sleep mode.

High-Voltage Outputs (LL1–LL4, COM)

Connect a liquid lens between the high-voltage outputs (LL_, COM) of the device. The RMS output voltage of LL_ and COM is controlled by the value set in the OIS_LSB and LLV1 to LLV4 registers (see the register definitions in Table 2). The internal H-bridge that drives the LL_ and COM switches is 5kHz (typ).

Boost Converter

The device boost converter works in discontinuous mode and regulates the output voltage by adjusting the frequency to allow adequate power transfer to the load. The boost converter output (V_H) is not intended to drive external circuitry.

Inductors values can range from 1.5µH up to 10µH and the peak inductor current can be configured by the current-limit IL[1:0] bits. The inductor's saturation current rating should meet or exceed the peak inductor current. The inductor resistance should be as low as possible to achieve high efficiency.

Use a fast switching diode with low reverse current as possible at +75V. The peak forward current of the diode should be equal to or greater than the peak inductor current configured in the I²C registers. Schottky diodes generally exhibit significant leakage current at high reverse voltages and high temperatures so an ultrafast junction rectifier may be the best choice.

The input capacitor from V_{DD} to PGND in step-up designs reduces the current peaks drawn from the battery or input power source and reduces switching noise. The impedance of the input capacitor at the switching frequency should be less than that of the input source so that high-frequency switching currents do not pass through the input source. A ceramic capacitor from 1µF to 10µF should be placed as close as possible to the boost inductor. The exact value required depends on the stray inductance and resistance of the power-supply trace.

The output filter capacitor from V_H to PGND (from 4.7nF to 100nF) is required to keep the output-voltage ripple small. A higher value capacitor reduces output ripple but increases the wake-up time of the device. The wake-up time can be configured according to the output capacitor to limit startup current through the FSTU[1:0] bits. The output filter capacitor must have low impedance at the switching frequency and low R_{ESR}, and its voltage rating must exceed the maximum applied capacitor voltage (+75V).

Designing a PCB

A good PCB layout is important to achieve optimal performance from the device. Poor design can cause excessive conducted and/or radiated noise, both of which are undesirable. Conductors carrying discontinuous currents should be kept as short as possible. Conductors carrying high currents should be made as wide as possible. A separate low-noise ground plane containing the reference and signal grounds should only connect to the power-ground plane at one point to minimize the effects of power-ground currents.

Nodes with high dv/dt (LX, LL_, and COM switching node) should be kept as small as possible and away from high-impedance nodes such as TM1/TM2.

Refer to the MAX14574 evaluation kit data sheet for a full example PCB design.

Shutdown Mode (EN)

The device features a shutdown mode that reduces supply current to less than 100nA. In shutdown mode, all registers are in a reset state and the I²C input buffers are disabled. Drive EN low to place the device in shutdown mode. Drive EN high for normal operation. Driving EN rail-to-rail minimizes power consumption.

Internal Temperature Sensor

The device can use an internal temperature sensing to measure temperature. The data in the TempSense register (when TS_INT = 1 and TS_EXT = 0) gives the temperature T_J measured inside the part according to the following formula:

$$T_J = (TS[7:0] - 127) \times +1.6°C - +60°C$$

0x00 = Measurement is not available.

0x01 to 0x7E = Temperature sensor accuracy is not guaranteed.

The internal temperature sensor covers a range from -60°C to +145°C with a resolution of +1.6°C.

Temperature T_J is related to ambient temperature through part thermal resistance and power dissipated:

$$T_J = T_A + \theta_{JA} \times PWR$$

where:

T_A is the ambient temperature.

PWR is the power dissipated inside the device.

θ_{JA} is the junction-to-ambient thermal resistance.

In a typical condition with no power delivered to the liquid lens, $T_J - T_A < +1°C$.

External Temperature Sensor

The device can use an external thermistor to measure temperature. A thermistor's resistance varies as a function of temperature. A negative temperature coefficient (NTC) thermistor (R_{THERM}) can be connected between TM2 and TM1, with a series resistor (R_1) between TM1 and GND.

The device forces V_{REF} on B4 bump TM2 (V_{REF} = +1V) and measures the voltage on TM1 with an 8-bit ADC with an input range of 0 to V_{REF}. The data in the TempSense register gives the voltage across the thermistor as a range of 0 to V_{REF} = +1V.

The voltage across the thermistor is related to temperature according to thermistor characteristics. With a suitable choice of thermistor and R_1, the relation between the temperature and voltage code can be approximated as linear in a small temperature range.

Sleep Mode

When EN is high and the sleep mode bit (SM) in the UserMode register is reset, the device is in sleep mode (see Table 2 for the register definition). During sleep mode, the power-on-reset circuit remains active, and, if no activity is detected on the I^2C interface, the I^2C input buffers are disabled to reduce current consumption to less than 6.5µA.

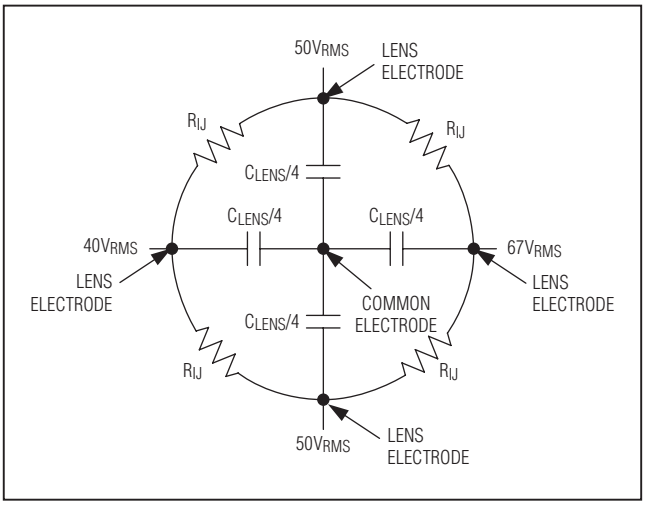


Figure 2. OIS Maximum Tilt Configuration

Table 1. Register Map

REGISTER	ADDR	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Status	0x00	R	REV2	REV1	REV0	LL_TH	X	BST_FAIL	X	X
Fail	0x01	R	X	FAIL_OP	FAIL_SH	COM_FAIL	LL4_FAIL	LL3_FAIL	LL2_FAIL	LL1_FAIL
TempSense	0x02	R	TS7	TS6	TS5	TS4	TS3	TS2	TS1	TS0
UserMode	0x03	R/$\overline{W}$	X	X	X	X	X	X	ACTIVE	SM
OIS_LSB	0x04	R/$\overline{W}$	V4_1	V4_0	V3_1	V3_0	V2_1	V2_0	V1_1	V1_0
LLV1	0x05	R/$\overline{W}$	V1_9	V1_8	V1_7	V1_6	V1_5	V1_4	V1_3	V1_2
LLV2	0x06	R/$\overline{W}$	V2_9	V2_8	V2_7	V2_6	V2_5	V2_4	V2_3	V2_2
LLV3	0x07	R/$\overline{W}$	V3_9	V3_8	V3_7	V3_6	V3_5	V3_4	V3_3	V3_2
LLV4	0x08	R/$\overline{W}$	V4_9	V4_8	V4_7	V4_6	V4_5	V4_4	V4_3	V4_2
Command	0x09	R/$\overline{W}$	X	X	X	X	X	X	UPD_OUT	CHK_FAIL
DriverConf	0x0A	R/$\overline{W}$	TS_INT	TS_EXT	RES	RES	FSTU1	FSTU0	IL1	IL0

Note: *All default reset values are 0x00, unless otherwise noted.*
X = Don't care.
RES = Reserved bit; must be set to 0.

Table 2. Register Definitions

FIELD NAME	READ/WRITE	BIT	POWER-ON RESET	DESCRIPTION
Status (I^2C address = 0x00)				
REV[2:0]	Read	[7:5]	000	Chip revision.
LL_TH	—	4	0	A read operation on this register returns a 1 for this bit if the device is in thermal shutdown, or a thermal shutdown event has occurred; otherwise, it reads a 0. LL_TH is reset by EN or SM.
BST_FAIL	Read	2	0	A read operation on this register returns a 1 for this bit if the B5 bump (V_H) is not able to reach the V_{PEAK} voltage; otherwise, it reads a 0.
Fail (I^2C address = 0x01)				
FAIL_OP	Read	6	0	A read operation on this register (2ms after CHK_FAIL = 1) returns a 1 for this bit if the device senses an open connection between the outputs; otherwise, it reads a 0.
FAIL_SH	Read	5	0	A read operation on this register (2ms after CHK_FAIL = 1) returns a 1 for this bit if the device senses a short-circuit connection between the outputs or from the outputs to ground; otherwise, it reads a 0.
COM_FAIL	Read	4	0	A read operation on this register (2ms after CHK_FAIL = 1) returns a 1 for this bit if the device senses a fail connection on the C1 bump (COM); otherwise, it reads a 0.
LL[4:1]_FAIL	Read	[3:0]	0000	A read operation on this register (2ms after CHK_FAIL = 1) returns a 1 for this bit if the device senses a fail connection on the C2 to C5 bumps (LL[4:1]); otherwise, it reads a 0.
TempSense (I^2C address = 0x02)				
TS[7:0]	Read	[7:0]	00000000	When the TS_INT bit = 1, these 8 bits are the result of the last temperature conversion of the internal temp sense. 0x00 = Measurement not available 0x01 to 0x7E = Temperature sensor accuracy not guaranteed 0x7F = -60°C … 0xFF = +145°C T_J = (TS[7:0] - 127) x +1.6°C - +60°C When the TS_EXT bit = 1, these 8 bits are the result of the last temperature conversion of the external temp sense. The external sensor converts the ratio between the thermistor and a fix resistor. 0x00 = Measurement not available 0x01 = 1/255 x V_{TM2} 0x02 = 2/255 x V_{TM2} … 0xFF = V_{TM2} (1V typ)
UserMode (I^2C address = 0x03)				
ACTIVE	Read/Write	1	0	Active bit. 0 = LL_ and COM are pulled down and not switching. The update command is ignored until this bit is set to 1. 1 = After one update command, the outputs start switching with the RMS configured as in the LLV_ registers.

Table 2. Register Definitions (continued)

FIELD NAME	READ/WRITE	BIT	POWER-ON RESET	DESCRIPTION
SM	Read/Write	0	0	Sleep mode bit. 0 = Sleep mode. 1 = Normal operation. All registers keep the same values as before shutdown unless a POR occurs.
OIS_LSB (I²C address = 0x04)				OIS LSB存的是10bit控制信号的低2bit，LLV1存的是高8bit
V4_[1:0]	Read/Write	[7:6]	00	These are the two LSBs of the 10-bit V4_[9:0] PWM linear-defined RMS output voltage for the LL4 output.
V3_[1:0]	Read/Write	[5:4]	00	These are the two LSBs of the 10-bit V3_[9:0] PWM linear-defined RMS output voltage for the LL3 output.
V2_[1:0]	Read/Write	[3:2]	00	These are the two LSBs of the 10-bit V2_[9:0] PWM linear-defined RMS output voltage for the LL2 output.
V1_[1:0]	Read/Write	[1:0]	00	These are the two LSBs of the 10-bit V1_[9:0] PWM linear-defined RMS output voltage for the LL1 output.
LLV1 (I²C address = 0x05)				
V1_[9:2]	Read/Write	[7:0]	00000000	These are the eight MSBs of the 10-bit V1_[9:0] PWM linear-defined RMS output voltage control. Code 0x000 = 24. $4V_{RMS}$ … Code 0x3FF = $69.7V_{RMS}$, linear scale $V_{LL1RMS} = 44.5mV_{RMS} \times N + 24.4V_{RMS}$ where N = code 0x000 to 0x3FF in decimal.
LLV2 (I²C address = 0x06)				
V2_[9:2]	Read/Write	[7:0]	00000000	These are the eight MSBs of the 10-bit V2_[9:0] PWM linear-defined RMS output voltage control. Code 0x000 = 24. $4V_{RMS}$ … Code 0x3FF = $69.7V_{RMS}$, linear scale $V_{LL2RMS} = 44.5mV_{RMS} \times N + 24.4V_{RMS}$ where N = code 0x000 to 0x3FF in decimal.
LLV3 (I²C address = 0x07)				
V3_[9:2]	Read/Write	[7:0]	00000000	These are the eight MSBs of the 10-bit V3_[9:0] PWM linear-defined RMS output voltage control. Code 0x000 = $24.4V_{RMS}$ … Code 0x3FF = $69.7V_{RMS}$, linear scale $V_{LL3RMS} = 44.5mV_{RMS} \times N + 24.4V_{RMS}$ where N = code 0x000 to 0x3FF in decimal.
LLV4 (I²C address = 0x08)				
V4_[9:2]	Read/Write	[7:0]	00000000	These are the eight MSBs of the 10-bit V4_[9:0] PWM linear-defined RMS output voltage control. Code 0x000 = $24.4V_{RMS}$ … Code 0x3FF = $69.7V_{RMS}$, linear scale $V_{LL4RMS} = 44.5mV_{RMS} \times N + 24.4V_{RMS}$ where N = code 0x000 to 0x3FF in decimal.

Table 2. Register Definitions (continued)

FIELD NAME	READ/WRITE	BIT	POWER-ON RESET	DESCRIPTION
Command (I^2C address = 0x09)				
UPD_OUT	Read/Write	1	0	Update output bit. 0 = The device operates normally. 1 = When the user sets this bit to 1, the device updates the output RMS voltage according to the content of the LLV_ registers at the beginning of the first half cycle available if ACTIVE = 1. At the end of the update procedure, this bit is automatically reset. If ACTIVE = 0, the update command is not performed and this bit remains at 1 until ACTIVE becomes 1.
CHK_FAIL	Read/Write	0	0	Check-fail bit. 0 = The device operates normally. 1 = When the user sets this bit to 1, the device checks for an open/short on the output connections. At the end of the checking procedure (2ms), the result appears in the Fail register and this bit is reset. During this check procedure, the output RMS is not controlled by the LLV_ registers. If ACTIVE is equal to 1 at the end of check-fail procedure, the part restarts switching. Any update command given during a check-fail procedure is served, but the effect appears only at the end of the check-fail procedure.
DriverConf (I^2C address = 0x0A)				
TS_INT	Read/Write	7	0	Internal temp-sensor enable bit: 0 = Internal temperature sensor is disabled. 1 = Internal temperature sensor is enabled if TS_EXT = 0. Setting this bit to 1 initially resets the TempSense register content. After 1.2ms and then every 1ms, the TempSense register is updated with the results of the temperature-sensor conversion.
TS_EXT	Read/Write	6	0	External temp-sensor enable bit: 0 = External temperature sensor is disabled. 1 = External temperature sensor is enabled. Setting this bit to 1 initially resets the TempSense register content. After 1.2ms and then every 1ms, the TempSense register is updated with the results of the temperature-sensor conversion.
RES	Read/Write	[5:4]	00	Reserved bits. These bits must always be set to 0.
FSTU[1:0]	Read/Write	[3:2]	00	Startup time configuration bits: These bits configure the startup ramp time for the B5 bump (V_H) from V_{DD} to +70V: 00: t_{STU} = 6.4ms 01: t_{STU} = 3.2ms 10: t_{STU} = 0.8ms 11: t_{STU} = 0.4ms The user can configure the startup time for the boost converter according to the tank capacitor and inductor current: $I_{OUT} = C_{TNK}$ 70V/t_{STU} Example: C_{TNK} = 100nF leads to I_{OUT} = 100nF x 70V/3.2ms = 2.2mA (same load of R_{IJ} = 75kΩ) C_{TNK} = 100nF leads to I_{OUT} = 100nF x 70V/6.4ms = 1.1mA (same load of R_{IJ} = 150kΩ)

PF：当前充电速度太慢？

Table 2. Register Definitions (continued)

FIELD NAME	READ/WRITE	BIT	POWER-ON RESET	DESCRIPTION
IL[1:0]	Read/Write	[1:0]	00	Inductor current-limit configuration bits. These bits configure the DC current limit for the inductor: 00 = 270mA 01 = 410mA 10 = 570mA 11 = 720mA DC value of the current limit (±10%). For effective maximum current limit, add to the DC level: ΔI_L = 50ns/(V_{DD}/L) where V_{DD} is the inductor supply voltage and L is the inductor value.

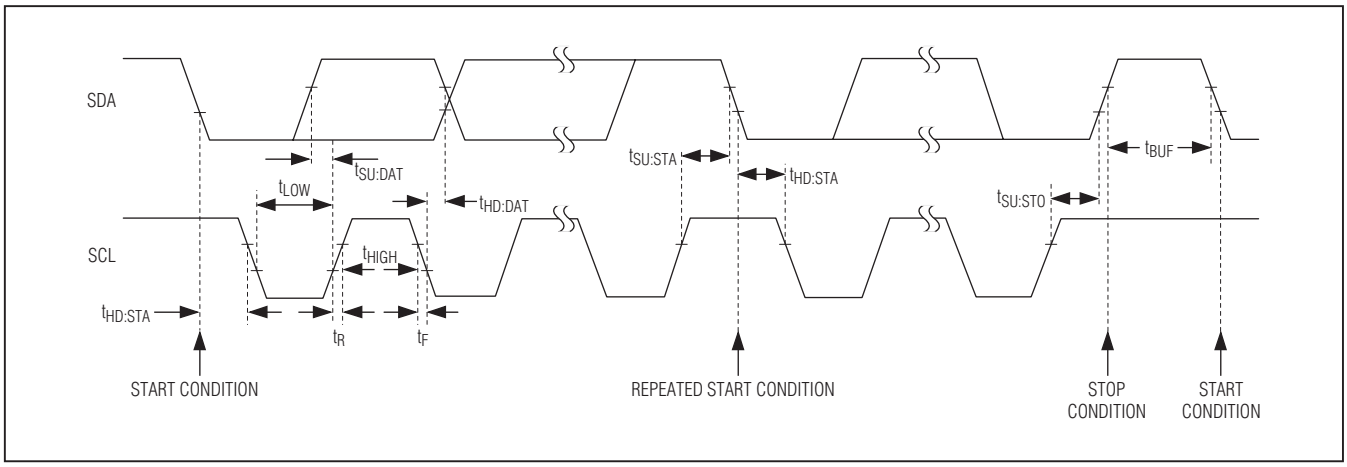


Figure 3. I²C Interface Timing Details

I²C Serial Interface

Serial Addressing

The device operates as a slave device that sends and receives data through an I²C-compatible 2-wire interface. The interface uses a serial-data line (SDA) and a serial-clock line (SCL) to achieve bidirectional communication between masters and slaves. A master (typically a microcontroller) initiates all data transfers to and from the device and generates the SCL clock that synchronizes the data transfer. The SDA line operates as both an input and an open-drain output. A pullup resistor is required on SDA. The SCL line operates only as an input. A pullup resistor is required on SCL if there are multiple masters on the 2-wire interface, or if the master in a single-master system has an open-drain SCL output. Each transmission consists of a START (S) condition sent by a master, followed by the device's 7-bit slave address plus a R/W bit, a register address byte, one or more data bytes, and finally a STOP (P) condition (Figure 3).

4-Channel, High-Voltage, Liquid Lens Driver for OIS/AF Systems

START and STOP Conditions

Both SCL and SDA remain high when the interface is not busy. A master signals the beginning of a transmission with a START condition by transitioning SDA from high to low while SCL is high (Figure 4). When the master has finished communicating with the slave, it issues a STOP condition by transitioning SDA from low to high while SCL is high. The bus is then free for another transmission.

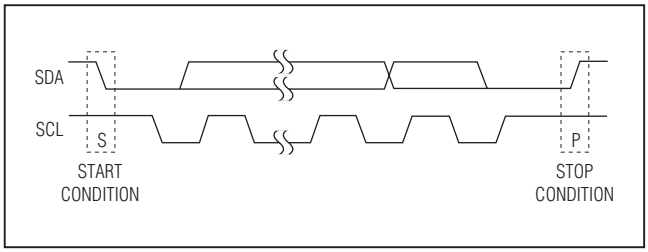


Figure 4. START and STOP Conditions

Bit Transfer

One data bit is transferred during each clock pulse (Figure 5). The data on SDA must remain stable while SCL is high.

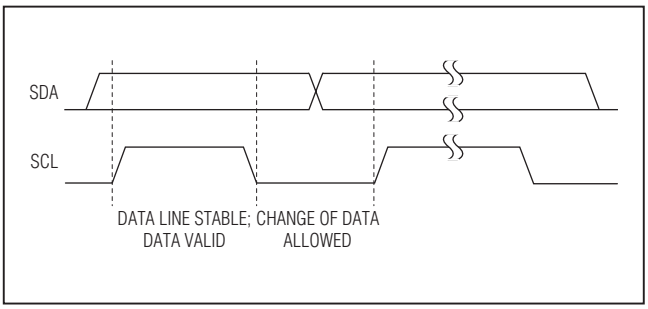


Figure 5. Bit Transfer

Acknowledge

The acknowledge bit (ACK) is a clocked 9th bit (Figure 6), which the recipient uses for handshake receipt of each byte of data. Thus, each byte transferred effectively requires 9 bits. The master generates the 9th clock pulse, and the recipient pulls down SDA during the acknowledge clock pulse, so the SDA line is stable low during the high period of the clock pulse. When the master is transmitting to the device, it generates the acknowledge bit because the device is the recipient. When the device is transmitting to the master, the master generates the acknowledge bit because the master is the recipient. Note that when reading data from the device, always send a not-acknowledge from the master on the last read data byte or the device does not relinquish the bus.

永远是接收方发送确认位

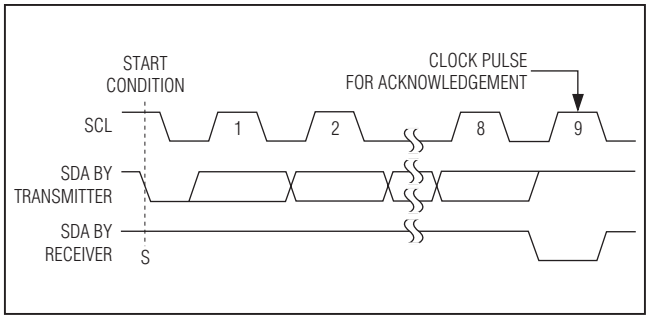


Figure 6. Acknowledge

Slave Address

The device has a 7-bit long slave address. The bit following a 7-bit slave address is the R/$\overline{W}$ bit, which is low for a write command and high for a read command. The slave address is 0xEE for write commands and 0xEF for read commands (Figure 7).

发地址时也需要确认位

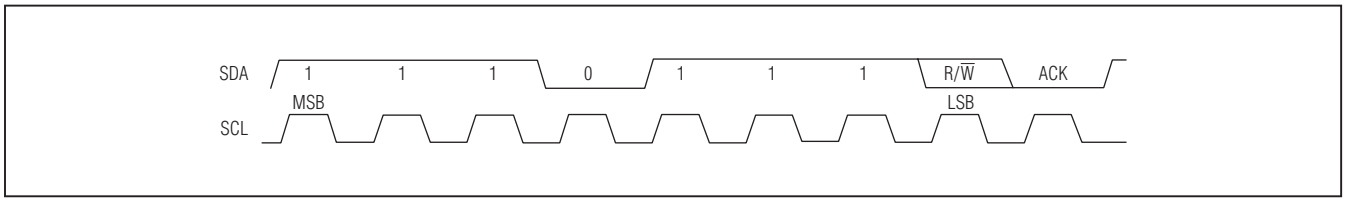


Figure 7. Slave Address

Format for Writing

To write to the device, the master generates a START condition and then transmits the slave address with the R/$\overline{W}$ bit set to zero, followed by at least one data byte. The first data byte is the register address, which determines which register to be written. The device asserts an ACK on SDA if a valid register address is detected. A data byte received after the register address goes into the selected register. For each additional byte received from the master, the device autoincrements the register address. After all bytes are written, the master generates a STOP condition. Figure 8 shows a single-register I²C write and Figure 9 shows a multiple-register I²C write.

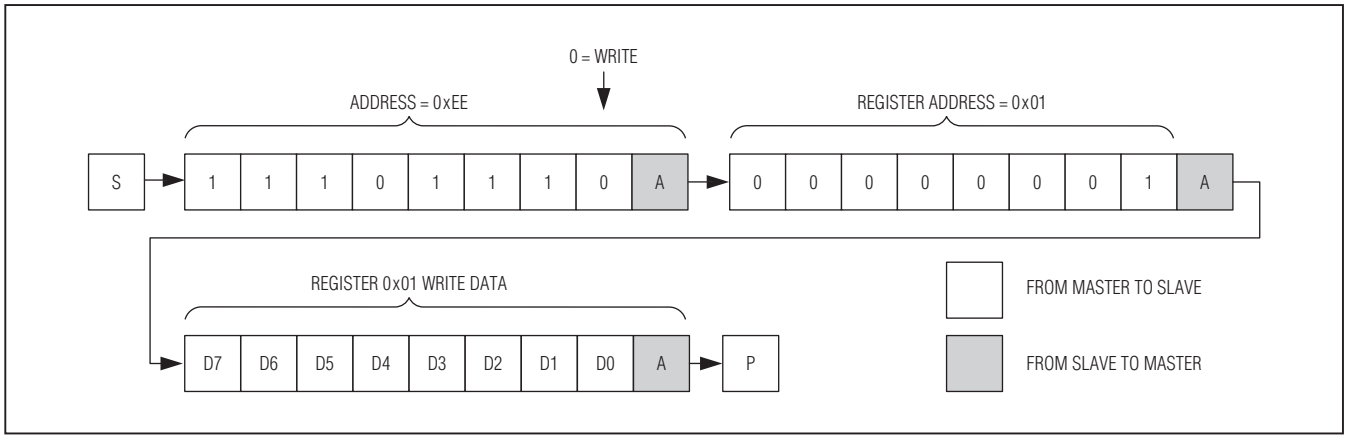


Figure 8. Format for I²C Write

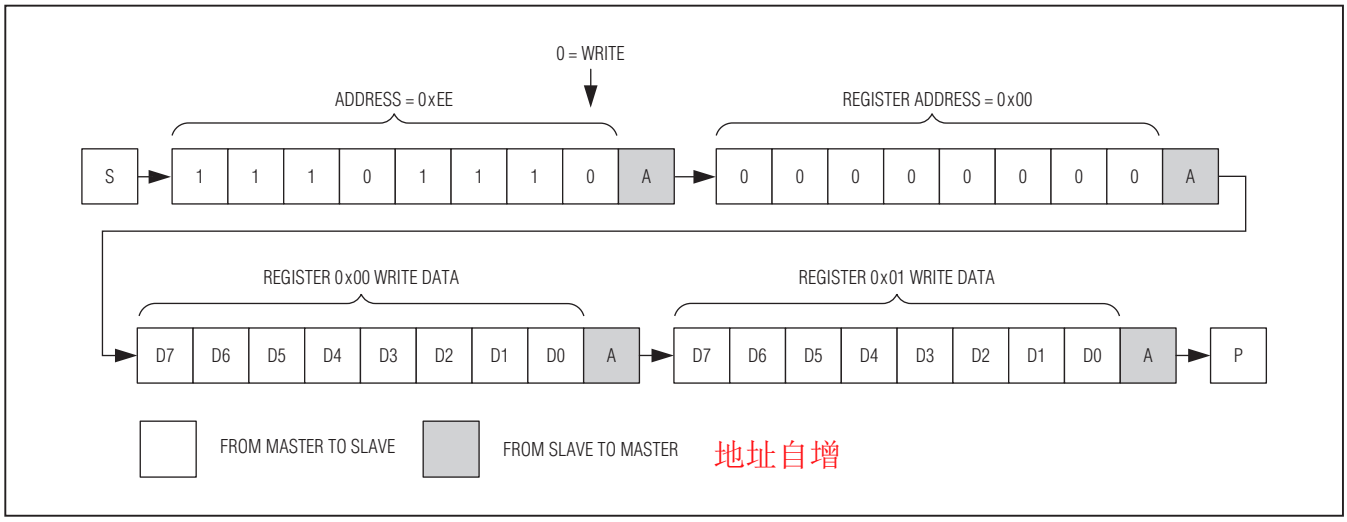


Figure 9. Format for Writing to Multiple Registers

4-Channel, High-Voltage, Liquid Lens Driver for OIS/AF Systems

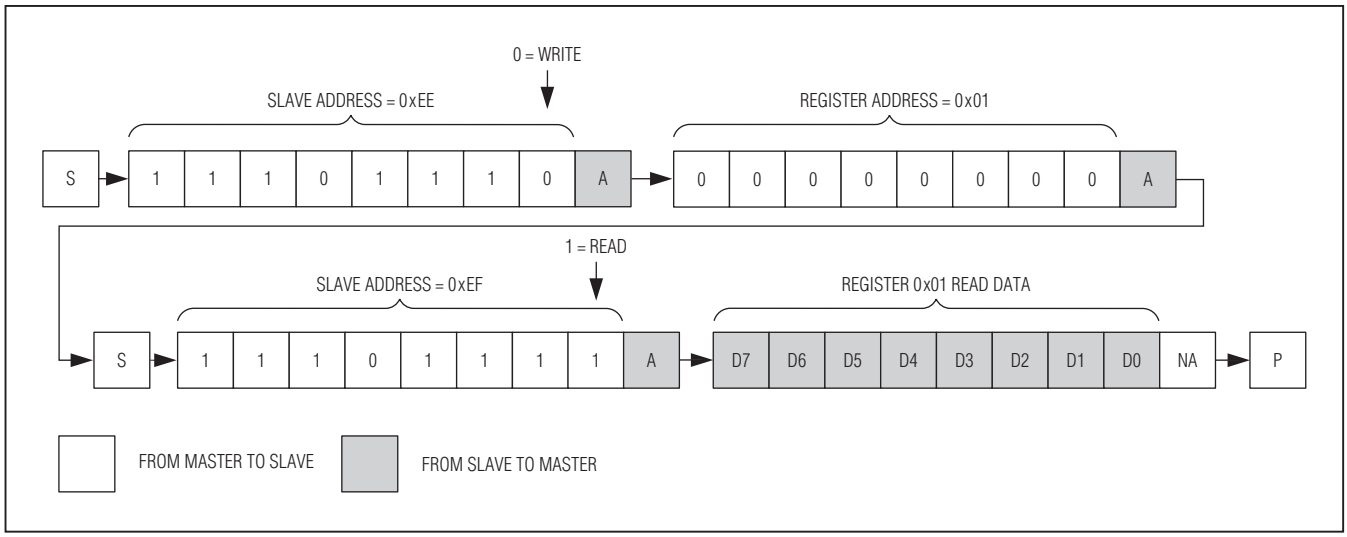


Figure 10. Format for Reading

Format for Reading

To read from the device, the master generates a START condition and then transmits the slave address with the R/$\overline{W}$ bit set to one. The master then sends the register address to be read. After the device asserts an ACK on SDA, the master sends a repeated START condition followed by the slave address with the R/$\overline{W}$ bit set to zero. The device then sends an ACK followed by the byte contained in the register. The device autoincrements the register address, and, if the master asserts an ACK, the device sends the next byte. To end the read transaction, the master must generate a NACK followed by a STOP condition.

Chip Information

PROCESS: CMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
15 WLP	W151A2+1	**21-0205**	Refer to **Application Note 1891**

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	12/10	Initial release	—