Single Cycle CPU Design

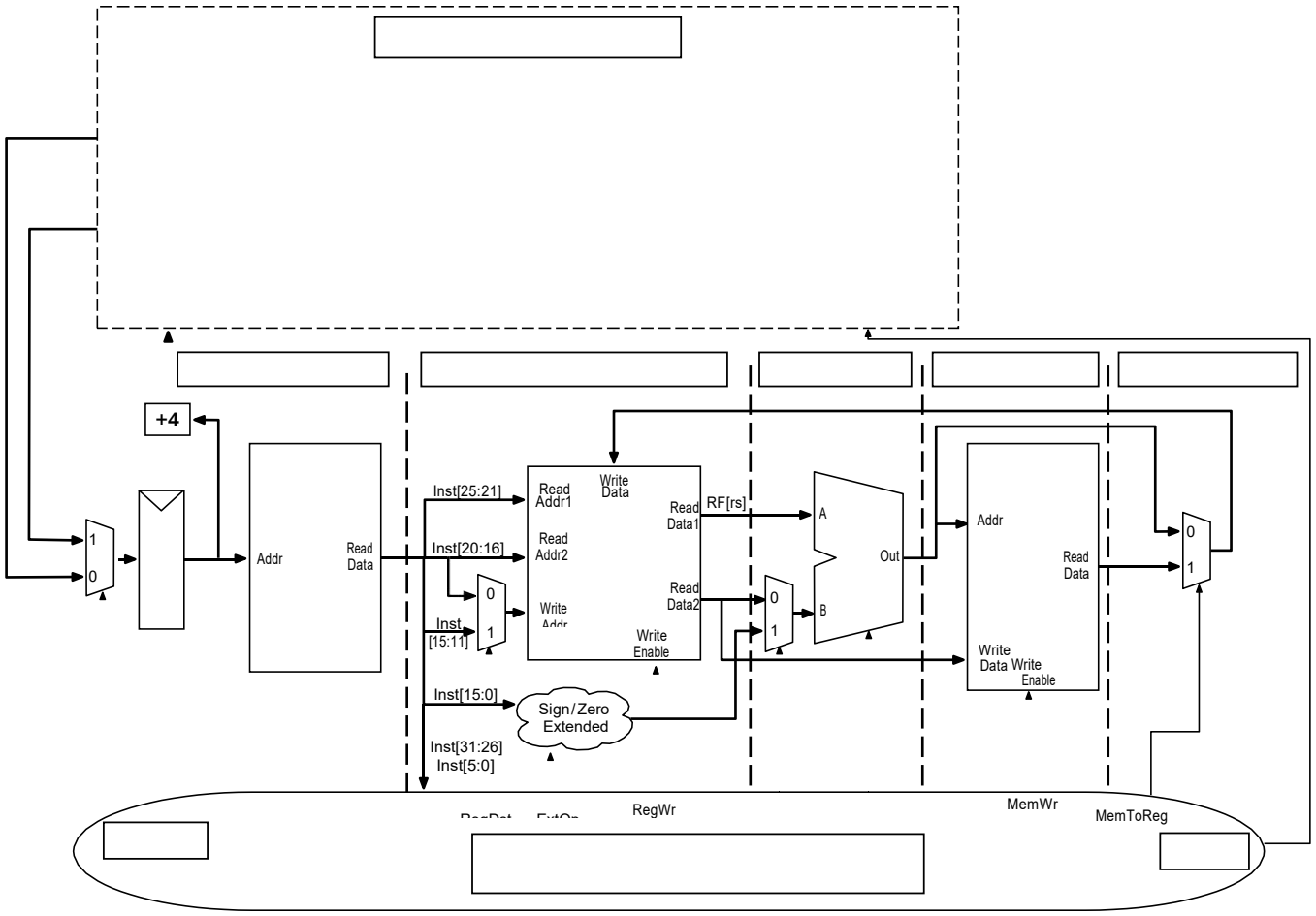
Here we have a single cycle CPU diagram. Answer the following questions:

1.Name each component.

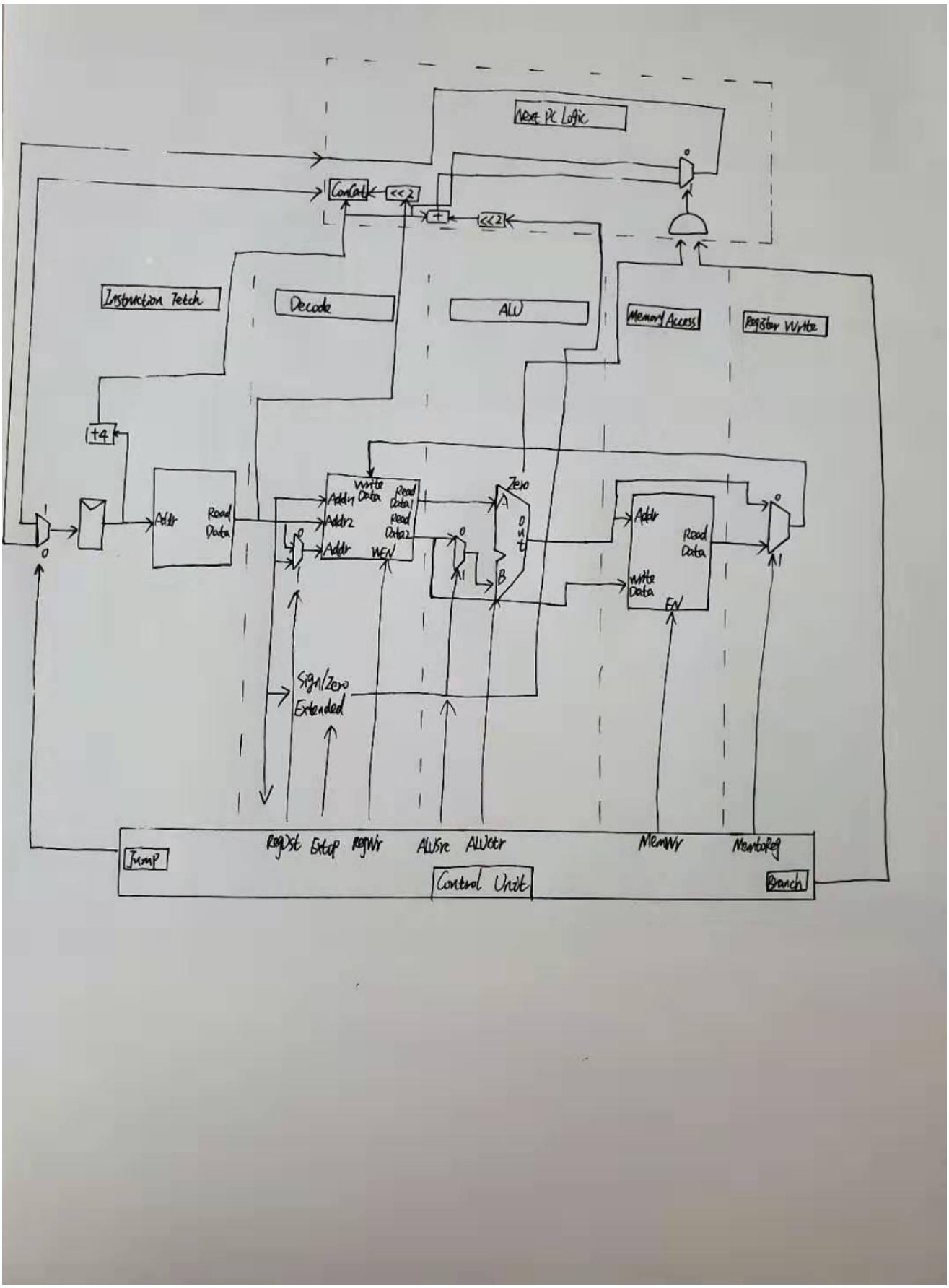
2.Name each datapath stage and explain its functionality.

Stag	Functionalit
取指令单元	Fetch the instruction:mem[PC],更新PC。
译码	取出指令后，从各域中得到数据首先读出0p码，决定指令类型及字段长度；接下来从相关部分读出数据。
ALU	算术逻辑单元，进行算术、逻辑运算。
内存访问	只有load、store在此阶段使用，其余指令在该阶段跳过或者空闲。
写寄存器	大多数指令将结果写入寄存器，有一些指令在该阶段跳过或者空闲。

3.Provide data inputs and control signals to the next PC logic.见下面图片。



4.Implement the next PC logic.



Single Cycle CPU Control Logic

Fill out the values for the control signals from the previous CPU diagram.

Instrs.	Control								
			RegDst	ExtOp	ALUSrc	ALUCtr	MemWr	MemtoR	RegWr
add			1	X	0	0010	0	0	1
ori			0	0	1	0001	0	0	1
lw			0	1	1	0010	0	1	1
sw			X	1	1	0010	1	X	0
beq			X	1	0	0110	0	X	0
j			X	X	X	XXXX	0	X	0

This table shows the ALUCtr values for each operation of the ALU:

Operation	AND	OR	ADD	SUB	SLT	NOR
ALUCtr	0000	0001	0010	0110	0111	1100

Clocking Methodology

- The input signal to each state element must stabilize before each rising edge.
- Critical path: Longest delay path between state elements in the circuit.
- $t_{clk} \geq t_{clk\text{-}to\text{-}q} + t_{CL} + t_{setup}$, where t_{CL} is the critical path in the combinational logic.
- If we place registers in the critical path, we can shorten the period by reducing the amount of logic between registers.

Single Cycle CPU Performance Analysis

The delays of circuit elements are given as follows:

Element	Registe	Registe	MUX	ALU	Me	Me	RegFil	RegFil
Paramet	t_{clk-}	t_{setu}	t_{mux}	t_{ALU}	$t_{MEMread}$	$t_{MEMwrit}$	t_{RFrea}	$t_{RFsetup}$
Delay(ps)	30	20	25	200	250	200	150	20

1.Give an instruction that exercises the critical path.

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2.What is the critical path in the single cycle CPU?

PC->I-Mem->Register File(Read)->ALU->D-Mem->Mux->Register File(Write)

3.What are the minimum clock cycle, $t_{clk,}$ and the maximum clock frequency, f_{clk}? Assume the $t_{clk\text{-}to\text{-}q}$ > hold time.

tclk=30+250+150+200+250+25+20=925ps(tclk-to-q、tMEMread、tRFread、tALU 、tMEMread、tmux、tRFsetup)

fclk=1/925ps=1.08GHz

4.Why is a single cycle CPU inefficient?

时钟周期由Critical Path决定,但并不是每个指令都需要经过Critical Path

5.How can you improve its performance? What is the purpose of pipelining?

采用流水线设计，缩短时钟周期，使CPU更高效的运行。