1.Direct mapped caches

How many bytes of data can our cache hold? How many words? 8bytes,2words

CPU Cache	Index Number	Offset			
		3	2	1	0
	0				
	1				

Tag bits	Index bits	Offset bits	Total
			32

Index bits=$\log_2$ (Number of index rows) Offset bits=$\log_2$ (Number of offsets columns)

2. Fill in the "Tag bits, Index bits, Offset bits" with the correct T:I:O breakdown according to the diagram. Tag bits=29,Index bits=1,Offset bits=2

3. Let's say we have a 8192KiB cache with an 128B block size, what is the tag, index, and offset of 0xFEEDF00D?

FE	ED	F0	0D
1111 1110	1110 1101	1111 0000	0000 1101

tag:111111101 index:1101101111100000 offset:0001101

4. Fill in the table below. Assume we have a write-through cache, so the number of bits per row includes only the cache data, the tag, and the valid bit.

Address size (bits)	Cache size	Block size	Tag bits	Index bits	Offset bits	Bits per row
16	4KiB	4B				
32	32KiB	16B				
32			16	12		
64	2048KiB			14		1068

Address size(bits)	Cache size	Block size	Tag bits	Index bits	Offset bits	Bits per row
16	4KiB	4B	4	10	2	37
32	32KiB	16B	17	11	4	146
32	64KiB	16B	16	12	4	145
64	2048KiB	128B	43	14	7	1068

5.Let's say you have a byte-addressed computer with a total memory of 1MiB. It features a 16KiB CPU cache with 1KiB blocks.

1）. How many bits make up a memory address on this computer? 20

2）. What is the T:I:O breakdown? 6：4：10

6. Given CPU base CPI = 1, clock rate = 4GHz Miss rate/instruction = 2%

Main memory access time = 100ns， With just primary cache， what is Average memory access time (AMAT)？

Hit time=1/4GHz*1=0.25

AMAT=100x2%+0.25=2.25

7. CPU with 1ns clock, hit time = 1 cycle, miss penalty = 20 cycles, I-cache miss rate = 5%， what is Average memory access time (AMAT)？

AMAT=1+20x5%=2

8. Given，I-cache miss rate = 2%，D-cache miss rate = 4%，Miss penalty = 100 cycles Base CPI (ideal cache) = 2， Load & stores are 36% of instructions， what is Actual CPI

Actual CPI=2+2%x100+4%x36%x100=5.44